Product Preview

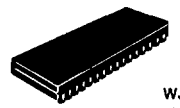
MCM67282

256K × 4 Bit Fast Static Random Access Memory

The MCM67282 is a 1,048,576 bit static random access memory organized as 262,144 x 4 bits. This device is fabricated using high-performance silicon-gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400-mil plastic small-outline J-leaded package.

- Single 5 V ±10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL-Compatible
- Three-State Outputs
- Fast Access Times: 10, 12 ns
- Center Power and I/O Pins for Reduced Noise



WJ PACKAGE
400-MIL SOJ
CASE 857A

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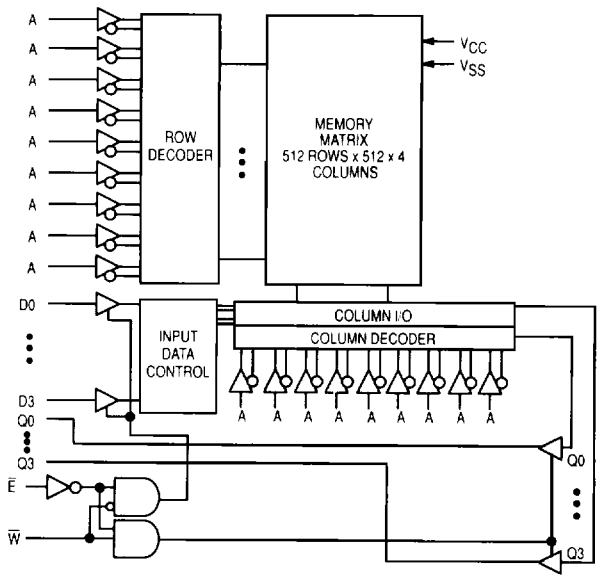
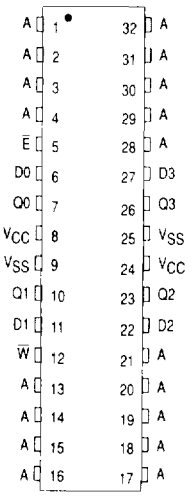
BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES

A0–A17	Address Input
E	Chip Enable
W	Write Enable
D0–D3	Data Input
Q0–Q3	Data Output
VCC	+ 5 V Power Supply
VSS	Ground

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	I_{SB1}, I_{SB2}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	− 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	1.2	W
Temperature Under Bias (T_A = 25°C)	T_{bias}	−10 to + 85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature—Plastic	T_{stg}	− 55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

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DC OPERATING CONDITIONS AND CHARACTERISTICS
(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Parameter	Symbol	Typ	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	5.0	4.5	5.5	V
Input High Voltage	V_{IH}	—	2.2	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	—	− 0.5**	0.8	V
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	±1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	—	±1.0	µA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = − 4.0 mA)	V_{OH}	—	2.4	—	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
**V_{IL} (min) = − 0.5 V dc; V_{IL} (min) = − 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	-10	-12	Unit
AC Active Supply Current (I_{out} = 0 mA) (V_{CC} = max, f = f_{max})	I_{CCA}	165	155	mA
Active Quiescent Current ($\overline{E}$ = V_{IL}, V_{CC} = max, f = 0 MHz)	I_{CC2}	90	90	mA
AC Standby Current ($\overline{E}$ = V_{IH}, V_{CC} = max, f = f_{max})	I_{SB1}	35	30	mA
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E}$ ≥ V_{CC} − 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{CC} − 0.2 V)	I_{SB2}	12	12	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address and Data Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Output Capacitance	C_{out}	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE TIMING (See Note 1)

Parameter	Symbol		-10		-12		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	10	—	12	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	10	—	12	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	10	—	12	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	3	—	3	—	ns	3,4,5
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	5	0	6	ns	3,4,5

NOTES: 1. $\overline{W}$ is high for read cycle.
2. All read cycle timings are referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, both for a given device and from device to device.
4. Transition is measured ± 200 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected ($\overline{E}$ = V_{IL}).
7. Addresses valid prior to or coincident with $\overline{E}$ going low.

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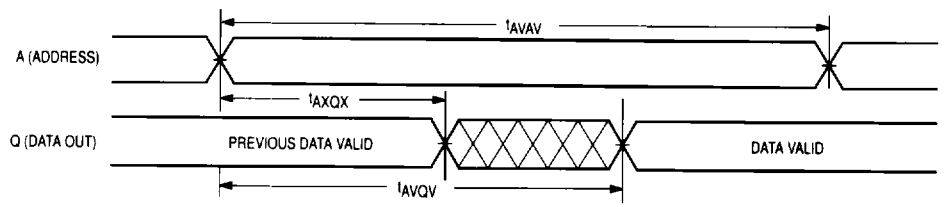
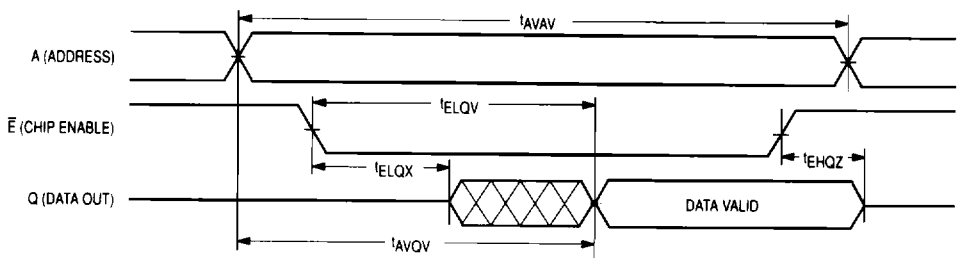
READ CYCLE 1 (See Note 6)



READ CYCLE 2 (See Note 7)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		-10		-12		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	6	—	7	—	ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	t_{WP} t_{WP}	6	—	7	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	5	0	6	ns	3,4,5
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES: 1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ± 200 mV from steady-state voltage with load of Figure 1B.
4. This parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol		-10		-12		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	10	—	12	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	7	—	8	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	7	—	8	—	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	7	—	8	—	ns	3,4
Data Valid to End of Write	t_{DVEH}	t_{DW}	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES: 1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timings are referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high-impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high-impedance condition.

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AC TEST LOADS

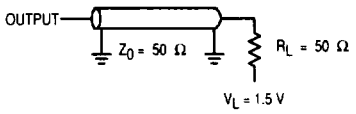

Figure 1A

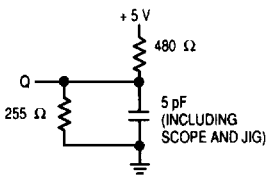

Figure 1B

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

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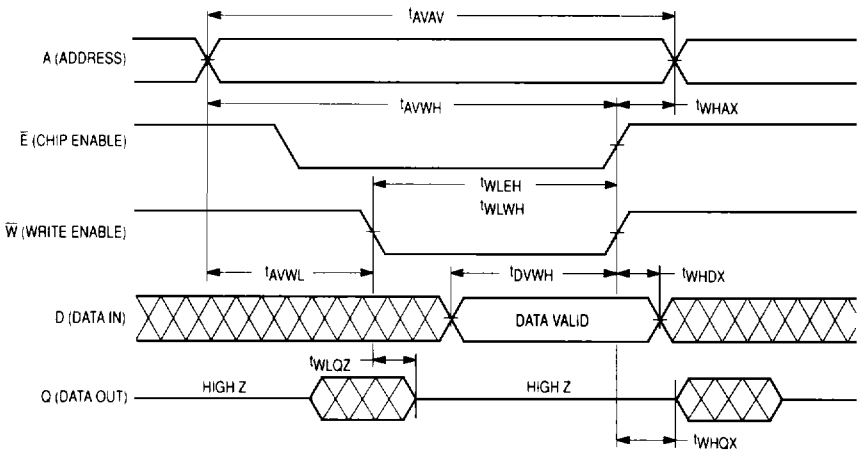
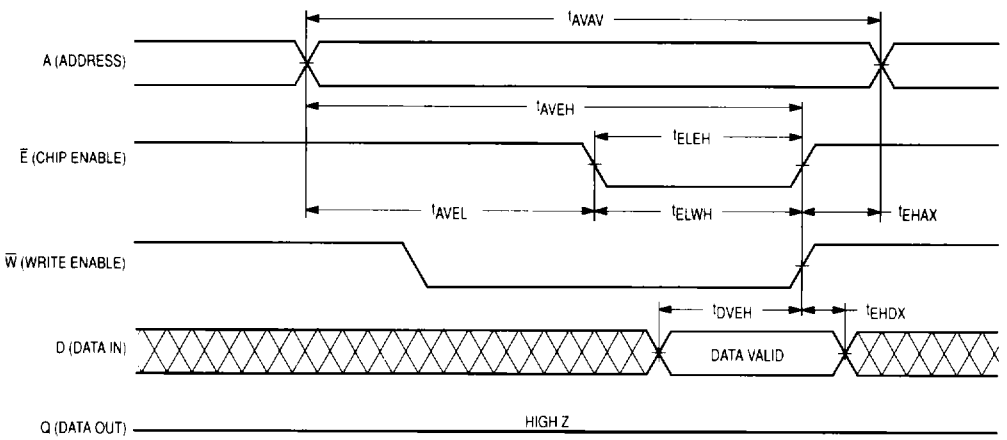
WRITE CYCLE 1



WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM	67282	WJ	XX	XX
Motorola Memory Prefix				
	Part Number			
		Package (WJ = 400-mil SOJ)		
			Speed (10 = 10 ns, 12 = 12 ns)	
				Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Number — MCM67282WJ10 MCM67282WJ12
MCM67282WJ10R2 MCM67282WJ12R2