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SSI 32P4920

PRML Read Channel with PR4, 8/9 ENDEC, 4-burst Servo Demodulator

Target Specification

February 1996

4

DESCRIPTION

The SSI 32P4920 is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire Partial Response Class 4(PR4) read channel for zoned recording hard disk drive systems with data from 65-200 Mbits/s.

Functional blocks include AGC, a continuous time programmable filter, FIR transversal filter, Viterbi qualifier, 8/9 GCR ENDEC, data synchronizer, time base generator, servo detector, four-burst servo demodulator. Programmable functions such as data rate, filter cutoff, filter boost, etc. are controlled by writing to the serial port registers so no external component changes are required to change zones. The part requires a single +5V supply.

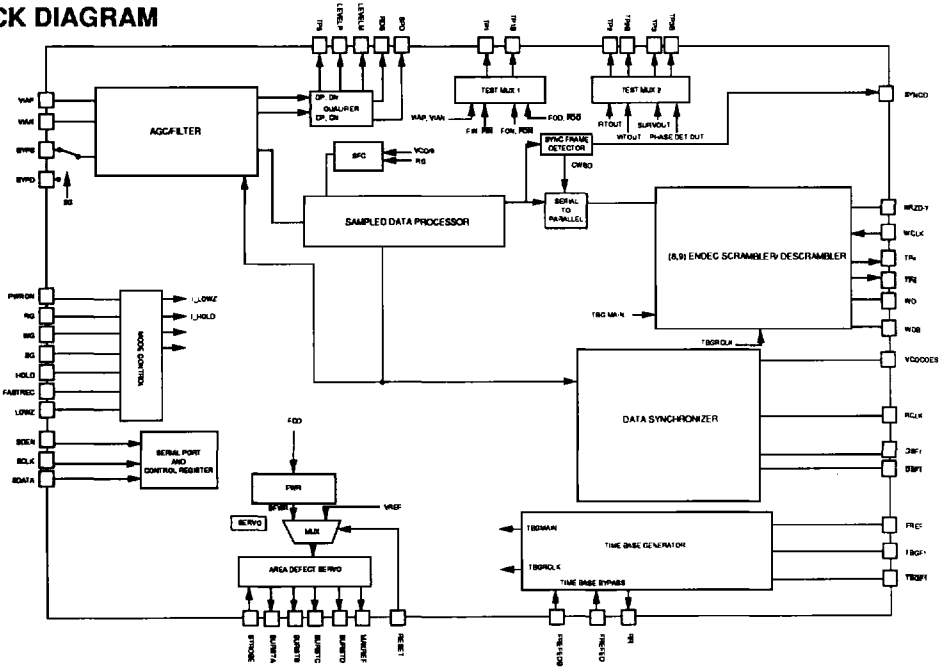
The SSI 32P4920 utilizes an advanced BiCMOS technology which, along with advanced circuit design techniques, result in a high performance device with low power consumption.

FEATURES

- **Register programmable data rates from 62-200 Mbit/s**
- **Sampled data read channel with Viterbi qualification**
- **Continuous time programmable filter**
- **Five tap transversal filter for PR4 equalization**
- **8/9 GCR ENDEC**
- **Data scrambler/descrambler**
- **Dual Level programmable write Precompensation**
- **Low operating power dissipation (1.46 W peak @ 5V)**

(continued)

BLOCK DIAGRAM



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FEATURES (continued)

- Register programmable power management (5 mW power down mode)
- Byte-wide bi-directional NRZ data interface
- Serial port interface for access to internal program storage registers
- Small footprint 100-lead VTQFP package
- Dynamic Power Management

AUTOMATIC GAIN CONTROL

- 1 Vp-pd capture voltage in read mode
- Programmable capture voltage in servo mode
- Dual mode AGC loop: continuous time during acquisition, sampled time during tracking
- Separate AGC level storage pins (BypD, BypS) for read and servo mode
- Dual rate attack and decay charge pump for rapid AGC recovery
- Fast Recovery mode with additional (user defined)Ultrafast Decay mode
- Charge pump currents track programmable data rate (idle and acquisition)
- Programmable, symmetric charge pump currents (tracking)
- Low drift AGC hold circuitry
- Wide bandwidth, precision full-wave rectifier
- Programmable LowZ & Fast Recovery time constants with external override (LowZ, FastRec and Hold)
- Separate registers define LowZ time constant for data and servo mode
- OpenZ feature allows optimization of AGC recovery

CONTINUOUS TIME FILTER

- Programmable 7-pole continuous-time filter provides:
  - Channel filter and pulse slimming equalization
  - Programmable cutoff frequency: 18 - 56 MHz in data mode
  - Programmable cutoff frequency: 5 - 25 MHz in servo mode
  - Programmable boost/equalization of 0 to 12 dB
  - Programmable phase equalization of ± 20% total delay
  - Independent controls for data and servo modes (Fc, Group Delay Equalization and Boost)
  - Fast switching recovery between data and servo modes
  - On chip calibration yields high accuracy cutoff frequency settings

FIR FILTER

- Five tap transversal filter for fine equalization to PR4
- Fully programmable taps
- LMS adaptation
- MSE output provides a measure of channel equalization quality

PULSE QUALIFICATION

- Sampled two states interleaved Viterbi qualification of signal equalized to PR4
- Programmable threshold
- Absolute or relative threshold mode
- Peak Detection qualification (Servo Gray code detection)
- Hysteresis or Dual comparator qualification strategy selectable through the serial port
- Independent positive and negative threshold settings in servo for use with asymmetrical amplitude signals (e.g. from MR heads)
- RdS and SpI outputs

TIME BASE GENERATOR

- Better than 0.5% frequency resolution
- Up to 280 MHz frequency output
- Less than ± tbd jitter
- Independent 8-bit M and N divide-by registers
- On chip calibration circuit
- Single external capacitor required for the loop filter
- Programmable damping factor
- Programmable bandwidth
- Programmable high frequency pole

CLOCK RECOVERY CIRCUITRY

- Fully integrated data separator includes data synchronizer and 8/9 GCR ENDEC
- Register programmable to 200 Mbit/s operation
- Fast acquisition, sampled data phase lock loop
- Decision directed clock recovery from data samples
- Adaptive clock recovery thresholds for use with asymmetrical amplitude signals (e.g. from MR heads)
- Programmable damping ratio for data synchronizer PLL
- Programmable bandwidth for data synchronizer PLL
- Selectable Gear Shift ratio
- Lead-Lag programmable filter
- Data scrambler/descrambler to reduce fixed pattern effects
- Integrated Sync Byte detection with programmable error threshold
- Byte-wide NRZ data interface
- Two level programmable write precompensation (+ 50%, in 2.5% steps) tracking Time Base VCO
- Differential PECL write data output. Internal Write Flip Flop guarantees operation at max. data rate

SERVO

- Area Detect 4-burst servo capture with A, B, C, D outputs
- Servo burst sequence ABCD or BADC selectable through serial port
- Internal hold capacitors
- External burst gating
- Separate, automatically selected registers for servo mode Fc, Boost and Group Delay Equalization
- Separate Bypass Capacitor for AGC loop during servo mode
- Servo information is derived from either the normal or differentiated filter output (serial port control)

4

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Patents: 5,162,678; 5,063,309
Patents Pending: 08/229354; 08/217435; 08/217493;
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