MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC54/74HC157
MC54/74HC158

Quad 2-Input Data Selectors/ Multiplexers

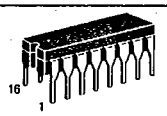
High-Performance Silicon-Gate CMOS

The MC54/74HC157 and HC158 are identical in pinout to the LS157 and LS158. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

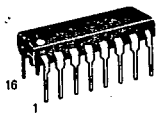
These devices route 2 nibbles (A or B) to a single port (Y) as determined by the Select input. The data is presented at the outputs in noninverted form for the HC157 and inverted form for the HC158. A high level on the Output Enable input sets all four Y outputs to a low level for the HC157 and a high level for the HC158.

The HC157 is similar in function to the HC257 which has 3-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 82 FETs or 20.5 Equivalent Gates (HC157)
  74 FETs or 18.5 Equivalent Gates (HC158)



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-06

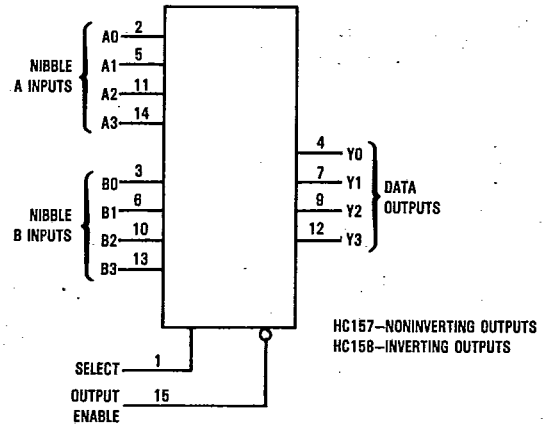
D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74HCXXXN	Plastic
MC54HCXXXJ	Ceramic
MC74HCXXXD	SOIC

T_A = −55° to 125°C for all packages.
Dimensions in Chapter 7.

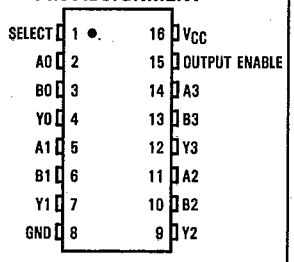
LOGIC DIAGRAM



HC157—NONINVERTING OUTPUTS
HC158—INVERTING OUTPUTS

PIN 16 = V_{CC}
PIN 8 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs Y0-Y3	
Output Enable	Select	HC157	HC158
H	X	L	H
L	L	A0-A3	$\overline{A0\text{-}A3}$
L	H	B0-B3	$\overline{B0\text{-}B3}$

X = don't care
A0-A3, B0-B3 = the levels of the respective Data-Word Inputs.

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MC54/74HC157•MC54/74HC158

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	−1.5 to V_{CC}+1.5	V
V_{out}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC}+0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
	SOIC Package†	500	
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		°C
	(Plastic DIP or SOIC Package)	260	
	(Ceramic DIP)	300	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: −10 mW/°C from 65° to 125°C
Ceramic DIP: −10 mW/°C from 100° to 125°C
SOIC Package: −7 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC}=2.0 V	0	1000	ns
	(Figure 1)	V_{CC}=4.5 V	0	500	
		V_{CC}=6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25°C to −55°C	≤85°C	≤125°C	
V_{IH}	Minimum High-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$ ≤20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low-Level Input Voltage	V_{out}=0.1 V or V_{CC}−0.1 V $\|I_{out}\|$ ≤20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V_{OH}	Minimum High-Level Output Voltage	V_{in}=V_{IH} or V_{IL} $\|I_{out}\|$ ≤20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V_{in}=V_{IH} or V_{IL} $\|I_{out}\|$ ≤4.0 mA	4.5	3.98	3.84	3.70	
		$\|I_{out}\|$ ≤5.2 mA	6.0	5.48	5.34	5.20	
V_{OL}	Maximum Low-Level Output Voltage	V_{in}=V_{IH} or V_{IL} $\|I_{out}\|$ ≤20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V_{in}=V_{IH} or V_{IL} $\|I_{out}\|$ ≤4.0 mA	4.5	0.26	0.33	0.40	
		$\|I_{out}\|$ ≤5.2 mA	6.0	0.26	0.33	0.40	
I_{in}	Maximum Input Leakage Current	V_{in}=V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in}=V_{CC} or GND I_{out}=0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			25°C to −55°C	≤85°C	≤125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1, 2, and 7)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Select to Output Y (Figures 3, 4, and 7)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Output Enable to Output Y (Figures 5, 6, and 7)	2.0	115	145	175	ns
		4.5	23	29	35	
		6.0	20	25	30	
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1, 2, and 7)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C_{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V_{CC} = 5.0 V 33 (HC157) 35 (HC158)	pF

PIN DESCRIPTIONS

INPUTS

A0, A1, A2, A3 (PINS 2, 5, 11, 14) — Nibble A inputs. The data present on these pins is transferred to the outputs when the Select input is at a low level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form for the HC157 and inverted form for the HC158.

B0, B1, B2, B3 (PINS 3, 6, 10, 13) — Nibble B inputs. The data present on these pins is transferred to the outputs when the Select input is at a high level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form for the HC157 and inverted form for the HC158.

OUTPUTS

Y0, Y1, Y2, Y3 (PINS 4, 7, 9, 12) — Data outputs. The selected input Nibble is presented at these outputs when the Output Enable input is at a low level. The data present on these pins is in its noninverted form for the HC157 and inverted form for the HC158. For the Output Enable input at a high level, the outputs are at a low level for the HC157 and at a high level for the HC158.

CONTROL INPUTS

SELECT (PIN 1) — Nibble select. This input determines the data word to be transferred to the outputs. A low level on this input selects the A inputs and a high level selects the B inputs.

OUTPUT ENABLE (PIN 15) — Output Enable input. A low level on this input allows the selected input data to be presented at the outputs. A high level on this input sets all outputs to a low level for the HC157 and to a high level for the HC158.

MC54/74HC157•MC54/74HC158

SWITCHING WAVEFORMS

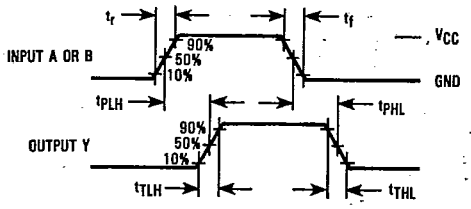


Figure 1. HC157

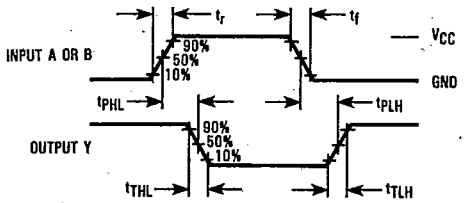


Figure 2. HC158

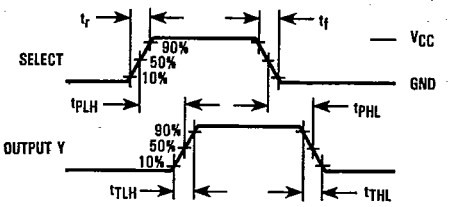


Figure 3. Y vs Select, Noninverted

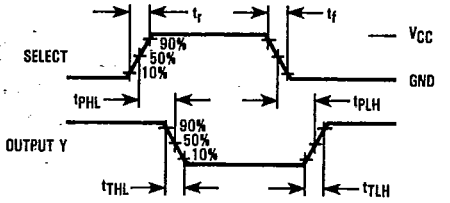


Figure 4. Y vs Select, Inverted

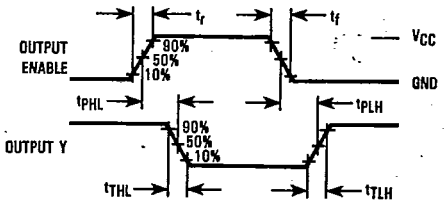


Figure 5. HC157

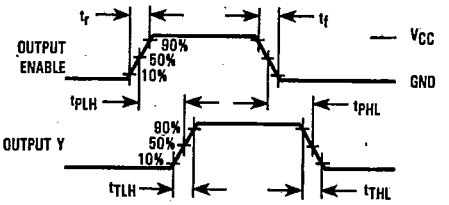
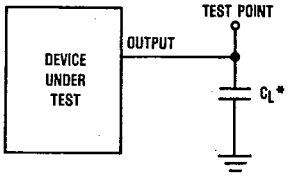


Figure 6. HC158



*Includes all probe and jig capacitance.

Figure 7. Test Circuit

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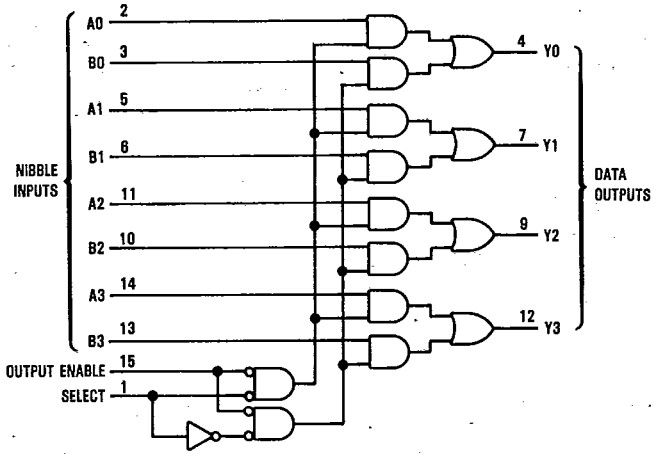
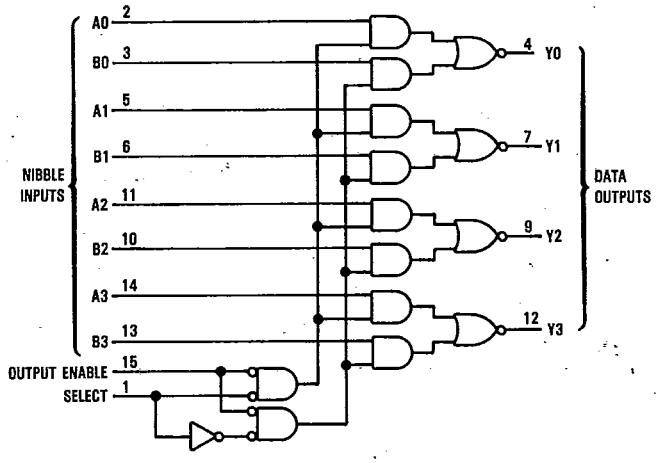
EXPANDED LOGIC DIAGRAMS



HC157



HC158

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