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INNOVATORS IN INTEGRATION

SSI 6020 10-Bit Tracking A-to-D Converter

Data Sheet

006652

GENERAL DESCRIPTION

Silicon Systems' new SSI 6020 tracking analog-to-digital converter contains an on-chip 2.5 volt bandgap reference; a reference amplifier which supplies the reference input to a current-switching DAC; an up/down counter with high speed window comparator and tracking logic, and a data output shift register/latch. The DAC is comprised of a current-switching array and a matrix of diffused resistors which do not require trimming.

SSI 6020 is made in mature bipolar technology, and is well suited for uses in robotics, avionics, process and industrial controls to digitize changing analog values.

FEATURES

- **10 bit accuracy**
- **3 temperature ranges**
- **TTL and CMOS compatible**
- **±5V supplies**
- **1 µsec conversion time (continuous tracking)**
- **On-chip reference with amplifier**
- **Input range as desired**
- **Parallel and serial outputs**
- **Rugged bipolar construction**

GENERAL CIRCUIT OPERATION

Figure 2 shows the typical connection of external components required to produce a fully functional tracking analog to digital converter. This example illustrates the use of the internal precision reference. However, an external reference voltage can be used and may vary by + or − 20% of the nominal value for ratiometric operation. Figure 3 shows the logic configuration of the converter. The comparator and control logic are configured as a window detector that provides the up or down clocks to the counter. Whenever the analog input voltage is outside of the window range, the comparator and control logic provide the correct up or down clock to enable the counter and DAC output to track the change in analog input. The counter is incremented or decremented on the negative going transition of the main clock input. When the analog input voltage is inside the window range, the clock to the up/down counter is inhibited and the count value remains the same.

Parallel data from the counter will be loaded into the output data latch/shift register when the TRANSFER DATA input is taken HIGH. The minimum pulse width for the TRANSFER DATA signal is 50 nanoseconds. TRANSFER DATA should not be taken HIGH until 150 nanoseconds after the MAIN CLOCK edge and should go LOW before the next MAIN CLOCK edge.

If the TRANSFER DATA input is held HIGH, the counter outputs will appear directly at the bit outputs. Serial output data (MSB first) can be clocked out of the MSB output (pin 27) by applying a clock signal to the DATA CLOCK input (pin 16). Data are clocked out of shift register on the negative going transition of the DATA CLOCK. The maximum clock frequency is limited to 1 MHz, with a minimum pulse width of 100 nano-seconds.

The SEND DATA (pin 17) must be HIGH to produce the serial output. When the SEND DATA input is LOW, the DATA CLOCK is inhibited. All the output transistors are turned off resulting in all outputs being HIGH.

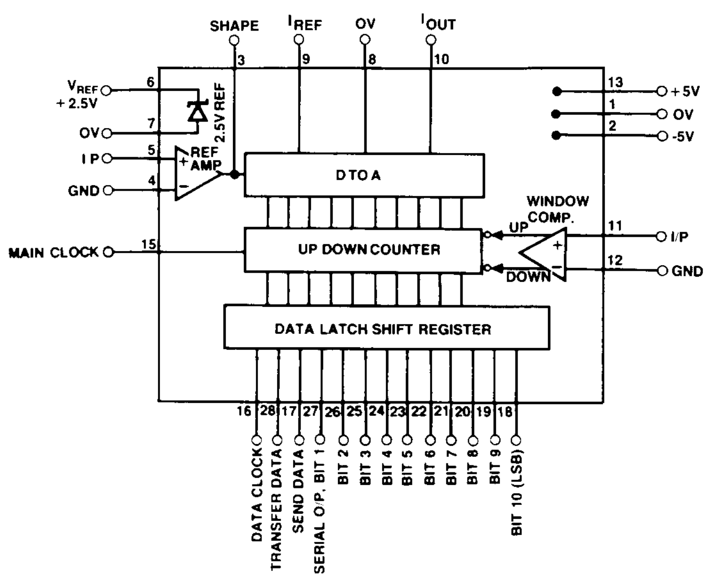

Figure 1 Circuit Diagram

SSI 6020
10-Bit Tracking D-to-A Converter

ABSOLUTE MAXIMUM RATINGS

Supply voltage .... ±7 volts
Logic input voltage............. $+V_{CC}$ and 0V
Storage temperature range .... −55° to +125°C

Ordering Info.	Package	Temp. Range
SSI 6020 MDE	Ceramic 28 Pin Dual In Line	−55°C to +125°C
SSI 6020 IDE	Ceramic 28 Pin Dual In Line	−40°C to +85°C
SSI 6020 CDE	Ceramic 28 Pin Dual In Line	0°C to +70°C

CHARACTERISTICS (at ±5V supplies and internal reference unless otherwise specified)

Parameter	Version	T_{AMB} = +25°C			Over Spec. Temp. Range		Units	Conds.
		Min.	Typ.	Max.	Min.	Max.		
Converter Accuracy (useful resolution)	6020 MDE 6020 IDE 6020 CDE	10			10		bits	*Note 1*
Non-linearity	All types			±0.5			LSB	
Differential non-linearity	All types		±0.5				LSB	*Note 1*
Operating temperature range	6020 MDE				−55	+125	°C	
	6020 IDE				−40	+85	°C	
	6020 CDE				0	+70	°C	
D to A reference current I_{REF} (pin 9)	All types	0.8		1.2	0.8	1.2	mA	*Note 2*
Max. clock rate	All types	1	1.2		1		MHz	*Note 3*
Nominal analog input range	All types	−2.5		+2.5			V	*Note 4*
Supply rejection	All types		0.1				% per V	

(continued on page 5)

Note 1: No missing codes over full temperature range at resolution appropriate to accuracy.
Note 2: The full scale D to A output current I_{OUT} = 4 times I_{REF}. For optimum performance I_{REF} = 1.0 mA.
Note 3: For main clock waveform see Figure 3. Input signals which do not change by more than 1 LSB/μs may be tracked continuously without the need for a sample and hold. This corresponds to a full scale bandwidth of 300 Hz. Higher frequencies may be tracked if the amplitude is reduced, e.g. the half full scale bandwidth is 600 Hz.
Note 4: Single polarity and other input ranges may be provided by different input resistor values (see Table 1). Contact SSI Applications Department.
Note 5: Excluding reference.
Note 6: For typical temperature performance see Figure 6.

CALCULATING VALUES OF EXTERNAL RESISTORS

Refer to the diagram in Figure 2. The reference amplifier and comparator are both operated in a virtual ground mode with R1 and R2 supplying the bias currents. Thus, R1 = R3, and R2 is equal to the parallel combination of R4, R5 and R6 at the plus input to the comparator.

High quality resistors are required for R3, R4, and R5 as these resistors can affect the gain and offset stability of the circuit.

I_{REF} should be 1.0 mA, but may be varied from 0.8 mA to 1.2 mA. Using the value of $I_{REF} = 1.0$ mA, the value of R3 can be calculated from $R3 = V_{REF}/I_{REF}$. Full scale I_{OUT} is equal to four times I_{REF} and has a value of 4 mA (I_{OUT} is 0 mA for zero reading). Analysis of the network gives the values for R4 and R5 as $R4 = -V_{REF}\ R5/V_{IN\ MIN}$. $R5 = (V_{IN\ MAX} - V_{IN\ MIN})/I_{OUT}$ full scale, where $V_{IN\ MAX}$ is the voltage for the digital output to be all HIGH, and $V_{IN\ MIN}$ is the voltage for the digital output to be all LOW. The value of R6 is chosen so that the parallel combination of R4, R5 and R6 is about 625 ohms; this will determine the digital-to-analog time constant and therefore the conversion time.

For calibration, the offset is adjusted by R4. The gain is adjusted by R3.

For unipolar operation where the value of R4 approaches infinity and a zero adjustment is required, the offset circuit in Figure 4 is suggested as a replacement for R4 (typical values only).

The above equations are tabulated for various input ranges and reference values. This is shown in Table 1.

LOGIC CODING

The logic coding for unipolar and bipolar operation is shown in Tables 2 and 3. FS in the tables is the full scale value and the analog inputs shown are nominal center values of code.

CALIBRATION PROCEDURE

Unipolar Operation

The offset and gain are adjusted by supplying an analog input of 0.5LSB for transition 0000000000 to 0000000001, and a value of Full Scale - 1.5LSB for transition 1111111111 to 1111111110.

Bipolar Operation

The offset and gain are adjusted by supplying an analog input of −(Full scale - 0.5LSB) for transition 0000000000 to 0000000001, and a value of Full scale - 1.5LSB for transition 1111111111 to 1111111110.

DYNAMIC CROSSPLOT TESTING

Figure 5 shows a typical setup for dynamic crossplot testing of the device. A 12 bit reference digital-to-analog converter is used to provide a programable input voltage to select the point of interest to be displayed on an oscilloscope. A triangle waveform generator with a peak to peak amplitude of + or − 4 times the LSB value is used to provide the X deflection to the scope, and is added to the output voltage produced by the reference DAC at the summing junction of the operational amplifier. The resulting analog signal is fed from the output of the operational amplifier to the input of the device under test. A 3 bit digital to analog converter with at least 6 bit accuracy is used to convert the bit 10, 9, and 8 outputs of the device under test into an analog signal which is applied to the vertical (Y) input of the display scope. Any differential non-linearity will be shown by horizontal lines which are shorter or longer than the rest.

Table 1

$V_{IN\ MAX}$	$V_{IN\ MIN}$	V_{REF}	$R_1$1	$R_2$1	R_3	R_4	R_5	$R_6$1
+2.5	−2.5	2.5	2.5KΩ	625Ω	2.5KΩ	1.25KΩ	1.25KΩ	∞
+2.5	−2.5	5*	5KΩ	625Ω	5KΩ	2.5KΩ	1.25KΩ	2.5KΩ
+2.5	0	2.5	2.5KΩ	625Ω	2.5KΩ	∞	625Ω	∞
+5	0	2.5	2.5KΩ	625Ω	2.5KΩ	∞	1.25KΩ	1.25KΩ
+4	−2	2.5	2.5KΩ	625Ω	2.5KΩ	1.875KΩ	1.5KΩ	2.5KΩ
+4	−2	12*	12KΩ	625Ω	12KΩ	1.875KΩ	1.5KΩ	2.5KΩ
+10	−10	2.5	2.5KΩ	625Ω	2.5KΩ	1.25KΩ	5KΩ	1.67KΩ

Note 1: Nearest preferred value may be used for R_1, R_2 and R_6
*Note 2: External reference

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LOGIC CODING

Table 2 Unipolar Operation

Analog Input*	Digital Output Code MSB LSB
FS − 1LSB	1111111111
FS − 2LSB	1111111110
¾FS	1100000000
½FS + 1LSB	1000000001
½FS	1000000000
½FS − 1LSB	0111111111
¼FS	0100000000
1LSB	0000000001
0	0000000000

*Analog inputs are nominal center values of code.

Table 3 Bipolar Operation

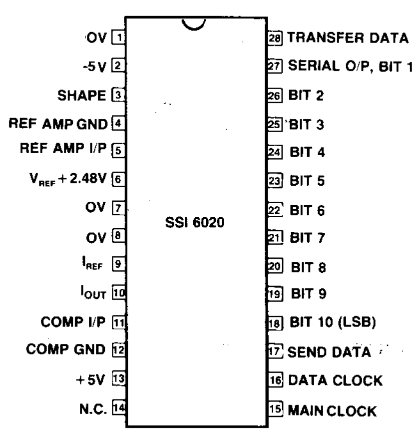
Analog Input*	Digital Output Code MSB LSB
+(FS − 1LSB)	1111111111
+(FS − 2LSB)	1111111110
+(½FS)	1100000000
+(1LSB)	1000000001
0	1000000000
−(1LSB)	0111111111
−(½FS)	0100000000
−(FS − 1LSB)	0000000001
−FS	0000000000

NOTES ON LOGIC SYSTEM:

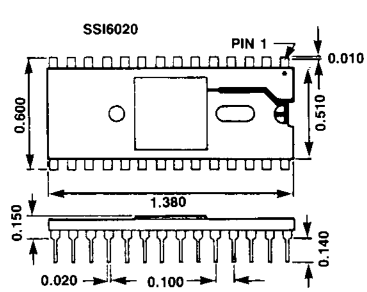
1. The Window Comparator and Control Logic determine whether the Counter will clock up or down to keep the same value on an active (negative going) edge of the Main Clock.
2. Parallel data from the Up/Down Counter will be loaded into the output Data Latch/Shift Register when the TRANSFER DATA input is HIGH. TRANSFER DATA should not be taken HIGH until 150 ns after the MAIN CLOCK edge and should go LOW before the next MAIN CLOCK edge. The minimum TRANSFER DATA pulse width is 50 ns.

   If TRANSFER DATA is held HIGH, then the Counter outputs will appear directly at the bit outputs.
3. Serial output data (MSB first) can be obtained from the MSB output (pin 27) by applying a DATA CLOCK (pin 16, 1 MHz maximum, 100 ns minimum pulse width).
4. A LOW on SEND DATA (pin 17) disables the DATA CLOCK and turns off all the output transistors so that all the bit outputs are HIGH (see diagram of output).

PIN CONNECTIONS



PACKAGE DETAILS
Dimensions in inches



ELECTRICAL CHARACTERISTICS (continued)

Parameter	Version	T_{AMB} = +25°C Min.	Typ.	Max.	Over Spec. Temp. Range Min.	Max.	Units	Conds.
Gain temperature coefficient *(Note 5)*			10				ppm/°C	
Zero temperature coefficient	All types		7				ppm/°C of FSR	
Supply voltage	All types	±4.5	±5	±5.5	±4.5	±5.5	V	
Supply current	All types		50				mA	
Power consumption	All types		500				mW	
Internal Voltage Reference Output voltage	All types		2.480				V	
Output voltage tolerance *(Note 6)*	All types			±1.5			%	
Slope impedance	All types		0.75				Ω	
Maximum reference load current			±4				mA	
Logic High level input voltage	All types	2.0			2.0		V	
Low level input voltage				0.8		0.8	V	
High level input current			7				μA	$V_S = \pm 5.5V$ $V_1 = 2.4V$
			50				μA	$V_S = \pm 5.5V$ $V_1 = 5.5V$
Low level input current			1				μA	$V_S = \pm 5.5V$ $V_1 = 0.4V$
High level output voltage		2.4			2.4		V	$I_{LOAD} = -40\mu A$
Low level output voltage				0.4		0.4	V	$I_{LOAD} = 1.6mA$

TYPICAL TEMPERATURE CHARACTERISTIC

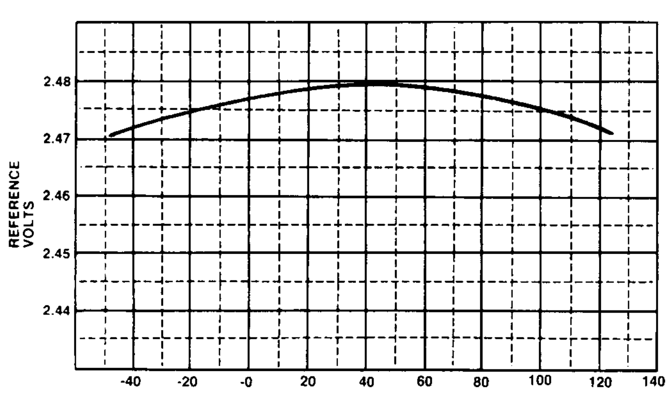


Figure 6 Typical Reference Voltage versus Temperature (All Types)

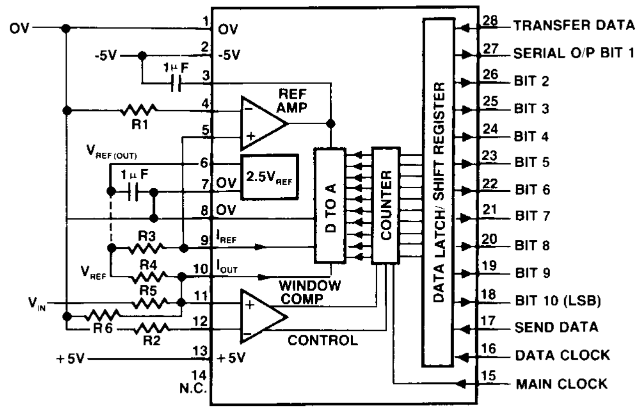


Figure 2 Typical External Components

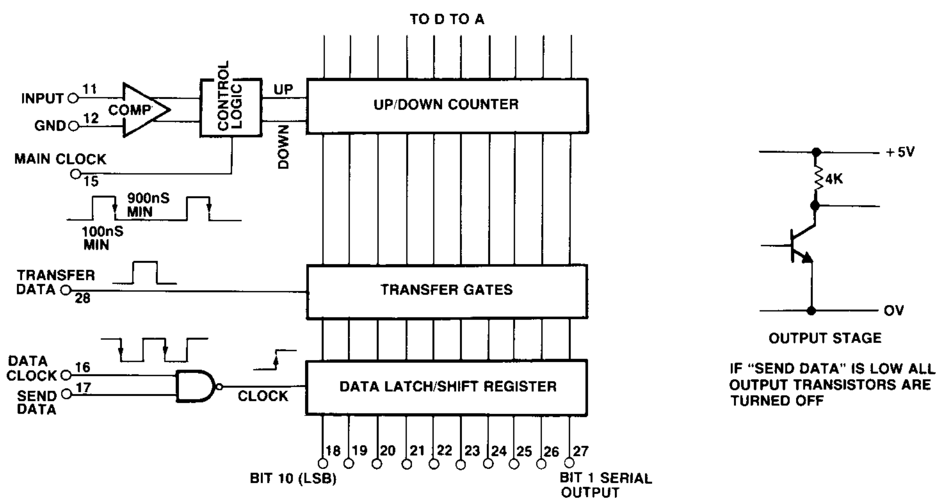


Figure 3 Logic System

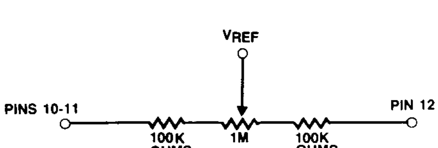


Figure 4 Offset Circuit with Unipolar Operation

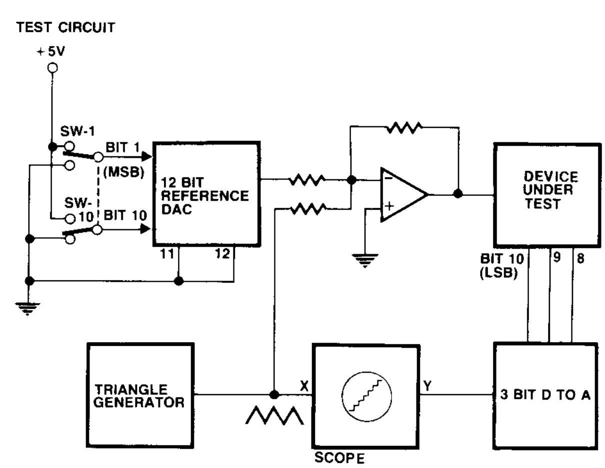


Figure 5 Dynamic Crossplot Accuracy Test