Delta Sheet, DS 9, Nov. 2001

# DFE-Q V2.1 Quad ISDN 2B1Q Echocanceller Digital Front End

## PEF 24911 Version 2.1


Wired Communications

Infineon technologies

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| | | |
|---|---|---|
| **PEF 24911** | | |
| **Revision History:** | **2001-11-08** | DS 9 |
| Previous Version: | 06.01 | DS 8 |
| Major changes since last revision:<br>Added notes and tables on test modes<br>Refined description of Digital Local Loops<br>Added description 'Hardware Reset Execution'<br>Added description MONITOR receiver timing to chapter Recognition Delay | | |
| Previous Version: | 03.01 | DS 7 |
| Major changes since last revision:<br>Activation with C/I-command AR0: UOA is set to binary 1.<br>C/I-Command LTD will be supported in V2.1 (same function as in V1.3)<br>New function: Disable Super Frame Marker introduced on pin 16: DSFM<br>Refined description of pin 49: CRCON<br>MON-8-Command PACE: added restriction 'Local Loop Testmode'<br>BER description refined (zeros must be sent by the user) | | |
| Previous Version: | 12.00 | DS 6 |
| Major changes since last revision:<br>Added differences in M4 filtering with pin CRCON<br>Added differences with MON8 PACE | | |
| Previous Version: | 09.00 | DS 5 |
| Major changes since last revision:<br>MTO Function removed<br>State Diagram updated | | |
| Previous Version: | 06.00 | DS 4 |
| Major changes since revision 05.99:<br>Typical values of Power Consumption added<br>Delay for Recognition of C/I code changed 2nd time<br>MON 8 Messages in State 'Reset' | | |
| | | |

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Table of Contents Page

**This Delta Sheet lists the add-on features and differences between the DFE-Q V2.1 and the DFE-Q V1.3.**

# 1 Power Supply

The DFE-Q V2.1 requires a +3.3 V ±0.3 V power supply. The inputs and outputs remain 5 V TTL compatible.

**Table 1 Power Consumption**

| Mode | Typ. values | Max. values | Unit | Test conditions |
|---|---|---|---|---|
| Power-up<br>all Channels | 85 | 100 | mA | 3.3 V, open outputs, inputs at $V_{DD}$ /$V_{SS}$ |
| Power-down | 35 | t.b.d. | mA | 3.3 V, open outputs, inputs at $V_{DD}$ /$V_{SS}$ |

All measurements of the power consumption are performed with random 2B+D data in active states, 3.3 V (0° C - 70° C)

# 2 Pinning

Table 2 lists the changes that were made concerning the pinning, Table 3 specifies new pin functions that were introduced with version 2.1.

**Table 2 Pinning Changes**

| Pin No. | V2.1 | V1.3 | Comment |
|---|---|---|---|
| 16 | DSFM | TPD | new function for suppression of short FSC evaluation |
| 32 | PUP | N.C. | additional push-pull mode for pin DOUT eases interface adaptation |
| 36 | n.c. | DSYNC | obsolete |
| 55 | SLOT0 | SLOT | renamed |
| 45 | SLOT1 | N.C. | increased max data rate (4 MBit/s) requires an additional SLOT pin |
| 49 | CRCON | CRCON | see Chapter 7 |
| 53 | LT | LT | dedicated LT mode pin is obsolete |
| 56 | SSP | TSP | dedicated pin for 'Send Single Pulses' test mode |
| 58 | PBX | PBX | function removed |
| 62 | DT | TP | dedicated pin for 'Data Through' test mode |
| 63 | $\overline{\text{TRST}}$ | TP1 | BScan power-on-reset is replaced by a dedicated reset line |

**Table 3 Pin Definitions and Functions**

| Pin No. | Symbol | Input (I) Output (O) | Function |
|---|---|---|---|
| 16 | DSFM | I (PD) | Disable Super Frame Marker<br>'1' = Inhibits the evaluation of the super frame marker on FSC. I.e the transmitted super-frame is not affected by an FSC pulse shorter than 2 DCL clock periods.<br>'0' = The position of the transmitted super-frame is synchronized to short FSC pulses. |
| 32 | PUP | I (PD) | Push Pull Mode<br>in push pull mode '0' and '1' is actively driven during an occupied time-slot, outside the active time-slots DOUT is high impedance (tristate)<br><br>'1'= configures DOUT as push/pull output<br>'0'= configures DOUT as open drain output |
| 49 | CRCON | I (PD) | CRC Check On/Off<br>defines the condition on which MON-2 messages and M4 bit will be passed on, the setting has effect on all ports<br>Pin CRCON is evaluated only after hardware reset.<br>'1'= CRC Check On<br>MON-2 messages are not issued and M4-bit are not forwarded to the statemachine if the CRC-check of the U-superframe containing M4-bit changes is not ok.<br>(MFILT= 0011 0xxx)<br>'0'= CRC Check Off<br>MON-2 messages are issued every time a change in at least one of the overhead bits (M4,5,6) of the U-interface is detected, regardless of the CRC checksum status.<br>M4-bit are forwarded to the statemachine with triple-last-look filtering (TLL).<br>(MFILT= 0000 0xxx) |

**Table 3 Pin Definitions and Functions** (cont'd)

| Pin No. | Symbol | Input (I) Output (O) | Function |
|---|---|---|---|
| 55 | SLOT0 | I | IOM®-2 Channel Slot Selection 0<br>assigns IOM®-2 channels in blocks of 4<br><br>SLOT1, 0:<br>'00'= IOM®-2 channels 0 to 3<br>'01'= IOM®-2 channels 4 to 7<br>'10'= IOM®-2 channels 8 to 11<br>'11'= IOM®-2 channels 12 to 15 |
| 45 | SLOT1 | I<br>(PD) | IOM®-2 Channel Slot Selection 1<br>assigns IOM®-2 channels in blocks of 4 |
| 53 | LT | I | reserved, clamp to one |
| 56 | SSP | I | Send Single Pulses (SSP) Test Mode<br>enables/disables SSP test mode<br><br>'1'= SSP test mode enabled,<br>alternating +/-3 pulses are issued at the four line ports in 1.5 ms intervals<br>'0'= SSP test mode disabled<br>*Note: For activation of SSP test mode, pin $\overline{RES}$ and pin DT must be inactive (see **Table 5**)* |
| 58 | PBX | I | reserved, clamp to zero |

**Table 3 Pin Definitions and Functions** (cont'd)

| Pin No. | Symbol | Input (I) Output (O) | Function |
|---|---|---|---|
| 62 | DT | I | Data Through (DT) Test Mode<br>enables/disables DT test mode<br><br>'1'= DT test mode enabled,<br>the U-transceiver is forced on all line ports to enter the 'Transparent' state<br>'0'= DT test mode disabled<br>*Note: For activation of DT test mode, pin $\overline{RES}$ and pin SSP must be inactive (see **Table 5**)* |
| 63 | $\overline{TRST}$ | I<br>(PU) | JTAG Boundary Scan Disable<br>resets the TAP controller state machine (asynchronous reset), internal pullup<br><br>'1'= reset inactive<br>'0'= reset active |

PU:Pull Up (e.g. 10-20 kOhms)

PD:Pull Down (e.g. 10-20 kOhms)

## Pin-Controlled Test Modes

**Table 4 Pin Controlled Test Modes with DFE-Q V1.x**

| Mode | RESQ Pin | TSP Pin |
|---|---|---|
| Reset (Master Reset) | 0 | 0 |
| Data-Through | 0 | 1 |
| Send-Single-Pulses | 1 | 1 |

**Table 5 Pin Controlled Test Modes with DFE-Q V2.1**

| Mode | $\overline{\text{RES}}$ Pin | SSP Pin | DT Pin |
|---|---|---|---|
| Reset (Master Reset) | 0 | don’t care | don’t care |
| Data-Through | 1 | 0 | 1 |
| Send-Single-Pulses | 1 | 1 | 0 |
| Undefined | 1 | 1 | 1 |

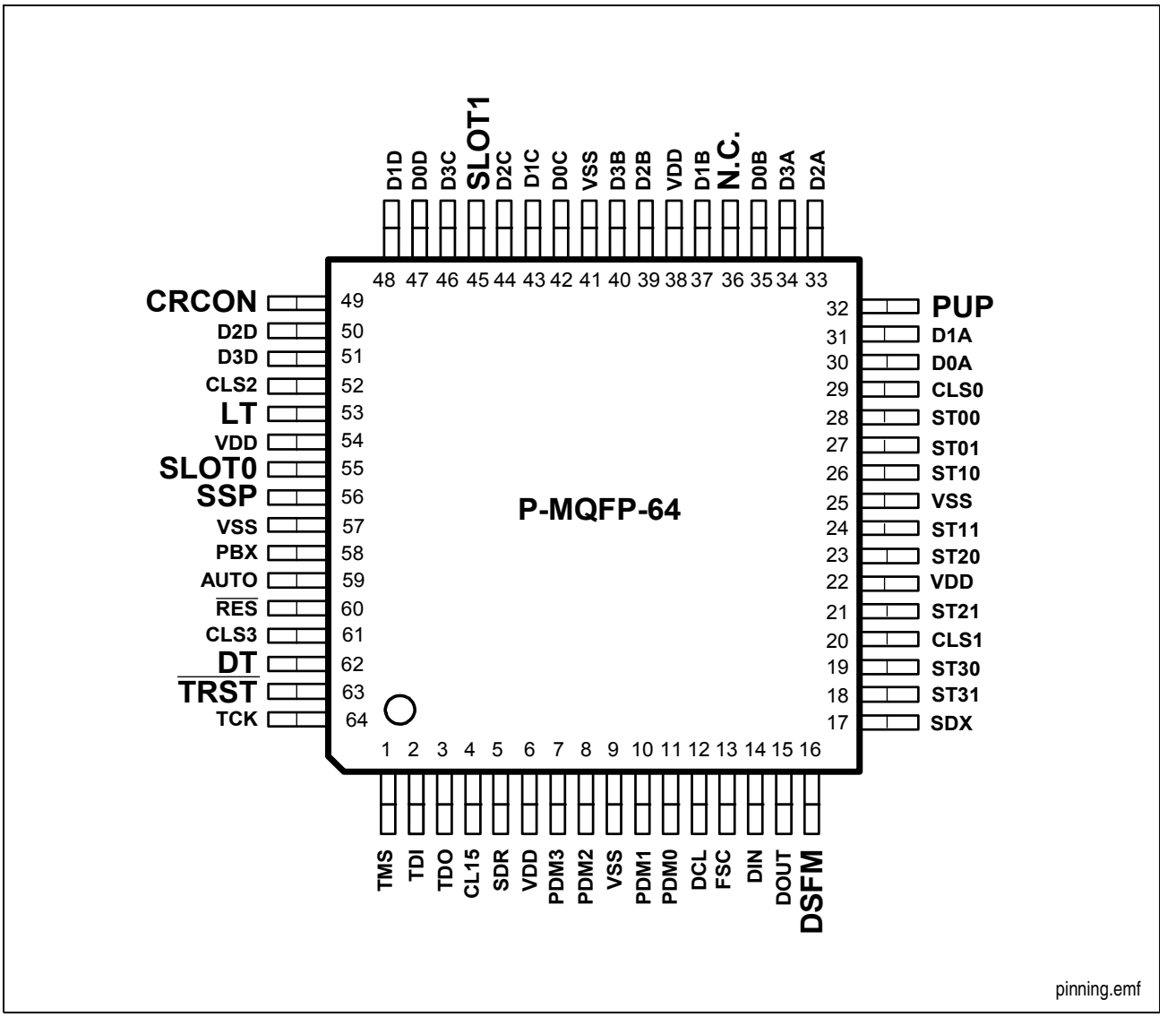


**Figure 1 Pin Diagram of the DFE-Q V2.1**

# 3 Max. Data Rate On IOM®-2 Doubled

With version 2.1 the maximum data rate on IOM®-2 is doubled from 2 MBit/s to 4MBit/s. The 4MBit/s mode corresponds to a DCL frequency of 8192 kHz.

# 4 MON-12 Protocol

MON-12 commands feature via the IOM®-2 Monitor channel direct access to the device internal register map. The MON-12 protocol works in the manner of a serial microprocessor interface.

New functions such as digital local loopbacks, BER measurement etc. are only accessible via MON-12 commands. Functions that were so far provided via MON-8 commands, e.g. FEBE/NEBE counter status retrieval, can be accessed as well via the MON-12 protocol. For a detailed description of the register set please refer to the data sheet of the DFE-Q V2.1

# 5 Bit Error Rate Measurement

For bit error rate monitoring the DFE-Q V2.1 features an 16-bit Bit Error Rate counter (BERC) per line. As soon as the BER function is enabled, the user must send zeros in the selected channels and incoming ones are counted until the BER function has been disabled again by the user.

# 6 Advanced Filter Options for MON-0 and MON-2 Messages

Additionally to the existing mode pins, AUTO and CRCON, the internal MFILT register provides a wide range of filter options for the passing on of MON-0 and MON-2 messages. The new MON-12 protocol gives access to the MFILT register. The following options are provided,

| | | |
|---|---|---|
| – MON-0: | Transparent (no filtering), On Change, TLL (Triple-Last-Look) | in EOC transparent mode |
| | TLL | in EOC automode |
| – MON-2: | On Change, TLL, CRC, CRC & TLL | vs. IOM®-2 |

*Note: The same filter options: On Change, TLL, CRC, CRC & TLL for reporting of M4 bit changes towards the State Machine may be selected.*

# 7 M4 Bit Filtering with Pin CRCON

The M4 bit filtering selected with pin CRCON='0' in version 2.1 is different to previous versions:

**Table 6 M4 Bit Filtering of Different DFE-Q Versions**

| | | M4 Filtering towards: | |
|---|---|---|---|
| **Version** | **Pin CRCON** | **Statemachine** | **MON-2 Reporting** |
| 1.2 | not supported | CRC-check | On-change |
| 1.3 | '0' (PD): | CRC-check | On-change |
| | '1': | CRC-check | CRC-check & on-change |
| 2.1 | '0' (PD): | TLL-check | On-change |
| | '1': | CRC-check | CRC-check & on-change |

With the new M4 filter option Triple-Last-Look (TLL) towards the statemachine the DFE-Q V2.1 conforms to Bellcore requirement TR-NWT-397 (1993). However, in case of very high bit error rates or occurrence of micro interruptions, the DFE-Q V2.1 issues C/I-indications different to 'AI' (e.g. 'EI2', 'UAI') due to forged M4 bits. Therefore, selection of CRCON='1' is recommended for DFE-Q V2.1.

# 8 Digital Local Loops

Besides the remote loopback stimulation and the local analog loopback (C/I= ARL) the DFE-Q V2.1 features digital local loopbacks via its internal register set. The local loopbacks that are additionally provided by the LOOP register are shown in **Figure 2**. The local loops LB1, LB2 and LBBD can be activated at any time independent of the current activation status using the MON-12 protocol. Before loop DLB may be closed, the DFE-Q V2.1 must be in a transparent state, e.g. by applying C/I-command 'Data Through DT'.

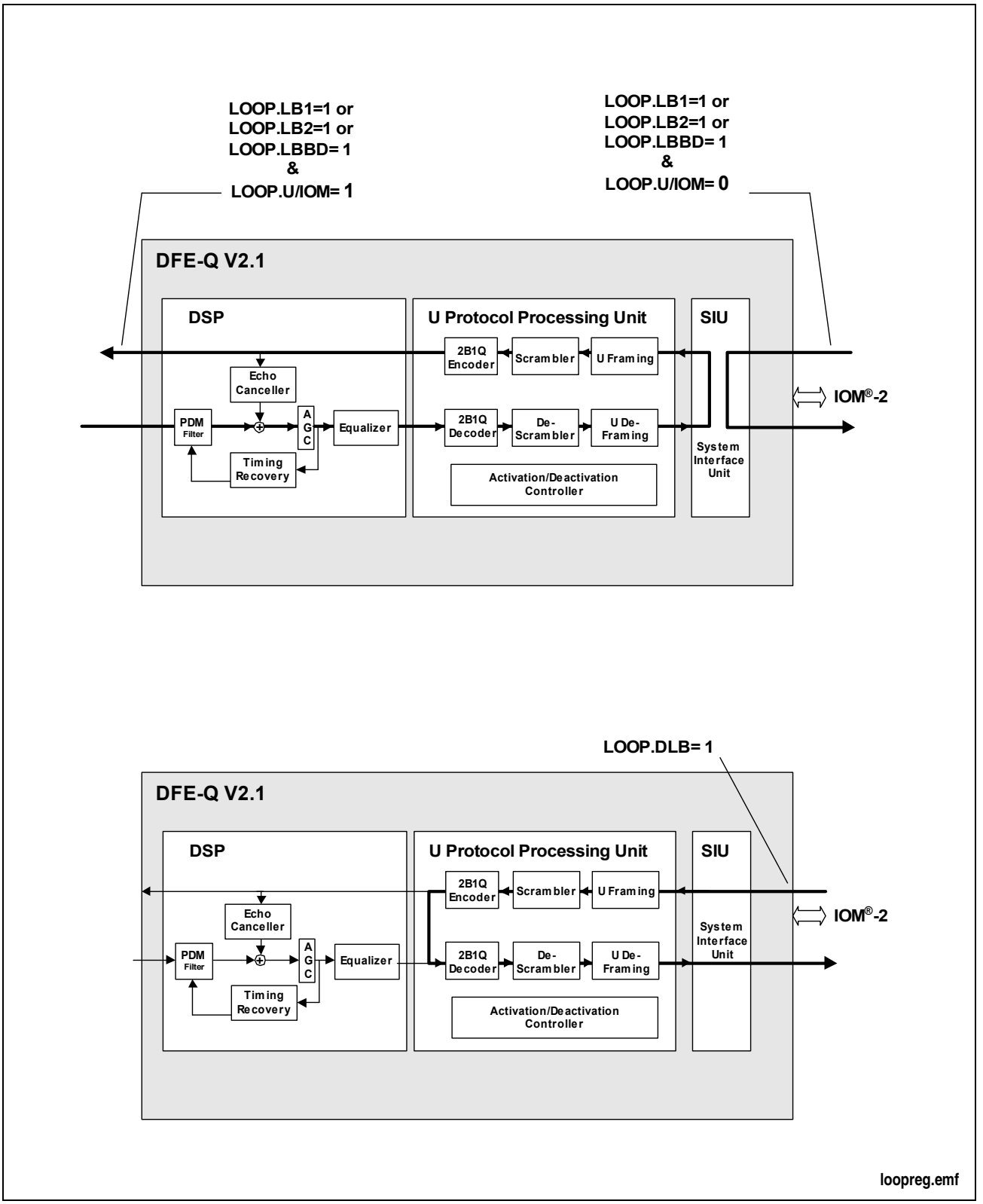


**Figure 2 Loopbacks Featured by Register LOOP**

# 9 D-Channel Arbitration

D-channel arbitration is not supported by version 2.1.

# 10 State Machine

Some minor changes were made regarding the state machine. The improvements are summarized and listed in **Table 7**. See also the state diagrams in **Figure 3** (V2.1) and **Figure 4** (V1.3).

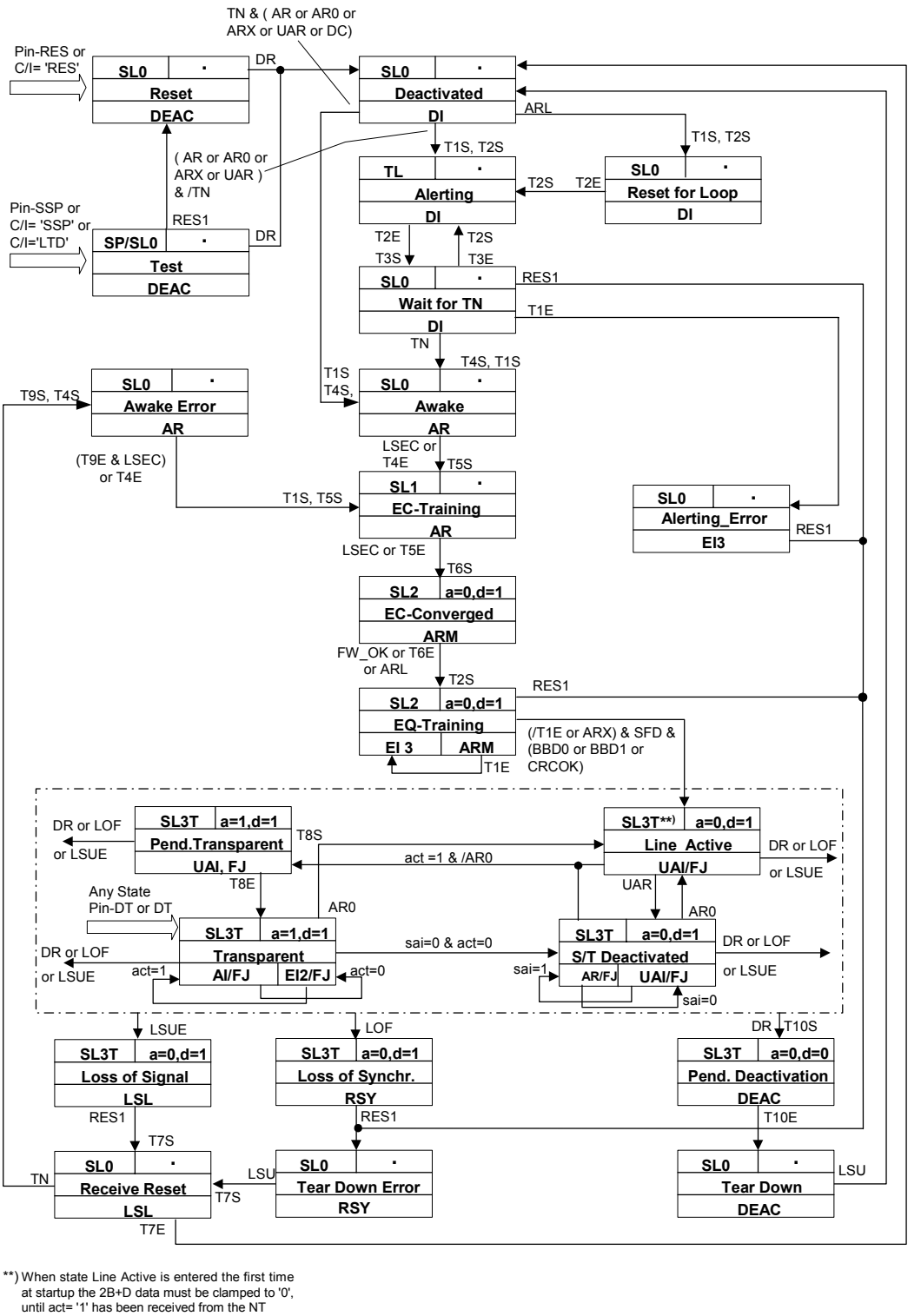


**Figure 3 State Diagram of V2.1**

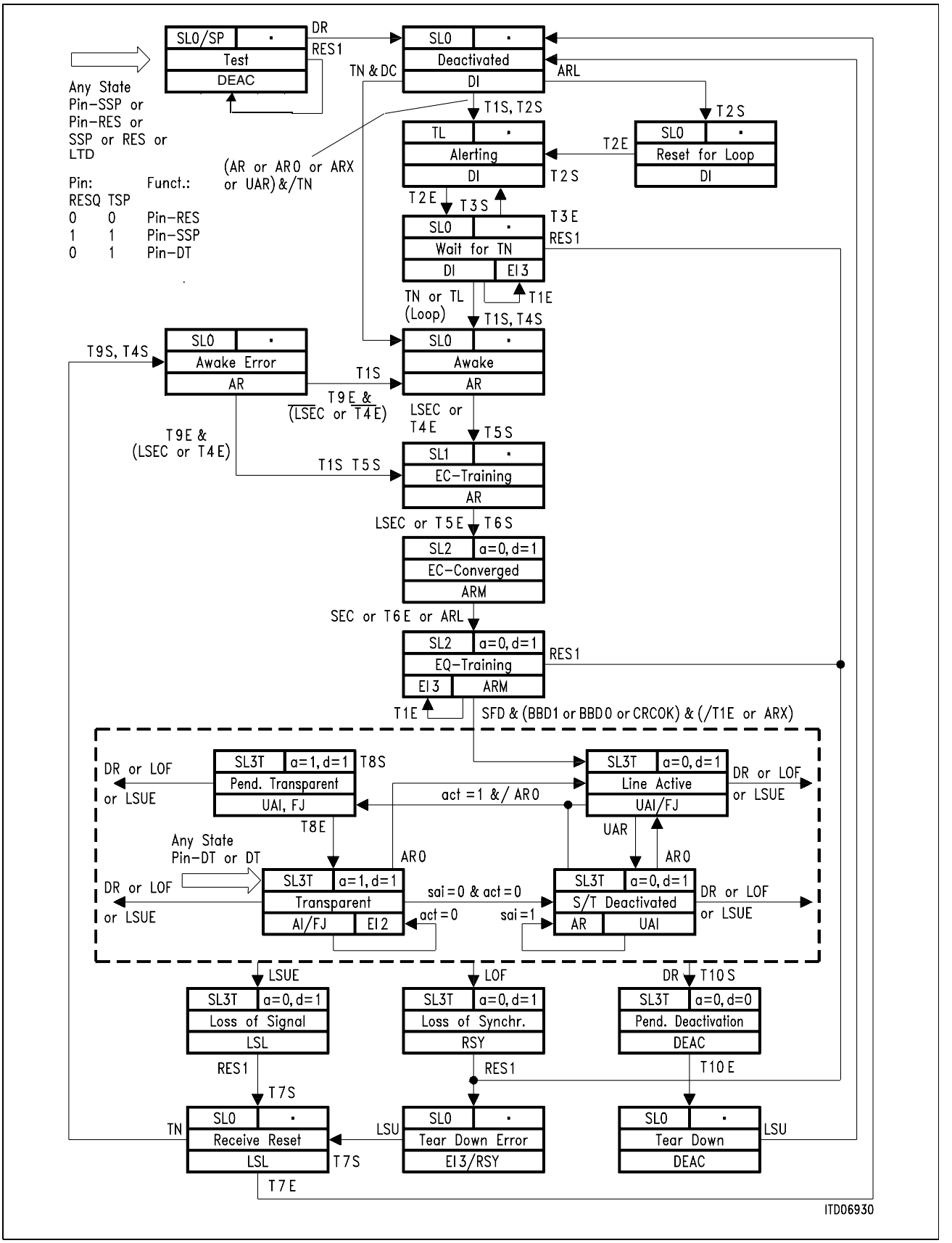


**Figure 4 State Diagram of V1.3**

**Table 7 Differences to LT-SM of DFE-Q V1.3**

| No. | V1.3 State/ Signal | Change in V2.1 | Comment |
|---|---|---|---|
| 1. | 'Test' State | split into two states<br>- Reset State<br>- Test State | defined reset and test states |
| 2. | | state 'Alerting Error' | introduced for a clear separation of the normal operation state from the error condition state (which will result in a deactivation) |
| 3. | state 'Transparent' | C/I code output in state 'Transparent' dependent on received act bit | |
| 4. | state 'S/T Deactivated' | C/I code output in state 'S/T Deactivated' dependent on sai bit status | |
| 5. | C/I code INT | C/I code 'INT' is not supported | INT was listed in former documents of V1.x due to an editorial fault |

# 11 RITL/WLL Functions

RITL/WLL functions are not supported by the DFE-Q version 2.1.

# 12 Retrieving Coefficients

MON-8 commands with bit r=1, that were defined for former versions, are no more supported.

# 13 Boundary Scan Instruction Set

The Boundary-Scan instructions 'CLAMP' and 'HIGHZ' are introduced in version 2.1. The instruction 'SSP' and 'DT' are omitted since these test functions can be triggered either by the pins SSP and DT or - channel selective - by the C/I codes SSP and DT.

**CLAMP** allows the state of the signals included in the boundary scan driven from the PEF 24911 to be determined from the boundary scan register while the bypass register is selected as the serial path between TDI and TDO. These output signals driven from the DFE-Q V2.1 will not change while CLAMP is selected.

**HIGHZ** sets all output pins included to the boundary scan path into a high impedance state. In this state, an in-circuit test system may drive signals onto the connections normally driven by the DFE-Q V2.1 outputs without incurring the risk of damage to the DFE-Q V2.1.

**Table 8 TAP Controller Instructions**

| **Code** | Instruction | Function |
|---|---|---|
| 0000 | EXTEST | External testing |
| 0001 | INTEST | Internal testing |
| 0010 | SAMPLE/PRELOAD | Snap-shot testing |
| 0011 | IDCODE | Reading ID code |
| 0100 | CLAMP | Reading outputs |
| 0101 | HIGHZ | Z-State of all boundary scan output pins |
| 1111 | BYPASS | Bypass operation |

# 14 Version Update of the Boundary Scan IDCODE Register

| Version | Device Code | Manufacturer Code | | Output |
|---|---|---|---|---|
| 0001 | 0000 0000 0111 0010 | 0000 1000 001 | 1 | --> TDO |

# 15 MON-8 AID Version Identification

On receiving the MON-8 Command RID the DFE-Q responds with the MONITOR message AID coded $8006_H$ .

This code is unique for version 2.1 with respect to other DFE-Q versions

# 16 Recognition Delay of Changes in the IOM®-2 Channel

The DFE-Q V2.1 has implemented a new architecture for low power consumption. Furthermore it is developed for complete compatibility in MONITOR and C/I messages. The new architecture , however, leads to changes in response times compared to former versions, that could affect the compatibility to software with rigid time-out settings.

The evaluation of changes of the incoming C/I-code takes longer than in former versions of the PEF 24911:

- Recognition of changes to unconditional commands (I.e.: to RES, SSP, LTD and DT) takes up to 2,5 msec instead of 0.25 msec in former versions
- In states 'Test' and 'Reset' recognition of changes in the C/I channel can also take up to 2,5 msec instead of 0.25 msec in former versions
- In states other than 'Reset' or 'Test' recognition of changes to all other conditional commands takes up to 0,5 ms instead of 0.25 msec in former versions

The C/I codes shall be repeated at least the times above, before the C/I code may be changed. Surveillance timers have to be set to values beyond the named times.

The MONITOR handshake procedure of the DFE-Q V2.1 conforms to the IOM®-2 specification, but leads to different reaction times as compared to former versions in the following cases:

- The DFE-Q V2.1 MONITOR receiver acknowledges the first byte of a monitor sequence in the third IOM®-2 frame or later (if for instance the double last look criterion is not fulfilled). In contrast, the former versions of the DFE-Q acknowledge the first byte of a monitor sequence in the second IOM®-2 frame or later.
- If the DFE-Q V2.1 is requested to return an answer, it will commence as soon as possible after reception of the MONITOR command. Former versions of the DFE-Q require one more IOM®-2 frame to commence.

# 17 MON-8 messages in State 'Reset'

The issuing of MON-8 messages has been improved in state 'Reset'

If the state 'Reset' is entered due to a hardware reset (pin $\overline{\text{RES}}$=0) the device will issue a MON-8 message AST afterwards if one of the pins STxy is high to communicate this status to the system software.

The usage of MON-8 commands is not blocked during a Software Reset, i.e. the C/I-command RES is applied. Even while the SW-reset is activated, the relay driver pins can be programmed by the MON-8 message SETD, and the status pins can be read with RST messages or will autonomously communicate changes of the status. The device will also answer on a RID-command with a AID-message.

# 18 C/I-channel indication in Hardware Reset

As long as pin $\overline{\text{RES}}$ is low, the issued C/I-code is DI ($1111_b$) instead of DEAC ($0001_b$) for all channels. After putting $\overline{\text{RES}}$ to high the C/I-codes change to DEAC.

# 19 MON-8-Command PACE

**Table 9** lists some minor differences of MON-8-command PACE in version V2.1 as compared to version V1.3:

**Table 9 Differences to MON-8 PACE Function in V1.3**

| | DFE-Q V2.1 | DFE-Q V1.3 |
|---|---|---|
| Channels affected | all channels, regardless which channel PACE has been sent in | channel, which PACE has been sent in |
| Reset of PACE | PACA command | 1. PACA command<br>2. deactivation<br>3. reset |
| Local Loop Tetsmode (C/I = 'ARL') | PACE not allowed[1)] | PACE allowed |

1) In Local Loop Testmode (initated by C/I-command 'ARL'), switching back and forth between PACE and PACA may cause a failure where the SAI/UOA bits toggle permanently.

# 20 Activation with C/I-Command AR0

The polarity of the transmitted UOA-bit depends on the received C/I-command AR0 according to **Table 10**:

**Table 10 Activation with C/I-Command AR0**

| | DFE-Q V2.1 | DFE-Q V1.3 |
|---|---|---|
| Activation with AR0 | sets UOA-bit to binary 1 | sets the UOA to the same value as the received SAI bit. After deactivation and subsequent activation the UOA-bit is set to binary 0 until a valid SAI-bit is received. |

*Note: This means, that C/I-inputs AR, ARX and AR0 command the new DFE-Q V2.1 to set the issued UOA-bit to binary 1. Thus, unintended deactivation of the downstream NT-device is avoided during all activation procedures.*

# 21 Hardware Reset Execution and Power-On Reset

In contrast to former versions of the DFE-Q, a hardware reset to the DFE-Q V2.1 by $\overline{\text{RES}}$ = ’0’ takes effect immediately and requires no clocks on IOM-2. However, the DFE-Q V2.1 must be supplied with 15.36 MHz masterclock on pin CL15. The end of reset execution is delayed internally for 900µs.

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