

HA16141P/FP, HA16142P/FP

PFC and PWM Controller

REJ03F0145-0500 (Previous: ADE-204-036D) Rev.5.00 Jun 15, 2005

Description

The HA16141P/FP and the HA16142P/FP are power supply controller ICs combining an AC-DC converter switching controllers for power factor correction and off-line power supply switching controllers. PFC (Power factor correction) section employs average current mode PWM and off-line power supply control section employs peak current mode PWM.

The HA16142P/FP is the change version of HA16141P/FP's PWM maximum on duty cycle.

The PFC operation can be turned on and off by external control signal. Use of this on/off function makes it possible to disable PFC operation at a low line voltage, or to perform remote control operation from the transformer secondary side. The PFC power supply boosted output voltage is not only fed to an error amplifier input signal but also fed to as the boost voltage monitor circuit. \overline{PG} signal is put out if the boost voltage is out-of-spec.

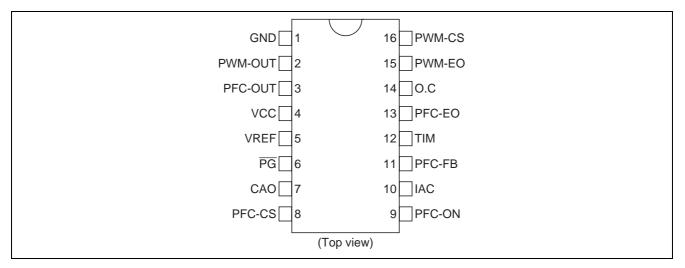
The PWM controller, which begins operation at the same time as release of the IC's UVLO (under-voltage lockout) is suitable for auxiliary power supply use in a multi-output power supply system.

Features

- Synchronized PFC and PWM timing
- Self oscillation with fixed frequency
- PFC : 100 kHz (±15 %) PWM : 200 kHz (±15 %)
- PFC function on/off control
- PFC boosted output voltage monitor
- High-output current gate drivers PFC driver peak current PWM driver peak current : ±1.5 A typ. : ±1.0 A typ.
- PWM maximum on duty cycle 72% min (HA16141P/FP) 49.5% max (HA16142P/FP)



Pin Arrangement

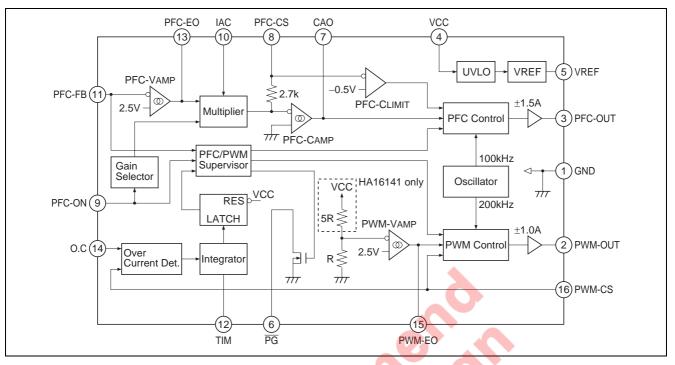


Pin Description

Pin No.	Symbol	Function				
1	GND	Ground				
1						
2	PWM-OUT	Power MOS FET driver output (PWM control)				
3	PFC-OUT	Power MOS FET driver output (PFC control)				
4	VCC	Supply voltage				
5	VREF	Reference voltage				
6	PG	Power Good signal output (open-drain output)				
7	CAO	Average current control error amp. output				
8	PFC-CS	PFC control current sense signal input				
9	PFC-ON	PFC function on/off signal input				
10	IAC	Multiplier reference current input				
11	PFC-FB	PFC control error amp. input				
12	ТІМ	Overcurrent timer time setting				
13	PFC-EO	PFC control error amp. output				
14	0.C	Overcurrent detector signal input				
15	PWM-EO	PWM control error amp. output (photocoupler input also possible) (HA16141 only)				
		PWM control feedback voltage signal input (HA16142 only)				
16	PWM-CS	PWM control current sense signal input				



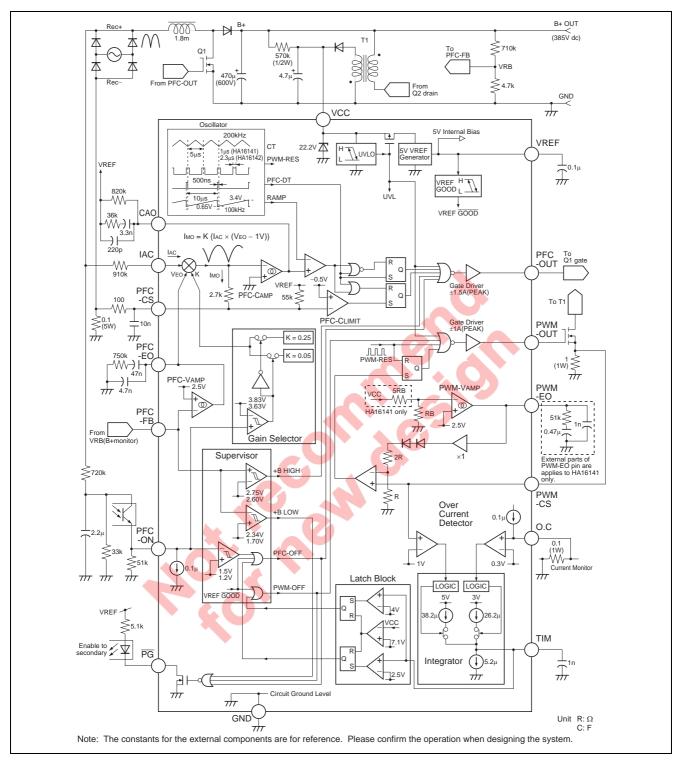
Block Diagram



rvw-EO



System Diagram



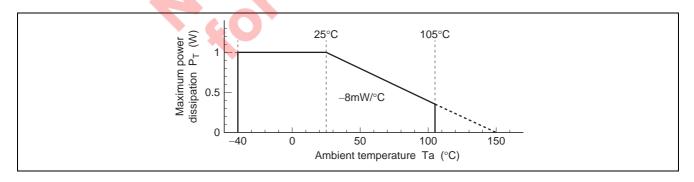


Absolute Maximum Ratings

				$(Ta = 25^{\circ}C)$
ltem	Symbol	Rating	Unit	Note
Supply voltage	V _{CC}	20	V	
Peak PFC-OUT current	lpk-pfc	±1.5	A	3
Peak PWM-OUT current	lpk-pwm	±1.0	A	3
DC PFC-OUT current	Idc-pfc	±0.15	A	
DC PWM-OUT current	ldc-pwm	±0.10	A	
Terminal voltage	Vi-group1	–0.3 to V _{CC}	V	4
	Vi-group2	–0.3 to Vref	V	5
CAO voltage	Vcao	–0.3 to Veoh-ca	V	
PFC-EO voltage	Vpfc-eo	–0.3 to Veoh-pfc	V	
PWM-EO voltage	Vpwm-eo	–0.3 to Veoh-pwm	V	
PFC-ON voltage	Vpfc-on	-0.3 to +7	V	
IAC voltage	Vi-ac	-0.3 to +5	V	
IAC current	li-ac	0.8	mA	
PFC-CS voltage	Vi-cs	-1.5 to +0.3	V	
TIM voltage	Vi-tim	–0.3 to +6	V	
VREF current	lo-ref	-20	mA	
PG voltage	Vo-pg	-0.3 to +7	V	
PG current	lo-pg	15	mA	
Power dissipation	PT		W	6
Operating temperature	Topr	-40 to +105	°C	
Storage temperature	Tstg	-55 to +150	°C	
Junction temperature	Tj	150	°C	

Notes: 1. Rated voltages are with reference to the GND pin.

- 2. For rated currents, inflow to the IC is indicated by (+), and outflow by (-).
- 3. Shows the transient current when driving a capacitive load.
- 4. Group1 is the rated voltage for the following pins: PFC-OUT, PWM-OUT
- 5. Group2 is the rated voltage for the following pins: VREF, PFC-FB, PWM-CS
- 6. This is the value when the ambient temperature (Ta) is 25°C or below. If Ta exceeds 25°C, the graph below applies. For the SOP package, this value is based on actual measurements on a 10% wiring density glass epoxy circuit board (40 mm × 40 mm × 1.6 mm).



Electrical Characteristics

Item		Symbol	Min	Тур	Max	Unit	Test Conditions
Supply	Start threshold	V _H	12.2	13.0	13.8	V	
	Shutdown threshold	VL	9.4	10.0	10.6	V	
	UVLO hysteresis	dV _{UVL}	2.6	3.0	3.4	V	
	Start-up current	Is	150	200	300	μA	$V_{CC} = 12V$
	Is temperature stability	dl _s /dTa	_	-0.3	_	%/°C	*1
	Operating current	Icc	4	7	9	mA	$IAC = 100\mu A, C_L = 0F$
	Latch current	I _{LATCH}	230	310	375	μΑ	$V_{CC} = 9V$
	Shunt zener voltage	Vz	21.2	22.2	23.2	V	$I_{CC} = 14mA$
	Vz temperature stability	dV _Z /dTa	-	+4	_	mV/°C	$I_{CC} = 14 mA^{*1}$
PFC-OUT	Minimum duty cycle	Dmin-pfc	_	_	0	%	CAO = 3.6V
	Maximum duty cycle	Dmax-pfc	90	95	98	%	CAO = 0V
	Rise time	t _r -pfc	_	30	100	ns	C _L = 1000p
	Fall time	t _f -pfc	-	30	100	ns	C _L = 1000p
	Peak current	lpk-pfc	-	1.5	_	A	$C_{L} = 0.01 \mu F^{*1}$
	Low voltage	Vol1-pfc	-	0.05	0.2	V	lout = 20mA
		Vol2-pfc	_	0.35	1.4	V	lout = 200mA
		Vol3-pfc	-	0.03	0.7	V	lout = 10mA, $V_{CC} = 5V$
	High voltage	Voh1-pfc	13.5	13.9	+	V	lout = -20mA
		Voh2-pfc	12.6	13.3	-	V	lout = -200mA
PWM-OUT	Minimum duty cycle	Dmin-pwm		-	0	%	PWM-EO = 1.3V PWM-CS = 0V
	Maximum duty cycle	Dmax-pwm	72	80	88	%	PWM-EO = 5V PWM-CS = 0V * ²
			42.5	46	49.5	%	PWM-EO = 5V PWM-CS = 0V * ³
	Rise time	t _r -pwm		30	100	ns	C _L = 1000p
	Fall time	t _f -pwm	-	30	100	ns	C _L = 1000p
	Peak current	lpk-pwm	-	1.0	-	А	$C_{L} = 0.01 \mu F^{*1}$
	Low voltage	Vol1-pwm	-	0.05	0.2	V	lout = 20mA
		Vol2-pwm	-	0.5	2.0	V	lout = 200mA
		Vol3-pwm	_	0.03	0.7	V	lout = 10mA, $V_{CC} = 5V$
	High voltage	Voh1-pwm	13.5	13.9		V	lout = -20mA
		Voh2-pwm	12.0	13.0	-	V	lout = -200mA
VREF	Output voltage	Vref	4.9	5.0	5.1	V	Isource = 1mA
	Line regulation	Vref-line	-	5	20	mV	Isource = 1mA V_{CC} = 12V to 18V
	Load regulation	Vref-load	-	5	20	mV	Isource = 1mA to 20mA
	Temperature stability	dVref	_	80	_	ppm/°C	Ta = -40 to 105°C * ¹

Notes: 1. Design spec.

2. Apply to HA16141.

3. Apply to HA16142.



Electrical Characteristics (cont.)

$(Ta = 25^{\circ}C, V_C)$	c = 14 V
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Item		Symbol	Min	Тур	Max	Unit	Test Conditions	
Oscillator Initial accuracy		fpwm	170	200	230	kHz	Measured pin: PWM-OUT	
		fpfc	85	100	115	kHz	Measured pin: PFC-OUT	
	fpwm temperature stability	dfpwm/dTa	-	±0.1	_	%/°C	Ta = -40 to $105^{\circ}C^{*1}$	
	fpwm voltage stability	fpwm(line)	-1.5	+0.5	+1.5	%	$V_{CC} = 12V$ to $18V$	
	Ramp peak voltage	Vramp-H	_	3.4	3.6	V		
	Ramp valley volatge	Vramp-L	_	0.65	_	V	*1	
PFC-ON	PFC on voltage	Von-pfc	1.3	1.5	1.7	V		
	PFC off voltage	Voff-pfc	1.0	1.2	1.4	V		
	PFC on-off hysteresis	dVon-off	0.15	0.30	0.45	V		
	Input current	Ipfc-on	_	0.1	1.0	μA	PFC-ON = 2V	
Supervisor/ PG	PFC GOOD threshold voltage	Vb-good	2.29	2.34	2.39	V	Input pin: PFC-FB	
	PFC FAIL threshold voltage	Vb-fail	1.66	1.70	1.74	V	Input pin: PFC-FB	
	+B High PFC inhibit voltage	Vb-h	2.69	2.75	2.81	V	Input pin: PFC-FB	
	+B High PFC restart voltage	Vb-res	2.54	2.60	2.66	V	Input pin: PFC-FB	
	PG leak current	loff-pg	_ (0.001	1.0	μA	PG = 5V	
	PG shunt current	lon-pg	5	15		mA	$\overline{PG} = 3V^{*2}$	
	Delay to PG	tg-pg		0.2	1	μs	Step signal (5 to 0V) to PFC-ON	
0.C	O.C threshold voltage	Voc	0.27	0.30	0.33	V		
(Over Current	PWM-CS threshold voltage	Vcs	0.9	1.0	1.1	V		
Detector)	O.C input current	loc		-0.1	-1.0	μΑ	O.C = 0V	
Integrator	Sink current	Isnk-tim	3.9	5.2	6.5	μΑ	TIM = 2V	
	Source current O.C trigger	Isrc-tim1	-16	-21	-26	μA	$TIM = 2V, O.C = 0.5V *^{1}$	
	Source Current PWM-CS trigger	Isrc-tim2	-25	-33	-41	μA	TIM = 2V, PWM-CS = 2V	
	Integrated time O.C trigger	t-tim1	88	110	132	μs	Step signal (0 to 1V) to O.C, Ctim = 1000p, Measured pin: \overline{PG}	
	Integrated Time PWM-CS trigger	t-tim2	53	67	81	μs	Step signal (0 to 2V) to PWM-CS, Ctim = 1000p, Measured pin: \overline{PG}	

Notes: 1. Design spec.

2. Maximum rating of PG current is 15 mA. Use series resistor to limit PG current lower than 15 mA.

ltem		Symbol	Min	Тур	Max	Unit	Test Conditions
Latch	Threshold voltage for PFC stop	Vlch-pfc	2.4	2.5	2.6	V	Input pin: TIM
	Threshold Voltage for PWM stop	Vlch-sys	3.8	4.0	4.2	V	Input pin: TIM
	Latch Reset Voltage	Vcc-res	6.1	7.1	8.1	V	
PWM-VAMP	Feedback V _{CC} voltage	Vfb-pwm	14.2	14.8	15.4	V	PWM-EO = 2.5V * ²
	Open loop gain	Av-pwm	_	45	_	dB	*1, *2
	High voltage	Veoh-pwm	5.1	5.7	6.3	V	V _{CC} = 14V, PWM-EO: Open
	Low voltage	Veol-pwm	-	0.1	0.3	V	V _{CC} = 16V, PWM-EO: Open * ²
	Source current	Isrc-pwm	_	-77	_	μΑ	* ¹ V _{CC} = 11V
	Sink current	Isnk-pwm	_	77	_	μA	$*^{1}$ V _{CC} = 18V $*^{2}$
	Transconductance respect to V _{CC}	Gm-pwm	19	27	35	μA/V	V _{CC} = 15V, PWM-EO = 2.5V * ²
PWM current sense	Delay to output	td-cs	-	210	300	ns	PWM-EO = 5V, PWM-CS = 0 to 2V
PFC current	Threshold voltage	V _{LM}	-0.47	-0.50	-0.53	V	
limit	Delay to output	td- _{LM}		280	500	ns	PFC-CS = 0 to -1V
PFC-VAMP	Feedback voltage	Vfb-pfc	2.45	2.50	2.55	V	PFC-EO = 2.5V
	Input bias current	lfb-pfc	-0.30	-0.07	+0.30	μΑ	Measured pin: PFC-F
	Open loop gain	Av-pfc		65	-	dB	*1
	High voltage	Veoh-pfc	5.1	5.7	6.3	V	PFC-FB = 2.3V, PFC-EO: Open
	Low voltage	Veol-pfc	3	0.1	0.3	V	PFC-FB = 2.7V, PFC-EO: Open
	Source current	Isrc-pfc	-62	-77	-93	μA	PFC-FB = 1.0V, PFC-EO = 2.5V
	Sink current	Isnk-pfc	62	77	93	μA	PFC-FB = 4.0V, PFC-EO = 2.5V
	Transconductance	Gm-pfcv	120	160	200	μA/V	PFC-FB = 2.5V, PFC-EO = 2.5V

Electrical Characteristics (cont.)

 $(Ta = 25^{\circ}C, V_{CC} = 14 \text{ V})$

Notes: 1. Design spec.

2. Apply to HA16141.

Test Conditions Unit Item Symbol Min Тур Max PFC-CAMP Input offset voltage Vio-ca mV ±7 _ *****1 Open loop gain Av-ca dB _ 65 _ High voltage Veoh-ca 5.1 5.7 6.3 V Low voltage Veol-ca 0.1 V 0.3 _ -77 μΑ $CAO = 2.5V *^{1}$ Source current Isrc-ca _ _ $CAO = 2.5V^{*1}$ Sink current Isnk-ca 77 μΑ _ _ μA/V Transconductance Gm-pfcc 120 160 200 IAC/ IAC PIN voltage Viac 0.7 1.0 1.3 V $IAC = 100 \mu A$ Multiplier Terminal offset current Imo-offset -56 -75 -94 IAC = 0A, PFC-CS = 0V,μΑ Measured pin: PFC-CS Output current PFC-EO = 2V, lmo1 _ -25 _ μΑ $IAC = 100 \mu A^{*1, *2}$ (PFC-ON = 3.4V)PFC-EO = 4V, Imo2 -75 _ μA _ $IAC = 100 \mu A^{*1, *2}$ PFC-EO = 2V, Output current Imo3 -5 μA _ _ $IAC = 100 \mu A^{*1, *2}$ (PFC-ON = 3.9V)PFC-EO = 4V,Imo4 -15 _ μΑ - $IAC = 100 \mu A^{*1, *2}$ **PFC-CS** resistance Rmo 2.7 kΩ _ _ Gain Threshold voltage V_{K-H} 3.71 3.83 3.95 V selector for K = 0.05V_{K-L} Threshold voltage 3.51 3.63 3.75 V for K = 0.25*1 V_K hysteresis voltage dVκ 0.15 0.20 0.25 V

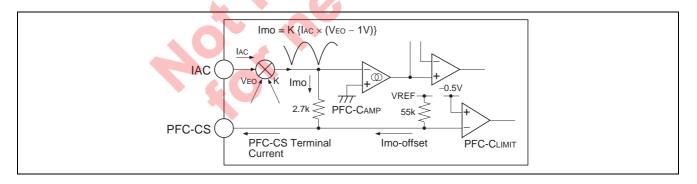
Electrical Characteristics (cont.)

$(Ta = 25^{\circ}C, V_{CC} = 14 \text{ V})$

Notes: 1. Design spec.

2. Imo1 to Imo4 are defined as,

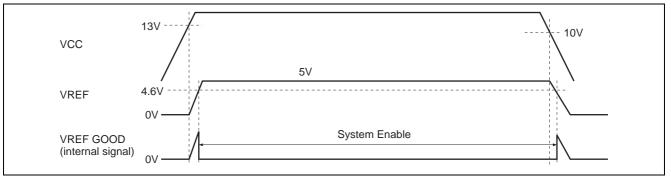
Imo = (PFC-CS Terminal Current) - (Imo-offset)



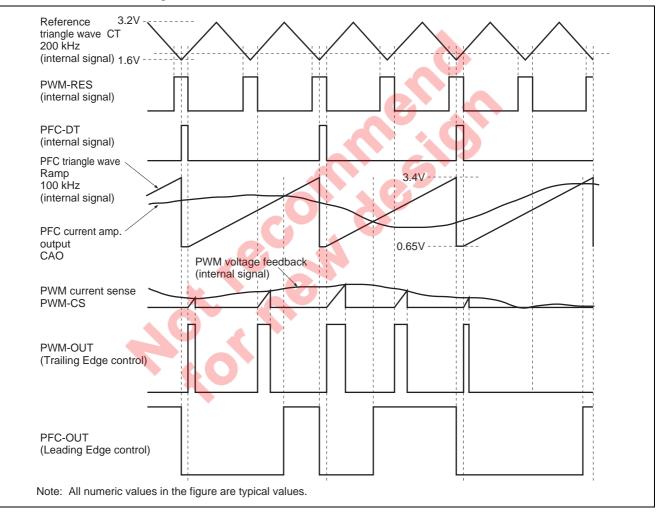


Internal Timing

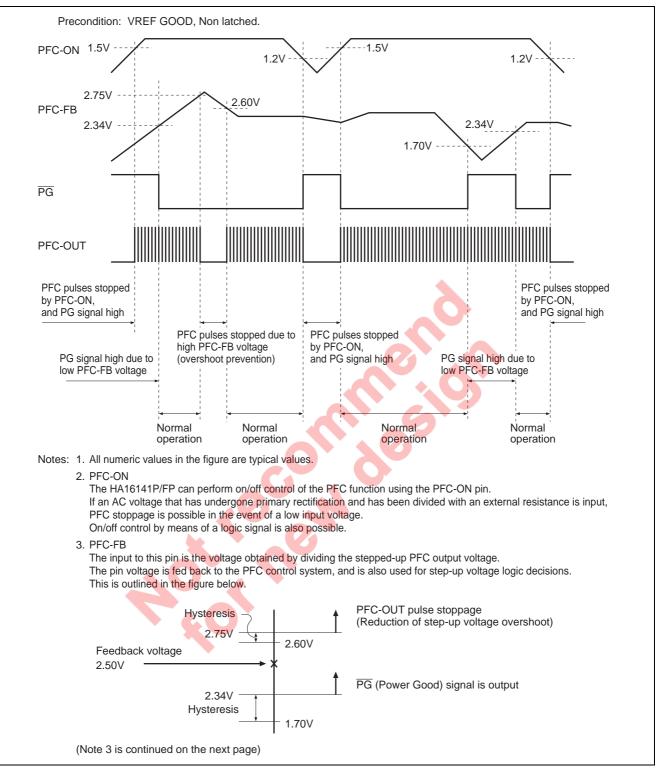




2. Oscillator, Gate driver output

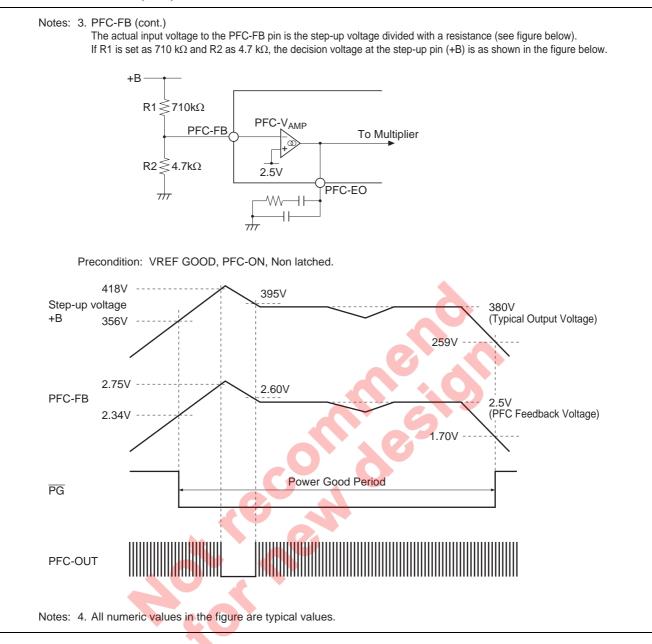


3. PFC controller status



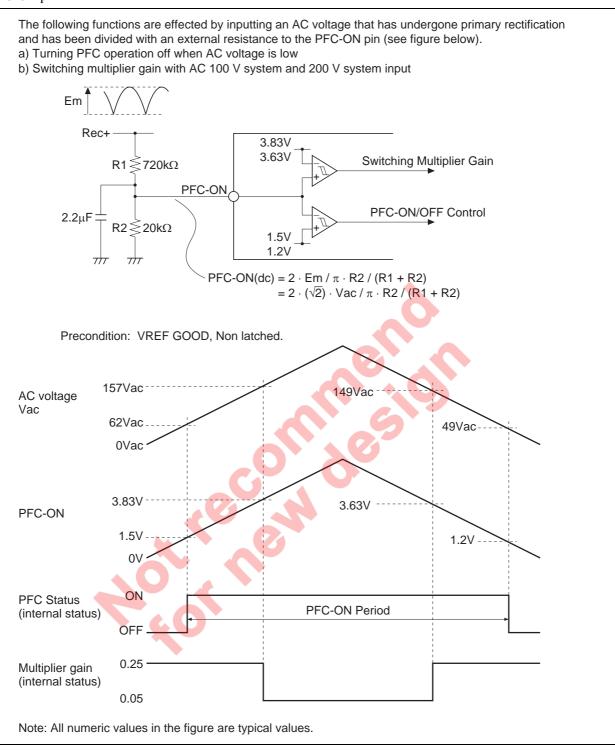


3. PFC controller status (cont.)





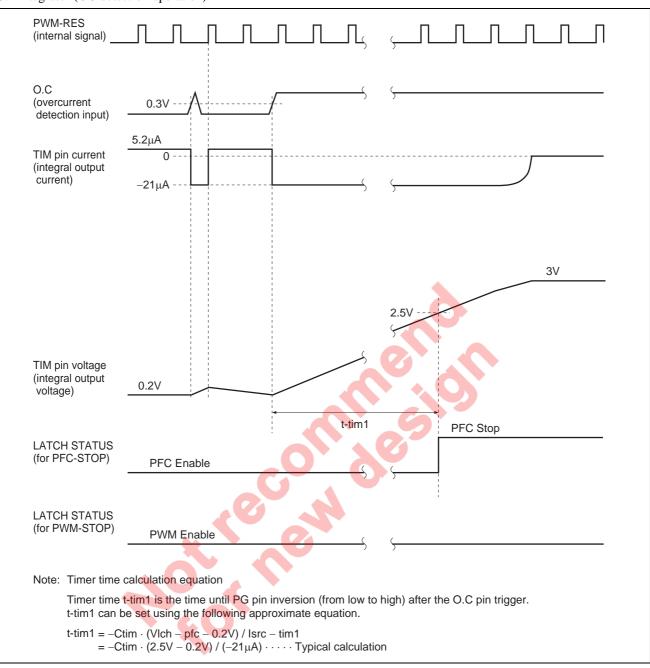
4. PFC-ON pin





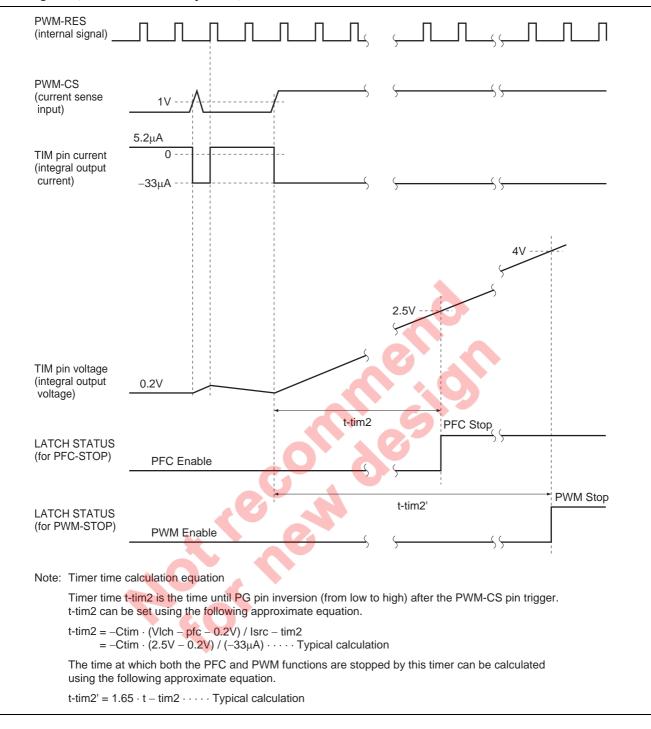
HA16141P/FP, HA16142P/FP

5. Integrator (OC detection operation)



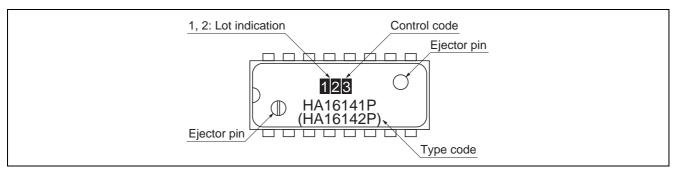


6. Integrator (PWM-CS detection operation)





Mark Pattern



Notes: 1. Example of lot indication.

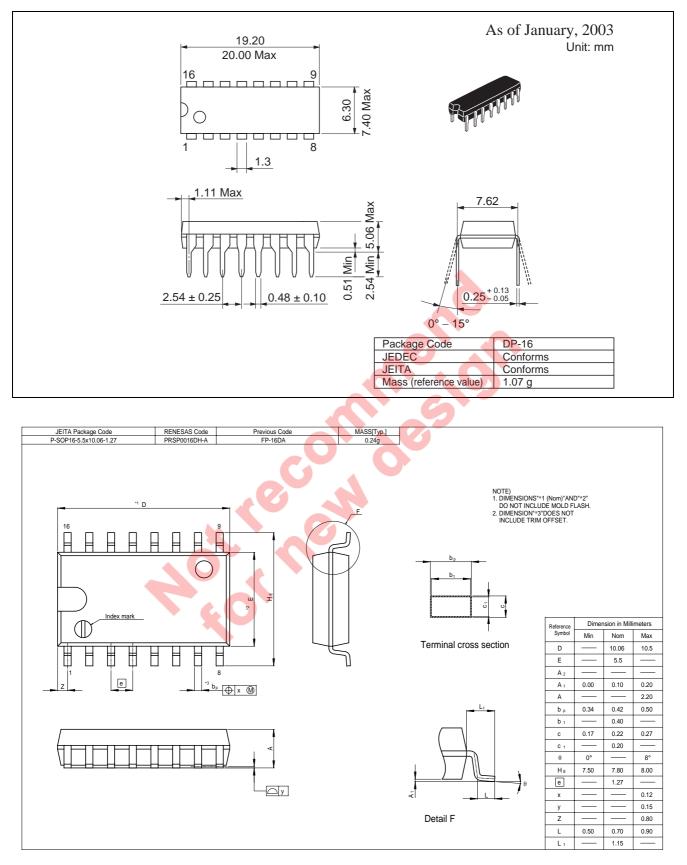
For example, a product manufactured in May 2000 has the markings "0E" in positions **1 2** in the above figure.

Produ	uction	Indication				
Month	Year	1	2			
May	200 <u>0</u>	0	E			

2. Laser marking is used.



Package Dimensions





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