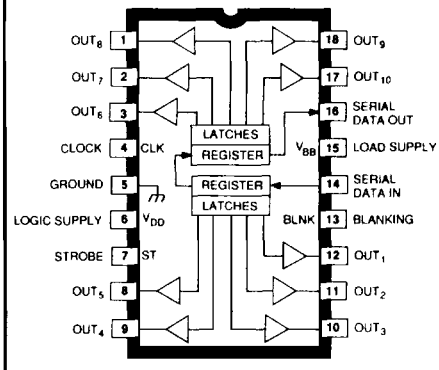
5810
MIL-STD-883 COMPLIANT

BiMOS II 10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER



Dwg. PP-029

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{OUT} . . . . . **60 V**
Logic Supply Voltage Range,
V_{DD} . . . . . **4.5 V to 15 V**
Driver Supply Voltage Range,
V_{BB} . . . . . **5.0 V to 60 V**
Input Voltage Range,
V_{IN} . . . . . **-0.3 V to V_{DD} + 0.3 V**
Continuous Output Current,
I_{OUT} . . . . . **-40 mA**
Package Power Dissipation, P_D **1.67W***
Operating Temperature Range,
T_A . . . . . **-55°C to +125°C**
Storage Temperature Range,
T_S . . . . . **-65°C to +150°C**

* Derate at 13.3 mW/°C above +25°C

Caution: This CMOS device has input static protection but is susceptible to damage when exposed to extremely high static electrical charges.

Combining low-power CMOS logic with bipolar source drivers, Type UCS5810H will simplify many display-system designs. Primarily intended for use with vacuum-fluorescent displays, this BiMOS 10-bit serial-input, latched driver can also be used with LED and incandescent displays within its output limitations of 60 V and 40 mA per driver.

BiMOS II devices have considerably better data input rates than the original BiMOS circuits. With a 5 V supply, they typically operate above 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS 10-bit shift register and associated latches are designed for operation over a 5 V to 15 V supply-voltage range. They cause minimal loading of data lines and are compatible with standard CMOS, PMOS, and NMOS logic. When used with standard TTL or low-speed TTL logic, appropriate pull-up resistors may be required to ensure an input logic high. A CMOS serial-data output allows cascading these devices for interface applications requiring many drive lines (dot matrix, alphanumeric, bargraph).

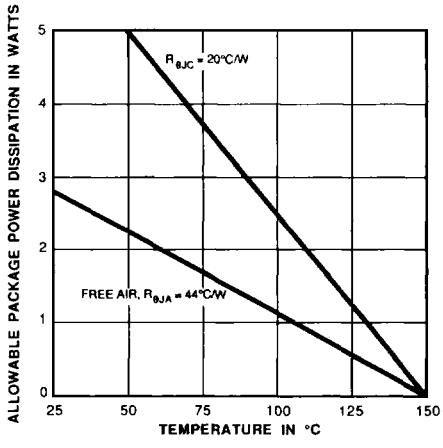
The 10 bipolar outputs are used as segment or digit drivers in vacuum-fluorescent displays. Under normal operating conditions, these devices will sustain 25 mA per output at 85°C at a duty cycle of 83%. Other combinations of number of conducting outputs and duty cycle are shown in the specifications.

Type UCS5810H, when combined with the UCS5815H, an 8-bit latched source driver, comprises a minimum component display subsystem requiring few, if any, discrete components. The UCS5810H is furnished in an 18-pin hermetic dual in-line side-brazed package. Reverse-bias burn-in and 100% high-reliability screening to MIL-STD-883, Class B, are standard.

FEATURES

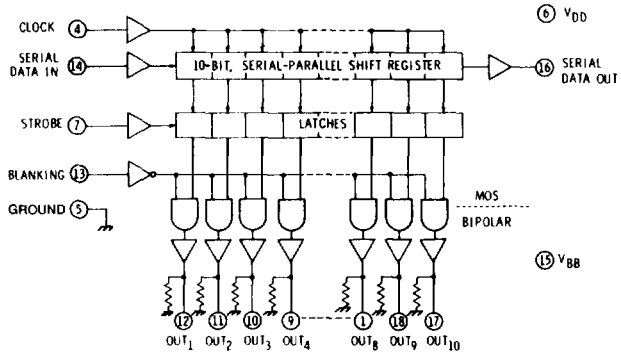
- 5 MHz Minimum Data Input Rate
- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Logic and Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range
- High-Reliability Screening to MIL-STD-883, Class B
- Operating Temperature -55°C to +125°C

Always order by complete number: **UCS5810H883**.



Dwg. GM-006

FUNCTIONAL BLOCK DIAGRAM



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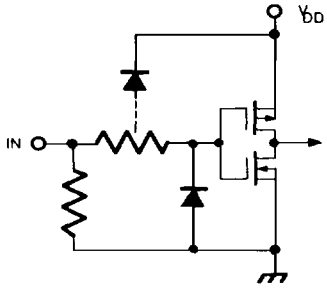
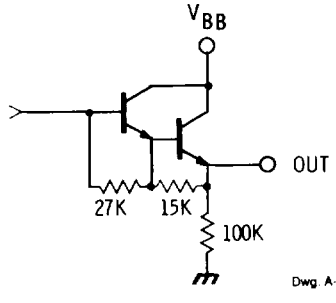
TYPICAL INPUT CIRCUIT



Dwg. EP-010-4

Number of Outputs ON (I_{OUT} = -25 mA)	Maximum Allowable Duty Cycle at V_{DD} = 5 V and T_A of 85°C
10	83%
9	93%
8	100%
7	100%
6	100%
5	100%

TYPICAL OUTPUT DRIVER



Dwg. A-10,981C

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 60 V, V_{DD} = 5 V to 12 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		I_{OUT} = -25 mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	850	µA
Output Leakage Current			—	-15	µA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	—	V
		V_{DD} = 12 V	10.5	—	V
	$V_{IN(0)}$		-0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN}$ = 5.0 V	—	100	µA
		$V_{DD} = V_{IN}$ = 12 V	—	240	µA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	V_{DD} = 5.0 V	—	20	kΩ
		V_{DD} = 12 V	—	6.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	13	mA
		All outputs OFF, Outputs open	—	200	µA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	µA
		V_{DD} = 12 V, All outputs OFF, All inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL of DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at T_A = -55°C, V_{BB} = 60 V, V_{DD} = 5 V to 12 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		I_{OUT} = -25 mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	300	850	µA
Output Leakage Current			—	-15	µA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.6	—	V
		V_{DD} = 12 V	11.0	—	V
	$V_{IN(0)}$		-0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN}$ = 5.0 V	—	145	µA
		$V_{DD} = V_{IN}$ = 12 V	—	430	µA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	35	—	kΩ
Serial Data Output Resistance	R_{OUT}	V_{DD} = 5.0 V	—	20	kΩ
		V_{DD} = 12 V	—	6.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	13	mA
		All outputs OFF, Outputs open	—	100	µA
	I_{DD}	V_{DD} = 5.0 V, Outputs OFF, All Inputs = 0 V	—	100	µA
		V_{DD} = 12 V, Outputs OFF, All inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA

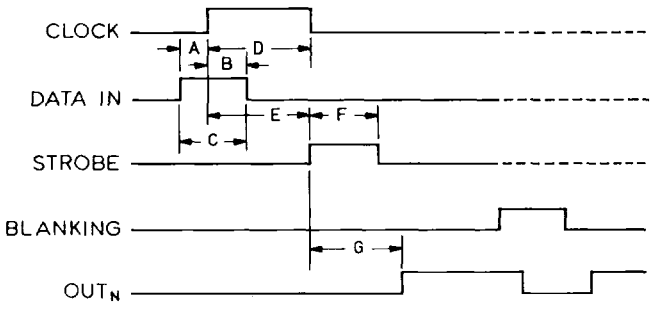
NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL of DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at T_A = +125°C, V_{BB} = 60 V, V_{DD} = 5 V to 12 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		I_{OUT} = -25 mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	1400	µA
Output Leakage Current			—	-30	µA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	—	V
		V_{DD} = 12 V	10.5	—	V
	$V_{IN(0)}$		-0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN}$ = 5.0 V	—	100	µA
		$V_{DD} = V_{IN}$ = 12 V	—	300	µA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	V_{DD} = 5.0 V	—	27	kΩ
		V_{DD} = 12 V	—	8.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	15	mA
		All outputs OFF, Outputs open	—	100	µA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	µA
		V_{DD} = 12 V, All outputs OFF, All inputs = 0 V	—	200	µA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 12 V, One output ON, All inputs = 0 V	—	3.0	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL of DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

5810
10-BIT SERIAL-INPUT, LATCHED SOURCE DRIVER



Dwg. No. A 12,649

TIMING CONDITIONS

(V_{DD} = 5 V, T_A = +25°C, Logic Levels are V_{DD} and Ground)

A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time) ..... **75 ns**
B. Minimum Data Active Time After Clock Pulse (Data Hold Time) ..... **75 ns**
C. Minimum Data Pulse Width ..... **150 ns**
D. Minimum Clock Pulse Width ..... **150 ns**
E. Minimum Time Between Clock Activation and Strobe ..... **300 ns**
F. Minimum Strobe Pulse Width ..... **100 ns**
G. Typical Time Between Strobe Activation and Output Transition ..... **1.0 µs**

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the BLANKING input low, the outputs are controlled by the state of the latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Blanking	Output Contents
H	⌐	H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L	⌐	L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X	¬	R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State