

October 1996

DESCRIPTION

The TSC 78Q8377A is a highly integrated Ethernet IC for use in Ethernet Network Interface Cards (NICs) in the ISA/NEC PC-98 Plug and Play (PnP) environment. It contains a full-duplex Media Access Controller (MAC), a 10 Mbit/s Manchester encoder/decoder (ENDEC), a 10BaseT transceiver, ISA/NEC PC-98 bus interface and an Attachment Unit Interface (AUI). The only external components required to build an Ethernet adapter card with the TSC 78Q8377A are buffer memory, a serial EEPROM and a few passive components. In full duplex operation, transmission line throughput doubles to the theoretical 20 Mbit/s. In this mode, the collision detection, SQE generation and carrier deference are disabled.

The TSC 78Q8377A has an integrated ISA and NEC PC-98 bus interface that physically connects to the bus without any additional glue logic. The TSC 78Q8377A is defined with "jumperless" configuration in mind. The configuration information is stored in serial EEPROM.

The TSC 78Q8377A fully supports the PnP ISA specification. The PnP logic can also be bypassed through a bit in the EEPROM. When the PnP logic is bypassed, the TSC 78Q8377A will power up active after loading the necessary configuration information from the serial EEPROM.

The popular microwire (4-wire) interface is supported by the TSC 78Q8377A to connect to serial EEPROM, which contains configuration information such as I/O Base address, Boot Device address, IRQ selection, MAC address, etc. Reading of essential configuration information like the I/O Base address and Boot Device address is done automatically by the TSC 78Q8377A. The driver software is then responsible to read the rest of the information and program the TSC 78Q8377A registers with the appropriate values read.

The TSC 78Q8377A allows for a diskless station to boot from the installed boot device. The boot feature can also be disabled through a bit in the serial EEPROM. Both read-only and read-write (e.g., flash) memory are supported by the TSC 78Q8377A. Furthermore, accidental write to the flash can be prevented through a write protect register bit.

FEATURES

- **Highly integrated Ethernet combo for Plug and Play (PnP) applications**
- **Integrated ISA and NEC PC-98 bus interface with PnP registers, compliant with PnP spec version 1.0a**
- **Compliant with Windows 95 and PC95 requirements**
- **16-bit address decoding**
- **"Glueless" and "jumperless" connection to ISA and NEC PC-98 bus**
- **Integrated 10Base-T transceiver:**
 - **Programmable/automatic selection of twisted pair (RJ45) or AUI port**
 - **Receive polarity detection/correction on twisted-pair inputs**
- **Manchester Encoder/Decoder circuit**
- **AUI port for connection to 10Base2/5 transceiver or AUI cable**
- **Programmable Full Duplex operation**
- **Serial EEPROM support with MICROWIRE (four wire) interface**
- **Supports both PnP and non-PnP environment through an EEPROM bit**
- **LED indicators for Link, RX, TX, COLL**
- **Integrated 24 mA data bus buffer**
- **Boot Device (either read-only or read-write memory) support through an external data buffer ('245) in ISA mode**
- **I/O base address selection in 16 byte increments**
- **8 interrupt lines supported**
 - **Supports edge and level-sensitive interrupts Tri-state implementation allows sharing of interrupts for both modes**
- **Register compatible to the TSC 78Q8373**
- **Power management options:**
 - **Intelligent power mode automatically shuts off unused circuitry**
 - **Standby mode reduces power while not in operation**
 - **Full shutdown mode offers maximum power savings**
- **128-lead QFP package and single 5 V supply**

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TSC 78Q8377A

10BaseT Ethernet Combo

for Plug and Play

FUNCTIONAL DESCRIPTION

The TSC 78Q8377A consists of six major blocks as shown in Figure 1.

- Buffer Manager (and SRAM Interface)
- Data Link Controller
- ISA Bus Interface
- Manchester ENDEC
- Twisted Pair Transceiver
- Power Management

BUFFER MANAGER

The Buffer Manager manages all accesses to the buffer memory through the SRAM interface. The buffer memory is connected directly to the Data Link Controller (DLC), thus eliminating the need for a local microprocessor. The Buffer Manager also keeps track of all buffer memory pointers automatically, simplifying the software driver task. Together with intelligent arbitration, this makes the TSC 78Q8377A a high performance LAN controller.

The buffer memory is divided into two portions: transmit memory and receive memory. The transmit memory portion can be partitioned into 2K, 4K, 8K or 16 Kbyte buffer sizes. There is only one transmit bank if a 2 KB transmit buffer size is selected. If the transmit buffer size is greater than 2 KB, then the transmit buffer is configured into two banks of equal size. With the two bank configuration, one transmit bank may be tied up during transmission but the host can still continue to load data packets into the second transmit bank to be transmitted later. The receive buffer has a ring architecture which can be configured from 4K to 62 KB depending on the buffer memory configuration which has a range of 8KB to 64 KB.

A central arbitrator inside the Buffer Manager prioritizes and services requests for access to the buffer memory from 4 sources: the Transmitter, the Receiver, Host Read and Host Write. If necessary, the TSC 78Q8377A will assert a 'not ready' handshake to the host while servicing the Transmitter and/or Receiver. The TSC 78Q8377A arbitration mechanism provides packet management by interleaving packet data accesses to the buffer memory such that the operations appear to be simultaneous.

For instance, in the situation where 2 transmit banks are configured, the host can load the first transmit bank and initiate a transmission. While the first transmit bank is being transmitted, the host can continue to load packets in the second transmit bank. At this stage, the TSC 78Q8377A can potentially be receiving data from the medium and loading it into the receive buffer (in the case of full duplex 10BaseT operation, or if the TSC 78Q8377A is in a loop back mode or if self-reception occurs).

DATA LINK CONTROLLER

The Data Link Controller (DLC) implements the ISO/ANSI/IEEE 8802-3 CSMA/CD protocol. It consists of a Transmitter, a Receiver and CRC logic. Automatic generation and stripping of the 64-bit preamble and the 32-bit CRC code are provided on-chip.

The TSC 78Q8377A includes support for Full Duplex operation making the line throughput 20 Mbit/s. In this mode, the collision detection and carrier deference are disabled. In addition to that, the Twisted Pair transceiver SQE generation and "natural" loopback are also turned off.

ISA AND NEC PC-98 INTERFACE

The TSC 78Q8377A has an integrated ISA and NEC PC-98 interface that physically connects to both bus types without any additional glue logic. The ISA pin is used to select between the two bus interfaces. The data bus buffers (24 mA) have also been integrated on chip. The TSC 78Q8377A is defined with "jumperless" configuration in mind. The configuration information is stored in the serial EEPROM.

PnP Logic

The TSC 78Q8377A fully supports the Plug and Play (PnP) Specification for the ISA system. The PnP logic can also be by-passed through the PnP_ACT bit in the EEPROM. This allows the TSC 78Q8377A to work in non-PnP as well as PnP environments. When the PnP logic is by-passed, the TSC 78Q8377A will power up active after loading the necessary configuration information from the serial EEPROM.

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Serial EEPROM Interface

The popular MICROWIRE (four wire) interface is supported by the TSC 78Q8377A to connect to the serial EEPROM. Compatible EEPROM devices include 93C56 and 93C66. The serial EEPROM is used to store a number of bytes: I/O base address, Boot Device address, IRQ selection, MAC address, TSC 78Q8377A register specific setting and PnP related data and control. The reading of the essential configuration information in the serial EEPROM like the I/O base address, Boot Device address and IRQ selection are done automatically by the TSC 78Q8377A. Software drivers are then responsible for reading the rest of the information and programming the TSC 78Q8377A registers with the appropriate values. Three register bits are provided as the interface points to the serial EEPROM; one for the chip select, one for the clock and the other for the data.

Optional Boot Device Support

In ISA mode TSC 78Q8377A diskless workstations by booting from the installed Boot Device. It supports 8 memory base addresses for the Boot Device with 16 Kbytes memory size or 4 memory base addresses with 32 Kbytes size or 2 memory base addresses with 64 Kbytes size. The boot feature can also be disabled through a bit in the serial EEPROM. Both read-only and read-write (eg. Flash) memory are supported by the TSC 78Q8377A. Furthermore, accidental write to the Flash can be prevented through a write protect register bit. Due to the low current drive capability of the boot device (normally 2 mA), a data buffer ('245) is needed to isolate the boot device from the bus. The TSC 78Q8377A provides the necessary control pins to the data buffer and the boot device.

MANCHESTER ENDEC

This block implements Manchester encoding and decoding. Serial NRZ data from the DLC is converted to Manchester encoded data and sent to either the twisted-pair transceiver block or to the Attachment Unit Interface (AUI) driver, depending on which block is active. The decoder section performs three functions: clock recovery, carrier detection and Manchester decoding. The recovered receive clock will be low at the end of reception and during idle to save power. Jitter of up to ± 18 ns can be tolerated by the decoder. This block also translates a 10 MHz collision signal to a logic-level signal before sending it to the DLC block if the AUI port is selected.

TWISTED PAIR TRANSCEIVER

The on-chip Twisted Pair module provides of a number of functions. It has a smart squelch circuitry to determine valid data present on the differential receive inputs TPIP/TPIN. Its transmit and pre-distortion drivers connect to the twisted pair network via the summing resistors and transformer/filter. The link detector/generator circuitry checks the integrity of the cable connecting the two twisted pair MAUs. Collision, jabber and SQE are also incorporated.

The TSC 78Q8377A includes support for Full Duplex operation making the line throughput 20 Mbit/s. In this mode, the collision detection and carrier deference are disabled. In addition to that, the Twisted Pair transceiver SQE generation and "natural" loopback are also turned off.

POWER MANAGEMENT

One very useful and important feature that the TSC 78Q8377A offers is intelligent power management. It supports three different power saving modes: Intelligent, Standby, and Full Shutdown. All modes are configurable through registers. In the Intelligent mode, clocks are active only when they are needed. For example, when not transmitting, the clock supplied to the transmitter circuit in the DLC block is not active while host read from buffer memory may be active. In Standby mode, the oscillator clock is disconnected from the rest of the circuits, so that only the oscillator circuits draw power. Full Shutdown turns off the oscillator, resulting in maximum power savings. Note that this mode is not available when using an external clock source.

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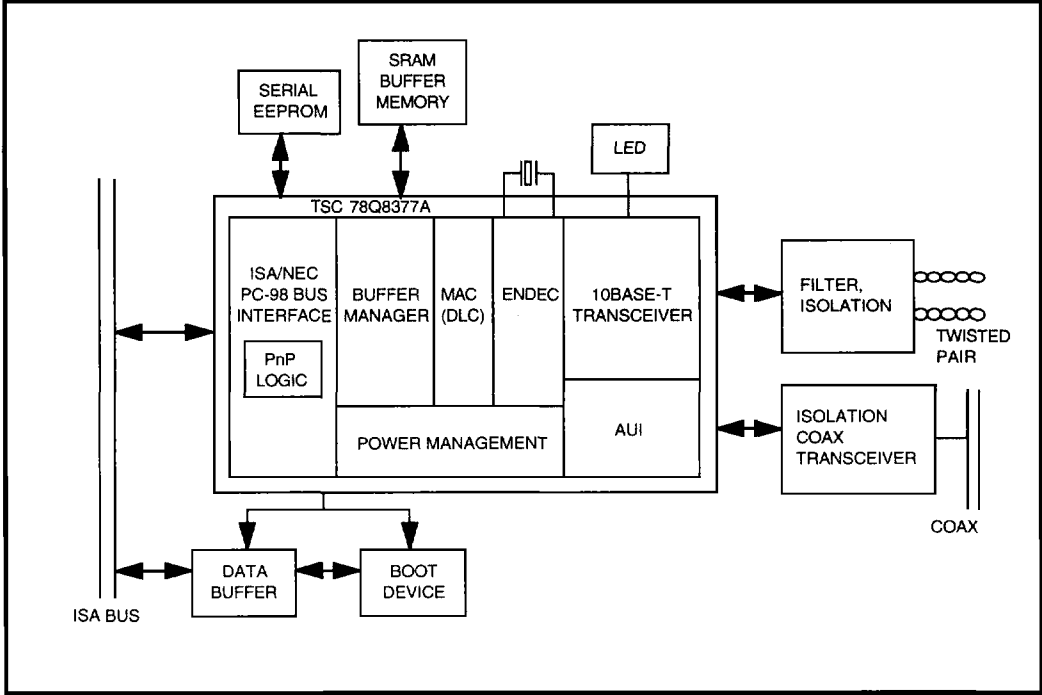


FIGURE 1: System Diagram

TSC 78Q8377A

10BaseT Ethernet Combo for Plug and Play

Pin Assignment Table (ISA bus)

PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE
1	RA1	04	33	$\overline{\text{IRQ5}}$	OT24	65	TPON	AO	97	RD14	IO2
2	RA0	04	34	$\overline{\text{IRQ4}}$	OT24	66	TPOP	AO	98	RD13	IO2
3	VSSIO	G	35	$\overline{\text{IRQ3}}$	OT24	67	VDDT	P	99	RD12	IO2
4	VDDIO	P	36	VSSC	G	68	DON	AO	100	RD11	IO2
5	SD15	IO24	37	SA0	I	69	DOP	AO	101	RD10	IO2
6	SD14	IO24	38	SA1	I	70	VSSA	G	102	RD9	IO2
7	SD13	IO24	39	SA2	I	71	RBIAS	R	103	RD8	IO2
8	SD12	IO24	40	SA3	I	72	VDDA	P	104	VSSIO	G
9	VSSIO	G	41	SA4	I	73	TPIN	AI	105	RD7	IO2
10	SD11	IO24	42	SA5	I	74	TPIP	AI	106	RD6	IO2
11	SD10	IO24	43	SA6	I	75	CIN	AI	107	RD5	IO2
12	SD9	IO24	44	SA7	I	76	CIP	AI	108	RD4	IO2
13	SD8	IO24	45	SA8	I	77	DIN	AI	109	RD3	IO2
14	VSSIO	G	46	SA9	I	78	DIP	AI	110	RD2	IO2
15	SD0	IO24	47	VDDC	P	79	VSSC	G	111	RD1	IO2
16	SD1	IO24	48	SA10	I	80	ISA	I	112	RD0	IO2
17	SD2	IO24	49	SA11	I	81	RSTDRV	SI	113	VSSIO	G
18	SD3	IO24	50	$\overline{\text{SMEMR}}$	I	82	$\overline{\text{BDCS}}$	O4	114	RA15	O4
19	VSSIO	G	51	$\overline{\text{SMEMW}}$	I	83	$\overline{\text{LEDL}}$	OD16	115	RA14	O4
20	SD4	IO24	52	SA14	I	84	$\overline{\text{LEDT}}$	OD16	116	RA13	O4
21	SD5	IO24	53	SA15	I	85	$\overline{\text{LEDR}}$	OD16	117	RA12	O4
22	SD6	IO24	54	SA16	I	86	$\overline{\text{LEDC}}$	OD16	118	RA11	O4
23	SD7	IO24	55	SA17	I	87	OSCO	O	119	RA10	O4
24	VDDIO	P	56	SA18	I	88	OSCI	CI	120	RA9	O4
25	VSSIO	G	57	SA19	I	89	VDDC	P	121	RA8	O4
26	$\overline{\text{IOCS16}}$	OD24	58	$\overline{\text{IOR}}$	I	90	EECS	O4	122	VSSIO	G
27	$\overline{\text{IOCHRDY}}$	OD24	59	$\overline{\text{IOW}}$	I	91	$\overline{\text{RWE}}$	O4	123	RA7	O4
28	$\overline{\text{IRQ15}}$	OT24	60	$\overline{\text{SBHE}}$	I	92	$\overline{\text{ROE}}$	IO4	124	RA6	O4
29	$\overline{\text{IRQ12}}$	OT24	61	AEN	I	93	$\overline{\text{RCS1}}$	O4	125	RA5	O4
30	$\overline{\text{IRQ11}}$	OT24	62	VSST	G	94	$\overline{\text{RCS0}}$	O4	126	RA4	O4
31	$\overline{\text{IRQ10}}$	OT24	63	TPDN	AO	95	VDDIO	P	127	RA3	O4
32	$\overline{\text{IRQ9}}$	OT24	64	TPDP	AO	96	RD15	IO2	128	RA2	O4

(See legend for pin description on following page)

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LEGEND

TYPE	Description	TYPE	Description	TYPE	Description
I	Input (TTL level)	O4	Output with IOL = 4 mA	P, G	Power, Ground
CI	CMOS level Input	OD16, OD24	Output Open Drain with IOL = 16 or 24 mA	R	Resistor to analog ground (20K ± 1%)
SI	Schmitt trigger Input	OT24	Output Tristate with IOL = 24 mA	IO2, IO24	Input (TTL level) & Output with IOL = 2 or 24 mA
AI	Analog Input	AO	Analog Output		

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Pin Assignment Table (NEC PC-98 bus)

PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE	PIN#	PIN NAME	TYPE
1	RA1	04	33	IR5	OT24	65	TPON	AO	97	RD14	IO2
2	RA0	04	34	IR6	OT24	66	TPOP	AO	98	RD13	IO2
3	VSSIO	G	35	IR3	OT24	67	VDDT	P	99	RD12	IO2
4	VDDIO	P	36	VSSC	G	68	DON	AO	100	RD11	IO2
5	DB15	IO24	37	AB0	I	69	DOP	AO	101	RD10	IO2
6	DB14	IO24	38	AB1	I	70	VSSA	G	102	RD9	IO2
7	DB13	IO24	39	AB2	I	71	RBIAS	R	103	RD8	IO2
8	DB12	IO24	40	AB3	I	72	VDDA	P	104	VSSIO	G
9	VSSIO	G	41	AB4	I	73	TPIN	AI	105	RD7	IO2
10	DB11	IO24	42	AB5	I	74	TPIP	AI	106	RD6	IO2
11	DB10	IO24	43	AB6	I	75	CIN	AI	107	RD5	IO2
12	DB9	IO24	44	AB7	I	76	CIP	AI	108	RD4	IO2
13	DB8	IO24	45	AB8	I	77	DIN	AI	109	RD3	IO2
14	VSSIO	G	46	AB9	I	78	DIP	AI	110	RD2	IO2
15	DB0	IO24	47	VDDC	P	79	VSSC	G	111	RD1	IO2
16	DB1	IO24	48	AB10	I	80	ISA	I	112	RD0	IO2
17	DB2	IO24	49	AB11	I	81	RESET	SI	113	VSSIO	G
18	DB3	IO24	50	AB12	I	82	NC	O4	114	RA15	O4
19	VSSIO	G	51	AB13	I	83	LEDL	OD16	115	RA14	O4
20	DB4	IO24	52	AB14	I	84	LEDT	OD16	116	RA13	O4
21	DB5	IO24	53	AB15	I	85	LEDR	OD16	117	RA12	O4
22	DB6	IO24	54	AB16	I	86	LEDC	OD16	118	RA11	O4
23	DB7	IO24	55	AB17	I	87	OSCO	O	119	RA10	O4
24	VDDIO	P	56	AB18	I	88	OSCI	CI	120	RA9	O4
25	VSSIO	G	57	AB19	I	89	VDDC	P	121	RA8	O4
26	NC	OD24	58	IOR	I	90	EECS	O4	122	VSSIO	G
27	IORDY	OD24	59	IOW	I	91	RWE	O4	123	RA7	O4
28	IR13	OT24	60	BHE	I	92	ROE	IO4	124	RA6	O4
29	IR12	OT24	61	CPUENB	I	93	RCS1	O4	125	RA5	O4
30	IR11	OT24	62	VSST	G	94	RCS0	O4	126	RA4	O4
31	IR10	OT24	63	TPDN	AO	95	VDDIO	P	127	RA3	O4
32	IR9	OT24	64	TPDP	AO	96	RD15	IO2	128	RA2	O4

(See legend for pin description on following page)

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LEGEND

TYPE	Description	TYPE	Description	TYPE	Description
I	Input (TTL level)	O4	Output with IOL = 4 mA	P, G	Power, Ground
CI	CMOS level Input	OD16, OD24	Output Open Drain with IOL = 16 or 24 mA	R	Resistor to analog ground (20K ± 1%)
SI	Schmitt trigger Input	OT24	Output Tristate with IOL = 24 mA	IO2, IO24	Input (TTL level) & Output with IOL = 2 or 24 mA
AI	Analog Input	AO	Analog Output		

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PIN DESCRIPTION

Note abbreviations: C = Component, AI = Analog Input, DI = Digital Input, AO = Analog Output, DO = Digital Output, DIO = Digital I/O

ISA/NEC BUS INTERFACE

NAME	TYPE	DESCRIPTION																								
ISA		ISA/NEC PC-98 bus select. Connect to VDD for ISA bus and connect to VSS for NEC PC-98																								
SD/DB [15:0]	DIO	System Data Bus. A bi-directional, tri-state bus with 24 mA drive capable of connecting directly to the ISA/NEC PC-98 data bus.																								
SA/AB [19:0]	DI	System Address Bus. All I/O access uses 12-bit address decoding. In NEC PC-98 bus mode, all I/O access uses 16-bit address decoding. SA[12] and SA[13] are taken from SMEMR and SMEMW respectively. SA[3:0] selects the set of TSC 78Q8377A internal registers. SA[19:14] are needed for Boot Device.																								
AEN/CPUENB	DI	Address Enable. When active (high), it indicates a DMA transfer. It is low during I/O and memory cycle and is used to qualify address decoding.																								
RSTDRV/RESET	DI	Reset Drive. This pin resets the TSC 78Q8377A internal pointers and registers to their appropriate state. It also puts the TSC 78Q8377A in an unconfigured state. This pin has to remain active for at least 200 ns.																								
SBHE/BHE	DI	System Byte High Enable. When active (low), it indicates a transfer of data on upper byte of the system data bus SD[15:8]. This signal is only applicable when the TSC 78Q8377A is in word mode (when HBYTE bit in DLCR6<5> is set to 0). The complete truth table of the byte/ word and lower/ upper bus transfer is given here.																								
		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>HBYTE</th> <th>SBHE</th> <th>SA0</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Word transfer</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Byte transfer on SD[15:8]</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>Byte transfer on SD[7:0]</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Reserved</td> </tr> <tr> <td>1</td> <td>X</td> <td>X</td> <td>Byte transfer (SD[7:0])</td> </tr> </tbody> </table>	HBYTE	SBHE	SA0	Function	0	0	0	Word transfer	0	0	1	Byte transfer on SD[15:8]	0	1	0	Byte transfer on SD[7:0]	1	1	1	Reserved	1	X	X	Byte transfer (SD[7:0])
		HBYTE	SBHE	SA0	Function																					
		0	0	0	Word transfer																					
		0	0	1	Byte transfer on SD[15:8]																					
		0	1	0	Byte transfer on SD[7:0]																					
1	1	1	Reserved																							
1	X	X	Byte transfer (SD[7:0])																							
The PnP register access is always through the lower data bus independent of HBYTE setting. NEC PC-98 bus mode is defined for 16-bit bus operation only. For those PnP registers located at odd addresses the register access will always utilize the higher data bits.																										
IOCHRDY/IORDY	DO	I/O Channel Ready. Open-drain signal with 24 mA drive. For normal register access this signal is always inactive (tristate). For accesses to the data port (BMR8), this signal may be pulled low by the chip to delay the completion of the current read or write operation. It will also be used if the device is unable to respond to read or write requests within 2.4 μ s. In these situations, the TSC 78Q8377A will also assert interrupt and the host read error status bit (DLCR1<6>) or host write error status bit (DLCR0<0>).																								

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TSC 78Q8377A

10BaseT Ethernet Combo

for Plug and Play

PIN DESCRIPTION (continued)

Note abbreviations: C = Component, AI = Analog Input, DI = Digital Input, AO = Analog Output, DO = Digital Output, DIO = Digital I/O

ISA/NEC BUS INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{\text{IOCS16}}$ (ISA Only)	DO	I/O Chip Select 16-bit. Active low, open-drain signal with 24 mA drive. When pulled low, it informs the host that TSC 78Q8377A device is capable of 16 bit access. Therefore, this signal can only be activated if HBYTE (DLCR6<5>) is set to zero. The TSC 78Q8377A follows the IEEE P996 specification that recommends this function be implemented as a pure decode of SA[9:0] and AEN, with no dependency on $\overline{\text{IOR}}$ or $\overline{\text{IOW}}$. Since the Plug and Play register is defined for 8-bit access only, the signal $\overline{\text{IOCS16}}$ will not go low for Plug and Play register access independent of the HBYTE setting. This signal is not used in NEC PC-98 bus mode.
$\overline{\text{IOR}}$	DI	I/O Read. Active low read strobe.
$\overline{\text{IOW}}$	DI	I/O Write. Active low write strobe.
$\overline{\text{SMEMR}}$ (ISA Only)	DI	System Memory Read. Active low memory read cycle strobe. It is active for memory read within the low 1 Mbyte of the memory space. This signal, together with the $\overline{\text{SMEMW}}$, is used to qualify for the Boot Device Chip Select ($\overline{\text{BDCS}}$).
$\overline{\text{SMEMW}}$ (ISA Only)	DI	System Memory Write. Active low memory write cycle strobe. It is active for memory write within the low 1 Mbyte of the memory space. This signal (when write protect is disabled), together with the $\overline{\text{SMEMR}}$, is used to qualify for the Boot Device Chip Select ($\overline{\text{BDCS}}$).
$\overline{\text{IRQ3}}, \overline{4}, \overline{5}, \overline{9}, \overline{10}, \overline{11}, \overline{12}, \overline{15}$ $\text{IR3}, 5, 6, 9, 10, 11, 12, 13$	DO	Interrupt Request. Tri-state with 24 mA drive. The TSC 78Q8377A supports both edge and level-sensitive interrupt. When edge mode interrupt is selected, the TSC 78Q8377A generates interrupts by driving a low followed by a high and then tri-stating the interrupt line. When level-sensitive mode is selected, the TSC 78Q8377A generates interrupts by pulling the IRQ line low. It continuously drives it low until the interrupt has been serviced; at which time the IRQ is returned to tristate. This tristate implementation allows for shareable interrupt lines with other cards in the system. In NEC PC-98 bus mode, $\text{IRQ}\$$ and $\text{IRQ!}\%$ are interrupt lines 6 and 13 respectively. In ISA mode, $\text{IRQ}\$$ and $\text{IRQ!}\%$ are interrupt lines 4 and 15 respectively.
$\overline{\text{BDCS}}$ (ISA Only)	DO	Boot Device Chip Select. Active low signal which indicates that the current memory access cycle is from or to the boot device. The boot device address bus connects directly to the ISA address bus and the data bus connects through a data buffer to the ISA data bus. The boot device $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins (eg. for flash memory) connect to the $\overline{\text{SMEMR}}$ and $\overline{\text{SMEMW}}$ signals respectively. When the WP bit (BMR12<3>) is set, writing to the boot device is prevented. This signal is not used in NEC PC-98 bus mode.

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10BaseT Ethernet Combo for Plug and Play

PIN DESCRIPTION (continued)

Note abbreviations: C = Component, AI = Analog Input, DI = Digital Input, AO = Analog Output, DO = Digital Output, DIO = Digital I/O

BUFFER MEMORY INTERFACE

NAME	TYPE	DESCRIPTION
RCS0, RCS1	DO	RAM Chip Select. RCS0 and RCS1 are active low chip select lines for the SRAM with RCS0 as the least significant byte.
ROE	DO	RAM Output Enable. Active low. This is the output enable asserted by the TSC 78Q8377A during buffer memory read cycles for the SRAM.
RWE	DO	RAM Write Enable. Active low. This is the write enable asserted by the TSC 78Q8377A during buffer memory write cycles for the SRAM.
RD[0:15]	DI/O	RAM Data Bus. This is the data bus between the TSC 78Q8377A and the buffer memory. It can be configured for byte or word transfer depending on register bit RBYTE (DLCR6 <4>) RAM BYTE. For word transfers, the ordering of the most and least significant byte is defined by the register bit, INTLMOT (DLCR7 <0>). In PCMCIA bus mode, this data bus is only 8 bits wide (RD[0:7]).
RA[0:15]	DO	RAM Address Bus. Addresses up to 64 KByte of SRAM buffer memory.

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NETWORK ATTACHMENT UNIT INTERFACE

DON, DOP	AO	Transmit Data Negative and Positive. Differential outputs to external transceiver for transmission.
DIN, DIP	AI	Receive Data Negative and Positive. Manchester differential inputs from external transceiver for reception.
CIN, CIP	AI	Collision Detect Negative and Positive. When an externally connected transceiver detects a collision on the medium, these differential inputs are driven by a 10 MHz signal.
RBIAS	C	Biassing Resistor. External biasing resistor. Connect to 20 k Ω \pm 1% to VSSA (Analog ground).

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PIN DESCRIPTION (continued)

NETWORK TWISTED-PAIR MEDIUM INTERFACE

NAME	TYPE	DESCRIPTION
TPON, TPOP	AO	Twisted-Pair Output Negative and Positive. Driver outputs to twisted-pair medium. Must be summed together with TPDN and TPDP by external resistors in a pre-equalization network to produce twisted-pair transmit signal.
TPDN, TPDP	AO	Twisted-Pair Delayed Negative and Positive. Delayed (50 ns) driver outputs to twisted-pair medium. Must be summed together with TPON and TPOP by external resistors in a pre-equalization network to produce twisted-pair transmit signal.
TPIN, TPIP	AI	Twisted-Pair Input Negative and Positive. Inputs from twisted-pair medium.

CRYSTAL OSCILLATOR

OSCI	DI	Oscillator In. Connection for one side of the 20 MHz crystal or an input for an external 20 MHz clock source.
OSCO	DO	Oscillator Out. Connection for other side of the 20 MHz crystal. Left unconnected if an external clock is used.

EEPROM PINS

EECS	DO	EEPROM Chip select.
EESK	DO	EEPROM Serial clock. Shared with $\overline{RCS1}$.
EEDI	DO	EEPROM Data input. Shared with $\overline{RCS0}$.
EEDO	DI	EEPROM Data output. Shared with \overline{ROE} .

LED PINS

\overline{LEDL}	DO	LED Link. Active low, open drain with 16 mA drive.
\overline{LEDT}	DO	LED Transmit. Active low, open drain with 16 mA drive.
\overline{LEDR}	DO	LED Receive. Active low, open drain with 16 mA drive.
\overline{LEDC}	DO	LED Collision. Active low, open drain with 16 mA drive. When Full Duplex mode is selected, this pin is always low.

POWER SUPPLY PINS

VDD		3 for I/O pads (VDDIO), 2 for digital core (VDDC); 1 for analog (VDDA); 1 for transmit drivers (VDDT).
VSS		8 for I/O pads (VSSIO), 2 for digital core (VSSC); 1 for analog (VSSA); 1 for transmit drivers (VSST).

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REGISTER DESCRIPTION

PLUG AND PLAY REGISTERS

Only three 8-bit ports are used by the software to access the Plug and Play registers. The Plug and Play registers are accessed by first writing the address of the desired register to the ADDRESS port, followed by a read of data from the RD_DATA port or a write of data to the WR_DATA port.

PORT NAME	LOCATION	TYPE
ADDRESS	0x0279 (Printer status port)	Write-only
WR_DATA	0x0A79 (0x0279 + 0x0800)	Write-only
RD_DATA	Relocatable in range 0x0203 to 0x03FF	Read-only

PLUG AND PLAY REGISTER MAP

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x00	RD_DATA_ADDR							
0x01	ISOLATION							
0x02	(0)	(0)	(0)	(0)	(0)	RST_CSN	RST_ST	RST_LD
0x03	WAKE[CSN]							
0x04	RESOURCE							
0x05	(0)	(0)	(0)	(0)	(0)	(0)	(0)	R_STAT
0x06	CSN							
0x07	LDN = 0							
0x08 - 0x2F	0							
0x30	0	0	0	0	0	0	0	ACTV
0x31	0	0	0	0	0	0	IORNG_EN	IORNG_V
0x32 - 0x3F	0							
0x40	0	0	0	0	1	1	0	BDA2
0x41	BDA1	BDA0	0	0	0	0	0	0
0x42	(0)	(0)	(0)	(0)	(0)	(0)	M16=0	UL=0
0x43	1	1	1	1	1	1	1	1
0x44	BDSZ1	BDSZ0	0	0	0	0	0	0
0x45 - 0x5F	0							
0x60	IOA15	IOA14	IOA13	IOA12	IOA11	IOA10	IOA9	IOA8
0x61	IOA7	IOA6	IOA5	IOA4	0	0	0	0
0x62 - 0x6F	0							

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PLUG AND PLAY REGISTER MAP (continued)

ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x70	(0)	(0)	(0)	(0)	IRQ3	IRQ2	IRQ1	IRQ0
0x71	(0)	(0)	(0)	(0)	(0)	(0)	IRQ_LVL	IRQ_TYPE
0x72	(0)	(0)	(0)	(0)	0	0	0	0
0x73	(0)	(0)	(0)	(0)	(0)	(0)	0	0
0x74	(0)	(0)	(0)	(0)	(0)	1	0	0
0x75	(0)	(0)	(0)	(0)	(0)	1	0	0
0x76 - 0xA8	0							
0xA9 - 0xFF	0							

* Please refer to TSC 78Q8377A Technical Reference Guide for a more detailed description of register bits.

LEGEND:

TYPE	DESCRIPTION
R	Readable
W	Writable
0/1	Power up / reset default value

SERIAL EEPROM MAP

ADDRESS	HIGH BYTE	LOW BYTE	DESCRIPTION
0		Bit 0: PnP_ACT	PnP Activate Reg
1	PnP0x41	PnP0x40	Plug and Play Configuration Register
2		PnP0x44	
3	PnP0x61	PnP0x60	
4	PnP0x71	PnP0x70	
5 to 7			Reserved
8 to 1F	Eg: IEEE Address, BMR default setting, etc		Custom Configuration
20	Vendor EISA ID Byte 1	Vendor EISA ID Byte 0	PnP Serial Identifier
21	Vendor Assigned ID Byte 1	Vendor Assigned ID Byte 0	
22	Serial Number Byte 1	Serial Number Byte 0	
23	Serial Number Byte 3	Serial Number Byte 2	
24		Checksum	
25 onwards			PnP Resource Data

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PNP ACTIVATE REGISTER

Only bit 0 (PnP_ACT) is defined in this register. This bit is provided to let the TSC 78Q8377A work in a non-PnP environment by powering up active. It also allows the TSC 78Q8377A to participate in the boot process in a non-PnP Bios system.

PNP CONFIGURATION REGISTER

The PnP configuration is also automatically read by the EEPROM logic and the values programmed into the appropriate PnP registers. This becomes the default configuration for the chip in the absence of PnP protocol. The configuration can only be changed through a "PnP protocol" utility.

CUSTOM CONFIGURATION

This space is allocated for custom configuration. The users may fill this space with defaults such as IEEE address, BMR register settings, etc. The software driver is responsible for reading this space and programming the appropriate registers (the TSC 78Q8377A EEPROM logic will not read this space).

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PNP SERIAL IDENTIFIER

Once the Isolation state is entered, the EEPROM logic will start loading the PnP serial identifier. The PnP serial identifier is loaded one word at a time after the serial isolation protocol has issued 16 pair of reads.

PNP RESOURCE DATA

Entering the Config state initiates the loading of the PnP resource data. After one word has been accumulated from the EEPROM, the R_STAT (resource status) bit is set to one. It will be reset to zero again after two reads from the RESOURCE register and the process repeats. If the Config state is entered from the Sleep state without going through the Isolation state, the first read from the RESOURCE data will return the PnP Serial Identifier data.

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REGISTER DESCRIPTION (continued)

APPENDIX

PLUG AND PLAY STATES

There are 4 PnP states defined in the Plug and Play Specification. They are:

- **Wait for Key** (W4K)
- **Sleep** (SLP)
- **Isolation** (ISO)
- **Config** (CFG)

Valid Commands and States

ADDRESS	REGISTER NAME	VALID ACCESS IN STATE		
		SLP	ISO	CFG
0x00	Read Data Address		*	* 1
0x01	Isolation		*	
0x02	Reset	*	*	*
0x03	Wake	*	*	*
0x04, 05	Resource			*
0x06	CSN		*	* 1
0x07	LDN			*
0x30	Activate			*
0x31	I/O Range Check			*
0x40-44, 0x60, 61, 0x70, 71	Memory, I/O, Interrupt		*	

Note 1: The PnP Spec V1.0a does not include the CFG state in this register access.

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Supply voltage, Vdd	-0.5 to 6.0V
Input voltage, Vin	-0.5 to Vdd + 0.5V
Output voltage, Vout	-0.5 to Vdd + 0.5V
Storage temperature, Tstg	-55 to 150°C
Lead temperature (max 10 sec soldering), Tl	250°C max

DC CHARACTERISTICS (Ta = 0 to 70°C, Vdd = 5V ±5%)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Low level input voltage V _{IL}	TTL inputs			0.8	V
	OSCI pin			1.6	V
	Schmitt inputs			1.1	V
High level input voltage V _{IH}	TTL inputs	2.2			V
	OSCI pin	3.8			V
	Schmitt inputs	3.5			V
Pull down current (RESET pin) I _{pd}		13		50	μA
Low level output voltage V _{OL}	Rated I _{OL}	0		0.4	V
High level output voltage V _{OH}	Rated I _{OH}	2.4		Vdd	V
Low level output current I _{OL} (with V _{OL} = 0.4V)	Pin types O4, IO4	4			mA
	Pin type OD16	16			mA
	Pin type IO2	2			mA
	Pin type OD24, OT24, IO24	24			mA
High level output current I _{OH} (with V _{OH} = 2.4V)	Pin types O4, IO4	-4			mA
	Pin type IO2	-2			mA
	Pin type OT24, IO24	-24			mA
Leakage current (input/output) I _L		-10		10	μA
Supply current I _{DD}	Fully active ⁽¹⁾			60	mA
	Idle			40	mA
Power down supply current I _{pwrdn}	Osc. on			20	mA
	Osc. off			200	μA

Note: (1) Fully active means 3 "simultaneous" operations: transmitting, receiving (through twisted-pair port) and either host write or read.

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ELECTRICAL SPECIFICATIONS (continued)

AUI CHARACTERISTICS

(VDD = 5V ± 5%, VSS = 0V, Ta = 0°C to +70°C)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Low Output Voltage for DOP, DON Vaol RL = 78Ω	Rext = 20 kΩ	Vdd -1.5		Vdd -0.75	V
High Output Voltage for DOP, DON Vaoh	Rext = 20 kΩ RL = 78Ω	Vdd -0.55		Vdd	V
DOP, DON Output Current Iao	Rext = 20 kΩ	8		14	mA
DIP, DIN, CIP, CIN Open Circuit Input Voltage (bias) Valb		2.45		3.33	V
DIP, DIN, CIP, CIN Diff Squelch Threshold Vasq		-300		-120	mV
DOP, DON Diff Idle Output Vadi	RL = 78Ω	-40		40	mV
DOP, DON Diff Peak Output Vadv	Rext = 20 kΩ RL = 78Ω	620		1100	mV
DOP, DON Output Resistance Rao				75	Ω

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TWISTED PAIR

(VDD = 5V ± 5%, Ta = 0°C to +70°C)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TPIP, TPIN Diff Input Resistance Rti		3			kΩ
TPIP, TPIN Open Circuit Input Voltage (bias) Vtib		2.45		3.33	V
TPIP, TPIN Diff Input Voltage Range Vtiv	VDD = 5V	-3.1		3.1	V
TPIP, TPIN Positive Squelched Threshold Vtps	Note 1	300		585	mV
TPIP, TPIN Negative Squelched Threshold Vtns	Note 1	-585		-300	mV
TPIP, TPIN Positive Unsquelched Threshold Vtpu	Note 2		180		mV
TPIP, TPIN Negative Unsquelched Threshold Vtnu	Note 2		-180		mV
TPIP, TPIN Positive Squelched Threshold Long Distance Mode Vltps	Note 1	120		300	mV
TPIP, TPIN Negative Squelched Threshold Long Distance Mode Vltns	Note 1	-300		-120	mV
TPIP, TPIN Positive Unsquelched Threshold Long Distance Mode Vltpu	Note 2		100		mV
TPIP, TPIN Negative Unsquelched Threshold Long Distance Mode Vltnu	Note 2		-100		mV
TPOP, TPON High Output Voltage Vtoh	I = 32 mA	Vddtp -0.44		Vddtp	V
TPOP, TPON Low Output Voltage Vtol	I = 32 mA	Vsstp		Vsstp +0.44	V
TPDP, TPDN High Voltage Vtdh	I = 16 mA	Vddtp -0.44		Vddtp	V
TPDP, TPDN Low Voltage Vtdl	I = 16 mA	Vsstp		Vsstp +0.44	V
TPDP, TPDN Output Resistance Rtd				27	Ω
TPOP, TPON Output Resistance Rto				13.5	Ω

Note 1: Sine wave at 2 MHz, 5 MHz and 7 MHz

Note 2: Sine wave : 5 MHz ≤ f ≤ 10 MHz

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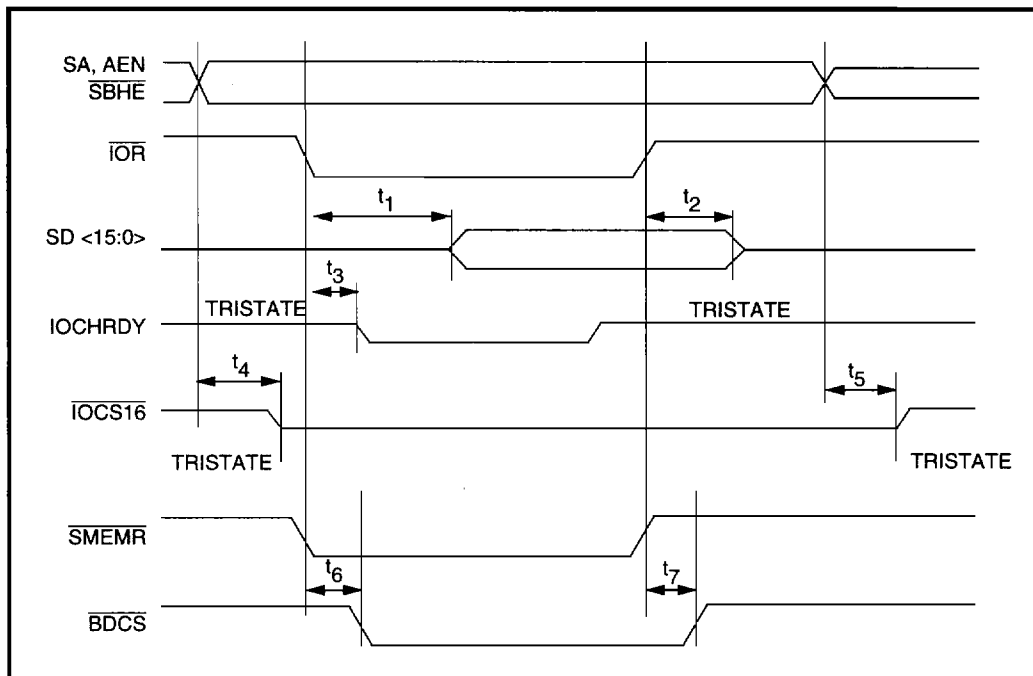


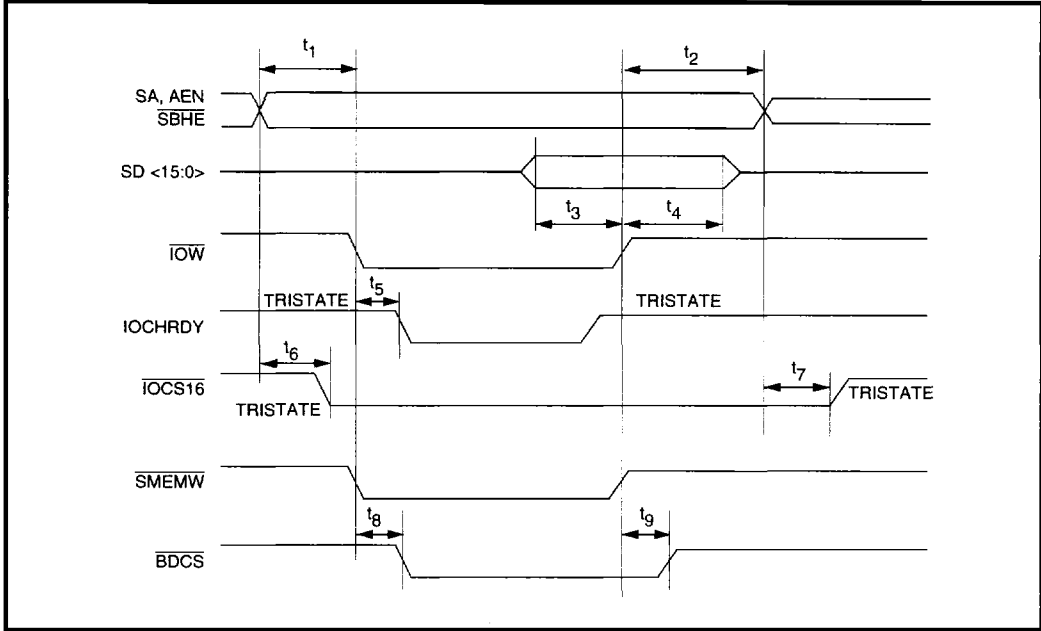
FIGURE 2: Read Cycle

ELECTRICAL SPECIFICATIONS (continued)

TABLE 1: Read Cycle

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{\text{IOB}}$ to SD<15:0> valid	t_1			45	ns
$\overline{\text{IOB}}$ to SD<15:0> tristate	t_2	8			ns
$\overline{\text{IOB}}$ to IOCHRDY not ready	t_3			18	ns
SA, AEN to $\overline{\text{SBHE}}$ to $\overline{\text{IOCS16}}$ Tristate to low	t_4			18	ns
SA, AEN to $\overline{\text{IOCS16}}$ low to Tristate	t_5			18	ns
SMEMR to BDCS active	t_6			25	ns
SMEMR to BDCS inactive	t_7			25	ns

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FIGURE 3: Write Cycle

TABLE 2: Write Cycle

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
SA, SBHE and AEN setup time to IOW low	t_1	15			ns
Hold time of SA, SBHE and AEN after IOW high	t_2	8			ns
Setup time of SD to IOW high	t_3	25			ns
Hold time of SD to after IOW low	t_4	8			ns
IOW to IOCHRDY not ready	t_5			18	ns
SA, AEN, SBHE to IOCS16 low to Tristate	t_6			18	ns
SA, AEN to IOCS16 Tristate to low	t_7	0		36	ns
SMEMW to BDCS active	t_8			25	ns
SMEMW to BDCS inactive	t_9			25	ns

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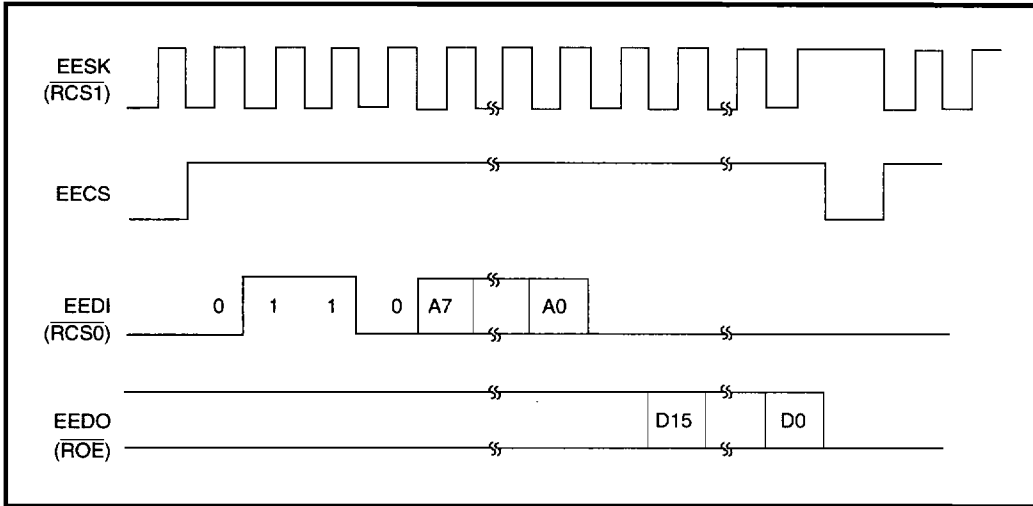


FIGURE 4: Serial Shift EEPROM Interface Read Timing

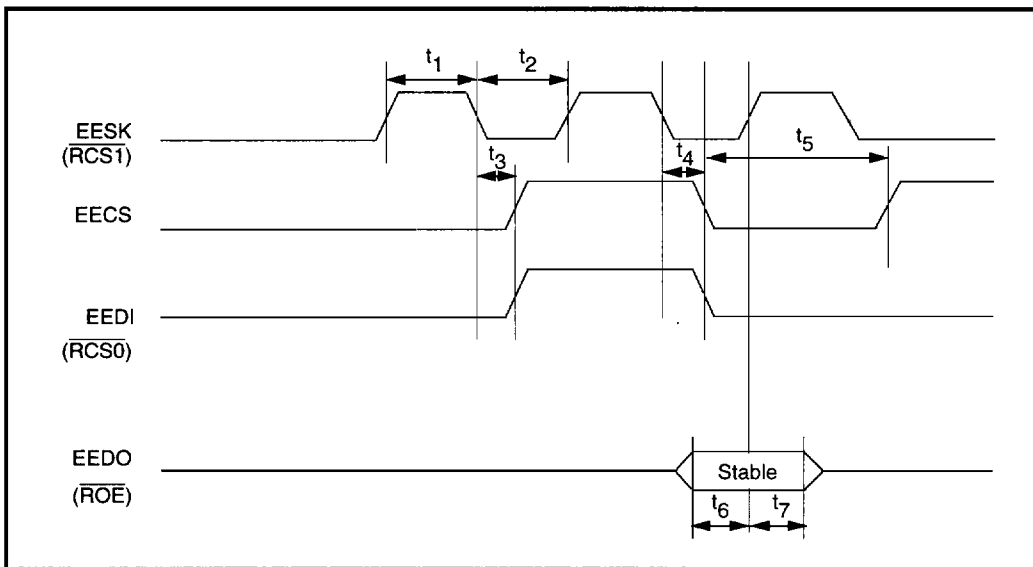


FIGURE 5: Serial EEPROM Control Timing

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ELECTRICAL SPECIFICATIONS (continued)

TABLE 3: Serial EEPROM Control Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
EESK High Time	t_1	790	800		ns
EESK Low Time	t_2	790	800		ns
\uparrow EECS, EEDI From \downarrow EESK	t_3	-15		15	ns
\downarrow EESK, EEDI From \downarrow EESK	t_4	-15		15	ns
EECS Low Time	t_5		1600		ns
EEDO Setup to \uparrow EESK	t_6	20			ns
EEDO Hold From \uparrow EESK	t_7	0			ns

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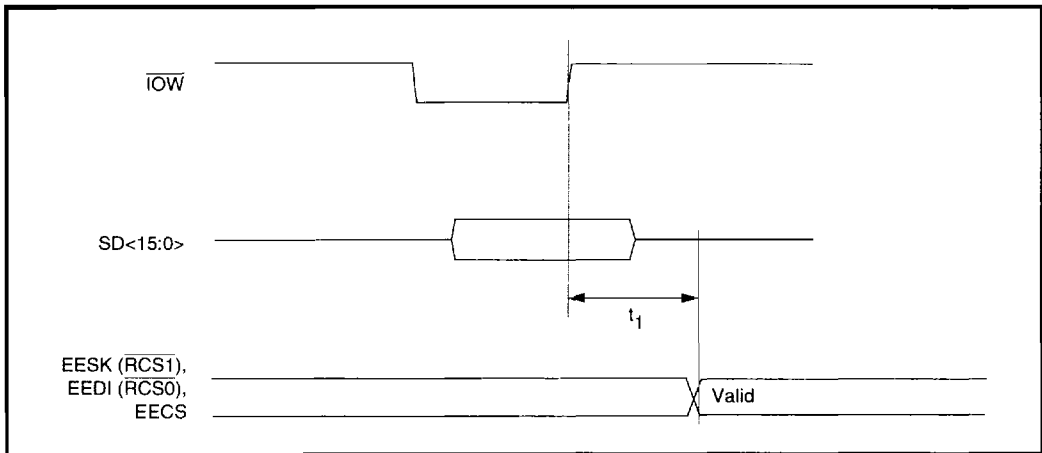


FIGURE 6: EEPROM Write Timing

TABLE 4: EEPROM Write Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{\text{IOW}}$ to EESK ($\overline{\text{RCS1}}$), EEDI ($\overline{\text{RCS0}}$), EECS valid	t_1			30	ns

Note: The SD signal is for reference only.

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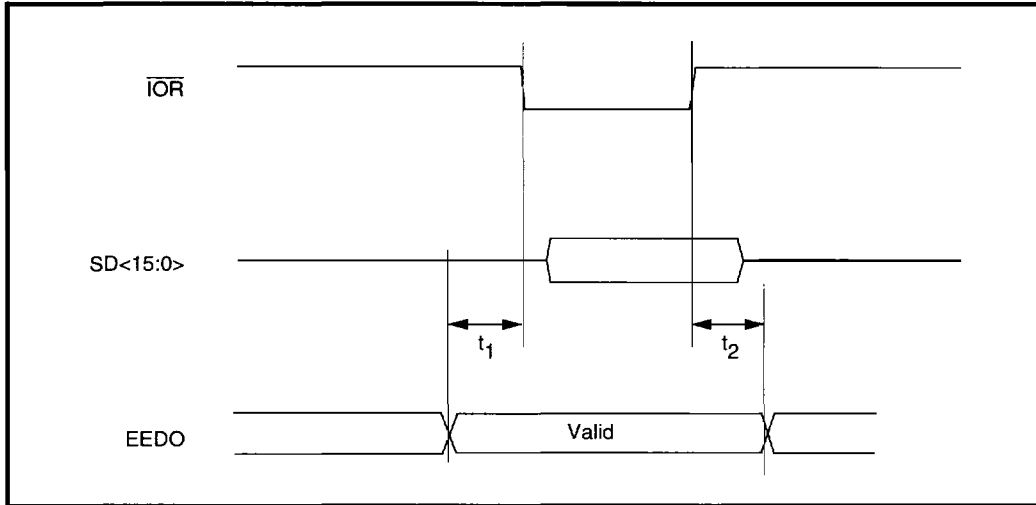


FIGURE 7: EEPROM Read Timing

ELECTRICAL SPECIFICATIONS (continued)

TABLE 5: EEPROM Read Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
EEDO valid to $\overline{\text{iOR}}$	t_1	0			ns
$\overline{\text{iOR}}$ to EEDO invalid	t_2	0			ns

Note: The SD signal is for reference only.

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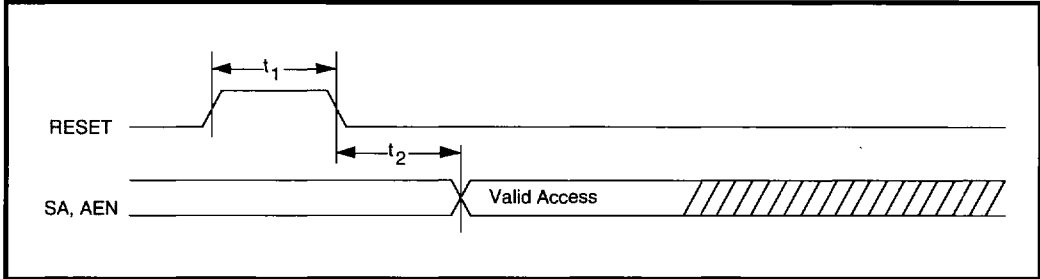


FIGURE 8: RESET Timing

TABLE 6: RESET Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
RESET pulse width	t_1	500			ns
RESET low to first valid access	t_2	800			ns

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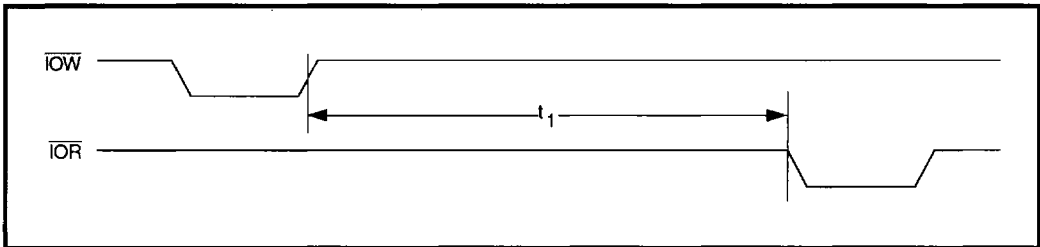


FIGURE 9: Skip Packet Timing

TABLE 7: Skip Packet Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Writing Skip Packet high to next Buffer Memory Port read	t_1	200			ns

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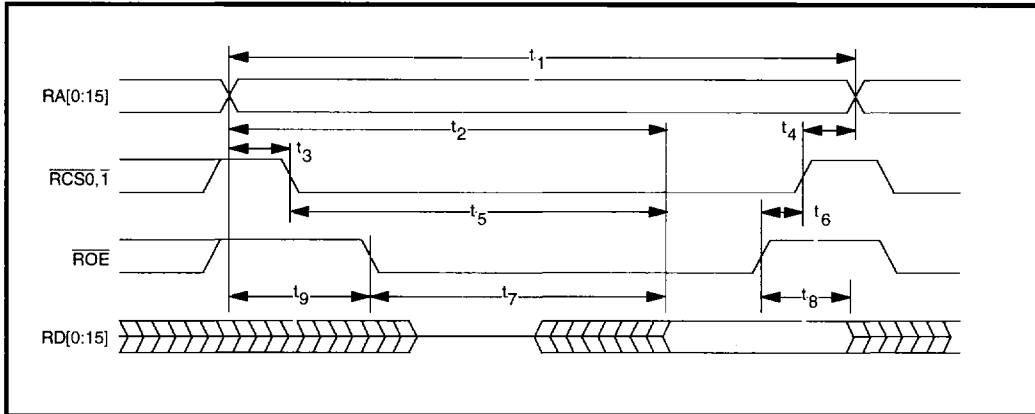


FIGURE 10: SRAM Read Timing

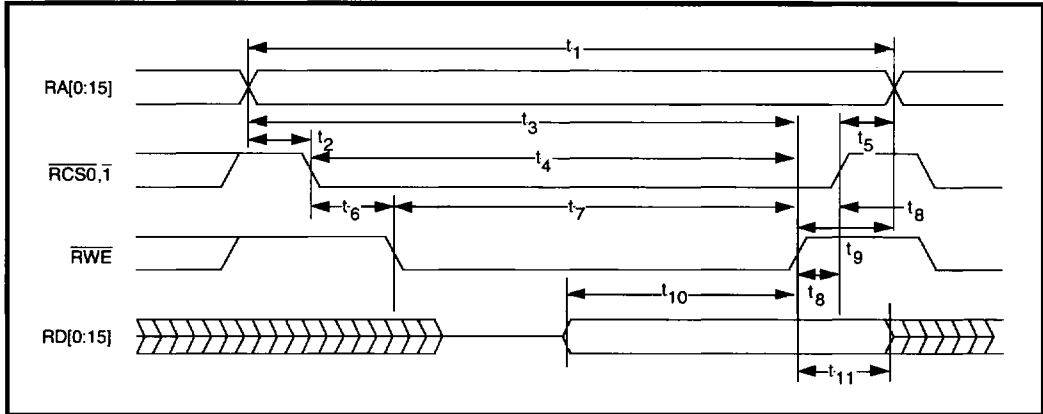
ELECTRICAL SPECIFICATIONS (continued)

TABLE 8: SRAM Read Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Read cycle	t_1 RAMSP = 1	95			ns
	RAMSP = 0	145			ns
Address access time	t_2 RAMSP = 1			75	ns
	RAMSP = 0			125	ns
Address valid to $\overline{RCS0,1}$ low	t_3			8	ns
$\overline{RCS0,1}$ high to address invalid	t_4	0			ns
Chip select access time	t_5 RAMSP = 1			75	ns
	RAMSP = 0			125	ns
\overline{ROE} high to $\overline{RCS0,1}$ high	t_6	0		8	ns
Output enable access time	t_7 RAMSP = 1			50	ns
	RAMSP = 0			100	ns
Data hold time	t_8	0			ns
Address valid to \overline{ROE} low	t_9			30	ns

Note: Use SRAM with address access time of 75 ns or less for RAMSP = 1 and 125 ns or less for RAMSP = 0. RAMSP is DLCR6 <6>.

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FIGURE 11: SRAM Write Timing

TABLE 9: SRAM Write Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Write Cycle t_1	RAMSP = 1	95			ns
	RAMSP = 0	145			ns
Address Valid to $\overline{RCS0,1}$ low t_2				8	ns
Address Valid to \overline{RWE} high t_3	RAMSP = 1	70			ns
	RAMSP = 0	120			ns
$\overline{RCS0,1}$ low to \overline{RWE} high t_4	RAMSP = 1	70			ns
	RAMSP = 0	120			ns
$\overline{RCS0,1}$ high to Address Invalid t_5		0			ns
$\overline{RCS0,1}$ low to \overline{RWE} low t_6		0			ns
\overline{RWE} Pulse Width t_7	RAMSP = 1	70			ns
	RAMSP = 0	120			ns
\overline{RWE} high to $\overline{RCS0,1}$ high t_8		0			ns
\overline{RWE} high to Address Invalid t_9		10			ns
Data Setup Time t_{10}	RAMSP = 1	40			ns
	RAMSP = 0	90			ns
Data Hold Time t_{11}		20			ns

Note: Use SRAM with address access time of 75 ns or less for RAMSP = 1 and 125 ns or less for RAMSP = 0. RAMSP is DLCR6 <6>.

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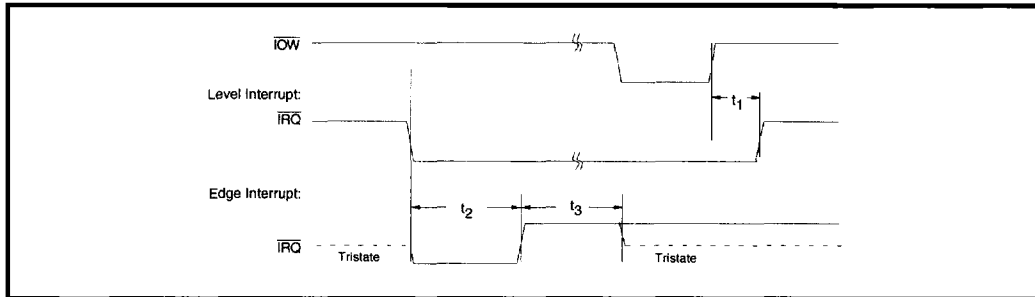


FIGURE 12: Interrupt Timing

ELECTRICAL SPECIFICATIONS (continued)

TABLE 10: Interrupt Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
$\overline{\text{IRQ}}$ signal clearing delay	t_1 level interrupt	7		40	ns
$\overline{\text{IRQ}}$ low pulse width	t_2 edge interrupt	150		200	ns
$\overline{\text{IRQ}}$ high driving time	t_3 edge interrupt	150		200	ns

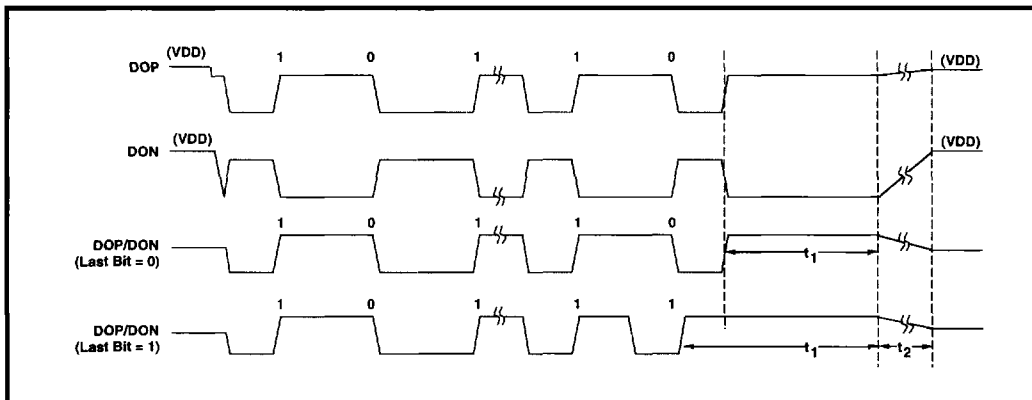
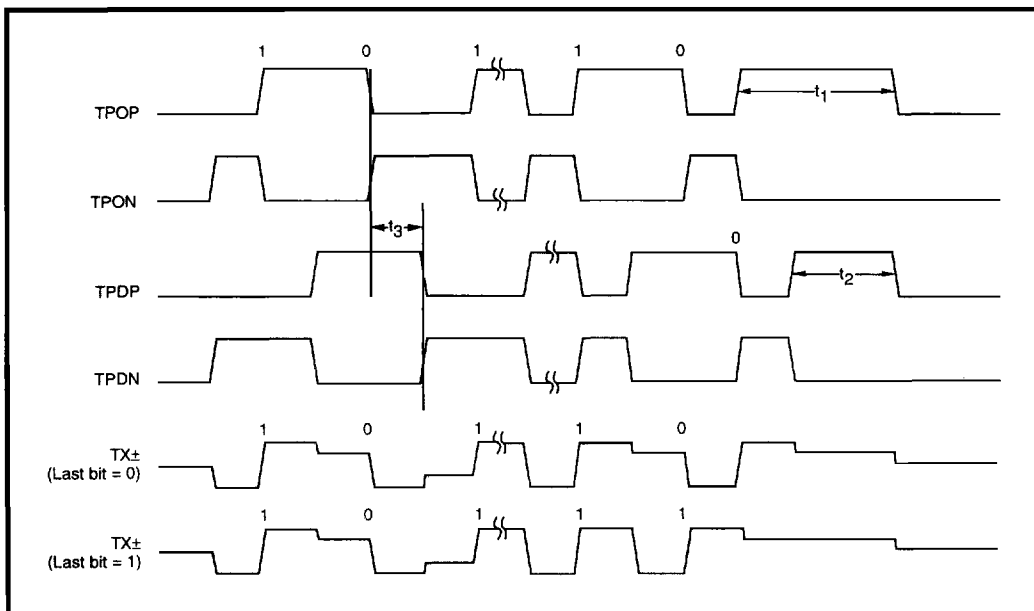


FIGURE 13: Transmit Timing (AUI)

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TABLE 11: Transmit Timing (AUI)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
DOP/DON end-of-packet delimiter	t_1	200			ns
DOP/DON line voltage transition	t_2			8	μ s



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FIGURE 14: Transmit Timing (TP)

TABLE 12: Transmit Timing (TP)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TPOP/TPON end-of-packet delimiter	t_1	250			ns
TPDP/TPDN end-of-packet delimiter	t_2	200			ns
TPOP to TPDP and TPON to TPDN delay	t_3		50		ns

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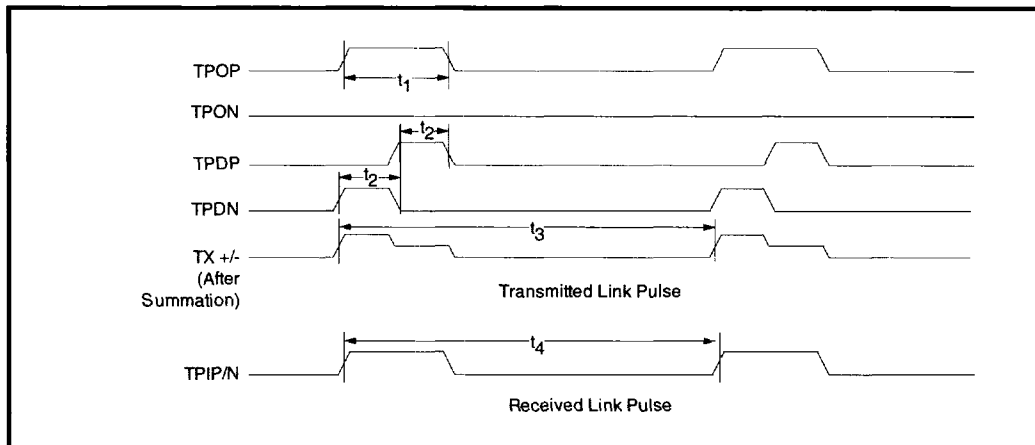


FIGURE 15: Link Test Timing

ELECTRICAL SPECIFICATIONS (continued)

TABLE 13: Link Test Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TPOP link pulse width	t_1		150		ns
TPDP/TPDN link pulse width	t_2		100		ns
Duration between transmitted link pulses	t_3	9		11	ms
Duration between received link pulses	t_4	4.1		65	ms

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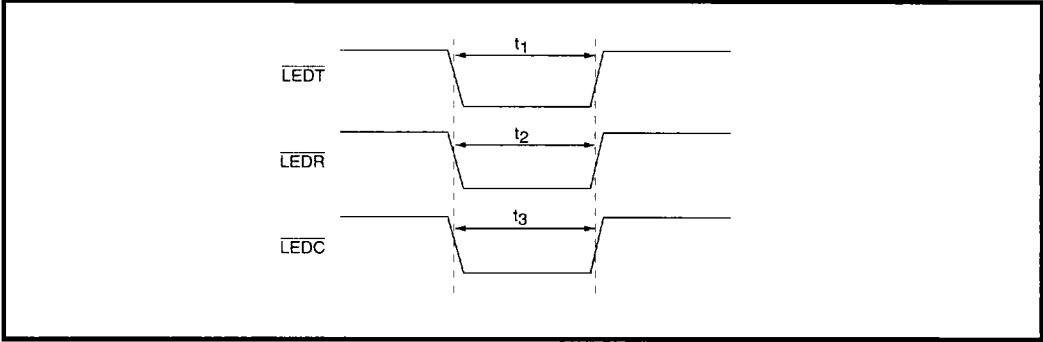


FIGURE 16: LED Timing

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TABLE 14: LED Timing

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Transmit blink-on timing t_1			100		ms
Receive blink-on timing t_2			100		ms
Collision blink-on timing t_3			100		ms

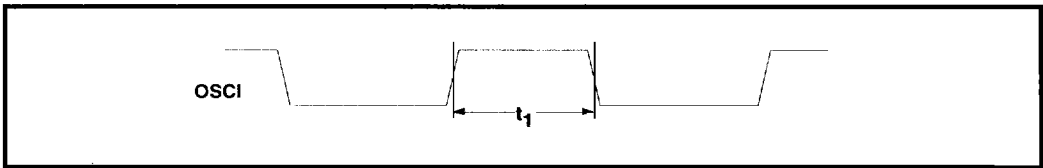


FIGURE 17: Oscillator Duty Cycle

TABLE 15: OSCI Duty Cycle

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Oscillator duty cycle t_1		40	50	60	%

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10BaseT Ethernet Combo

for Plug and Play

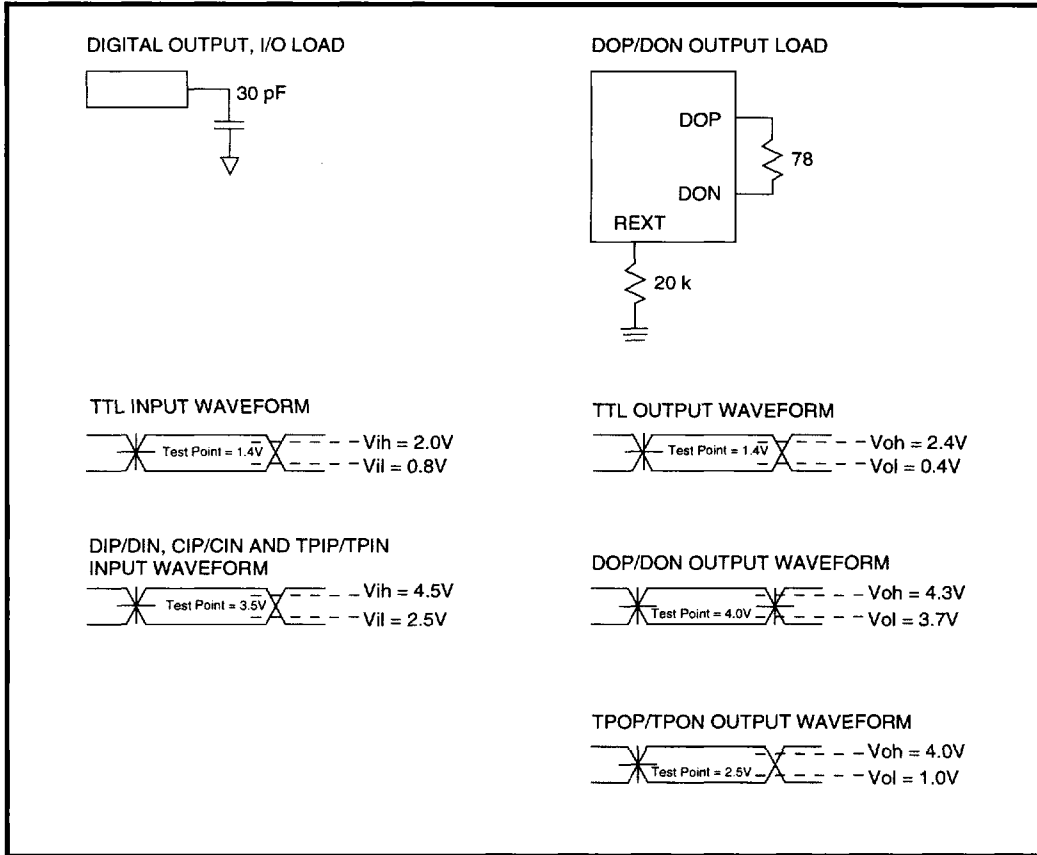


FIGURE 18: Test Conditions

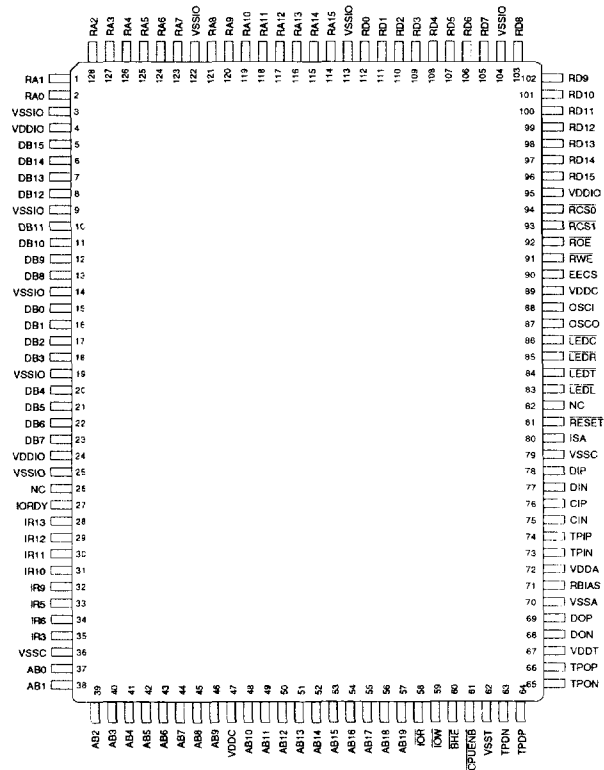
TSC 78Q8377A

10BaseT Ethernet Combo

for Plug and Play

PACKAGE PIN DESIGNATIONS

(Top View)



3

128-Lead QFP
NEC PC-98 Bus Mode

CAUTION: Use handling procedures necessary for a static sensitive component.

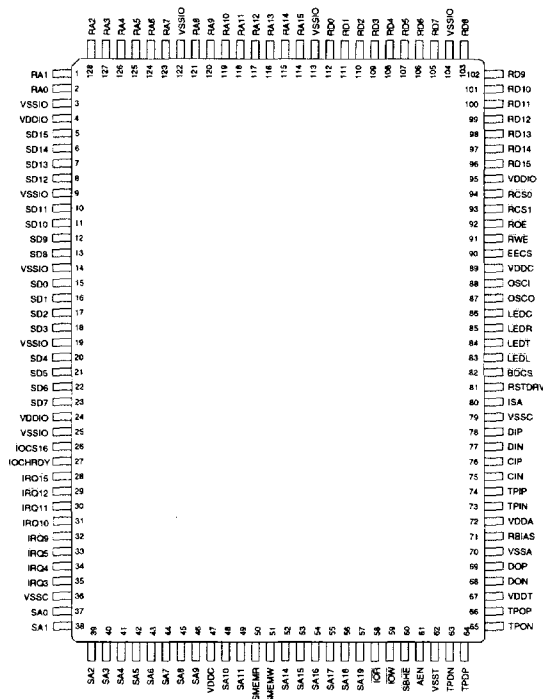
TSC 78Q8377A

10BaseT Ethernet Combo

for Plug and Play

PACKAGE PIN DESIGNATIONS

(Top View)



128-Lead QFP
ISA Bus Mode

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
TSC 78Q8377A 10BaseT Ethernet Control for Plug and Play 128-Lead QFP	TSC 78Q8377A	TSC 78Q8377A

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