Integrated Device Technology, Inc.

256K (32K x 8-BIT) CMOS STATIC RAM MODULE

IDT7M856S

FEATURES:

- High-density 256K (32K x 8-bit) CMOS static RAM module
- Equivalent to JEDEC standard for future monolithic 32K x 8 static RAMs
- High-speed — 40ns (max.) commercial; 55ns (max.) military
- Low-power consumption; typically less than 1W operating, less than 1mW in standby
- Utilizes IDT7198s—high-performance 64K static RAMs produced with advanced CEMOS™ technology
- CEMOS process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Assembled with IDT's high-reliability vapor phase solder reflow process
- Pin compatible with IDT7M864 (8K x 8 SRAM module)
- Offered in the JEDEC standard 28-pin, 600 mil wide ceramic sidebraze DIP
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Modules available with semiconductor components 100% screened to MIL-STD-883, Class B
- Finished modules tested at Room, Hot and Cold temperatures for all AC and DC parameters as per customer requirements

DESCRIPTION:

The IDT7M856 is a 256K (32,768 x 8-bit) high-speed static RAM constructed on a co-fired ceramic substrate using four IDT7198 (16,384 x 4) static RAMs in leadless chip carriers. Functional equivalence to proposed monolithic 256K static RAMs is achieved by utilization of an on-board decoder, used as an inverter, that interprets the higher order address A_{14} to select two of the four 16K x 4 RAMs. Extremely fast speeds can be achieved with this technique due to use of 64K static RAMs and the decoder fabricated in IDT's high-performance, high-reliability CEMOS technology.

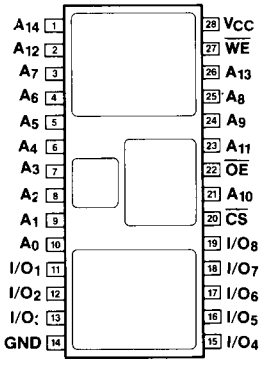
The IDT8M856 is available with maximum access times as fast as 40ns for commercial and 55ns for military temperature ranges, with maximum power consumption of only 2 watts. The circuit also offers a reduced power standby mode. When CS goes high, the circuit will automatically go to a standby mode with power consumption of only 1.1mW (max.). Substantially lower power levels can be achieved in a full standby mode (440mW max.).

The IDT8M856 is offered in a 28-pin, 600 mil center sidebraze DIP. This provides four times the density of the IDT7M864 (8K x 8 module) in the same socket with only minor pin assignment changes. In addition, the JEDEC standard for 256K monolithic pinouts has been adhered to, allowing for compatibility with future monolithics.

All inputs and outputs of the IDT7M856 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used requiring no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are 100% processed to the test methods of MIL-STD-883 Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

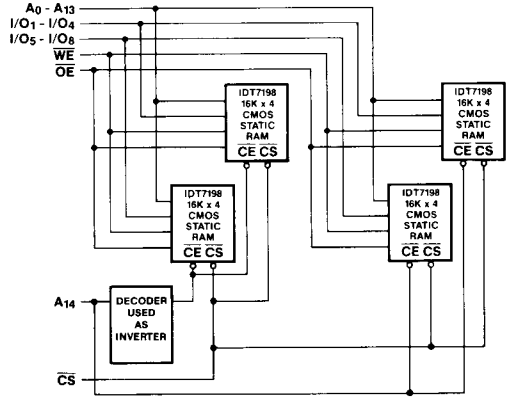


DIP
TOP VIEW

PIN NAMES

A_0 - A_{14}	ADDRESSES
I/O_1 - I/O_8	DATA INPUT/OUTPUT
$\overline{CS}$	CHIP SELECT
V_{CC}	POWER
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
GND	GROUND

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING(1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	4.0	4.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE:
1. V_{IL} min = -3.0V pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	15	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = 5.5V, $\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	15	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = 0	—	190	380	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, Output Open, V_{CC} = 5.5V, f = f Max.	—	190	380	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH} (TTL Level), V_{CC} = 5.5V, Output Open	—	90	200	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V (CMOS Level) V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	—	0.2	80(2)	mA
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = 4.5V I_{OL} = 8mA, V_{CC} = 4.5V	— —	— —	0.5 0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = 4.5V	2.4	—	—	V

NOTES:
1. V_{CC} = 5V, T_A = +25°C
2. I_{SB1} at commercial temperature = 60mA.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

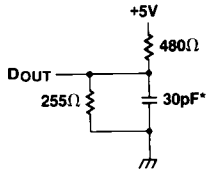

Figure 1. Output Load

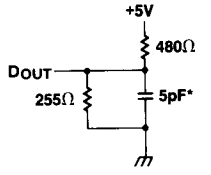

Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig

AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

SYMBOL	PARAMETER	IDT7M856S40 MIN.	IDT7M856S40 MAX.	IDT7M856S50 MIN.	IDT7M856S50 MAX.	IDT7M856S60 MIN.	IDT7M856S60 MAX.	IDT7M856S70 MIN.	IDT7M856S70 MAX.	IDT7M856S85 MIN.	IDT7M856S85 MAX.	UNITS
READ CYCLE												
t_{RC}	Read Cycle Time	40	—	50	—	60	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	40	—	50	—	60	—	70	—	85	ns
t_{ACS}	Chip Select Access Time	—	40	—	50	—	55	—	65	—	80	ns
t_{CLZ}	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	30	—	35	—	40	—	45	—	55	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}	Chip Select to Output in High Z	—	15	—	15	—	20	—	25	—	30	ns
t_{OHZ}	Output Disable to Output in High Z	—	15	—	15	—	20	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time	—	40	—	50	—	60	—	70	—	85	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	40	—	50	—	60	—	70	—	85	—	ns
t_{CW}	Chip Select to End of Write	35	—	45	—	50	—	60	—	75	—	ns
t_{AW}	Address Valid to End or Write	35	—	45	—	50	—	60	—	75	—	ns
t_{AS}	Address Setup Time	5	—	5	—	10	—	10	—	10	—	ns
t_{WP}	Write Pulse Width	30	—	35	—	40	—	45	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output High Z	—	20	—	20	—	25	—	30	—	40	ns
t_{DW}	Data to Write Time Overlap	20	—	20	—	25	—	30	—	40	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

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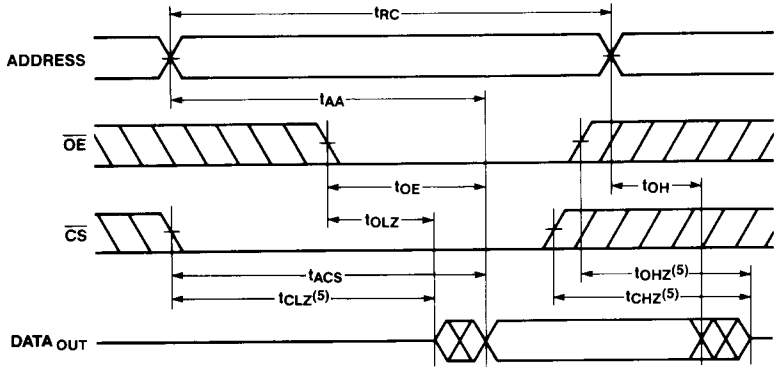
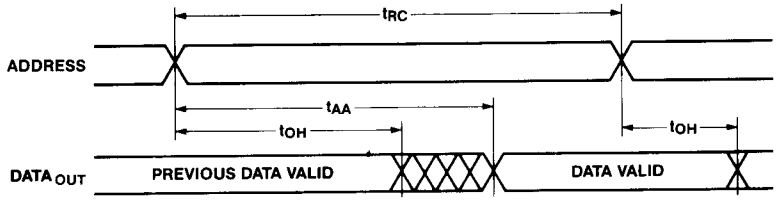
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT7M856S55 MIN.	IDT7M856S55 MAX.	IDT7M856S65 MIN.	IDT7M856S65 MAX.	IDT7M856S75 MIN.	IDT7M856S75 MAX.	IDT7M856S90 MIN.	IDT7M856S90 MAX.	IDT7M856S100 MIN.	IDT7M856S100 MAX.	UNITS
READ CYCLE												
t_{RC}	Read Cycle Time	55	—	65	—	75	—	90	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	65	—	75	—	90	—	100	ns
t_{ACS}	Chip Select Access Time	—	55	—	55	—	65	—	80	—	90	ns
t_{CLZ}	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	40	—	45	—	50	—	60	—	65	ns
t_{OLZ}	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ}	Chip Select to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OHZ}	Output Disable to Output in High Z	—	20	—	25	—	30	—	35	—	40	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU}	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect to Power Down Time	—	55	—	65	—	75	—	90	—	100	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	55	—	65	—	75	—	90	—	100	—	ns
t_{CW}	Chip Select to End of Write	50	—	55	—	65	—	75	—	85	—	ns
t_{AW}	Address Valid to End of Write	50	—	55	—	65	—	75	—	85	—	ns
t_{AS}	Address Setup Time	5	—	10	—	10	—	15	—	15	—	ns
t_{WP}	Write Pulse Width	40	—	45	—	45	—	50	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ}	Write Enable to Output High Z	—	25	—	30	—	40	—	50	—	50	ns
t_{DW}	Data to Write Time Overlap	25	—	30	—	35	—	45	—	45	—	ns
t_{DH}	Data Hold from Write Time	5	—	5	—	5	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

TIMING WAVEFORM OF READ CYCLE NO. 1(1)

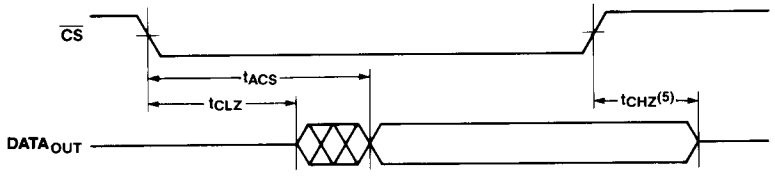


TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



SRD7198S/L-008

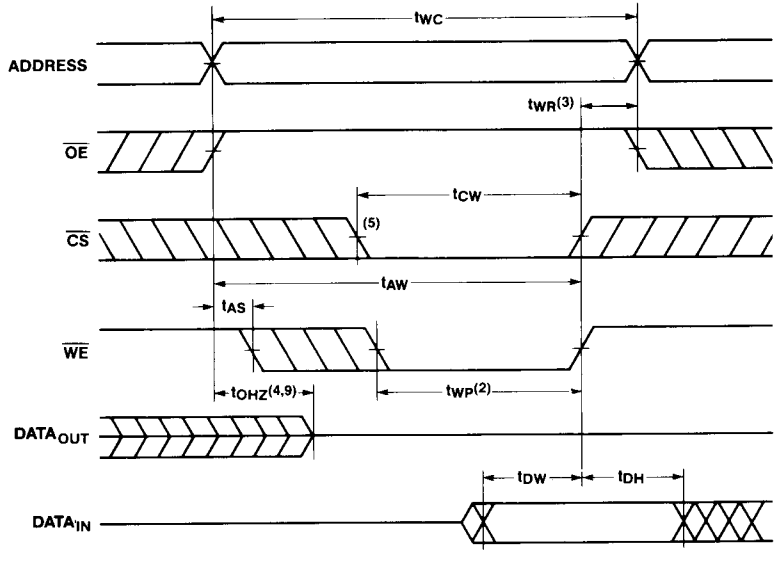
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



SRD7198S/L-009

NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)(1)



SRD7198S/L-010

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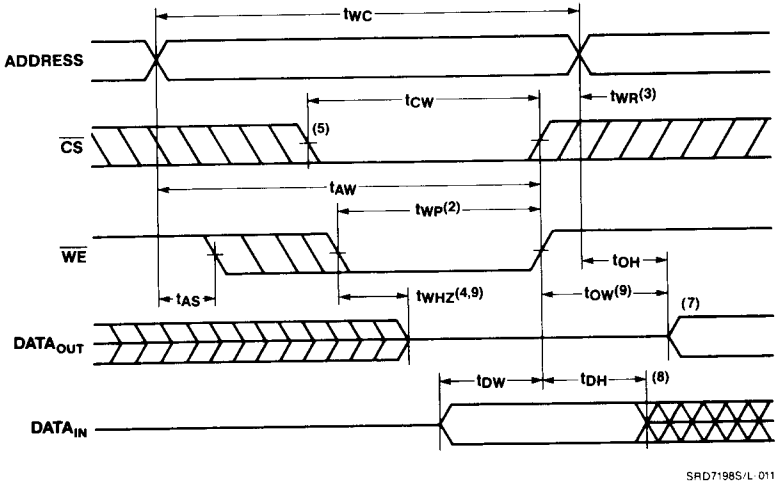
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1,6)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. DATA OUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TRUTH TABLE

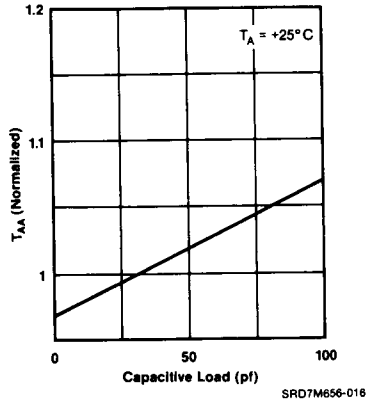
MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	High Z	Standby
Read	L	L	H	D_{OUT}	Active
Read	L	H	H	High Z	Active
Write	L	X	L	D_{IN}	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

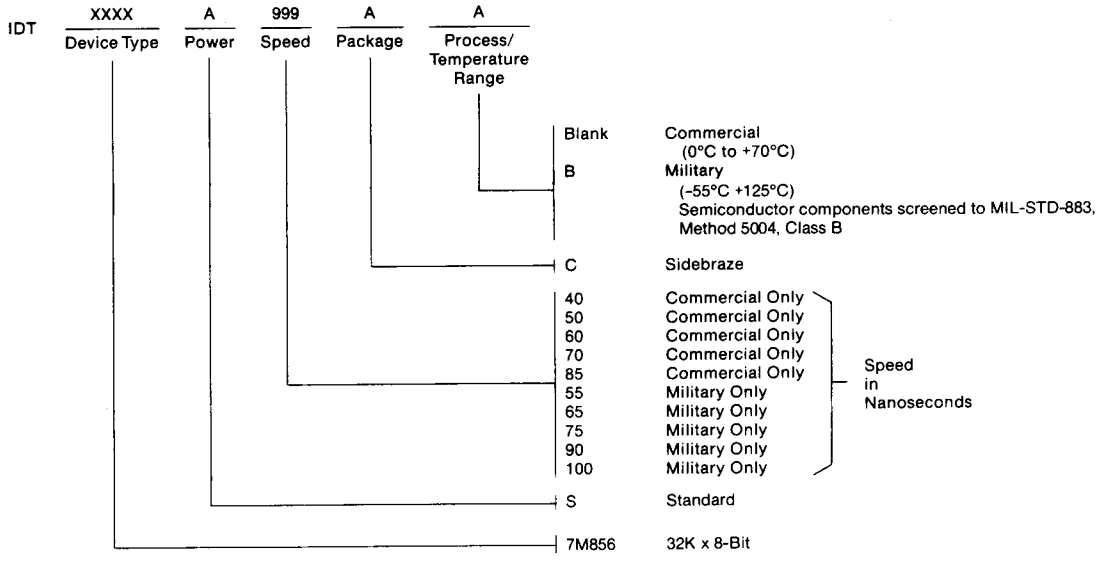
SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	26	pF

NOTE:
1. This parameter is sampled and not 100% tested.

Address Access Time vs. Capacitive Load



ORDERING INFORMATION



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