Raytheon Electronics
Semiconductor Division

TMC2360

Video Output Processor
VGA to NTSC/PAL

Features

- Single-package graphics to video conversion
- Multiple input formats
  - 640x480 50/60 Hz, 800x600 50 Hz
- Multiple output standards
  - NTSC, NTSC-EIA, PAL-B/G/H/I, PAL-M
- Composite and S-video output formats
- No external memory required
- Horizontal and vertical positioning inputs
- Configuration set by 11 switches
  - Microcontroller port optional
- Internal color bars
- 3-channel 8-bit input digitizer
- 3-channel 9-bit output D/A converters
- Accepts programming through H and V timing
  - VESA DPMS, filter modes, video standard
- Single +5V power supply

Applications

- VGA to video converter modules
- Computer video outputs
- Video games

Description

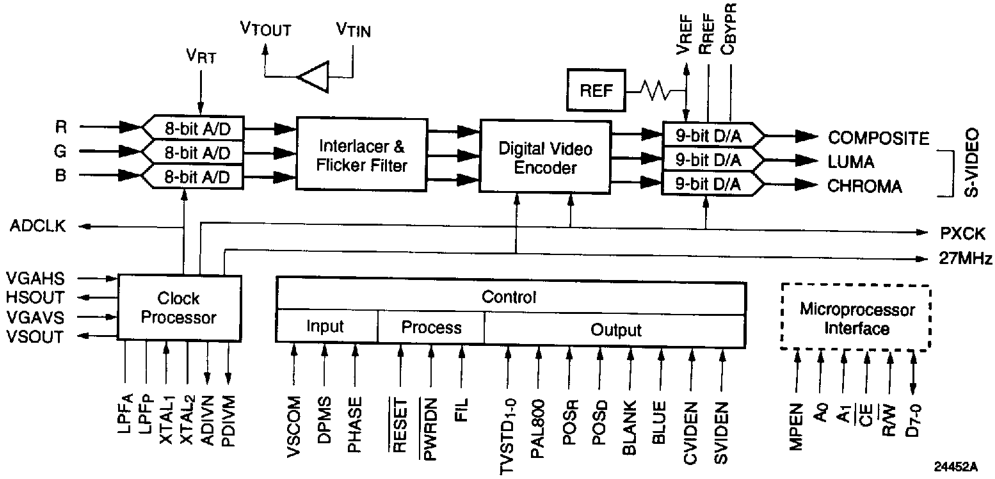
The TMC2360 converts RGB video and sync from a standard VGA source into broadcast-quality NTSC or PAL video. Composite and S-Video outputs are compliant with SMPTE-170M and CCIR-656 specifications. A fully-integrated 3-line adaptive flicker filter provides three selectable operating modes.

System implementation requires an absolute minimum of external components, with critical timing derived from a single 27 MHz crystal or an external clock reference.

All functions are directly controlled via package pins. Some functions, including video and filtering modes may be programmed through either a microcontroller port or VSYNC timing. VESA Display Power Management Signaling (DPMS) is supported.

Powered from a single +5V supply, the TMC2360 is available in an 80-lead Metric Quad Flat Pack (MQFP) and an 84-lead Plastic Leadless Chip Carrier (PLCC).

Block Diagram



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Rev. 0.9.1

Functional Description

The TMC2360 is a VGA to Video converter capable of producing broadcast-quality signals conforming to NTSC and PAL standards using a single low-cost application circuit. Included is all of the active circuitry required to generate a television signal with outstanding image quality in a stand-alone application.

Incoming VGA source signals must be 2X the frame and 2X the line rate of the outgoing TV standard within a ±2% tolerance. Supported VGA formats are 640x480 at 60 Hz for NTSC and PAL-M, and 640x640 and 800x640 at 50 Hz for PAL B/G/H/I.

The TMC2360 is ideal for portable converter applications, as well as integration into notebook and palmtop computers and video games.

Input Section

Analog VGA signals are digitized by three 8-bit A/D converters, operating at rates of up to 36 Ms/s. The signal range is 0 to 700 mV established by the reference voltage, VRT.

By connecting VTOUT to VIN, VRT may be supplied by an on-chip voltage follower with an input, VTIN, that may be varied from 0 to 2 volts to accommodate different input levels.

Clock Processor

Two phase-locked loops synthesize clocks from the VGA Horizontal Sync signal. One loop generates ADCLK, which is used internally as the A/D sample clock. A second PLL generates PXCK, which is used internally as the digital encoder clock.

Either internal or external phase-locked loops may be selected by programming pins A1 and A0. For internal loops, loop filters must be connected to LPFA and LPFP.

With external phase-locked loops, the internal divide by N and divide by M counters are still used. Only the phase detector, charge pump and VCO need be located in the external controller.

A stable timebase reference for subcarrier generation is derived from a 27 MHz crystal, or a TTL clock applied to pin XTAL1.

To synchronize the video encoder, vertical timing is derived from VGAVS, the VGA vertical sync signal. VGAHS and VGAVS signals of either polarity are accepted.

VESA Display Power Management Signaling functions may be enabled with the DPMS pin. Using the DPMS protocol, operational commands may be communicated to the TMC2360 via VGAHS and VGAVS signals. DPMS STAND-BY or DPMS SUSPEND modes set the processor to sleep and blanks the screen. DPMS OFF sets the processor, A/Ds and D/As to sleep with a blanked screen.

Vertical Sync Communications may be enabled with the VSCOM pin to detect the number of VGAHS pulses during the VGAVS period. With VSCOM, the Flicker Filter mode and the Video Standard may be selected by commands communicated via the VGA sync signals.

Flicker Filter

Flicker may be traded-off against vertical resolution with a three-line adaptive flicker filter. A single toggle pin (FIL) selects either High Filter, Medium Filter, or No Filter modes. A fourth mode, Color Bars, is useful for video setup and as a reference point for filter selection.

Video Encoder

Unless VSCOM is enabled, TVSTD1-0 pins select the TV standard to be either NTSC, PAL or PAL-M.

Relative to the bezel framed by horizontal and vertical sync, the image may be moved right/left, and down/up by pulsing the POSR and POSD pins. BLANK suppreses the image, setting the screen either black or blue according to the state of the BLUE pin.

NTSC (SMPTE 170M) and PAL (CCIR 624) video signals are produced by three 9-bit D/A converters that can drive the 37.5Ω load of a double-terminated 75Ω line. Digital 2X oversampling minimizes sinX/X distortion, facilitating use of low-cost output filters.

Composite and S-Video D/As are independently enabled via CVIDEN and SVIDEN pins to minimize power dissipation.

Control Processor

TMC2360 setup and control is derived from external switches and push buttons. Schmitt trigger inputs reject external noise. Unused controls may be preset by hardwiring inputs to ground or VCC.

Encoder Output Current

Output current is established by VREF and an external resistor connected between RREF and ground. An internal 1.235 volt reference is buffered from VREF by a resistor, so VREF may be overridden by an external voltage. Output current may be calibrated by resistor selection or setting a potentiometer attached to RREF.

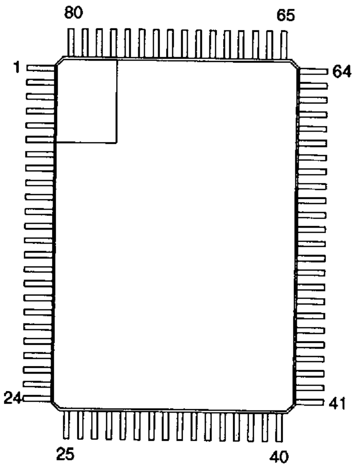
To minimize DAC noise, a bypass capacitor must be connected from CBYPR to an adjacent VDDA pin.

Microprocessor Port

Instead of utilizing control pin inputs, two operational modes, TV Standard and Flicker Filter, may be selected by writing to the VGA control register. Five registers may be read: address, VGA0, VGA1, Revision ID and Part ID.

Pin Assignments

80-Lead MQFP (KL) Package



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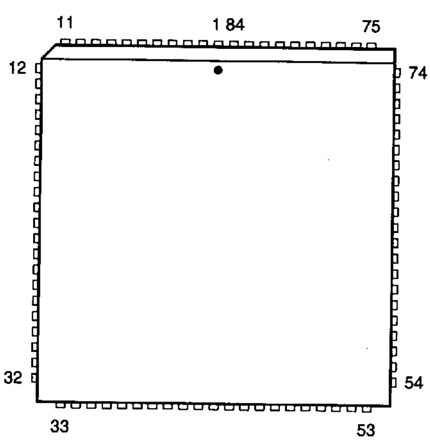
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	AGND	21	D_4	41	PAL800	61	DGND
2	COMPOSITE	22	D_3	42	FIL	62	V_{DD}
3	R_{REF}	23	D_2	43	DPMS	63	AGND
4	V_{REF}	24	D_1	44	VSCOM	64	LPF_A
5	DGND	25	D_0	45	VGAVS	65	V_{DDPLLA}
6	PHASE	26	VSOUT	46	VGAHS	66	AGND
7	V_{DD}	27	HSOUT	47	POS_R	67	LPF_P
8	DGND	28	DGND	48	POS_D	68	V_{DDPLLP}
9	V_{DD}	29	V_{DD}	49	AGND	69	$XTAL_2$
10	DGND	30	MPEN	50	B	70	$XTAL_1$
11	27MHZ	31	A_1	51	V_{DDA}	71	$\overline{RESET}$
12	PXCK	32	A_0	52	V_{DDA}	72	$\overline{PWRDN}$
13	ADCLK	33	$R/\overline{W}$	53	G	73	SVIDEN
14	V_{DD}	34	$\overline{CE}$	54	AGND	74	CVIDEN
15	DGND	35	V_{DD}	55	V_{RT}	75	V_{DDA}
16	ADIVN	36	DGND	56	V_{TOUT}	76	V_{DDA}
17	PDIVM	37	BLUE	57	V_{TIN}	77	C_{BYPR}
18	D_7	38	BLANK	58	AGND	78	CHROMA
19	D_6	39	$TVSTD_1$	59	R	79	AGND
20	D_5	40	$TVSTD_0$	60	V_{DDA}	80	LUMA

84-Lead PLCC (R0) Package



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Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	$\overline{PWRDN}$	22	ADCLK	43	A_0	64	G
2	SVIDEN	23	V_{DD}	44	$R/\overline{W}$	65	AGND
3	CVIDEN	24	DGND	45	$\overline{CE}$	66	V_{RT}
4	V_{DDA}	25	ADIVN	46	V_{DD}	67	V_{TOUT}
5	V_{DDA}	26	PDIVM	47	DGND	68	V_{TIN}
6	C_{BYPR}	27	D_7	48	BLUE	69	AGND
7	CHROMA	28	D_6	49	BLANK	70	R
8	AGND	29	D_5	50	$TVSTD_1$	71	V_{DDA}
9	LUMA	30	D_4	51	$TVSTD_0$	72	DGND
10	AGND	31	D_3	52	PAL800	73	V_{DD}
11	COMPOSITE	32	DNC	53	FIL	74	DNC
12	R_{REF}	33	DNC	54	DPMS	75	DNC
13	V_{REF}	34	D_2	55	VSCOM	76	AGND
14	DGND	35	D_1	56	VGAVS	77	LPF_A
15	PHASE	36	D_0	57	VGAHS	78	V_{DDPLLA}
16	V_{DD}	37	VSOUT	58	POS_R	79	AGND
17	DGND	38	HSOUT	59	POS_D	80	LPF_P
18	V_{DD}	39	DGND	60	AGND	81	V_{DDPLLP}
19	DGND	40	V_{DD}	61	B	82	$XTAL_2$
20	27MHZ	41	MPEN	62	V_{DDA}	83	$XTAL_1$
21	PXCK	42	A_1	63	V_{DDA}	84	$\overline{RESET}$

Pin Descriptions

Pin Name	Pin Number		Type/ Value	Pin Function Description
	MQFP	PLCC		
Clocks				
ADCLK	13	22	TTL	**A/D Converter Clock Output.** Generated by an internal phase-locked loop slaved to VGAHS.
ADIVN	16	25	TTL	**Internal ADCLK divided by N Output.** Enabled by A_0 and A_1 pins according to Table 1 or by VGA Control Register 1.
LPF_A	64	77	—	**A/D PLL Loop Filter Connection.** An external RC network is connected here.
PXCK	12	21	TTL	**Encoder Clock Output.** Generated by an internal phase-locked loop slaved to VGAHS.
PDIVM	17	26	TTL	**Internal PXCK divided by M Output.** Enabled by A_0 and A_1 pins according to Table 1 or by VGA Control Register 1.
LPF_P	67	80	—	**Encoder PLL Loop Filter Connection.** An external RC network is connected here.
$XTAL_{1-2}$	70,69	83, 82	—	**Subcarrier Reference Crystal/Clock.** Connection terminals for an external 27 MHz crystal. Alternatively, the $XTAL_1$ pin may be used as an input from an external oscillator or clock. Subcarrier frequency accuracy is based on this clock.
27MHZ	11	20	TTL	**Subcarrier Reference Clock Output.** Buffered TTL output from 27MHz crystal oscillator/reference clock.
VGAHS	46	57	$CMOS_S$	**VGA Horizontal Sync.** Incoming VGA sync may be of either polarity (active LOW or active HIGH). VGAHS frequency must be within 2% of the nominal specified value. The VGAHS pin has a light pull-up and a Schmitt trigger.
VGAVS	45	56	$CMOS_S$	**VGA Vertical Sync.** Incoming VGA sync may be of either polarity (active LOW or active HIGH. The VGAVS pin has a light pull-up and a Schmitt trigger.
HSOUT	27	38	TTL	**Buffered Horizontal Sync Output.** Follows VGAHS.
VSOUT	26	37	TTL	**Buffered Verical Sync Output.** Follows VGAVS.
Global Controls				
$TVSTD_{1-0}$	39, 40	50, 51	$CMOS_P$	**Video Output Standard Select.** Preprogrammed into the TMC2360 are timing, subcarrier frequency and phase parameters corresponding to worldwide NTSC and PAL standards. $TVSTD_{1-0}$ select one of four sets of parameters to set up the encoder. Frame rate of the graphics source must be twice the frame rate of the selected video standard.
PAL800	41	52	$CMOS_P$	**Resolution select for PAL.** Sets number of samples per VGA line.
DPMS	43	54	$CMOS_P$	**Display Power Management Signaling Enable.** When HIGH, the operational state of the TMC2360 is controlled by the pulse activity on VGAHS and VGAVS. When LOW, the state of the TMC2360 is controlled only by input pins.
FIL	42	53	$CMOS_S$	**Flicker Filter Mode Select.** The adaptive flicker reduction filter may be configured for HIGH filtering, MEDIUM filtering, or NO filtering by pulsing this input HIGH. FIL defaults to HIGH-filter mode upon power-up. If VSCOM is HIGH, the filter mode will be selected by the pulsewidth of VGAVS, and FIL will be ignored. The FIL input is a Schmitt trigger.

Preliminary Information

Pin Descriptions (continued)

Pin Name	Pin Number MQFP	PLCC	Type/ Value	Pin Function Description
VSCOM	44	55	CMOSP	**Vertical Sync Communications Enable.** When HIGH, vertical sync pulse width (VGAVS) will control the filter mode, and FIL will be ignored.
$\overline{PWRDN}$	72	1	CMOSP	**Power-Down Control.** When HIGH, the TMC2360 is fully operational and enabled. When LOW, the TMC2360 is configured for minimum power consumption. D/A converters and clocks are disabled. Previously established set-up conditions are retained and remain in effect when $\overline{PWRDN}$ goes HIGH.
$\overline{RESET}$	71	84	CMOSP	**Reset.** Initializes internal registers.
PHASE	6	15	CMOSP	**Sampling Phase Control.** Shifts the A/D sampling phase by 180°.
Encoder Controls				
CVIDEN	74	3	CMOSP	**Composite Video D/A Power Enable.** When HIGH, the COMPOSITE D/A converter is enabled. When LOW it is disabled to save power.
SVIDEN	73	2	CMOSP	**S-Video D/A Power Enable.** When HIGH, the CHROMA and LUMA D/A converters are enabled. When LOW, they are disabled to save power.
BLANK	38	49	CMOSP	**Blank Screen Generator.** When HIGH, the color selected by BLUE is displayed on the screen. When LOW, incoming video from the internal FIFO is encoded.
BLUE	37	48	CMOSP	**Blank Screen Color Selector.** When HIGH, the screen will be blanked to blue when BLANK is HIGH. When LOW, the screen will be blanked to black when BLANK is HIGH.
POSR, D	47, 48	58, 59	CMOSS	**TV Image Position Controls.** Position controls shift the VGA image horizontally or vertically, revealing portions that are found near the edges or in the overscan areas. Default power-up position is the midpoint of the adjustment range. POSD,R inputs are Schmitt triggers.
A/D Converter Interface				
R, G, B	59, 53, 50	70, 64, 61	700 mV	**Analog RGB inputs.** Analog red, blue and green inputs to the A/D converters from incoming VGA signals. Nominal voltage range is 0.0 to +700 mV.
VTIN	57	68	750 mV	**A/D Converter Reference Buffered Input.** Buffer is a voltage follower that may be connected to VRT.
VTOUT	56	67	750 mV	**A/D Converter Reference Buffered Output.** May be connected to V_{RT} to suppliy current to A/D converter reference resistors. In power down mode, VTOUT drops to zero.
VRT	55	66	750 mV	**A/D Converter Reference Input, Unbuffered.** Supplies current to A/D converter reference resistors. May be driven from VTOUT. Voltage range is 0.5 to 2.0 volts.

PERSONAL COMPUTERS

Pin Descriptions (continued)

Pin Name	Pin Number		Type/ Value	Pin Function Description
	MQFP	PLCC		
Video Outputs				
COMPOSITE	2	11	1 V p-p	**NTSC/PAL Video Output, Composite Video.** NTSC/PAL baseband composite output can drive 1 Volt p-p video into a 37.5 Ohm load. Contains sync, subcarrier and active video information to drive monitors, projectors, VCRs, and other video devices.
LUMA	80	9	1 V p-p	**Luminance-only Video.** This analog monochrome video output can drive 1 Volt p-p video into a 37.5 Ohm load. Contains all sync and active video information necessary to drive black-and-white video devices.
CHROMA	78	7	1 V p-p	**Chrominance-only Video.** This analog output can drive a 37.5 Ohm load. CHROMA signal, when combined with LUMA comprises an S-Video signal suitable for driving monitors, projectors, VCRs, and other S-Video devices.
Voltage Reference				
V_{REF}	4	13	+1.23 V	**Voltage Reference Input/Output.** Output of an internal 1.23 Volt band-gap voltage reference. If unconnected, except for a 0.1F capacitor to ground for noise decoupling, the internal reference will be used for the three D/A converters. An externally generated voltage reference of +1.2 Volts applied to the V_{REF} pin will override the internal voltage reference and become the new reference for the D/A converters.
C_{BYPR}	77	6	0.1 µF	**Reference Bypass Capacitor.** An external 0.1F capacitor should be connected between C_{BYPR} and V_{DDA} to reduce noise on the internal reference circuitry.
R_{REF}	3	12	392Ω	**Current-setting Resistor.** A 392Ω resistor connected between the R_{REF} terminal and ground establishes the reference current for the three internal D/A converters. Resistor value determines the full-scale output current (and therefore the peak video level) of the D/A converters.
Microprocessor Interface				
MPEN	30	41	TTL	**Microprocessor port enable.** With MPEN = LOW, the port is disabled and control is via individual pins. With MPEN = HIGH, selected functions may be accessesd through the microprocessor port.
A_0	32	43	TTL	**External PXCK Phase-locked Loop Select/Address Bit.** Dual function pin. If MPEN = HIGH, A_0 is the microprocessor port address bit A0. If MPEN = LOW, A_0 configures the PXCK PLL inputs and outputs.
A_1	31	42	TTL	**External ADCLK Phase-locked Loop Select.** If MPEN = LOW, A1 configures the ADCLK PLL inputs and outputs.
$R/\overline{W}$	33	44	TTL	**Read/Write.** Read/Write selects the direction of the 8-bit data bus.
$\overline{CE}$	34	45	TTL	**Chip Enable.** When $\overline{CE}$ = H, D_{7-0} are high impedance. When $\overline{CE}$ = H, $R/\overline{W}$ sets D_{7-0} to either the read or write state.

Preliminary Information

Pin Descriptions (continued)

Pin Name	Pin Number		Type/ Value	Pin Function Description
	MQFP	PLCC		
D7-0	18, 19, 20, 21, 22, 23, 24, 25	27, 28, 29, 30, 31, 34, 35, 36	TTL	**Data bits.** Data bus is high impedance unless $\overline{CE}$ = L and R/$\overline{W}$ = H.
Power and Ground				
VDD	7, 9, 14, 29, 35, 62,	16, 18, 23, 40, 46, 73	+5.0 V	**Digital Power Supply.** Supplies +5V power to internal digital circuits.
VDDA	51, 52, 60, 75, 76	4, 5, 62, 63, 71	+5.0 V	**Analog Power Supply.** Supplies +5V power to internal analog circuits. VDD and VDDA must originate from the same source.
VDDPLLA	65	78	+5.0 V	**A/D Phase Locked Loop +5V Power.** VDDPLLA and VDD must originate from the same source.
VDDPLLP	68	81	+5.0 V	**Encoder Phase Locked Loop +5V Power.** VDDPLLP and VDD must originate from the same source.
DGND	5, 8, 10, 15 28, 36, 61	14, 17,19, 24, 39, 47, 72	0.0 V	**Digital Ground.** Ground point for internal digital circuits.
AGND	1, 49, 54, 58, 63, 66, 79	8, 10, 60, 65, 69, 76, 79	0.0 V	**Analog Ground.** Ground point for internal analog circuits. DGND and AGND should be connected to the same ground plane.
DNC	—	32, 33, 74, 75		Do Not Connect.

Notes:
CMOSP = CMOS with light pull-up
CMOSS = CMOS with Schmitt Trigger

PERSONAL COMPUTERS

Clocks

There are three internal clocks, ADCLK, PXCK, and 27MHz. ADCLK is the clock for the A/D converters with sampling on the edge selected by PHASE. PXCK is the encoder clock for sequencing data to the D/A converters at a 2X rate. 27MHz is the reference clock from which the chroma subcarrier data is synthesized.

ADCLK and PXCK clocks may be derived from internal or external phase-locked loops. Only an external controller containing the phase detector, charge pump, and VCO is needed for each loop. An internal divider programmed with the correct counts is included within the TMC2360.

Control of the internal/external PLL modes is either via the A0 and A1 pins (see Table 1) or through the VGA1 Control register, which can be programmed via the microprocessor port.

With control via A0 and A1 pins, outputs, PDIVM and ADIVN are high impedance unless either PLL is programmed to be external. A0 and A1 also control the direction of the ADCLK and PXCK clock pins. Each clock (ADCLK and PXCK) is an output in the internal mode and an output in the external mode.

Table 1. Internal/External Phase-locked loop selection (MPEN = L)

A1	A0	PLLA	PLLP	ADIVN	PDIVM	ADCLK	PXCK
0	0	Internal	Internal	High-Z	High-Z	Output	Output
0	1	Internal	External	1/N	1/M	Output	Input
1	0	External	Internal	1/N	1/M	Input	Output
1	1	External	External	1/N	1/M	Input	Input

Preliminary Information

A/D Clock (ADCLK)

ADCLK is the buffered analog-to-digital converter clock output which is derived from incoming VGA horizontal sync (VGAHS) by a phase-lock loop (PLL). Either an internal PLL or an external PLL controller may be selected by programming pin A1.

A/D Clock frequency is set by the PLL divide-by-N counter where N is the number of A/D samples between the horizontal sync pulses in each VGA line.

Pre-programmed values selected by the $TVSTD_{1-0}$ and PAL800 control inputs set N and the clock frequency as shown in Table 2.

Table 2. VGA A/D Clock

Television Standard	$TVSTD_{1-0}$	PAL800	ADCLK Freq. (MHz)	N
NTSC	0x	0	25.175	800
PAL640	10	0	25.250	808
PAL800	10	1	36.000	1152
PALM	11	0	25.175	800

For an internal loop, the recommended loop filter to be connected to the LPF_A pin is shown in Figure 1.

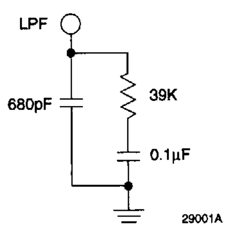

Figure 1. PLL Low Pass Filter

Pixel Clock (PXCK)

PXCK is the buffered video encoder clock output which is derived from the incoming VGA HSYNC signal by a second phase-lock loop. Either an internal PLL or an external PLL controller may be selected by programming pin A_0.

With the internal loop selected, Figure 1 shows the recommended loop filter, which should be connected to LPF_P.

Clock frequency is set by the PLL divide-by-M counter. M is the number of encoder samples between horizontal sync pulses. Because of 2X oversampling, the pixel rate is twice the TV square pixel rate. Table 3 shows the video output clock rates and M values.

Table 3. NTSC and PAL Pixel Clocks

Television Standard	Line Rate (kHz)	Pixel Rate (MHz)	M
NTSC	15.734	24.540	780
PAL	15.625	29.500	944
PALM	15.750	24.570	780

Reference Clock

Accuracy of the PAL/NTSC subcarrier depends on the 27 MHz reference signal applied to the $XTAL_1$. This signal may be derived from a clock connected directly to the $XTAL_1$ pin or a crystal and capacitors connected across $XTAL_{1-2}$ as shown in Figure 2.

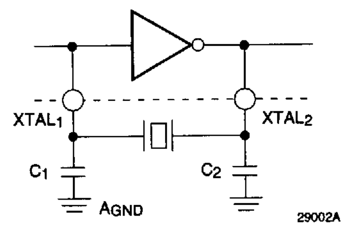

Figure 2. Crystal Oscillator Circuit

Capacitors C_1 and C_2, must be adjusted to trim the frequency within 20 ppm. C_1 and C_2 have the same value, with series capacitance equal to the load recommended for the crystal.

Typical crystal parameters are 50 ppm accuracy with a 20 pF load and ±80 ppm pullability.

Digitizing

A/D Reference

An on-chip voltage follower is included to supply current to the ADC reference V_{RT} from V_{TOUT}. A stable voltage source greater than the input peak amplitude should be connected to V_{TIN}.

Input Signal Conditioning

ADC performance can be optimized by driving the RGB video inputs with either a 75 ohm or a low impedance source.

Input Format Selection

One of four input VGA formats can be accepted by setting the $TVSTD_{1-0}$ and PAL800 inputs as shown in Table 4. Each VGA input option corresponds to a VGA active video area, frame rate and line rate with a corresponding TV output format.

Table 4. VGA Input Formats

$TVSTD_{1-0}$	PAL800	H x V Input Pixels	Frame Rate (Hz)	Line Rate (kHz)
0x	0	640 x 480	59.94	31.469
10	0	640 x 480	50	31.250
10	1	800 x 600	50	31.250
11	0	640 x 480	60	31.469

Sampling Phase Control

Conversion can be optimized by using the PHASE control to set the sampling points of the A/D clock to lie between the VGA pixel transitions. Figure 3 shows optimum sampling of VGA pixels on the rising edge of the ADCLK signal.

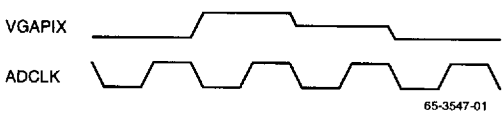

Figure 3. Sampling of VGA Pixels

PHASE selects the conversion edge of the ADCLK. If PHASE = LOW, the rising edge is selected. If PHASE = HIGH, the falling edge is selected.

Processing

Flicker Filter

Annoying artifacts can be eliminated by selecting one of three filter modes, which trade-off vertical resolution against flicker. Without the filter, one contrasting VGA line may be encoded into one field of the TV video, which will flicker at 30 Hz with NTSC and 25 Hz with PAL.

As shown in Table 5, if VSCOM = LOW, pulsing the FIL pin indexes the TMC2360 through a loop of three filter modes and a color bar pattern.

Table 5. FIL Filter Mode Select Sequence

FIL	Filter Mode
↓ ↑	HIGH (default)
↓	MEDIUM
↓	No filter
└─┘	Color bars

Video Encoder

D/A Reference

Peak D/A converter current for the video outputs is set by a resistor connected to R_{REF}. For 1 volt video, with a 37.5 ohm load, the correct value of R_{REF} is 392 ohm. To trim the video output level, R_{REF} can be replaced with a potentiometer. (See the Applications Circuit, Figure 12).

Television Standard Selection

NTSC and PAL standards are preprogrammed into the TMC2360 to preset horizontal and vertical timing, subcarrier frequency, and chrominance phase. Frame rate of the VGA source must match the field rate of the selected video standard.

Depending upon the status of the Vertical Sync Communications (VSCOM) pin, the video output format may be selected by either the $TVSTD_{1-0}$ pins or by VSCOM codes.

Table 6 shows how the $TVSTD_{1-0}$ pins select the TV output format with VSCOM = LOW.

Table 6. TVSTD Control When Under Manual Control (VSCOM = 0)

$TVSTD_{1-0}$	Television Standard	Video Field Rate
00	NTSC	59.94 Hz
01	NTSC-EIA	59.94 Hz
10	PAL/B, G, I	50 Hz
11	PAL/M	60 Hz

If VCSOM = HIGH, Vertical Sync Communications are enabled. VSCOM is described under the Vertical Sync Command section below.

Image Positioning

POS_D and POS_R position controls change encoder timing relative to incoming PC video, shifting the viewed image either horizontally or vertically to reveal portions of the image located near the edges or in the overscan areas. At power-up, the default position is the midpoint of the adjustment range.

Each POS_D HIGH pulse moves the TV window down eight lines. At the lowest position (-64 lines) the direction reverses and the pulses move the image up in 8-line increments to the highest position (+64 lines). At this point the direction again reverses and the next sixteen pulses move the image down to the lowest position.

Each POS_R HIGH pulse moves the TV window eight pixels to the right. At the maximum right position (+64 pixels) the direction reverses and the next sixteen pulses move the window left to the maximum left position (-64 pixels). Direction again reverses and the next sixteen pulse move the image right.

Without a RESET, $POS_{D,R}$ controls will loop, causing the window to move down/up, right/left.

Preliminary Information

Blank and Blue

TV video can set to active (converted VGA source), blank or blue by the BLANK and BLUE inputs.

Table 7. Video Output for BLANK and BLUE inputs

BLANK	BLUE	Video
L	X	Video
H	L	Black
H	H	Blue

Power Management

D/A Power Control

Table 8 shows how the Composite and S-video ouputs are enabled by the CVIDEN and SVIDEN controls. If DPMS = LOW, the display will be blue if either or both VGAHS or VGAVS are inactive.

Table 8. Video Output Control

CVIDEN	SVIDEN	VGAHS & VGAVS	Composite Video	S-Video
H	X	YES	Active	X
X	H	YES	X	Active
L	L	X	Blank	Blank
H	H	NO	Blue	Blue

Powerdown Mode

$\overline{\text{PWRDN}}$ eliminates current drain by the D/A converter, VTOUT voltage follower and clock outputs. With $\overline{\text{PWRDN}}$ = HIGH, all outputs are enabled. If $\overline{\text{PWRDN}}$ = LOW, all outputs are disabled including the ADCLK, PXCK, VTOUT and the D/A converters.

Software Control

Display Power Management Signaling (DPMS)

Display Power Management is compliant with VESA DPMS Proposal 1.0. With DPMS = HIGH, the operational state of the TMC2360 is controlled by the pulse activity on VGAHS and VGAVS.

Table 9 shows how the TMC2360 responds. "No Pulses" on VSYNC or HSYNC is declared on the second missing VSYNC or HSYNC pulse. Following an OFF state, detection of VGAHS and/or VGAVS restores either the Suspend, Standby, or On state.

Regardless of the state of DPMS, absence of VGAHS and/or VGAVS pulses will cause the TMC2360 processor to sleep. However, with DPMS = HIGH, in the Off state. the A/Ds, D/As, and clocks are also set to sleep.

Vertical Sync Communications (VSCOM)

VSCOM is a unique feature incorporated into the TMC2360. With VSCOM = HIGH, the TMC2360 interprets commands that are encoded within the VGA vertical sync period. TV Standard and Flicker Filter may be selected by commands from the PC sourcing the VGA signal.

During the vertical sync period, the number of horizontal sync pulses is counted. Table 10 shows how the selected Television Standard changes with the code set into the $TVSTD_{1-0}$ inputs and the number of horizontal syncs per vertical sync interval.

Table 11 shows how the Filter Mode is selected with VSCOM. Notice that if one standard, such as PAL800 is selected, then counts of 10, 11 and 12 enable selection of three filter modes.

Table 9. Display Power Management Signaling (DPMS) States

State	VGAHS	VGAVS	TMC2360 State
On	Pulses	Pulses	On, video active
Stand-by	No Pulses	Pulses	Stand-by, screen blanked (color set by BLUE)
Suspend	Pulses	No Pulses	Stand-by, screen blanked (color set by BLUE)
Off	No Pulses	No Pulses	Off, screen black (equivalent to $\overline{\text{PWRDN}}$, except A/D Clock and 27MHZ oscillator are active.)

Table 10. TVSTD Control When Under Software Control (VSCOM = 1)

$TVSTD_{1-0}$	Hsyncs per Vsync Interval	Television Standard	VGA Frame Rate
XX	10,11,12	PAL 800 (B, G, I)	50 Hz
X0	6,7,9	PAL 640 (B, G, I)	50 Hz
01	6,7,9	PAL-M	60 Hz
11	6,7,9	(reserved)	
0X	1-5,8,14,15	NTSC	60 Hz
10	1-5,8,14,15	NTSC-EIAJ	60 Hz
11	1-5,8,14,15	(reserved)	
XX	0,13	Blank (with prior standard)	50/60 Hz

Table 11. VSCOM Filter Command Interpretation (VSCOM=1)

HSYNCs per VSYNC Interval	Filter Mode
5, 9, 12	No Filter
4, 7, 11	2-line filter
1, 2, 3, 6, 8, 10, 14, 15	3-line filter
0, 13	Blank (with prior mode)

Microprocessor Interface

Table 12 shows the five registers that may be read after the Address Register has been loaded. Only the two VGA registers and the Address Register may be written. For microprocessor control, 40h must be written into VGA register 1. To disable control through VGA Register 0, 00h must be written into register 1. Bit assignments of VGA register 0 are listed in Table 13. Bit assignments of VGA register 1 are listed in Table 14.

For communications through the microprocessor port, set MPEN = HIGH. Read and write timing is shown in Figure 4 and Figure 5. To access a VGA register, write the address of the selected register into the lower four bits of the eight bit Address Register with A_0 = LOW. Then with A_0 = HIGH, read or write to the selected register.

Table 12. Microprocessor Addressable Registers

A1	A0	Address Register Value	Register
0	0	x	Address Register
0	1	x0	VGA Register 0
0	1	x1	VGA Register 1
0	1	x6	Revision ID (xxh)
0	1	x7	Part ID (0Fh)

Table 13. VGA Control Register 0 Bit Map

Bit #	Name	Function
7	—	0 (reserved)
6-5	FIL	0 0 No Filter
		0 1 2-line Filter
		1 x 3-line Filter
4-2	TVSTD	0 0 0 NTSC
		0 0 1 NTSC-EIA
		0 1 0 PALM
		0 1 1 PAL640
		1 x x PAL800
1-0	VIDEO	0 0 Black
		0 1 Ramp
		1 0 Color Bars
		1 1 Normal

Table 14. VGA Control Register 1 Bit Map

Bit #	Name	Function
7	—	0 (reserved)
6	MODE	0 Normal
		1 Bypass FIL and TVSTD Pins
5-3	—	0 (reserved)
2	DIVMN	0 (reserved)
		1 Enable ADIVN and PVIDM
1	EXTPLL	0 Disable external PXCK PLL
		1 Enable external PXCK PLL
0	EXTPLLA	0 Disable external ACLK PLL
		1 Enable external ACLK PLL

PERSONAL COMPUTERS

Video Formats

Incoming VGA Formats

Table 15 and Table 16 show expected VGA Video input formats.

Outgoing TV Formats

Table 17 shows the four different TV formats that may be selected as outputs by the $TVSTD_{1-0}$ inputs.

Table 18 and Table 19 show the Horizontal and Vertical Timing for the NTSC and PAL formats.

Table 15. VGA Horizontal Timing Parameters

Television Standard	$TVSTD_{1-0}$	PAL800	Line Rate (kHz)	Front Porch (pixels)	Horiz Sync (pixels)	Back Porch (pixels)	Active Video (pixels)
NTSC(-EIA)	0x	0	31.469	18	96	46	640
PAL/B, G, I	10	0	31.250	18	96	54	640
PAL/B, G, I	10	1	31.250	98	96	158	800
PAL/M	11	0	31.500	18	96	46	640

Table 16. VGA Vertical Timing Parameters

Television Standard	$TVSTD_{1-0}$	PAL800	Frame Rate (Hz)	Line Rate (kHz)	Full Frame (lines)	Front Porch (lines)	Vert. Sync (lines)	Vsync + Back Porch (lines)	Active Video (lines)
NTSC(-EIA)	0x	x	59.94	31.469	525	13	2-16	32	480
PAL/B, G, I	10	0	50	31.250	625	61	2-16	84	480
PAL/B, G, I	10	1	50	31.250	625	1	2-16	24	600
PAL/M	11	x	60	31.469	525	13	2-16	32	480

Table 17. TVSTD Control When Under Manual Control (VSCOM = 0)

$TVSTD_{1-0}$	Television Standard	Field Rate
00	NTSC	60 Hz
01	NTSC-EIA	60 Hz
10	PAL/B, G, I	50 Hz
11	PAL/M	60 Hz

Table 18. NTSC and PAL Horizontal Timing

Television Standard	Field Rate (Hz)	Lines per frame	Line Rate (kHz)	2x pix Rate (MHz)	fsc Freq. (MHz)	Front Porch pixels	Horiz Sync pixels	Back Porch pixels	Active Video pixels	Line H pixels
NTSC	59.94	525	15.734	24.546	3.579	18	58	58	646	780
PAL	50.00	625	15.625	29.500	4.433	18	70	82	774	944
PALM	60	525	15.734	25.570	3.576	18	58	58	646	780

Table 19. NTSC and PAL Vertical Timing

TV Std	Field Rate (Hz)	Lines per frame	Line Rate (kHz)	Front Porch (lines)	Vertical Sync (lines)	Back Porch (lines)	Active Video (lines)
NTSC	59.94	525	15.734	3-3.5	3	14-14.5	242.5
PAL	50.00	625	15.625	2.5	2.5	21	286.5
PALM	60.00	525	15.750	3	3	14	242.5

Timing Diagrams

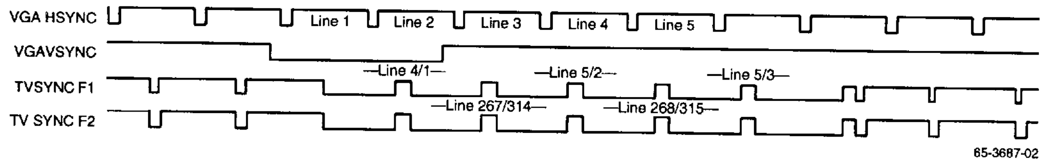

Figure 4. Nominal VGA-NTSC/PAL Vertical Sync Timing

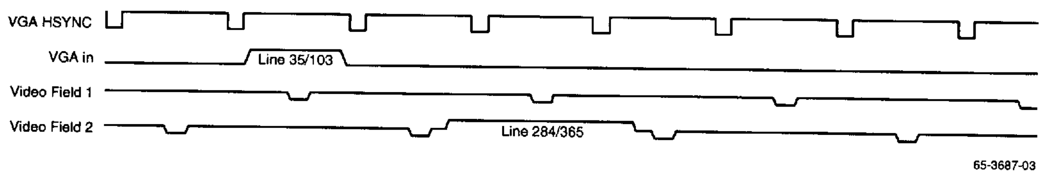

Figure 5. Nominal VGA640-NTSC/PAL, No Filter Timing

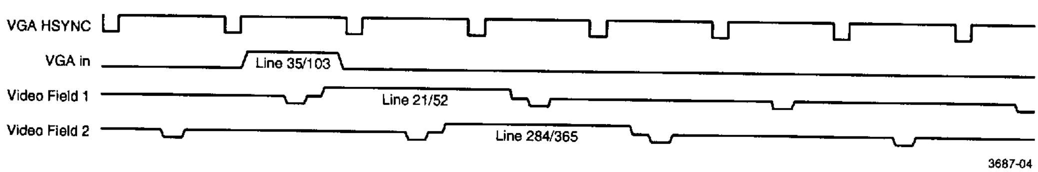

Figure 6. Nominal VGA-NTSC/PAL, Medium Filter Timing

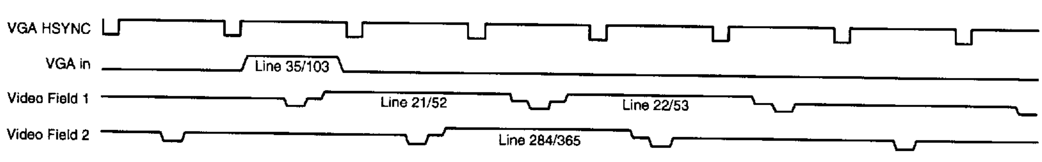

Figure 7. Nominal VGA-NTSC/PAL, High Filter Timing

Timing Diagrams (continued)

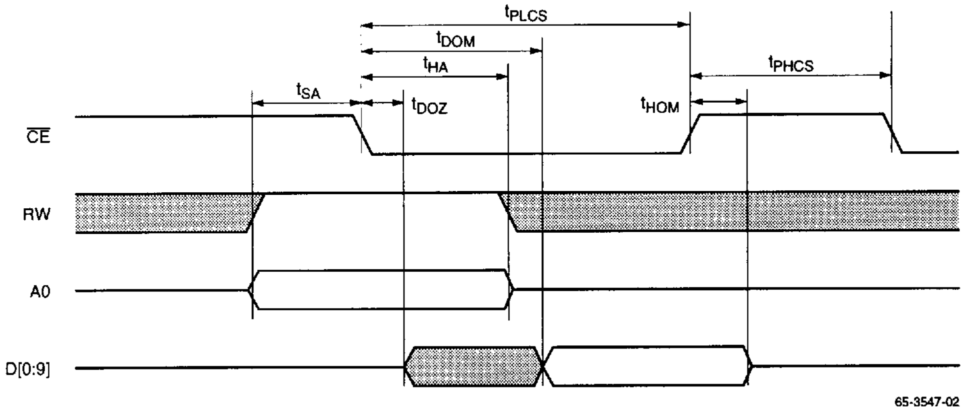

Figure 8. Microprocessor Read Timing

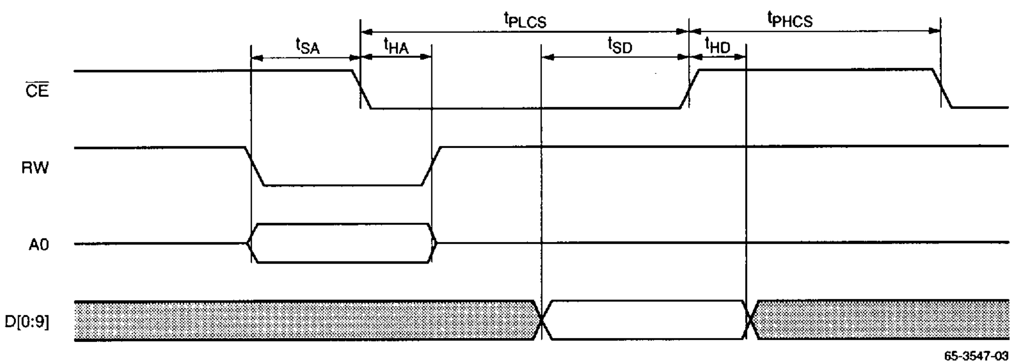

Figure 9. Microprocessor Write Timing

Preliminary Information

Equivalent Circuits

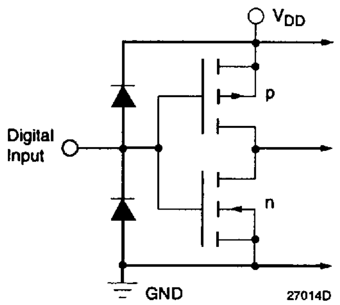

Figure 10. Equivalent Digital Input Circuit

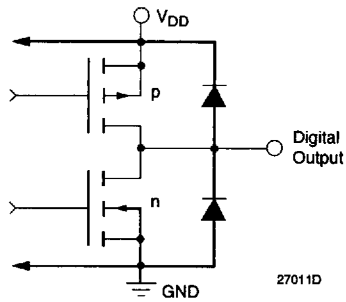

Figure 11. Equivalent Digital Output Circuit

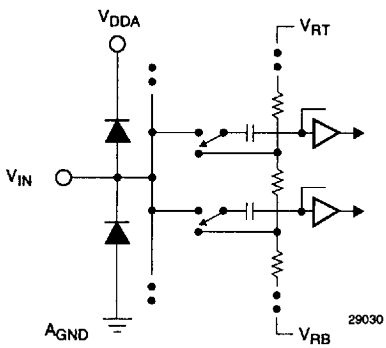

Figure 12. Equivalent A/D Input Circuit

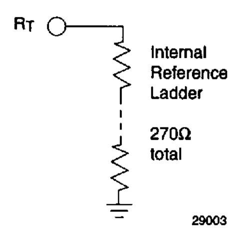

Figure 13. Equivalent A/D Reference Input Circuit

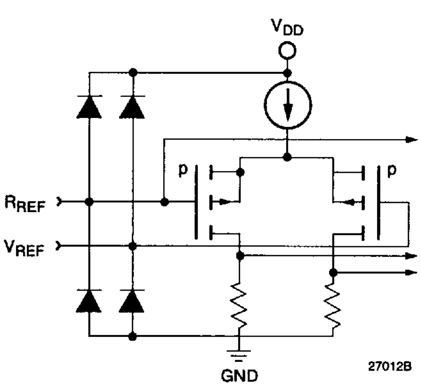

Figure 14. Equivalent D/A Reference Input Circuit

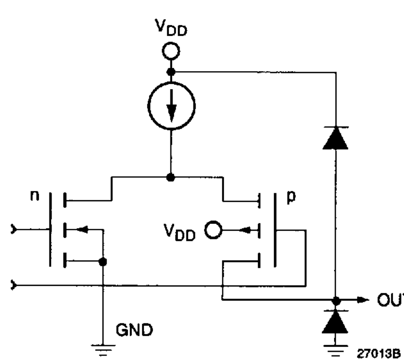

Figure 15. Equivalent D/A Output Circuit

Preliminary Information

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Typ	Max	Unit
Power Supply Voltages				
V_{DDA} (Measured to AGND)	-0.5		7.0	V
V_{DD} (Measured to DGND)	-0.5		7.0	V
V_{DDA} (Measured to VDD)	-0.5		0.5	V
A_{GND} (Measured to DGND)	-0.5		0.5	V
Digital Inputs				
Applied Voltage (Measured to DGND)[2]	-0.5		V_{DD} + 0.5	V
Forced current [3, 4]	-10.0		10.0	mA
Analog Inputs				
Applied Voltage (Measured to AGND)[2]	-0.5		V_{DDA} + 0.5	V
Forced current [3, 4]	-10.0		10.0	mA
Digital Outputs				
Applied Voltage (Measured to DGND)[2]	-0.5		V_{DD} + 0.5	V
Forced current [3, 4]	-6.0		6.0	mA
Short circuit duration (single output in HIGH state to ground)			1	second
Temperature				
Operating, Ambient	-20		110	°C
Junction			150	°C
Lead Soldering (10 seconds)			300	°C
Vapor Phase soldering (1 minute)			220	°C
Storage	-65		150	°C
Electrostatic Discharge[5]			±150	V

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.
5. EIAJ test method.

Operating Conditions

Parameter		Min	Nom	Max	Units
V_{DD}	Digital Power Supply Voltage	4.75	5.0	5.25	V
V_{DDA}	Analog Power Supply Voltage	4.75	5.0	5.25	V
A_{GND}	Analog Ground (Measured to D_{GND})	-0.1	0	0.1	V
V_{RT}	Reference Voltage, Top	0.5	0.75	2.0	V
V_{IN}	Analog Input Range	0		V_{RT}	V
V_{REF}	External Reference Voltage		1.235		V
I_{REF}	D/A Converter Reference Current ($I_{REF} = V_{REF}/R_{REF}$, flowing out of the R_{REF} pin)		3.15		mA
R_{REF}	Reference Resistor, V_{REF} = Nom		392		Ω
R_{OUT}	DAC Total Output Load Resistance		37.5		Ω

Operating Conditions (continued)

Parameter		Min	Nom	Max	Units
V_{IH}	Input Voltage, Logic HIGH	2.0			V
V_{IL}	Input Voltage, Logic LOW			0.8	V
I_{OH}	Output Current, Logic HIGH			-2.0	mA
I_{OL}	Output Current, Logic LOW			4.0	mA
T_A	Ambient Temperature, Still Air	0		70	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
Power Supply Currents						
I_{DD}	Operating	CVIDEN = L, SVIDEN = H		250		mA
I_{DDS}	Standby	CVIDEN = L, SVIDEN = H		220		mA
I_{DDQ}	Power-Down	$\overline{PWRDN}$ = L		5		mA
I_{SDAC}	S-Video DACs	37.5 ohm load, I_{REF} = 3.15 mA		140		mA
I_{CDAC}	Composite Video DAC	37.5 ohm load, I_{REF} = 3.15 mA		70		mA
Digital Inputs and Outputs						
C_I	Input Capacitance			5	10	pF
C_O	Output Capacitance			10		pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
V_{T+}	Schmitt Trigger Positive Threshold			3.0		V
V_{T-}	Schmitt Trigger Negative Threshold			0.8		V
V_{OH}	Output Voltage, HIGH	I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	I_{OL} = Max			0.4	V
Analog Intputs						
C_{AI}	A/D Input Capacitance	ADCLK = LOW ADCLK = HIGH		4 12		pF pF
R_{IN}	A/D Input Resistance		500	1000		KΩ
I_{CB}	A/D Input Current				±1	µA
V_{RO}	Voltage Reference Output		0.988	1.235	1.482	V
Z_{RO}	V_{REF} Output Impedance			3		KΩ
Analog Outputs						
V_{OC}	Video Output Compliance		-0.4		2	V
R_{OUT}	Video Output Resistance			15		KΩ
C_{OUT}	Video Output Capacitance	C_{OUT} = 0 mA, Freq. = 1 MHz		15		pF
I_{OS}	Short-Circuit Current		-20		-80	mA

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
Clocks						
f_{XTAL}	Crystal/Reference Clock Frequency			27		MHz
f_{XTOL}	Crystal/Reference Clock Frequency Tolerance				±1350	Hz
t_{PWH}	Reference Clock Pulse Width, HIGH					ns
t_{PWL}	Reference Clock Pulse Width, LOW					ns
Syncs						
f_H	VGAHS Frequency	60 Hz Modes	30.840	31.469	32.100	KHz
		50Hz Modes	30.630	31.250	31.880	KHz
N_H	Lines per VGA frame	60 Hz Modes		525		
		50Hz Modes		625		
		Tolerance			±0	
t_{PWHS}	VGAHS Pulsewidth		2			µs
t_{VS-HS}	VGAVS to VGAHS Delay		0			ns
t_{DS}	Sync Delay (VGA Sync to Sync Out)					ns
Video Output						
t_{DOV}	Analog Output Delay (PXCK Out to Video Out)					ns
t_R	D/A Output Current Risetime (10% to 90%)			2		ns
t_F	D/A Output Current Falltime (90% to 10%)			2		ns
SKEW	D/A to D/A Skew				1	ns
Controls						
t_{PWH}	Control Input Pulse Width, HIGH			5		µs
t_{PWL}	Control Input Pulse Width, LOW			5		µs
Microprocessor Interface						
t_{PLCS}	$\overline{CS}$ Pulse Width, LOW		50			ns
t_{PHCS}	$\overline{CS}$ Pulse Width, HIGH		25			ns
t_{SA}	Address Setup Time		0			ns
t_{HA}	Address Hold Time		10			ns
t_{SD}	Data Setup Time		15			ns
t_{HD}	Data Hold Time		0			ns
t_{DOZ}	Output Delay, $\overline{CS}$ to low-Z		5			ns
t_{HOM}	Output Hold Time, $\overline{CS}$ to high-Z		5			ns
t_{DOM}	Output Delay, $\overline{CS}$ to Data Valid				30	ns

Preliminary Information

System Performance Characteristics

Parameter		Conditions	Min	Typ	Max	Unit
A/D Converter Input						
E_{LI}	A/D Integral Linearity Error, Independent	V_{RT} = 2.0V		±0.3	±0.5	LSB
E_{LD}	A/D Differential Linearity Error	V_{RT} = 2.0V		±0.3	±0.5	LSB
E_{AP}	Aperture Error			30		ps
E_{OT}	Offset Voltage, Top	$R_T - V_{IN}$ for most positive code transition	-5	-15	-25	mV
E_{OB}	Offset Voltage, Bottom	V_{IN} for most negative code transition	25	35	45	mV
D/A Converter Output						
RES	D/A Converter Resolution		9	9	9	Bits
dp	Differential Phase	PXCK = 27 MHz, 40 IRE Ramp			1.0	degree
dg	Differential Gain	PXCK = 27 MHz, 40 IRE Ramp			1.5	%
CNLP	Chroma Nonlinear Phase	NTC-7 Combination			±1.25	degree
CNLG	Chroma Nonlinear Gain	NTC-7 Combination			±1.0	%
CLIM	Chroma/Luma Intermodulation	NTC-7 Combination				IRE
CLGI	Chroma/Luma Gain inequality	NTC-7 Composite				%
CLDI	Chroma/Luma Delay inequality	NTC-7 Composite				ns
LNLD	Luma Nonlinear Distortion	NTC-7				IRE
FTWD	Field Time Waveform Distortion	NTC-7				IRE
LTWD	Line Time Waveform Distortion	NTC-7				IRE
LOTWD	Long Time Waveform Distortion, initial and peak overshoot	10% / 90% APL Bounce				IRE
LOTWD	Long Time Waveform Distortion, peak overshoot	after 5 seconds, 10% / 90% APL Bounce				IRE
LDCOFF	Line-by-Line DC Offset					IRE
DYNG	Dynamic Gain	NTC-7				IRE
NOISE	Noise Level[2]	100% unmod. ramp				dB rms
NOISE	Noise Level[3]	100% unmod. ramp				dB rms
CAMN	Chroma AM Noise	Red field				dB rms
CPMN	Chroma PM Noise	Red field				dB rms
SYRF	Sync Pulse Rise and Fall Time					ns
BERF	Burst envelope Rise and Fall Time					ns
PSRR	Power Supply Rejection Ratio	C_{BYP} = 0.1 µF, f = 1 KHz		0.5		%/ %V_{DD}

Notes:
1. Values shown in Typ column are typical for $V_{DD} = V_{DDA}$ = +5V and T_A = 25°C.
2. Noise Level is unified weighted, 10 kHz to 5.0 MHz bandwidth, with Tilt Null ON measured using VM700 "Measure Mode."
3. Noise Level is unified weighted, 10 kHz to 5.0 MHz bandwidth, measured using VM700 "Auto Mode".

Application Notes

Grounding

Analog and digital circuits are separated within the TMC2360. To keep digital system noise from the A/D and D/A converters, it is recommended that power supply voltages (V_{DD} and V_{DDA}) originate from the same low-noise source, and that ground connections (DGND and AGND) be made to the analog ground plane. Power supply connections should be individually decoupled at each pin. Digital circuitry deriving input from the TMC2360 should be referred to the system digital ground plane.

Printed Circuit Board Layout

Designing with high-performance mixed-signal circuits demands printed circuits with ground planes. Overall system performance is strongly influenced by the board layout. Capacitive coupling from digital to analog circuits may result in poor A/D conversion. Consider the following suggestions for layout:

1. Keep the critical analog traces as short as possible and as far as possible from all digital signals. Locate the TMC2360 near the board edge, close to the analog input/output connectors.

2. The power plane for the TMC2360 should be separate from that which supplies the rest of the digital circuitry. A single power plane should be used for all of the V_{DD} pins. If the power supply for the TMC2360 is the same as that of the system's digital circuitry, power to the TMC2360 should be decoupled with ferrite beads and 0.1μF capacitors to reduce noise.

3. The ground plane should be solid, not cross-hatched. Connections to the ground plane should have very short leads.

4. Decoupling capacitors should be applied liberally to V_{DD} pins. Remember that not all power supply pins are created equal. They supply different circuits on the integrated circuit, each of which generate varying amounts and types of noise. For best results, use 0.1μF ceramic capacitors. Lead lengths should be minimized. Ceramic chip capacitors are the best choice.

5. If the digital power supply has a dedicated power plane layer, it should not be placed under the TMC2360, the voltage reference, or the analog inputs. Capacitive coupling of digital power supply noise from this layer to the TMC2360 and its related analog circuitry can have an adverse effect on performance.

The 27 MHz clock reference or crystal should be handled carefully. Jitter and noise on this clock will degrade performance. With an external clock, the line should be terminated to eliminate overshoot and ringing.

Locate phase locked loop components close to the relevant TMC2360 pins. Isolate these components from noise.

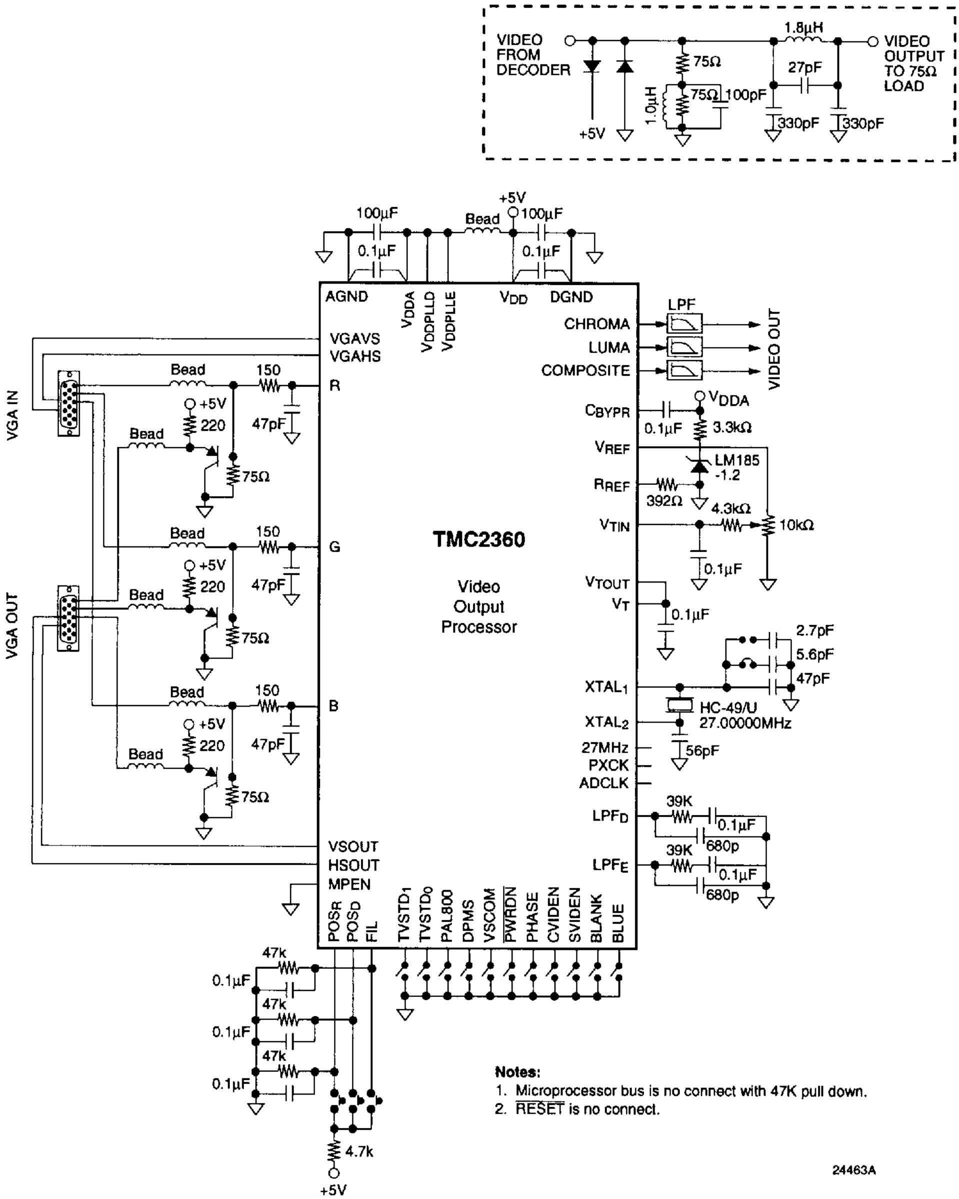

Figure 12. Typical application circuit with internal phase-locked loops

Suggested User Instructions

For a product incorporating the TMC2360, part of the documentation is expected to include operating instructions describing the functions of the TMC2360 user controls. A recommended text fragment follows:

Three external controls may be used to:

1) position the image within the boundaries of the TV screen.

2) control vertical resolution.

Each control is a button that can be momentarily depressed to execute one cycle of the selected function.

Position Controls

Position controls shift the viewed image horizontally or vertically to reveal portions of the image that are located near the edges or in the overscan areas. At power-up, the default position is the midpoint of the adjustment range.

Each time the VERTICAL POSITION button is depressed, the TV window moves down by eight lines. At the lowest position (-64 lines) the direction reverses and depressing the button moves the image up in 8-line increments to the highest position (+64 lines). At this point the direction again reverses and the next sixteen pulses move the image down to the lowest position.

When the HORIZONTAL POSITION button is depressed, the TV window moves eight pixels to the right. At the maximum right position (+64 pixels) the direction reverses and the next sixteen pulses move the window left to the maximum left position (-64 pixels). Direction again reverses and the next sixteen pulses move the image right.

Flicker Filter

Annoying artifacts can be eliminated by selecting one of three filter modes which trade-off vertical resolution against flicker. For example, without the filter, a single VGA line is encoded into only one field of the TV display. If there is high contrast between this line and adjacent lines, it will flicker at 30 Hz in NTSC or 25 Hz in PAL.

Depressing the FILTER button indexes through the filter functions shown in the table below:

FIL	Filter Mode
↓ ↑	Soft vertical resolution without flicker
↓	Medium vertical resolution, some flicker
↓	Sharp vertical resolution with flicker
└┘	Color bars

The filter should be selected for best appearance on the TV screen. Optimal selection will depend on the image being encoded.

Related Products

- TMC2302 Image Manipulation Sequencer

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2360KLC	0°C to 70°C	Commercial	80 Lead MQFP	2360KLC
TMC2360R0C	0°C to 70°C	Commercial	84 Lead PLCC	2360R0C