



SANYO Semiconductors

APPLICATION NOTE

An ON Semiconductor Company

STK673-010-E Thick-Film Hybrid IC Bipolar Fixed-current Chopper (external Excitation PWM) Built-in Microstepping Control

STK673-011-E 3-Phase Stepping Motor Driver (Sine wave drive) Output Current 2.4A

Overview

The STK673-010/011-E is a 3-phase-stepping motor driver hybrid IC with built-in microstepping controller having a bipolar constant-current PWM system, in which a power MOSFET is employed at an output stage.

It includes a 3-phase distributed controller for a 3-phase stepping motor to realize a simple configuration of the motor driver circuit.

This number of motor revolution can be controlled by the frequency of external clock input. 2, 2-3, w2-3-phase excitation modes are available. The base step angle of the stepping motor can be separated as much as one-eighth 2-3-phase to 2w2-3-phase excitation mode control quasi-sine wave current, thereby realizing low vibration and low noise.

Features

- Number of motor revolution can be controlled by the frequency of external clock input.
- 4 types of modes, i.e., 2, 2-3, w2-3 and 2w2-3 phase excitations, are available which can be selected based on rising of clock signals, by switching highs and lows of Mode A and B terminals.
- Setting a Mode C terminal Low allows an excitation mode that is based on rising and falling of a clock signal.
 - By setting the Mode C terminal Low, phases that are set only by Mode A and Mode B can be changed to other phases as follows without changing the number of motor revolution: 2-phase may be switched to 2-3-phase; 2-3-phase may be switched to w2-3-phase; and w2-3-phase may be switched to 2w2-3-phase.
- Phase is maintained even when excitation mode is changed.
- An MOI output terminal which outputs 1 pulse per 1 cycle of phase current.
- A CW/CCW terminal which switches the rotational direction.
- A Hold terminal which can temporarily hold the motor in a state where the phase current is normal operation.
- An Enable terminal which can forcibly turn OFF a MOSFET of a 6 output driving element in normal operation.
- Schmitt inputs with built-in pull-up resistor (20kΩ typ)
- Motor current can be set by changing the voltage of the Vref terminal (0.63V per 1A, dealing as much as 0 to 1/2 Vcc2 (4A)).
- The clock input for controlling the number of motor revolution rises from 0 to 50 KHz.
- Supply voltage: Vcc1=16 to 30V, Vcc2=5.0V±5%.
- A built-in current detection resistor (0.227Ω).
- A motor current during revolution can deal with as 2.4A at Tc=105deg and as high as 4A at Tc=50deg or lower.

Applications

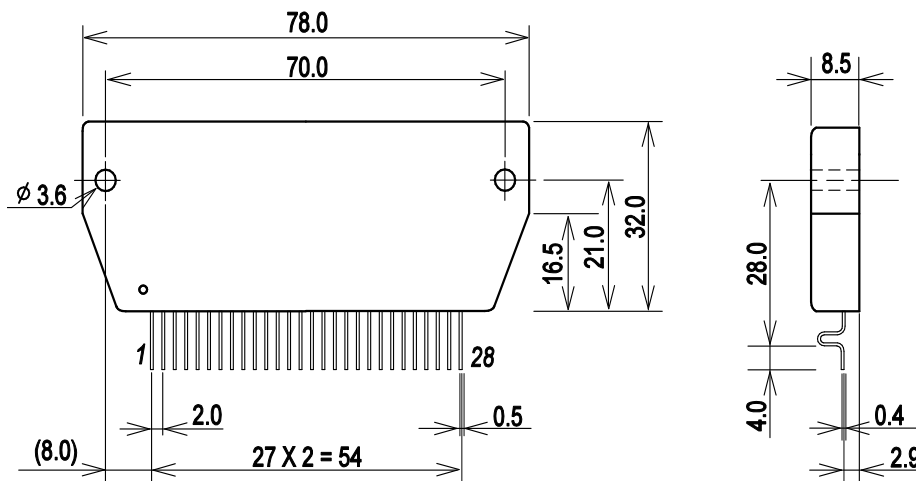
- Facsimile stepping motor drive (send and receive)
- Paper feed and optical system stepping motor drive in copiers
- Laser printer drum drive
- Printer carriage stepping motor drive
- X-Y plotter pen drive
- Other stepping motor applications

Selection Guide

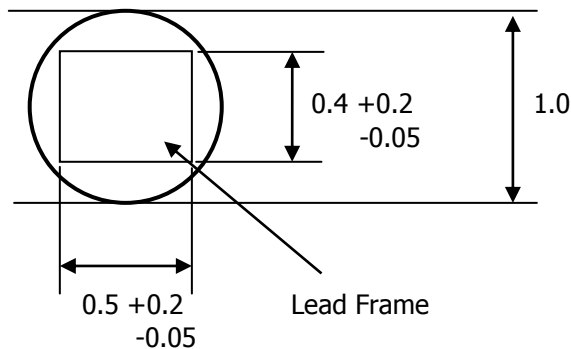
Parameter	STK673-010	STK673-011
Output current	2.4A	
Internal current detection resistor	0.227Ω	
Micro-step-resolution	Full(1/1) step(2 excitation)	
	1/3 step(2-3 excitation)	
	1/6step(W2-3 excitation)	
	1/12step(2W2-3 excitation)	

Package Dimensions

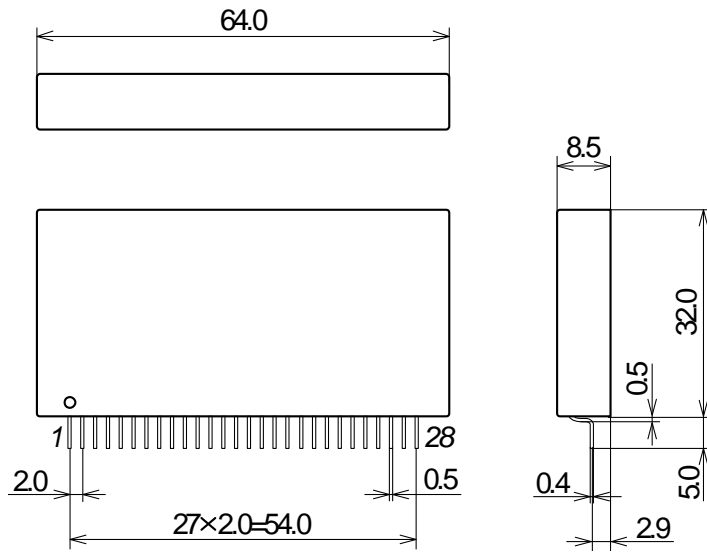
STK673-010-E
 unit : mm (typ)
 4130



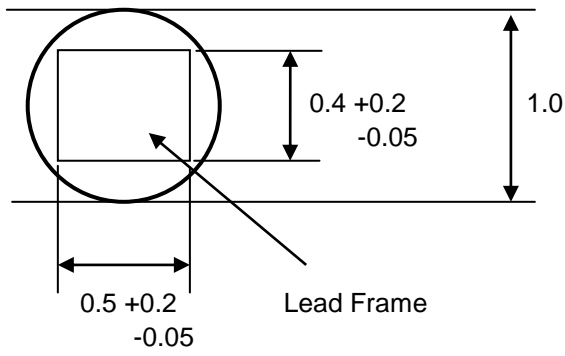
Recommend hole size for Lead Frame on PCB; 1.0 mm(max)



STK673-011-E
 unit : mm (typ)

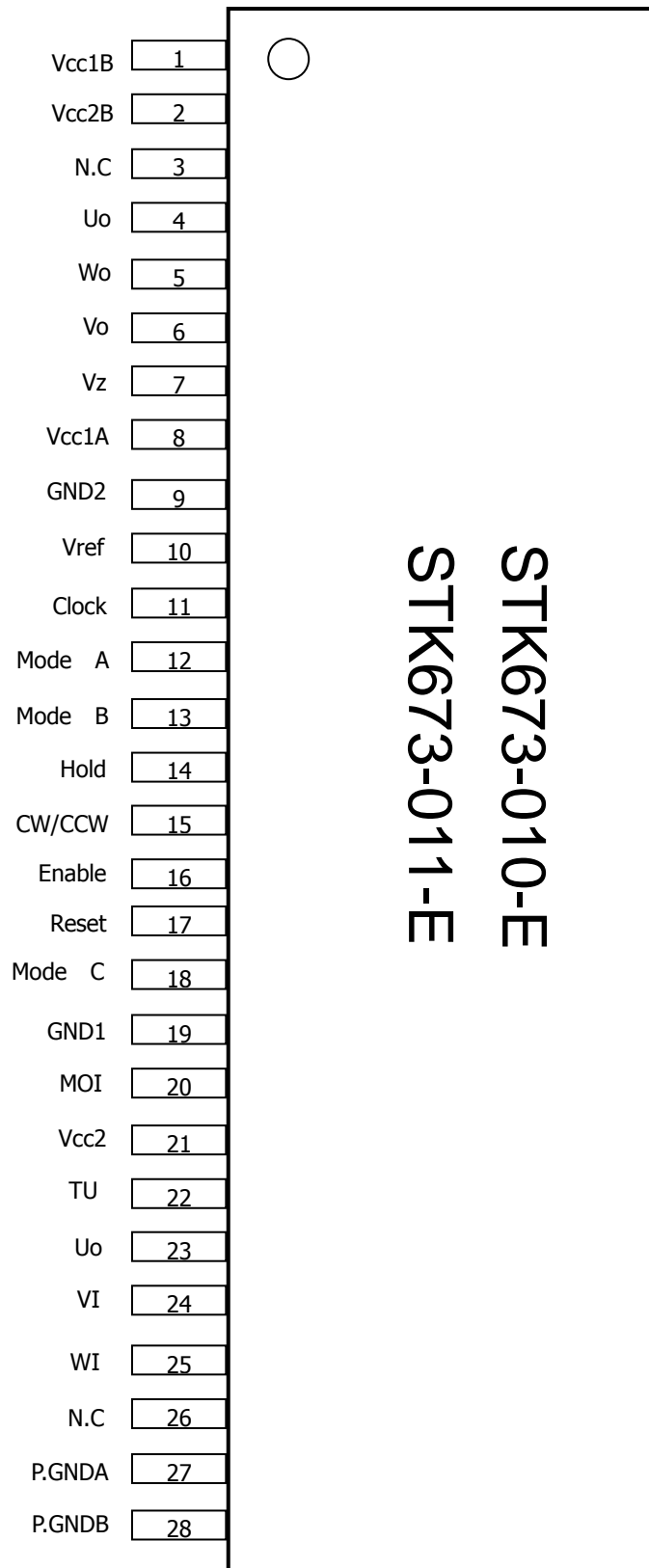


Recommend hole size for Lead Frame on PCB; 1.0 mm(max)

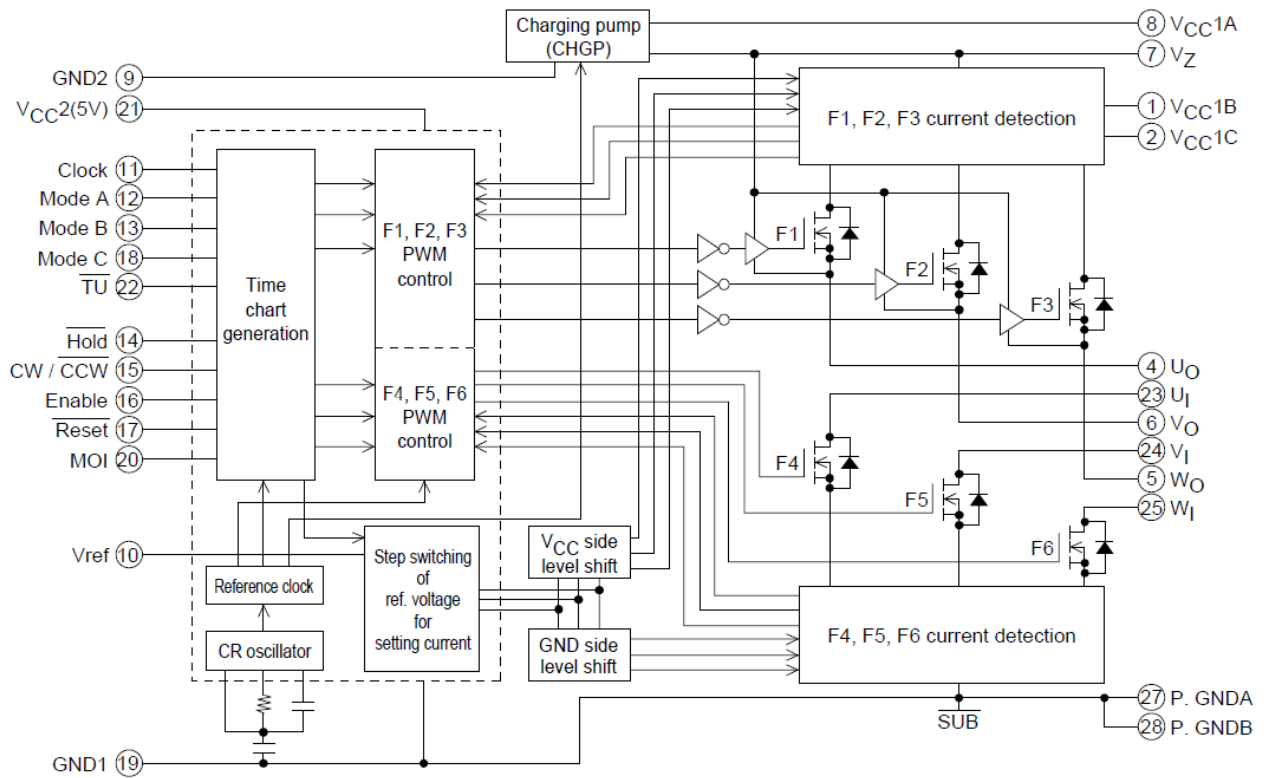


Pin Assignment

STK673-010-E and STK673-011-E



STK673-010-E, STK673-011-E
Equivalent Block Diagram



Absolute Maximum Ratings at Tc=25°C

Parameter	Symbol	Condition	Raitings		unit
			STK673-010	STK673-011	
Maximum supply voltage 1	Vcc1max	No signal	36		V
Maximum supply voltage 2	Vcc2max	No signal	-0.3 to 7.0		V
Input voltage	Vinmax	Logic input pins	-0.3 to 7.0		V
Output current	IOHmax	Vcc2=0V Clock \geq 100Hz	4.0		A
Operating substrate temperature	Tcmax		105		°C
Junction temperature	Tjmax		150		°C
Storage temperature	Tstg		-40 to 125		°C

Allowable Operating Ratings at Ta=25°C

Parameter	Symbol	Condition	Raitings		unit
			STK673-010	STK673-011	
Operating supply voltage 1	Vcc1	With signals applied	16 to 30		V
Operating supply voltage 2	Vcc2	With signals applied	5.0±5%		V
Input voltage	VIH		0 to Vcc2		V
Phase output urrent1	Io1	Without heat sink	1.7		A
Phase output urrent2	Io2	Tc=105°C	2.4		A
Clock frequency	fcL	Pin11 input frequency	0 to 50		KHz

Electrical Characteristics1 at Ta=25°C, Vcc1=24V, Vcc2=5.0V

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Vcc2 supply current	Icco	ENABLE=Low		6.1	12	mA
Output saturation voltage (STK673-010,011)	Vsat	RL=23Ω		1.0	1.6	V
Effective output current (STK673-010,011)	Ioave	Each phase R/L=2Ω/6mH 2W2-3-phase excitation Vref=0.61v	0.62	0.69	0.76	Ams
FET diode forward voltage (STK673-010, 011)	Vdf	If=1.0A(RL=23Ω)		1.0	1.6	V
Output leakage current	IOL	RL=23Ω			0.1	mA
Input high voltage	VIH	9 terminals, Pins 11 to 18,22	4			V
Input Low voltage	VIL	9 terminals, Pins 11 to 18,22			1	V
Input current	IIL	Pins 11 to 18 pin=GND level Pull-up resistance 20kΩ(typ)	115	250	550	μA
Vref Input voltage	VrH	Pin 10	0		Vcc2/2	V
Vref Input current	Ir	Pin 10, pin 2.5V	440	625	810	μA
MOI output high voltage	VOH	Pin20, pin20 to 19=820Ω	2.5			V
MOI output low voltage	VOL	Pin20, pin21 to 20=1.6kΩ			0.4	V
PWM frequency	fc			63		kHz

Electrical Characteristics2 at Ta=25°C, Vcc1=24V, Vcc2=5.0V

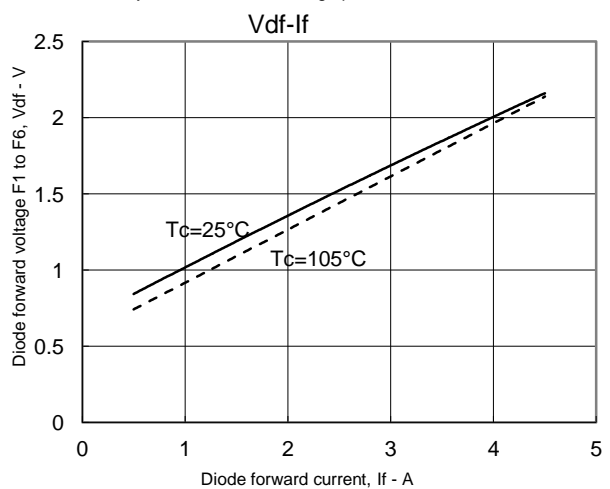
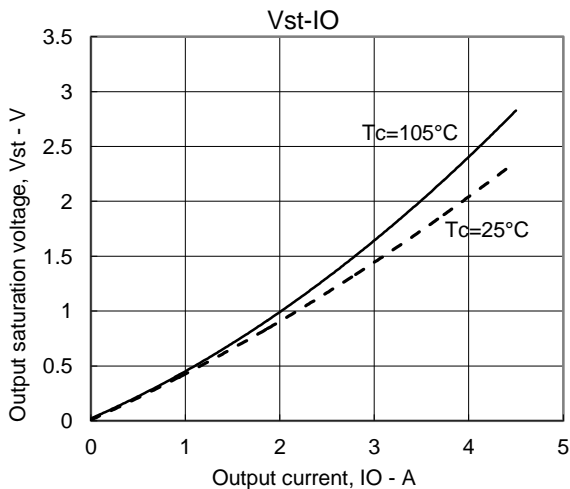
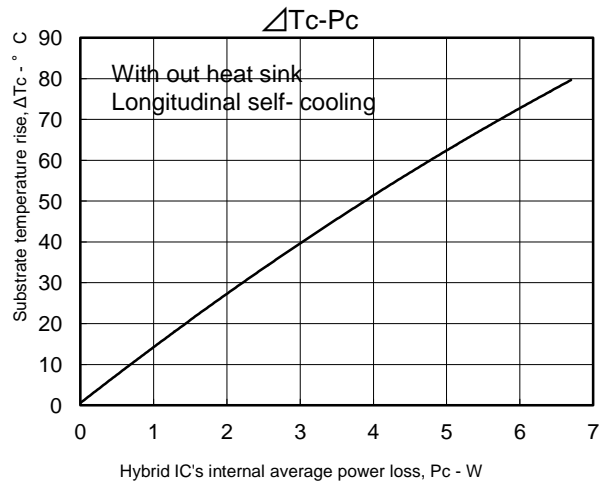
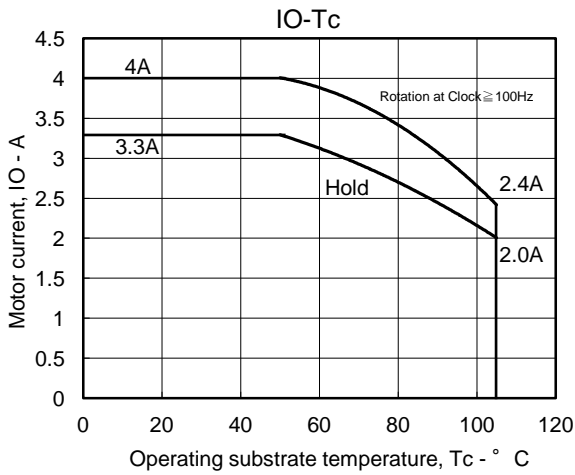
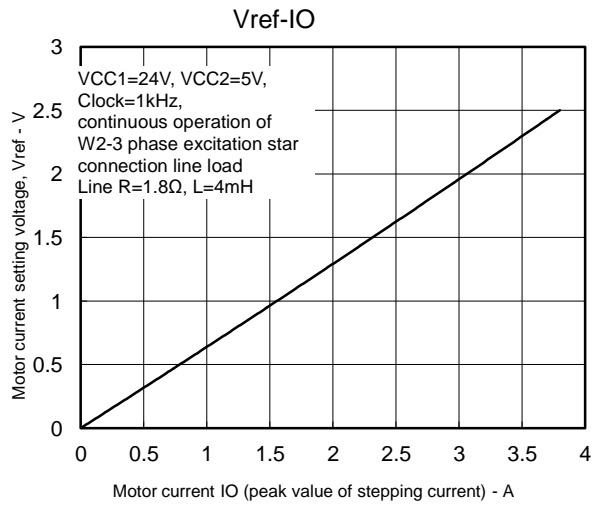
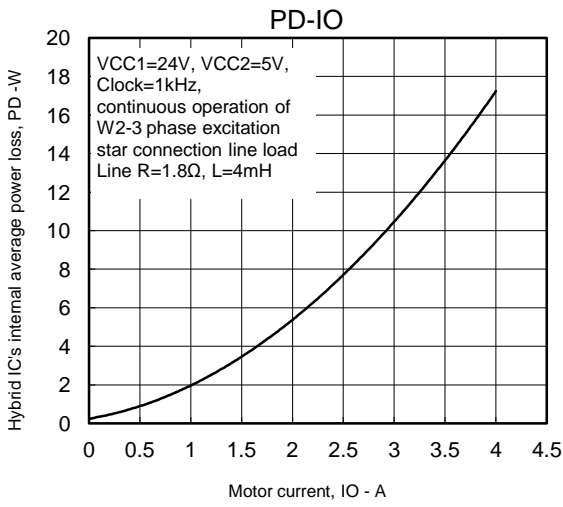
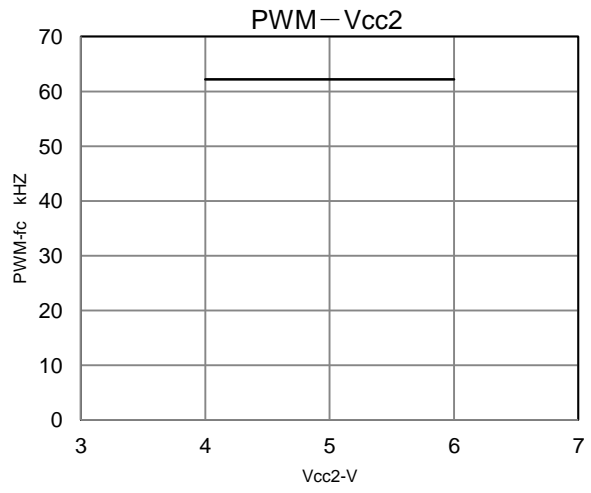
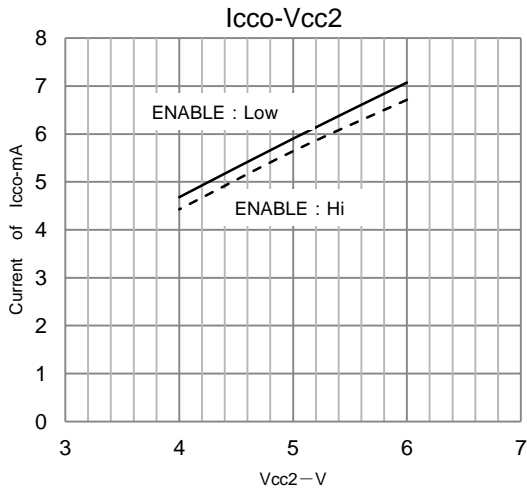
Current division ratio at phase current of 1/4 electrorotation, in each excitation mode(unit=%,typ.)

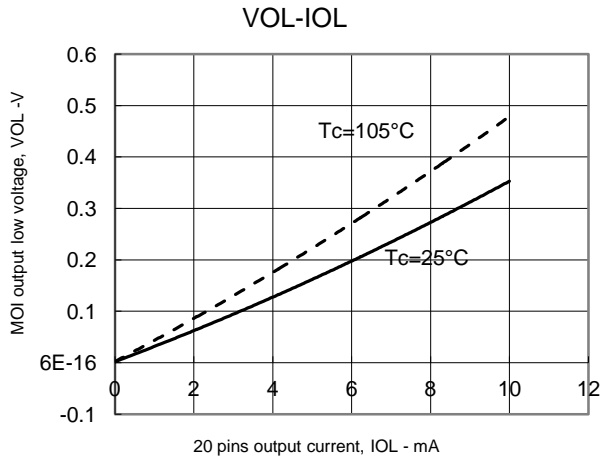
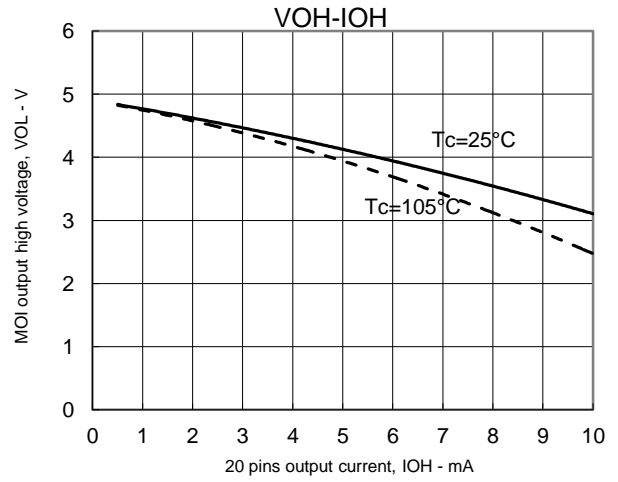
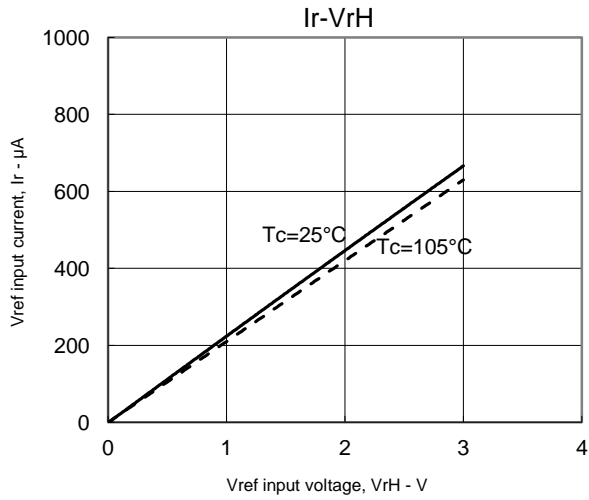
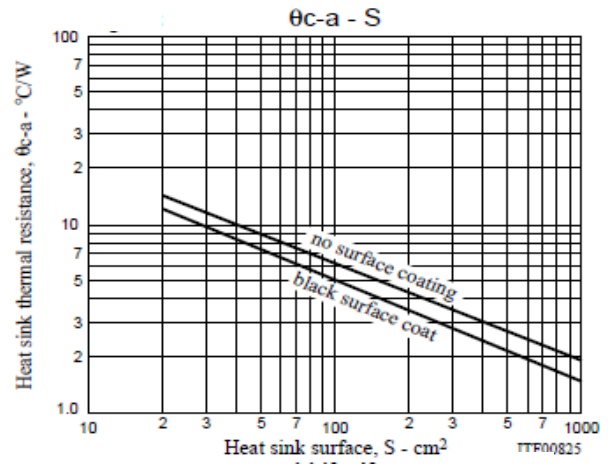
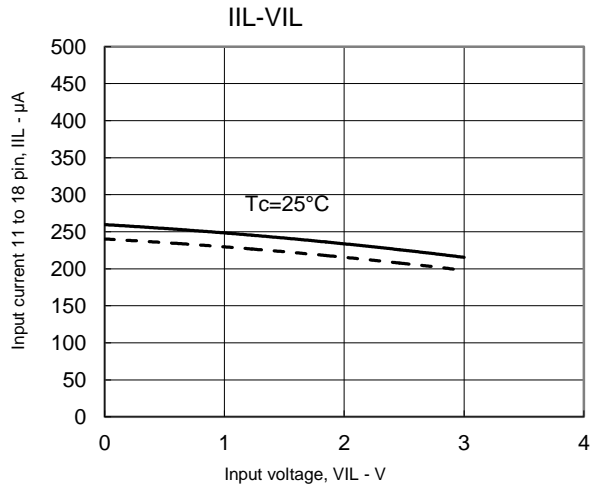
Number of current division is put in perenthese.

Current division	2phase(1)	2-3phase(3)	W2-3 phase(6)	2w-3 phase(12)
1/96	0	0	0	0
2/96			13	
3/96			26	
4/96			26	
5/96		50	50	38
6/96				50
7/96				61
8/96				71
9/96	100	87	87	79
10/96				87
11/96				92
12/96				96
13/96		100	100	96
14/96				98
15/96				98
16/96				100
17/96				
18/96				
19/96				
20/96				
21/96				
22/96				
23/96				
24/96				

Note:Constant voltage supply is used as power supply

Electrical Characterristic 2 represents design values. Measurement for controlling the standard value is not conducted.





Pin Functions

Pin No.	Pin Name	Pin Function	Equivalent circuit
1	Vcc1B	Moto power supply connection pin	
2	Vcc1C	Moto power supply connection pin	
3	NC	—	
4	Uo	U phase output pin	
23	UI		
5	Wo	W phase output pin	
24	WI		
6	Vo	V phase output pin	
25	WI		
7	Vz	Hi Voltage power supply connection pin	
8	Vcc1A	Moto power supply connection pin	
9	GND2	Signal ground pin2	
10	Vref	Current value setting	
11	Clock	External CLK (motor rotation instruction) input pin	
12	Mode A	Step mode selection input pin	
13	Mode B		
14	Hold		
15	CW/CCW	Sets the direction of rotation of the motor axis input pin	
16	ENABLE	Motor current OFF input pin	
17	RESETB	System reset input pin	
18	Mode C	Step mode selection input pin	
22	TU	Sensing ground pin for Vref	
19	GND1	Signal ground pin2	
20	MOI	Motor phase excitation output pin	
21	Vcc2(5v)	5v power supply connection pin	-
26	NC	—	-
27	P.GNDA		
28	P.GNDB		

Description of operation

Input Signal Functions and Timing

(1) Input terminal use of 5V system

[RESET and Clock (timing of input signal upon rising of power supply)]

The driver is configured to include a 5V system logic section and a 24V MOSFETs section. The MOSFETs on both VCC1 side and GND side are N-channels. Thus, the MOSFETs on the VCC1 side are provided with a charging pump circuit for generating a voltage higher than that of VCC1. When a Low signal is input to a RESET terminal for operating the RESET, the charging pump is stopped. After the release of the RESET (High input), it requires a period of 1.7ms to rise the charging pump. Accordingly, even when a Clock signal is input during the rising of the charging pump circuit, the MOSFET cannot be operated. Such timing needs to be taken into consideration for inputting a Clock signal.

An example of timing is shown in Figure 1.

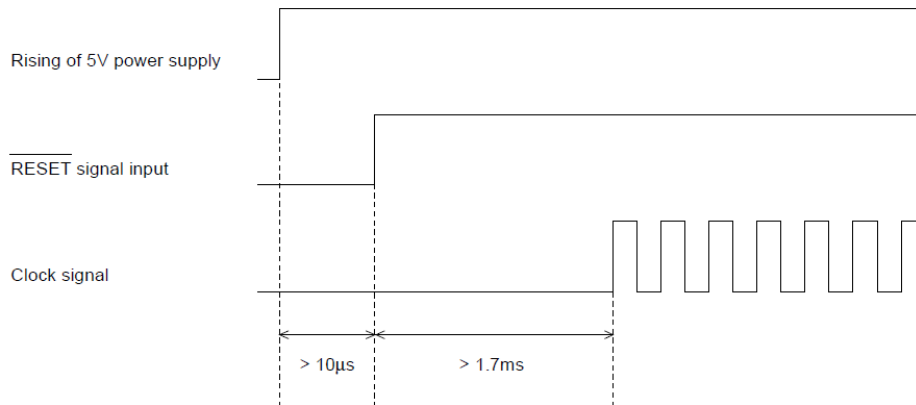


Figure 1. Timing chart of RESET signal and Clock signal

When the RESET terminal switches from Low to High where a High period is 1.7ms or longer and the Clock input is conducted in a Low state, each phase current of the motor is maintained at the following values.

Phase	Current in the case where the initial Clock signal is maintained at Low level (Other than 2-3-phase TU excitation)	Current in the case where the initial Clock signal is maintained at Low level (2-3-phase TU excitation)
U phase	0	0
V phase	-87% of peak current during normal rotation	-100% of peak current during normal rotation
W phase	+87% of peak current during normal rotation	+100% of peak current during normal rotation

Refer to the timing charts for operations.

(2)Clock (phase switching clock)

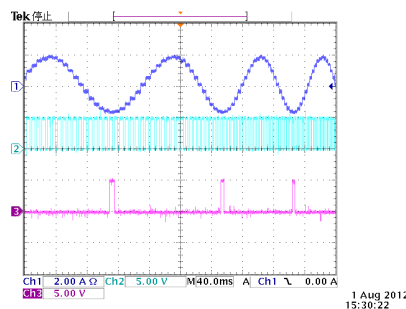
Clock signals should be input under the following conditions so that all 9 types of excitation modes shown in the Excitation Mode Table.

Input frequency range DC to 50kHz

Minimum pulse width 10µs

High level duty 40 to 60%

When Mode C is not used, it is an operation based on rising of the Clock and thus the above-mentioned condition of high level duty is negligible. A minimum pulse width of 10µs or more allows excitation operation by Mode A and Mode B. Since the operation is based on rising and falling of the Clock under the use of Mode C, it is most preferable to set the high level duty to 50% so as to obtain uniform step-wise current widths.



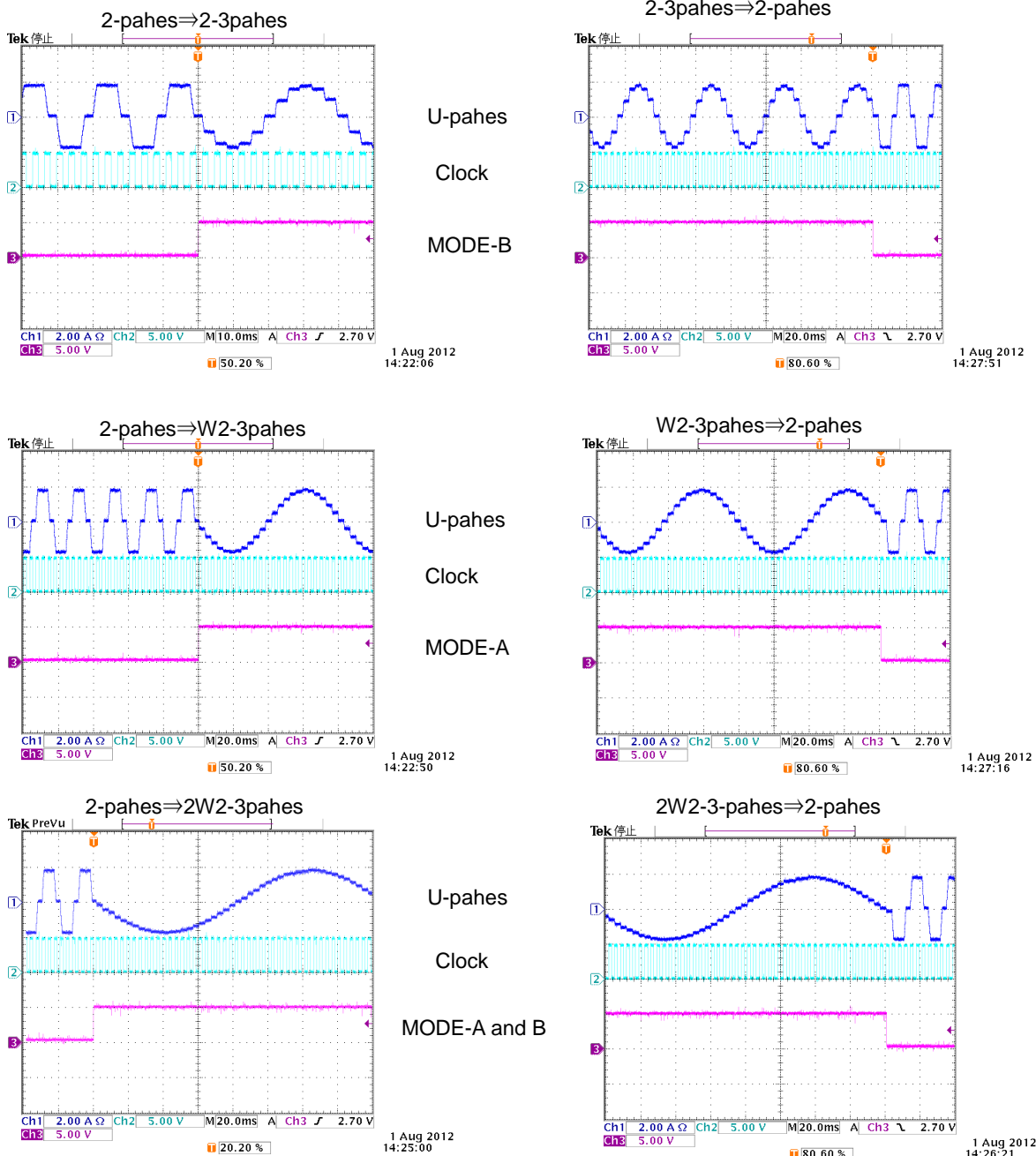
(2) Mode A, Mode B, Mode C and TU

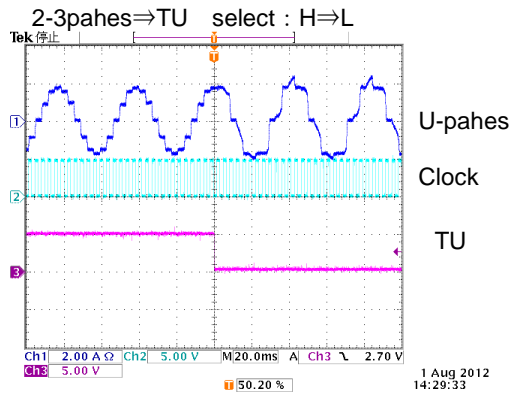
These 4 terminals allow selection of excitation modes. For specific operations, refer to Excitation Mode Table and Timing Charts.

Input condition				Excitation No.	Excitation Mode.	Number of current steps	Number of clock cycle of phase current
Mode A	Mode B	Mode C	TU				
0	0	1	1	(1)	2-pahes	1	6
0	1	1	1	(2)	2-3-phase	3	12
0	1	1	0	(3)	2-3-phase TU	1	12
1	0	1	1	(4)	W2-3-phase	6	24
1	1	1	1	(5)	2W2-3-phase	12	48
0	0	0	1	(6)	2-3-phase	3	6
0	0	0	0	(7)	2-3-phase TU	1	6
0	1	0	1	(8)	W2-3-phase	6	12
1	0	0	1	(9)	2W2-3-phase	12	24

As shown in the table, TU terminal is only effective for Excitation Nos. (3) and (7). Although the present hybrid IC is not damaged even when TU = 0 is mistakenly input in Excitation, other than Excitation Nos. (3) and (7), motor vibration or motor current may increase.

* Timing charts for 3-phase stepping motor driver is illustrated on pages 9 to 13 for exemplary operations of Enable Hold, CW/CCW for Excitation Nos. (1), (2), (3), (4), (5) and (9), and Excitation No. (4).

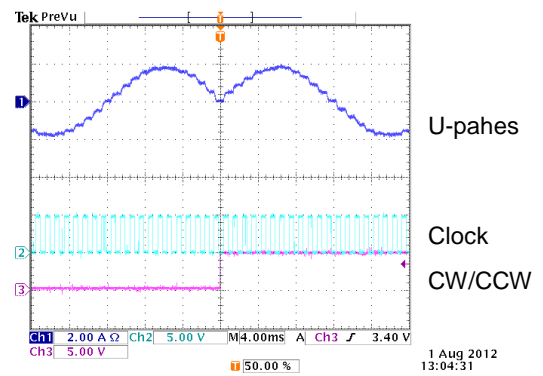
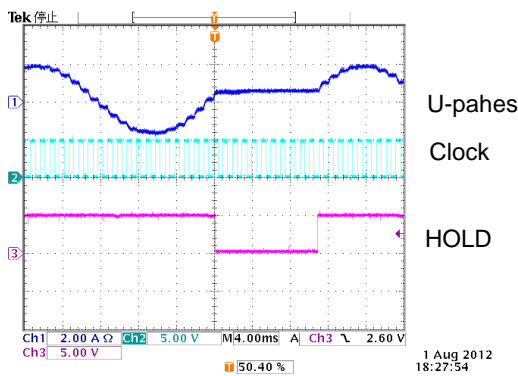




(3) Hold, CW/CCW

Hold temporary holds the motor while a phase current of the motor is conducted, even when there are clock inputs of Low input. High input releases the hold, and the motor current changes again synchronizing with the rising of Clock signals. Refer to Timing Chart for exemplary operations.

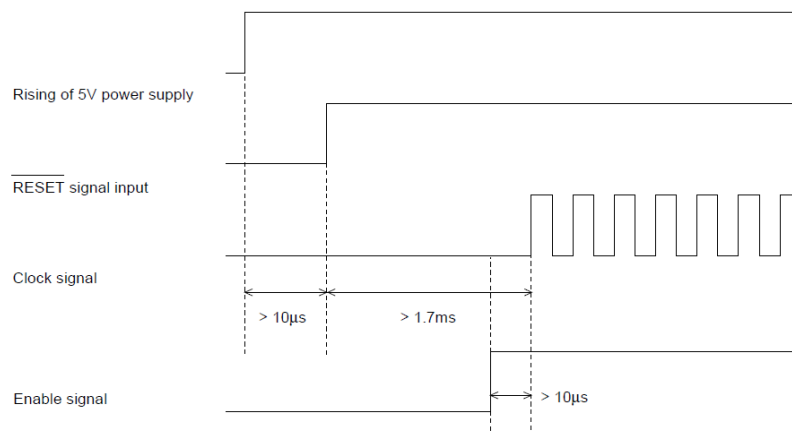
CW/CCW switches the rotational direction of the motor. Switching to High gives a rotational operation of CW, and Low gives a rotation operation of CCW. The timing of switching the rotation is synchronizes the rising of the clock signals. Refer to Timing Chart for exemplary operations.

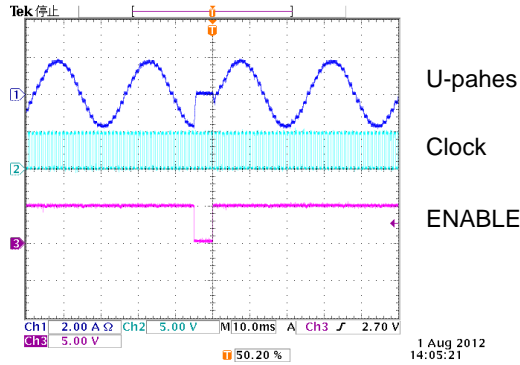


(4) Enable

High input renders a normal operation and Low input forcibly renders a gate signal of MOSFETs Low, thereby cutting a motor current. Once again High input renders a current to conduct in the motor. The timing of the current does not synchronize with the clock.

Since Low input of Enable forcibly cuts the motor current, it can be used to cut a V-phase or W-phase while Clock is maintained in a Low level state after the RESET operation.





(5) Reset terminal (Resets all parts of the system.)

- All circuit states are set to their initial values by setting the RESETB pin low

At this time, the U, V, and W phases are set to their origin, regardless of the excitation mode.

(6) Vref (Setting motor current peak value)

A peak value of a motor current IO is determined by R01, R02, VCC2 (5V) and the following set equation (I).

Set equation of peak value of motor current IO

$$IO\ peak = Vref \div K (I)$$

Where $Vref \leq 0.5 \times VCC2$ $K = 0.63 (V/A)$

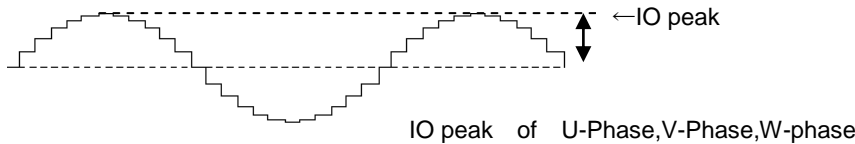
$$Vref = VCC2 \times Rox \div (R01 + Rox)$$

$$Rox = (R02 \times 4.0k\Omega) \div (R02 + 4.0k\Omega)$$

- R02 is preferably set to be 100Ω in order to minimize the effect of the internal impedance (4.0kΩ ± 30%) of STK673-010-E and STK673-011-E
- K in the above-mentioned set equation varies with in ±5 to ±10% depending on the inductance L and resistance value

R of the used motor. Check the peak value setting of IO upon actual setting.

* Refer to Figure 4 for an example of Vref-IO characteristics



(7) Allowable operating ranges of motor current

Set the peak value of the motor current IO so as to lie within a region below the curve shown in Figure 5 on page 13.

When the operation substrate temperature Tc is set to 105°C, IO max should be 2.4A or lower and a Hold operation should be conducted where IO max is 2.0A or lower.

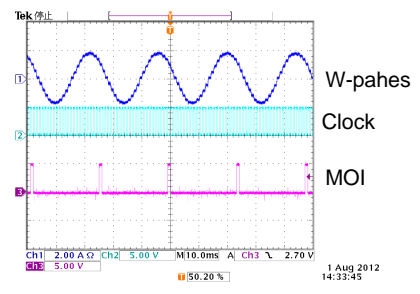
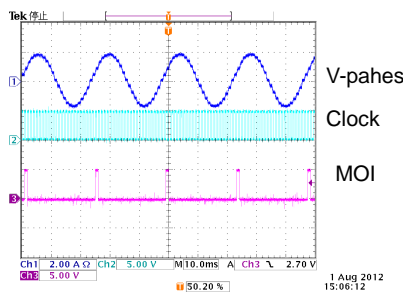
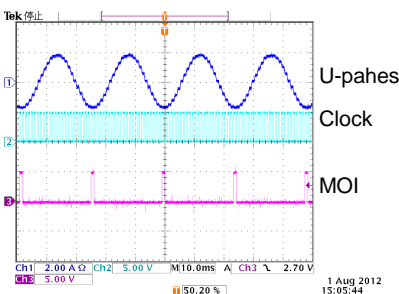
For operation where Tc = 50°C, IO max should be 4.0A or lower and a Hold operation should be conducted where IO max is 3.3A or lower.

Output pin Functions and Timing

(1) MOI

Phase excitation origin monitor

MOI outputs a Low level when internal comparator reference voltage level is set 100 % (U-Phase)



Heat Radiation Design

Heat radiation design for reducing the operation substrate temperature of the hybrid IC is effective in enhancing the quality of the hybrid IC.

The size of a heat sink varies depending on the average power loss Pd in the hybrid IC. As shown in Figure 6 on page 14, Pd increases in accordance with the increase of the output current.

Since the starting current and the stationary current coexist in an actual motor operation, Pd cannot be obtained only from the data shown in Figure 6. Therefore, Pd is obtained assuming that the timing of the actual motor operation is a repeated operation shown in the following Figure 3.

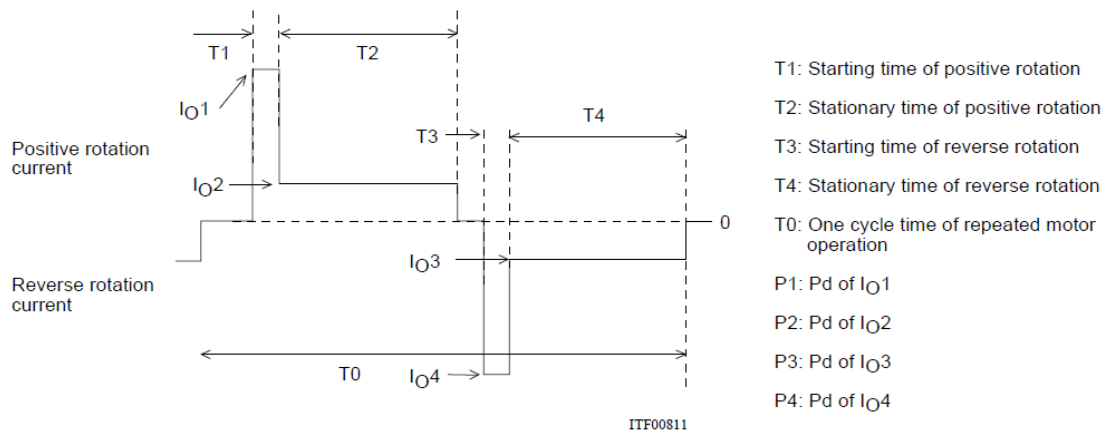


Figure 3. Timing Chart of Motor Operation

The average power loss Pd in the hybrid IC upon an operation shown in Figure 3 can be obtained by the following equation (II):

$$Pd = (T1 \times P1 + T1 \times P2 + T3 \times P3 + T4 \times P4) \div T0 \text{ (II)}$$

When the value obtained by the above equation (II) is equal to or less than 3.4W and the ambient temperature Ta is equal to or lower than 60°C, there is no need of providing a heat sink.

Refer to Figure 7 for data of the operation substrate temperature when no heat sink is used.

The size of the heat sink can be decided depending on θc-a obtained by the following equation (III) and from Fig. 8.

$$\theta_{c-a} = (Tc \text{ max} - Ta) \div Pd \text{ (III)}$$

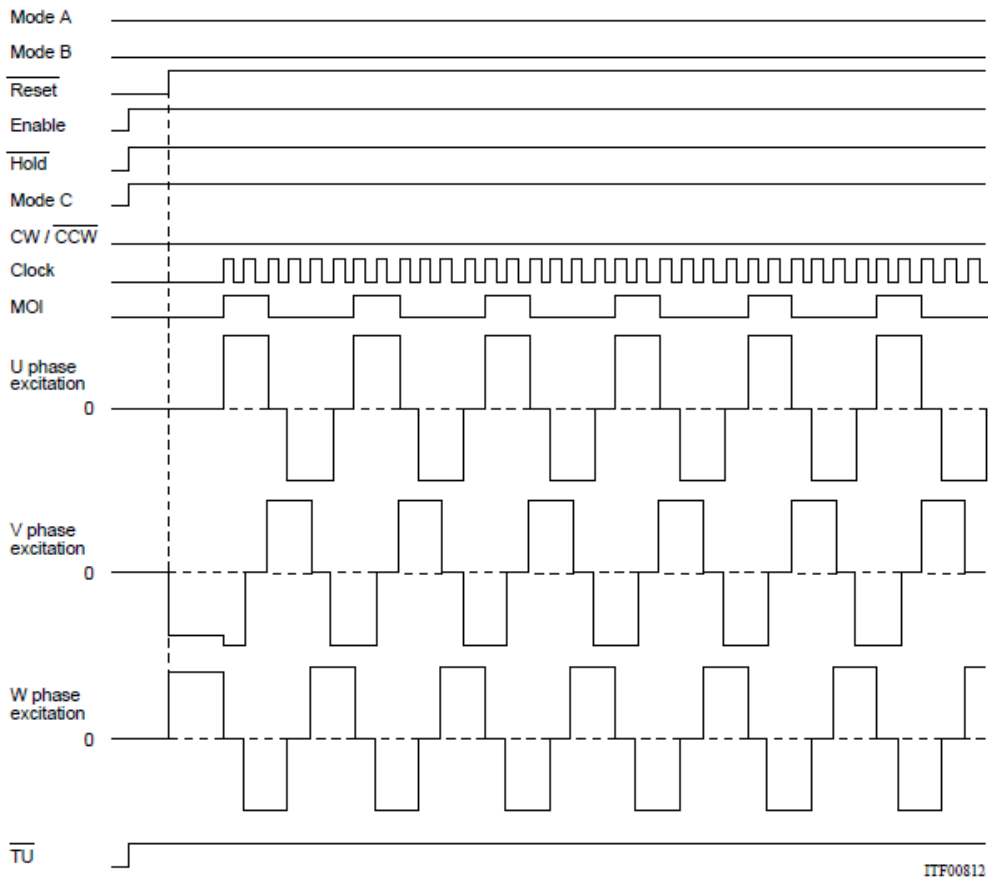
Where Tc max: Maximum operation substrate temperature = 105°C

Ta: Ambient temperature of hybrid IC

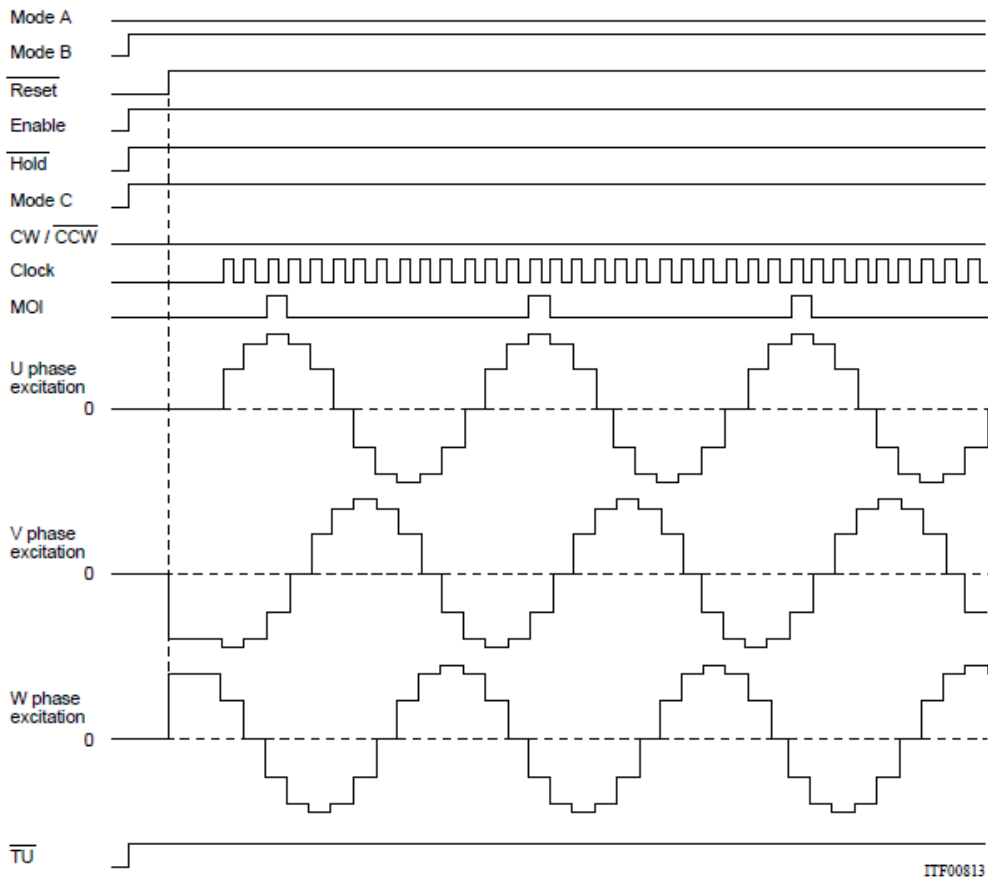
Although heat radiation design can be realized by following the above equations (II) and (III), make sure to check that the substrate temperature Tc is equal to or lower than 105°C after mounting the hybrid IC into a set.

Excitation Time and Timing Charts

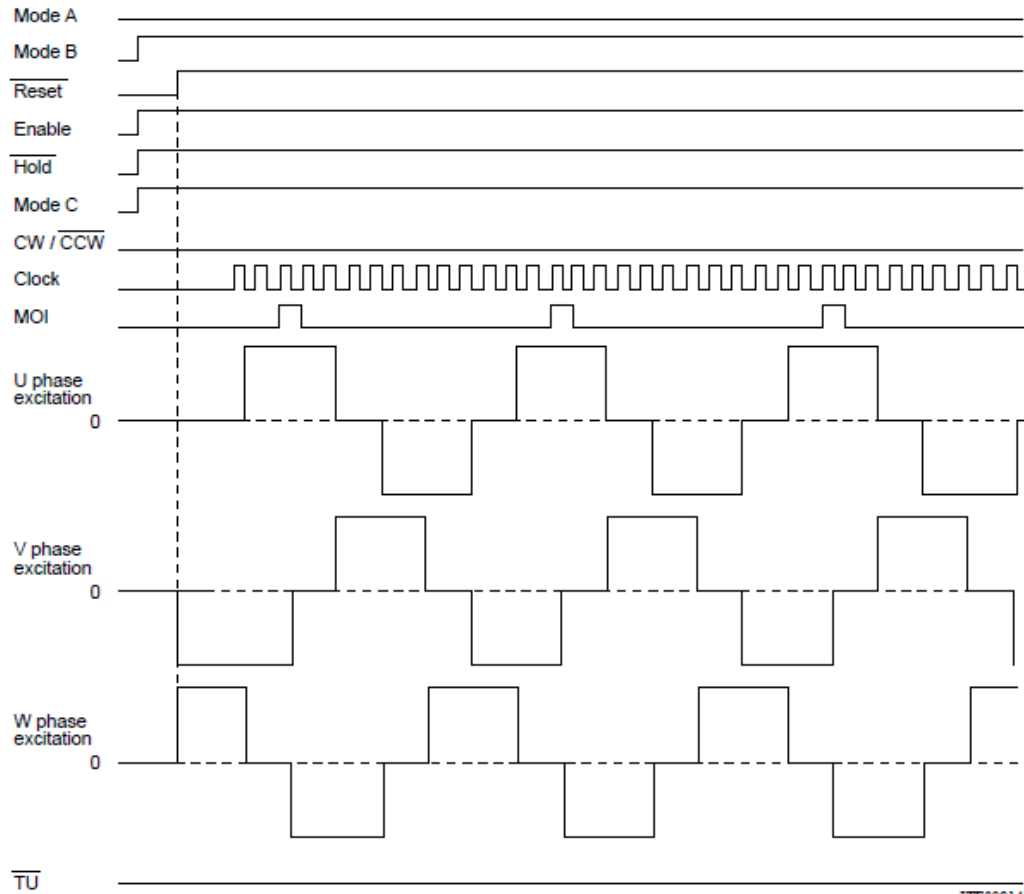
2-phase excitation



2-3 phase excitation

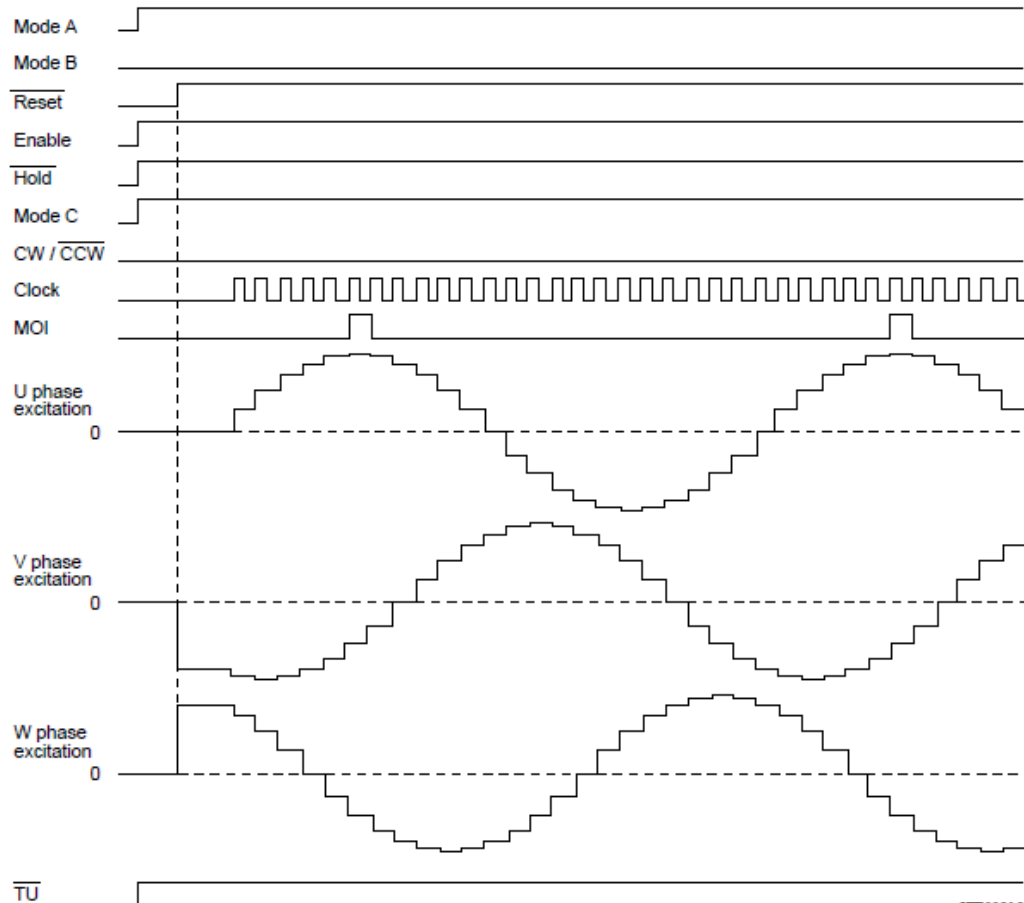


2-3 phase excitation TU



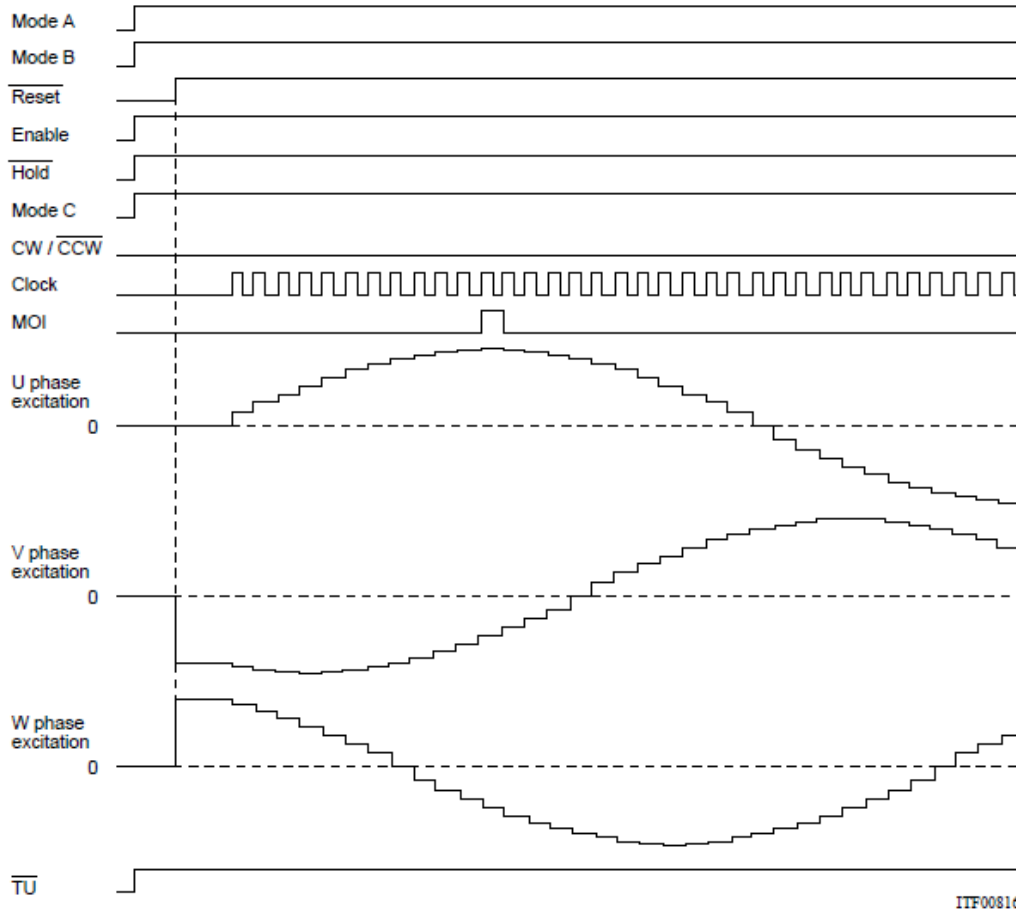
ITF00814

W2-3 phase excitation



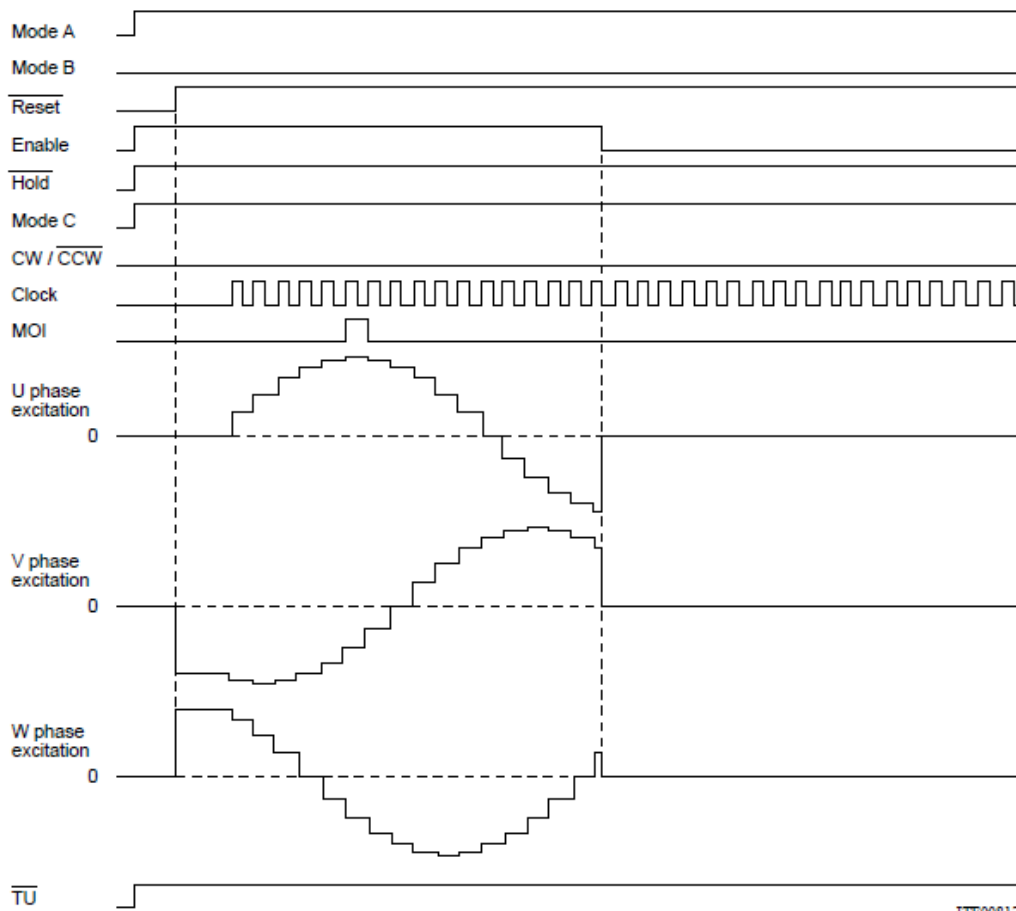
ITF00815

2W2-3 phase excitation



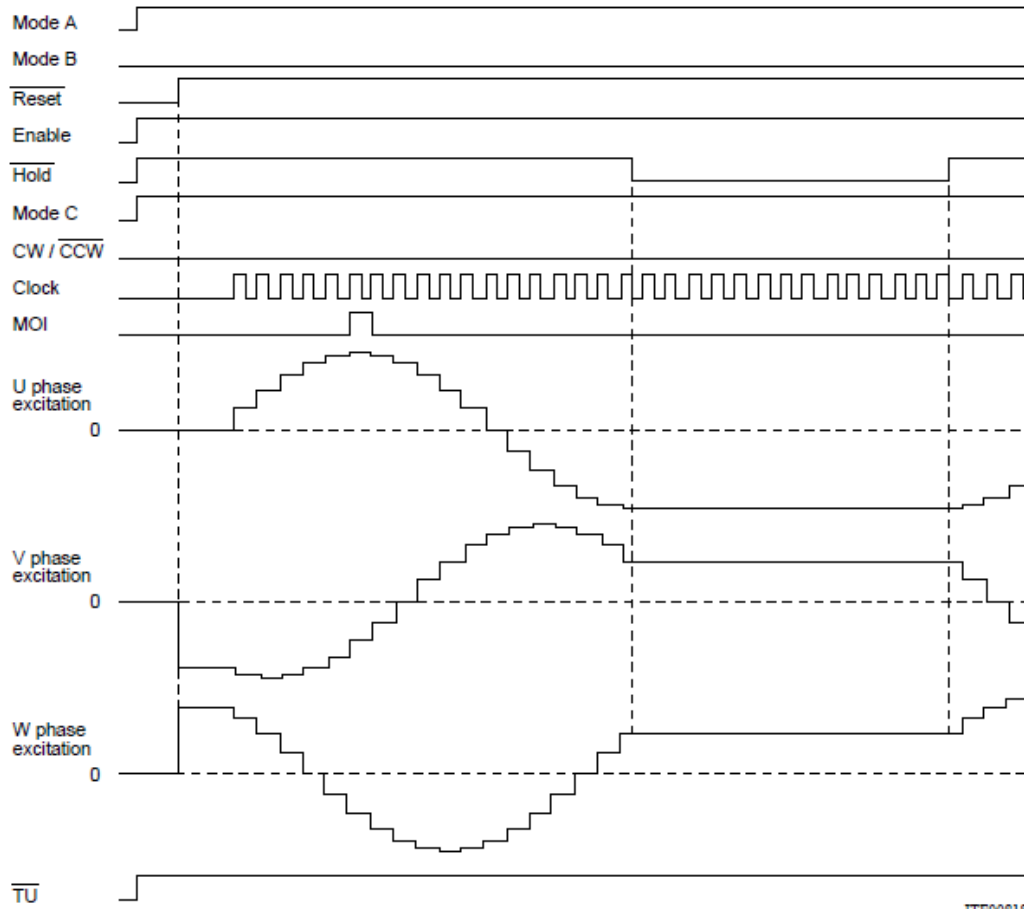
ITF00816

W2-3 phase excitation (Enable operation)



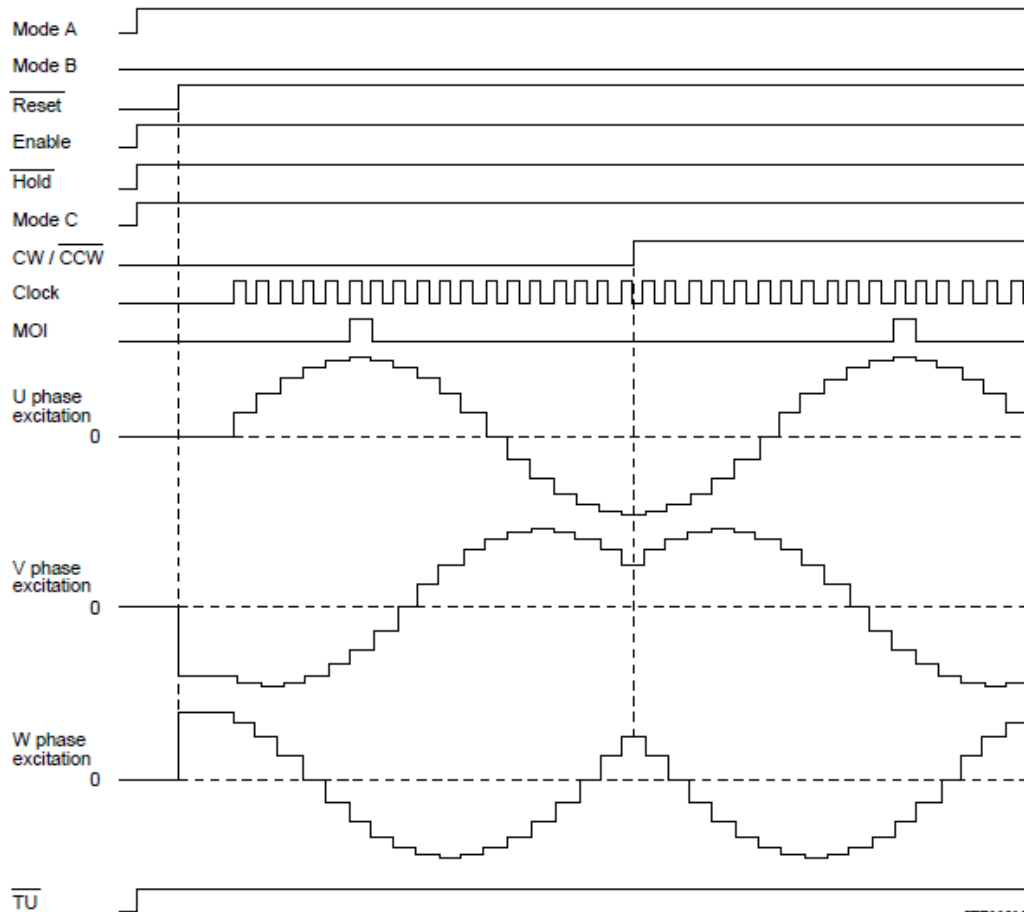
ITF00817

W2-3 phase excitation ($\overline{\text{Hold}}$ operation)



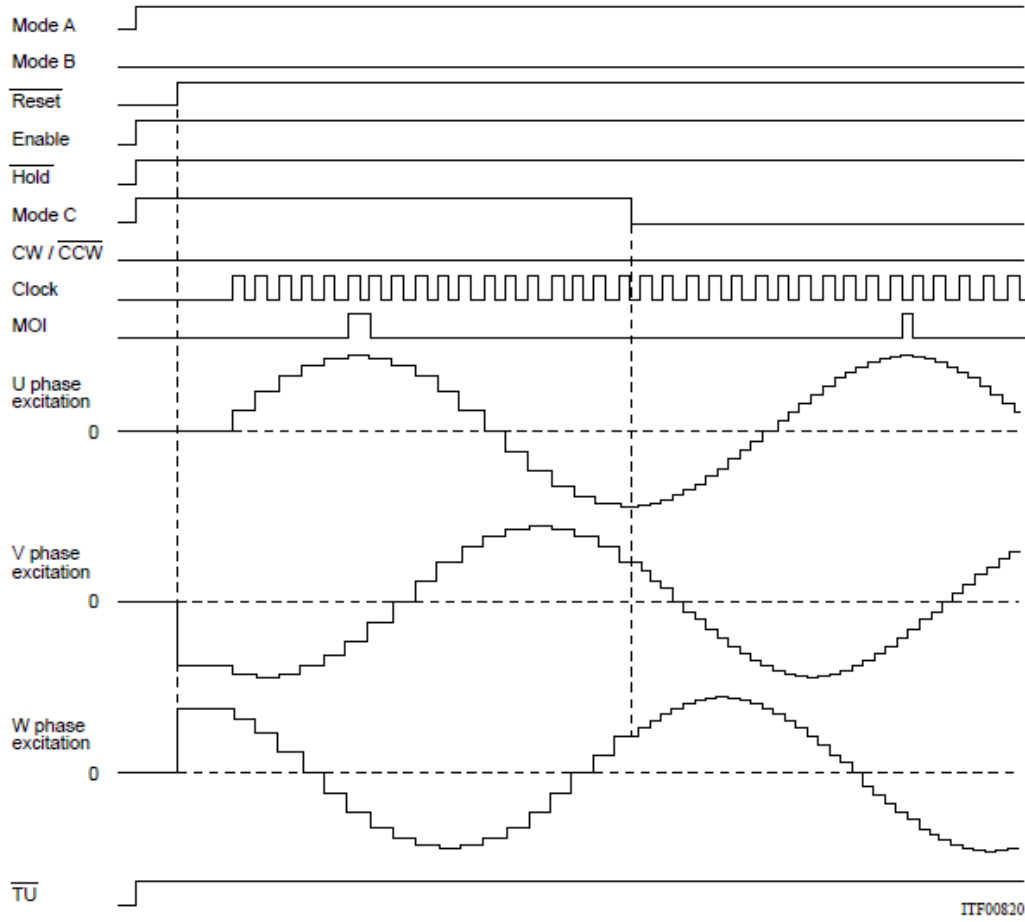
ITF00818

W2-3 phase excitation ($\text{CW}/\overline{\text{CCW}}$ operation)

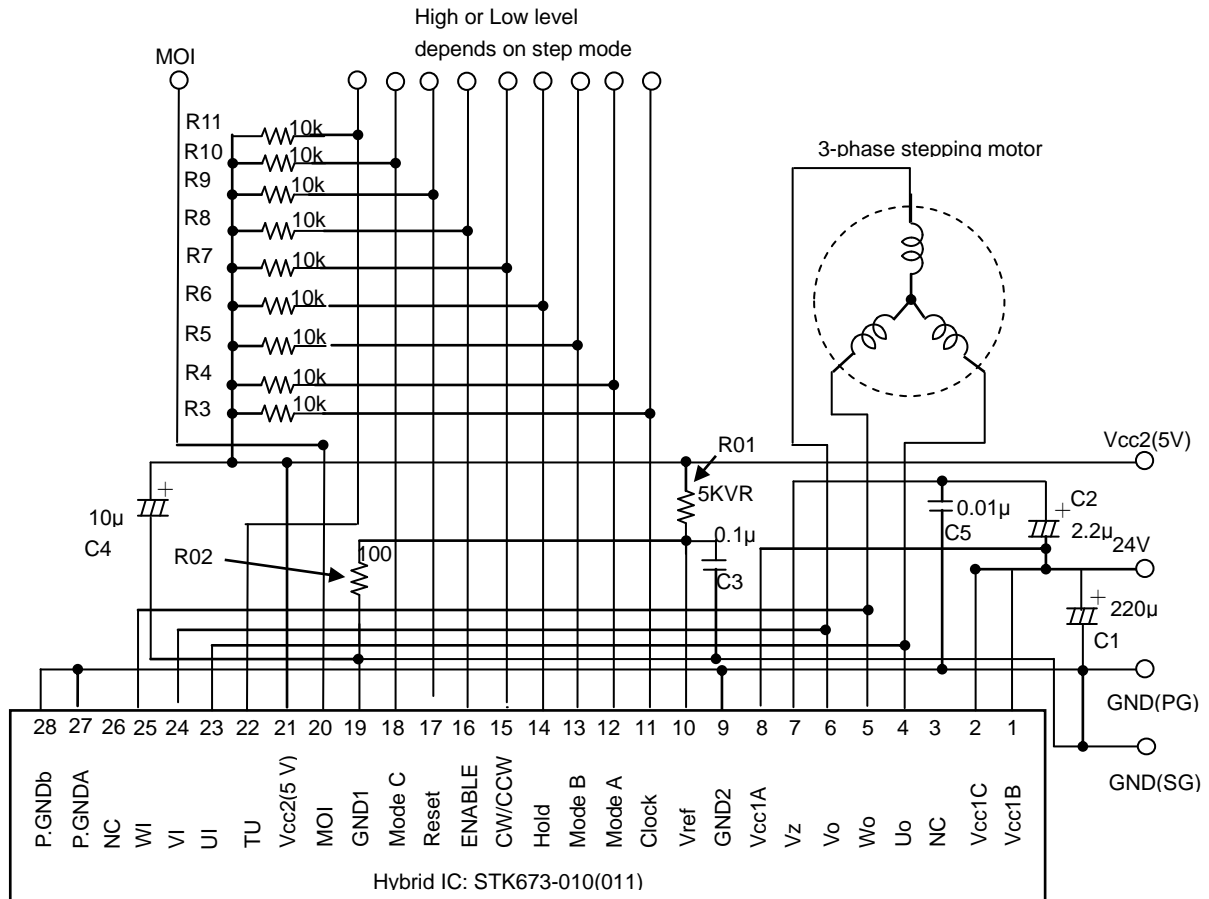


ITF00819

W2-3 phase excitation to 2W2-3 phase excitation (Mode C operation)



Application Circuit Example



Set Equation of Output Current IO Peak Value

$$IO \text{ peak} = Vref \div K \quad K = 0.63 \text{ (V/A)}$$

where $Vref \leq 0.5 \times VCC2$

$$Vref = VCC2 \times Rox \div (R01 + Rox)$$

$$Rox = (R02 \times 4.0k\Omega) \div (R02 + 4.0k\Omega)$$

- R02 is preferably set to be 100Ω in order to minimize the effect of the internal impedance (4.0kΩ ±30%) of STK673-010-E

- For noise reduction in 5V system, put the GND side of bypass capacitor (220µF) of VCC1 (shown in a thick line in the above Sample Application Circuit) in the vicinity of pins 27 and 28 of the hybrid IC.

- Set the capacitance value of the bypass capacitor C1 such that a ripple current of a capacitance, which varies in accordance with the increase of motor current, lies in an allowable range.

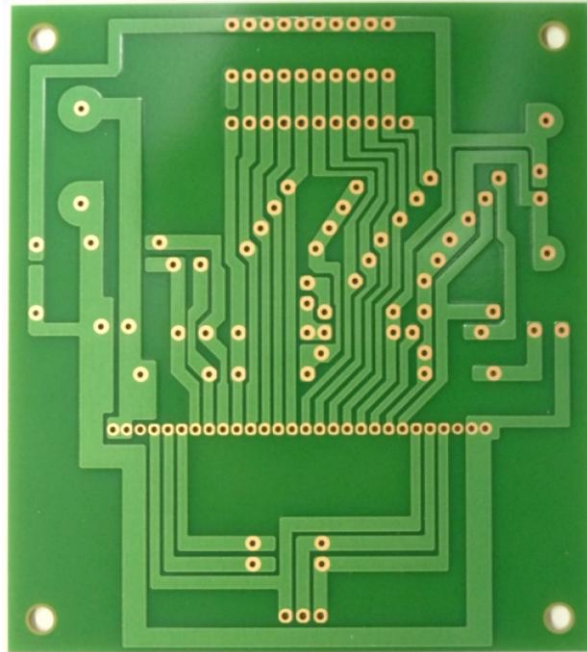
- K in the above-mentioned set equation varies within ±5 to ±10% depending on the inductance L and resistance value R of the used motor. Check the peak value setting of IO upon actual setting.

Input/Output Terminals Functions of 5V System

Terminal name	No.	Function	Conditions upon Functioning 0 = Low, 1 = High
Clock	11	Basic clock for switching phase current of motor Input frequency range: DC to 50kHz Minimum pulse width: 10µs. High level duty: 40 to 60%	Rising edge in Mode C = 1 Rising and falling edge in Mode C = 0
Mode A	12	Sets excitation mode	See table listed below
Mode B	13	Sets excitation mode	See table listed below
Mode C	18	Sets excitation mode	See table listed below
TU	22	Sets excitation mode. Switches 2-3 phase excitation of step current to rectangular current. More effective in increasing torque than in lowering vibration of motor	See table listed below
Hold	14	Temporarily holds the motor in a state	0
CW/CCW	15	Switches the rotational direction of the motor	1 = CW, 0 = CCW
Enable	16	Turns OFF all of the driving MOSFET	0
Reset	17	System reset Make sure to input a reset signal of 10µs or mor	0
MOI	20	Monitors the number of revolution of the motor	Outputs 1 pulse of a high level signal per one cycle of phase current
Vref	10	Sets the peak value of the motor current set at 0.63V per 1A	Maximum value 0.5 × VCC2 (4A max)

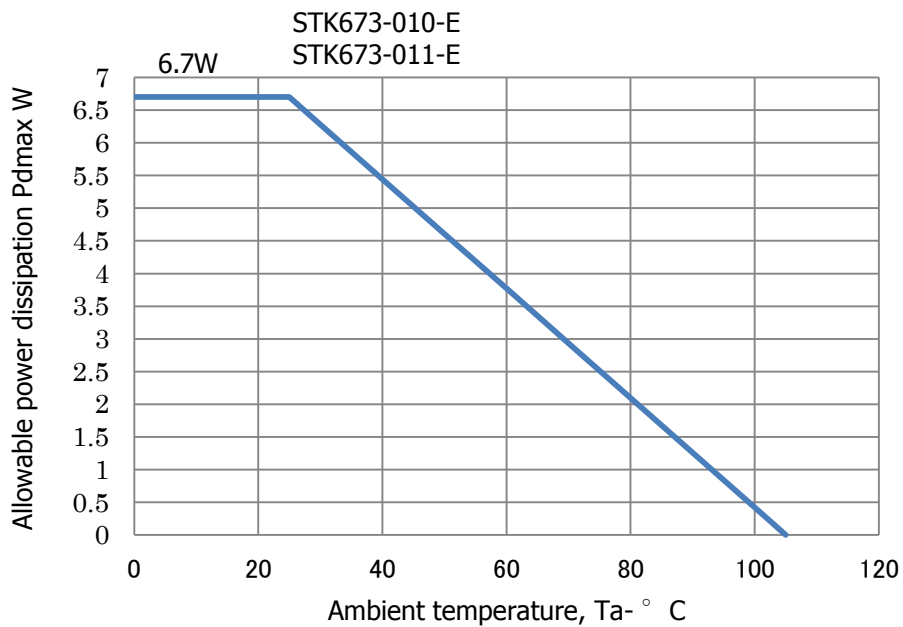
Substrate Specifications (Substrate recommended for operation of STK673-010(011-E))

Size : 85mm × 95mm × 1.6mm 1-layer board
 Material : Phenol



Copper side (35μ)

Allowable power dissipation(Reference value)



Evaluation board

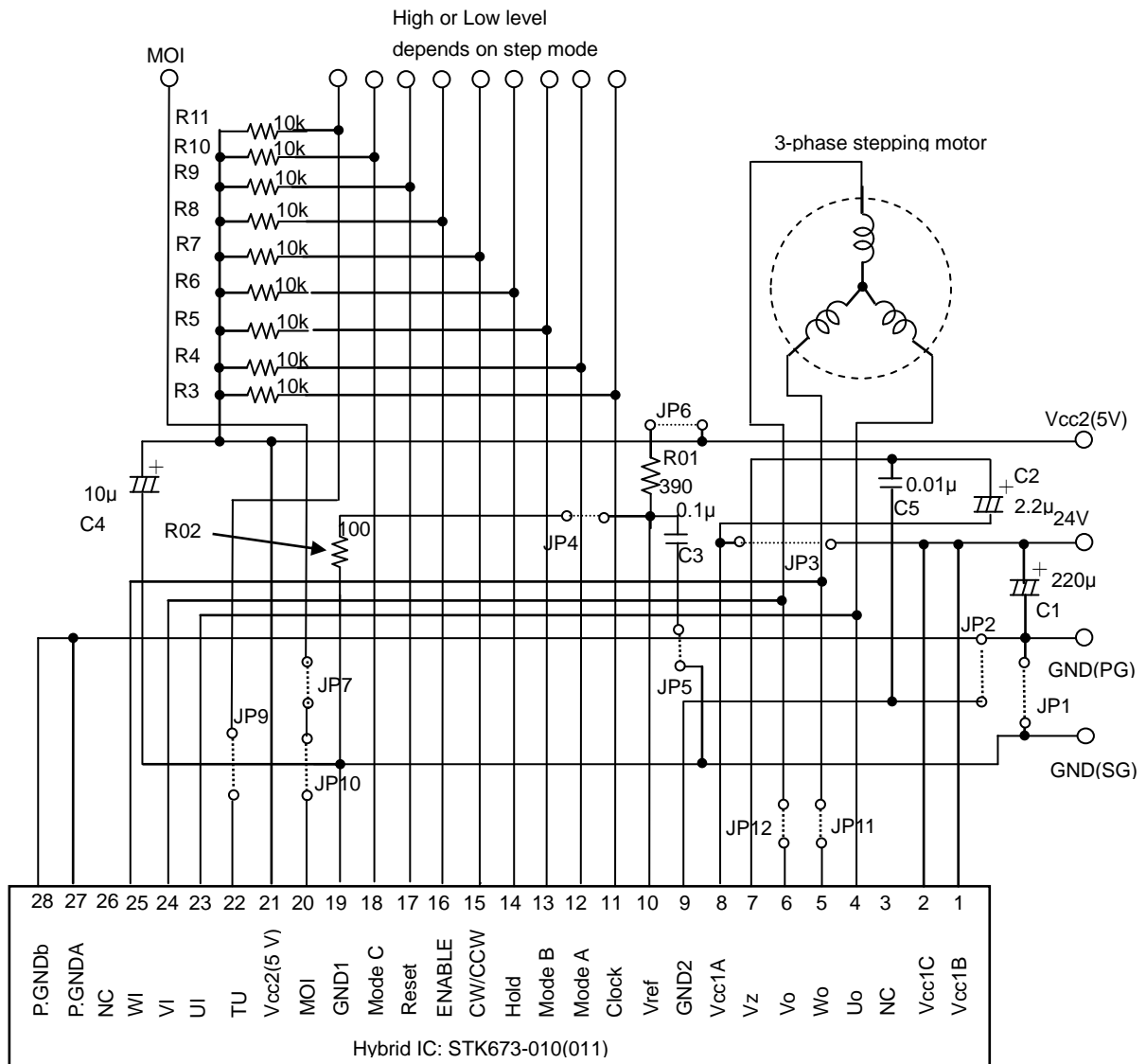
Bill of Materials for STK673-010-E (011-E) Evaluation Board

Designator	Quantity	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number	Substitution Allowed	Lead Free
C1	1	Vcc1 Bypass Capacitor	220 μ F /50V	\pm 20%		SUN ELECTRONICS	50ME220CA	YES	YES
C2	1	Charge Pump Capacitor	2.2 μ F /50V	\pm 20%		SUN ELECTRONICS	50ME2R2CA	YES	YES
C3	1	Vref stabilization Capacitor	0.1 μ F /50V	\pm 10%		Panasonic	ECQV1H104JL2	YES	YES
C4	1	Vcc2 Bypass Capacitor	10 μ F /50V	\pm 20%		SUN ELECTRONICS	50ME10CA	YES	YES
C5	1	Vcc1 Bypass Capacitor	0.01 μ F /50V	\pm 10%		Panasonic	ECQV1H103JL2	YES	YES
R01	1	Resistor to set Vref		\pm 1%		AKAHANE ELECTRONICS	RN14S****FK	YES	YES
R02	1	Resistor to set Vref		\pm 1%		AKAHANE ELECTRONICS	RN14S****FK	YES	YES
R03 to R11	9	Pull-up Resistor	10 k Ω	\pm 5%		AKAHANE ELECTRONICS	RN14S103JK	YES	YES
HIC	1	Hybrid IC				SANYO semiconductor	STK673-010-E STK673-011-E	NO	YES
CN	1	Vertical Header				MOLEX	5045-03A	YES	YES
Slide swich	1	Dip slide swich				OMRON	A6T-0104	YES	YES
JP1-7, 9-12	11	Jumper				Mac-Eight	JR-4	YES	YES

Notes: R01 and R02 are used to Vref for current setting. Therefore their value do not mention on this table.

Caution: JP8 and 13 do not implement a part.

Evaluation Circuit



Notes

Heat sink size is used in more than STK673-010-E IOH=1.8A:

100mm X 40mm X 2.0mm Al plate (no surface finish)

The Tc temperature should be checked in the center of the metal surface of the product package.

Evaluation Board Manual

[Supply Voltage] Vcc1 (10 to 30V): Power Supply for stepping motor
 Vref (0 to 2.5V) : Const. Current Control for Reference Voltage
 Vcc2 (5V) : Power Supply for internal logic IC

[Slide Switch State] ON Side: Low (GND)
 OFF Side: High (5V pull up resistors)

[Operation Guide]

1. Motor Connection:
 Connect the stepping motor to U,V,W.
2. Initial Condition Setting:
 Set "ON" the slide switch Reset, and set "ON or OFF" ModeA to ModeB depend on step mode, and set "ON or OFF" CW/CCW, and set low clock.
3. Power Supply:
 At first, supply DC voltage to Vcc2, and VREF.
 Next, supply DC voltage to Vcc1.
4. Ready for Operation from Standby State:
 Turn "OFF" the slide switch Reset.
5. Motor Operation: Input the Clock signal into the terminal Clock.

[Setting the motor current]

The motor current IOH is set by the Vref voltage on the hybrid IC pin 10. The following formula gives the relationship between IOH and Vref.

STK673-010-E (-011-E)

$$IO\ peak = Vref \div K \quad K = 0.63 (V/A)$$

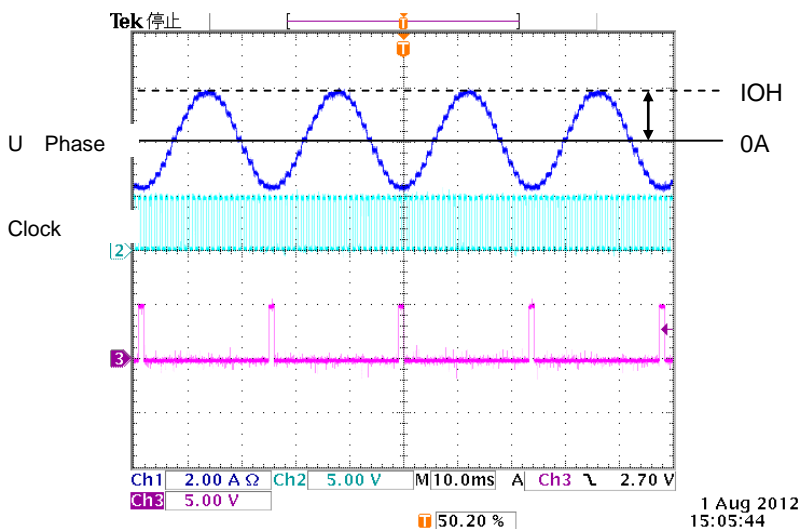
Where $Vref \leq 0.5 \times VCC2$

$$Vref = VCC2 \times Rox \div (R01 + Rox)$$

$$Rox = (R02 \times 4.0k\Omega) \div (R02 + 4.0k\Omega)$$

In case of IOH=1.7A, Vref=1.7 × 0.63=1.071V

Wave of IOH



Notes in design**(1) Allowable operating range**

Operation of this product assumes use within the allowable operating range. If a supply voltage or an input voltage outside the allowable operating range is applied, an overvoltage may damage the internal control IC or the MOSFET.

If a voltage application mode that exceeds the allowable operating range is anticipated, connect a fuse or take other measures to cut off power supply to the product.

(2) Input pins

If the input pins are connected directly to the PC board connectors, electrostatic discharge or other overvoltage outside the specified range may be applied from the connectors and may damage the product. Current generated by this overvoltage can be suppressed to effectively prevent damage by inserting 100Ω to 1kΩ resistors in lines connected to the input pins.

Take measures such as inserting resistors in lines connected to the input pins.

(3) Power connectors

If the motor power supply VCC is applied by mistake without connecting the GND part of the power connector when the product is operated, such as for test purposes, an overcurrent flows through the Vcc1 decoupling capacitor, C1, to the parasitic diode between the Vcc2 of the internal control IC and GND, and may damage the power supply pin block of the internal control IC.

(4) Input signal lines

Do not use an IC socket to mount the driver, and instead solder the driver directly to the PC board to minimize fluctuations in the GND potential due to the influence of the resistance component and inductance component of the GND pattern wiring.

To reduce noise caused by electromagnetic induction to small signal lines, do not design small signal lines (sensor signal lines, and 5V power supply signal lines) that run parallel in close proximity to the motor output line U (Pin 4,23), V(Pin 6,24),W (Pin 5,25) phases.

- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of August, 2012. Specifications and information herein are subject to change without notice.