Rockwell

R23256 AND R23257
256K (32K × 8) STATIC ROMS

PRELIMINARY

DESCRIPTION

The R23256 and R23257 are 262,144-bit static Read-Only Memories (ROMs), organized as 32,768 eight-bit bytes, that offer maximum access times of 200 nanoseconds. These ROMs are in industry-standard 28-pin, dual in-line packages, and are available in ceramic or low-cost plastic. These fully-static 256K-bit ROMs are compatible with industry standard microprocessors and are designed for installation in systems requiring high-performance large-capacity storage and simple interfacing.

The R23256 and R23257 ROMs operate totally asynchronously, and require no clock input. These ROMs offer TTL input and output levels with a minimum noise immunity of 0.4 volts. The R23256 has a Chip Select (S1/$\overline{S1}$) input which allows two of these ROMs to be wire-ORed without external decoding. The R23256 also has an Output Enable (G/$\overline{G}$) input to eliminate bus contention in multiple-bus systems. The R23256 has two Chip Select (S1/$\overline{S1}$ and S2/$\overline{S2}$) inputs which allow up to four of these ROMs to be wire-ORed without external decoding.

The chip enable input ($\overline{E}$) functions as a chip enable with power down standby mode. When this line is high the chip is disabled and enters a low power standby state.

The R23256 is pin compatible with the 2764 EPROM and the R23257 is pin compatible with the 2564 EPROM, which eliminates the need to redesign printed circuit boards for volume mask programmable ROMs after prototyping with EPROMs.

FEATURES

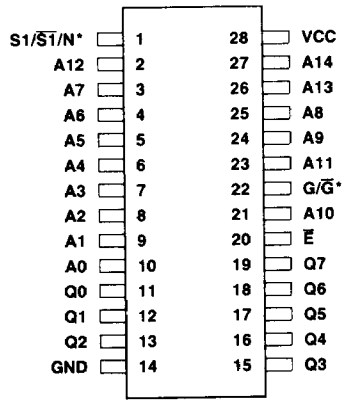
- 32,768 × 8 organization
- Access times: 200 ns, 250 ns, and 450 ns (max)
- Low max. power dissipation: 400 mW (active), 100 mW (standby)
- Drives two TTL loads and 100 pF
- Single +5V ±10% power supply
- Totally static operation, no input clock required
- Completely TTL compatible
- Mask-programmable chip select/output enable lines
- Tri-state outputs for memory expansion
- R23256 pin compatible with 2764 EPROM
- R23257 pin compatible with 2564 EPROM

ORDERING INFORMATION

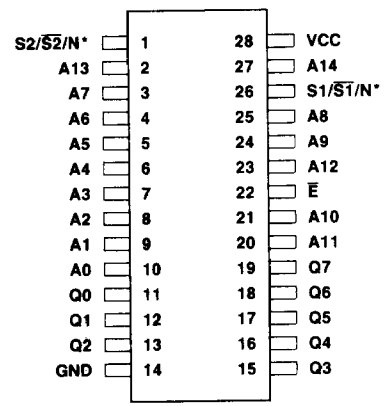
Part Number: R23256 _ _ _ _
R23257 _ _ _ _

- Package:
  - C = Ceramic
  - P = Plastic
- Temperature Range:
  - No letter = 0°C to +70°C
  - E = −40°C to +85°C
- Access Time (Max):
  - 20 = 200 ns
  - 25 = 250 ns
  - 45 = 450 ns

Note: Submit ROM codes using Rockwell ROM Code Order Form, Order No. 2137.



R23256



R23257

*Mask-programmable option.
N = No effect on selection logic, however, voltage greater than logic level shall not be applied.

R23256 and R23257 Pin Configurations

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ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Input Voltage	V_{IN}	−0.5 to +7.0	Vdc
Output Voltage	V_{OUT}	−0.5 to +7.0	Vdc
Temperature under Bias Commercial Industrial	T_A	 −10 to +80 −50 to +95	°C
Storage Temperature	T_{STG}	−65 to +150	°C
Power Dissipation	P	1.0	W

***NOTE**: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

V_{CC} = 5.0V ±10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ	Max	Units	Test Conditions
V_{OH}	Output HIGH Voltage	2.4		V_{CC}	V	V_{CC} = 4.5V, I_{OH} = −1.0 mA
V_{OL}	Output LOW Voltage			0.4	V	V_{CC} = 4.5V, I_{OL} = 3.2 mA
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
I_{LI}	Input Load Current			10	μA	V_{CC} = 5.5V, 0V ≤ V_{IN} ≤ 5.5V
I_{LO}	Output Leakage Current			±10	μA	V_{CC} = 5.5V, chip deselected, V_{OUT} = +0.4V to V_{CC}
I_{CC}	Power Supply Current, Active			80	mA	V_{CC} = 5.5V
I_{SB}	Power Supply Current, Standby			20	mA	$\overline{E}$ = V_{IH}
C_I	Input Capacitance[1]			7	pF	V_{CC} = 5.0V, chip deselected, pin under test at 0V, T_A = 25°C f = 1 MHz.
C_O	Output Capacitance[1]			10	pF	

Notes:
1. This parameter is periodically sampled and is not 100% tested.

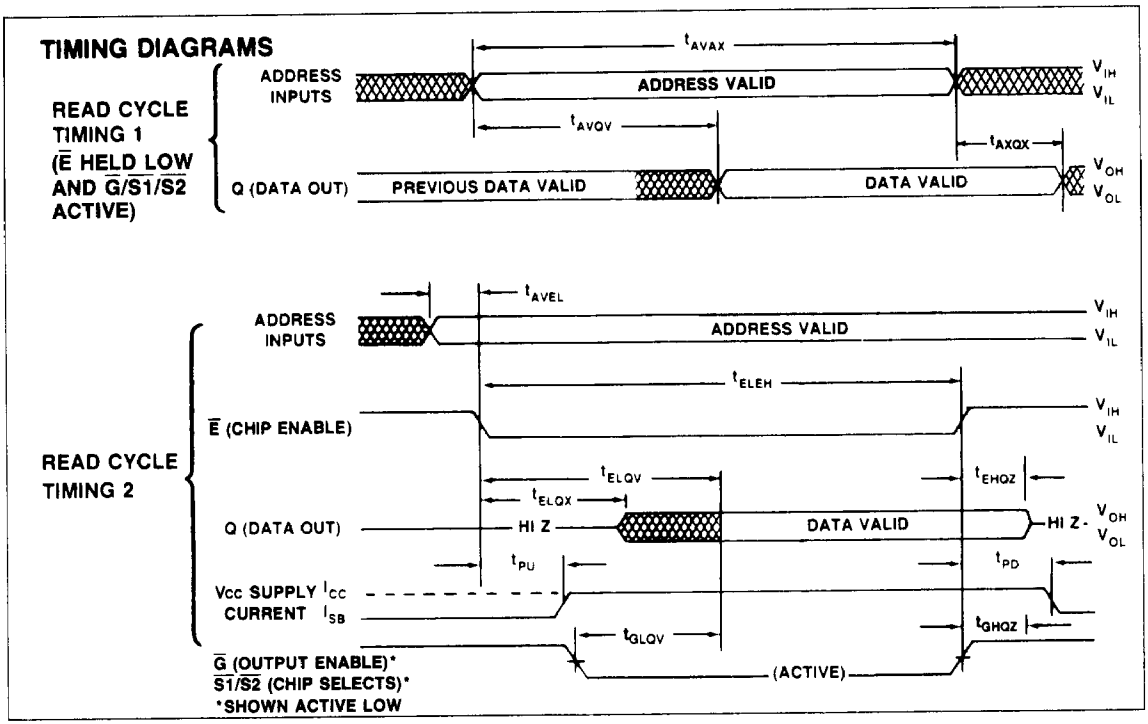
AC CHARACTERISTICS

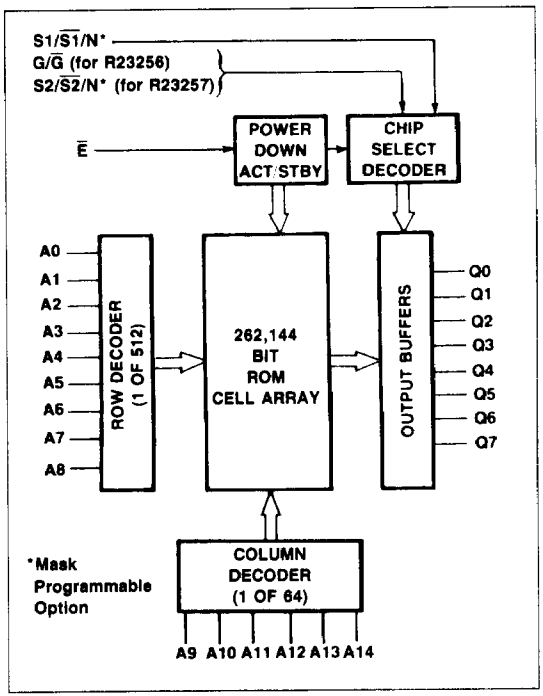
V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	R23256-20 R23257-20		R23256-25 R23257-25		R23256-45 R23257-45		Units
		Min	Max	Min	Max	Min	Max	
t_{AVAX}	Address Valid to Address Don't Care	200		250		450		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	200		250		450		ns
t_{AVQV}	Address Valid to Output Valid (t_{ACC})(Access)		200		250		450	ns
t_{ELQV}	Chip Enable Low to Output Valid (Access)		200		250		450	ns
t_{AXQX}	Address Change to Output Invalid (t_{OH})	10		10		10		ns
t_{ELQX}	Chip Enable Low to Output Active (t_{CO})	10		10		10		ns
t_{EHQZ}	Chip Enable High to Output High Z (t_{DF})		85		100		150	ns
t_{PU}	Chip Selection to Power Up Time	0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time		85		100		150	ns
t_{AVEL}	Address Setup to Chip Enable Low	0		0		0		ns
t_{GLQV}	Output Enable Low to Output Valid	10	85	10	100	10	150	ns
t_{GHQZ}	Output Enable High to Output High Z		85		100		150	ns

Notes:
1. Test Conditions: Output Load: 2 TTL loads and 100 pF; Input transition time: 20 ns; Timing reference levels: Input: 1.5V; Output: 0.8V, 2.0V.
2. Add 20 ns for extended temperature devices (−40°C to +85°C).
3. $\overline{G}$ may be delayed up to $t_{AVQV} - t_{GLQV}$ after the falling edge of $\overline{E}$ without impact on t_{AVQV}. Data is available at the Q outputs after a delay of t_{GLQV} from the falling edge of $\overline{G}$, provided that $\overline{E}$ has been low (V_{IL}) and addresses have been valid for at least $t_{AVQV} - t_{GLQV}$.
4. t_{GHQZ} and t_{EHQZ} are specified from $\overline{G}$ or $\overline{E}$ whichever occurs first.

TIMING DIAGRAMS

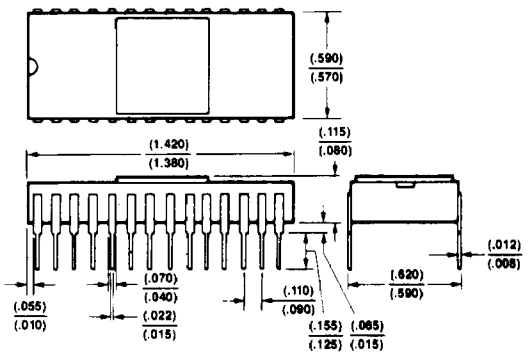




R23256 and R23257 Block Diagram

PACKAGE DIMENSIONS

28-PIN CERAMIC DIP



28-PIN PLASTIC DIP