MPM38111

Dual 1A, 2.7V-6V, Power Module, Synchronous, Step-Down Converter with Integrated Inductors

The Future of Analog IC Technology

DESCRIPTION

The MPM38111 is a dual-channel DC/DC module. The module includes a monolithic, step-down, switch-mode converter with built-in, internal power MOSFETs and inductors. The MPM38111 is designed to simplify power system design and provide ease of use.

The MPM38111 operates from a 2.7V to 6V input, generates an output voltage as low as 0.608V, and has a 45µA quiescent current, making it ideal for powering portable equipment that run on a single-cell Lithium-ion (Li+) battery. The MPM38111 integrates dual, 85mΩ, high-side switches and 40mΩ synchronous rectifiers for high efficiency without an external Schottky diode. Peak-current-mode control and internal compensation limit the minimum number of readily available external components. Full protection features include cycle-by-cycle current limiting and thermal shutdown.

The MPM38111 is available in a small, surface-mounted, QFN-14 (4mmx4mmx1.6mm) package.

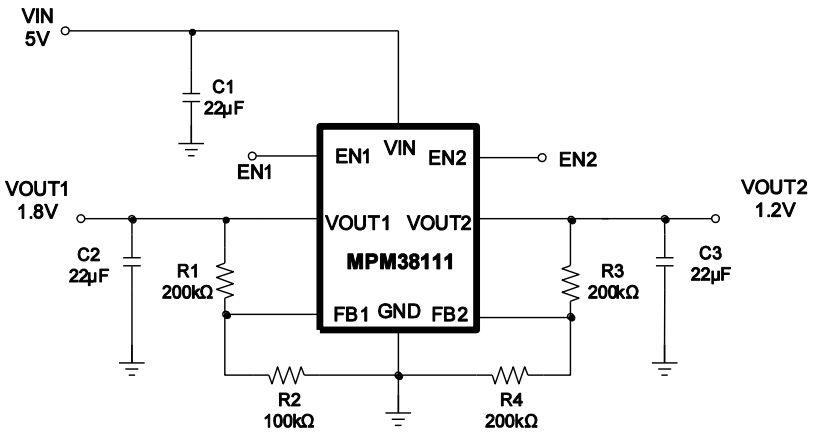
FEATURES

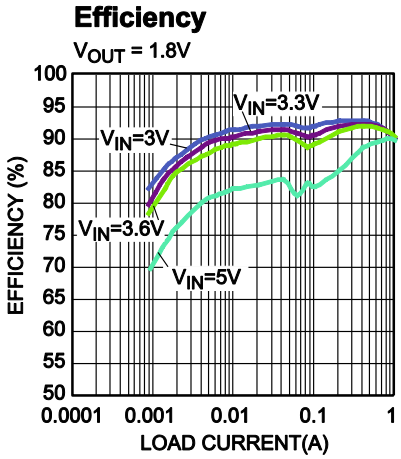
- Dual 1A Output Current
- >93% Peak Efficiency
- >80% Light-Load Efficiency
- Ultra-Low I_Q: 45µA
- 85mΩ and 40mΩ Internal Power MOSFET
- Wide 2.7V to 6V Operating Input Range
- Default 1MHz Switching Frequency
- 180° Phase-Shifted Operation
- 100% Duty Cycle Operation
- Cycle-by-Cycle Over-Current Protection (OCP)
- Short-Circuit Protection (SCP) with Hiccup Mode
- Thermal Shutdown
- Available in a Small QFN-14 (4mmx4mmx1.6mm) Package

APPLICATIONS

- Optical Modules
- Industrial Products
- IoT Devices
- LDO Replacement
- Medical Devices

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MPM38111GR	QFN-14 (4mmx4mmx1.6mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MPM38111GR–Z)

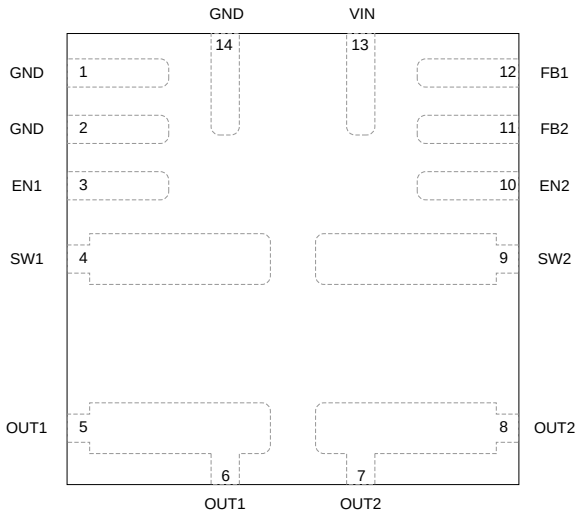
TOP MARKING

MPSYWW
M38111
LLLLLL
M

MPS: MPS prefix
Y: Year code
WW: Week code
M38111: Product code of MPM38111GR
LLLLLL: Lot number
M: Module

PACKAGE REFERENCE

TOP VIEW



QFN-14 (4mmx4mmx1.6mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) 6.5V
V_{SW} ..... -0.3V (-5V for <10ns) to 6.5V (9V for <10ns)
All other pins ..... -0.3V to +6.5V
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Continuous power dissipation (T_A = +25°C) (2) 2.8W

Recommended Operating Conditions (3)

Supply voltage (VIN) ..... 2.7V to 6V
Output voltage (V_{OUT}) ..... 0.608V to VIN
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN-14 (4mmx4mmx1.6mm)	44	9	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JEDEC51-7, 4 layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = EN = 3.6V, T_J = -40°C to +125°C(5), typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameters	Symbol	Condition		Min	Typ	Max	Units
Feedback voltage	V_{FB}	2.7V ≤ V_{IN} ≤ 6V	T_J = 25°C	-2%	0.608	2%	V
			T_J = -40°C to 125°C	-3%	0.608	3%	
Feedback bias current	$I_{BIAS(FB)}$	V_{FB} = 0.63V			±10	50	nA
P-FET switch on resistance	$R_{DS(ON)\_P}$	V_{IN} = 5V			85		mΩ
N-FET switch on resistance	$R_{DS(ON)\_N}$	V_{IN} = 5V			40		mΩ
Inductor DC resistance	L_{DCR}				45		mΩ
Inductor inductance(7)	L				1		µH
Inductor rated DC current(7)	I_{SAT}	ΔL/L = 30%			3.3		A
	I_R	ΔT = 40°C			2.7		A
Switch leakage current		V_{EN} = 0V, V_{IN} = 6V, V_{SW} = 0V and 6V, T_J = 25°C		-1	0	1	µA
P-FET peak current limit	I_{LIMIT_HS}	Sourcing, D = 40%		2.0			A
Switching frequency	f_{SW}	T_J = -40°C to +125°C(5)		-20%	1000	+20%	kHz/%
Max duty cycle					100		%
Minimum off time	T_{MIN_OFF}				100		ns
Minimum on time(6)	T_{MIN_ON}				90		ns
Internal soft-start time	T_{SS_ON}				0.5		ms
IN under-voltage lockout threshold		Rising edge		2.4	2.5	2.65	V
IN under-voltage lockout threshold hysteresis					300		mV
EN input logic high voltage		-40°C ≤ T_J ≤ +125°C		1.2			V
EN input logic low voltage		-40°C ≤ T_J ≤ +125°C				0.4	V
Supply current (shutdown)	I_{SD}	V_{EN} = 0V			0	1	µA
Supply current (quiescent)	I_Q	V_{IN} = 3.6V, V_{EN} = 2V, V_{FB} = 0.65V		35	45	55	µA
Thermal shutdown threshold(6)		Hysteresis = 30°C			160		°C
Phase shift					180		degree

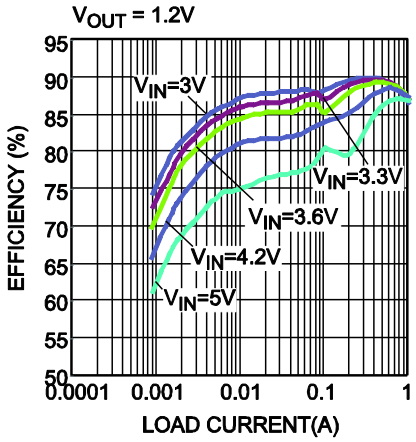
NOTES:

5) Not tested in production, guaranteed by over-temperature correlation.
6) Guaranteed by engineering sample characterization.
7) Not tested in production, guaranteed by the inductor's datasheet.

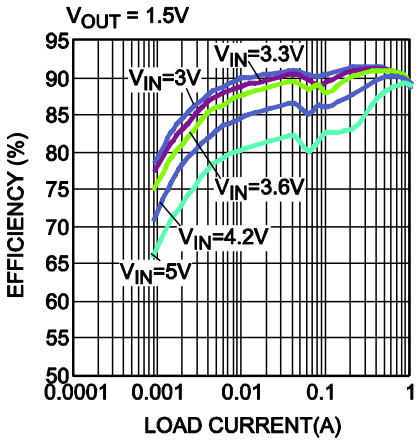
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L = 1µH, C_{OUT1} = C_{OUT2} = 22µF, T_A = 25°C, unless otherwise noted.

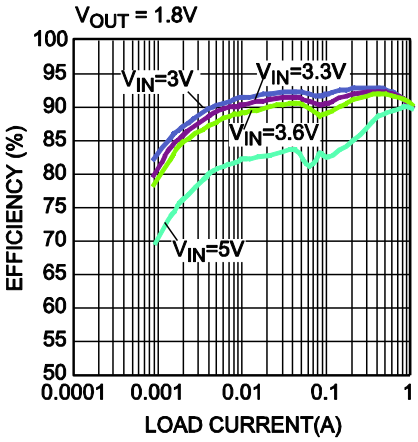
Efficiency



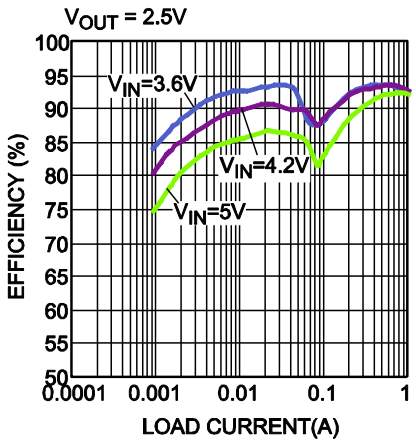
Efficiency



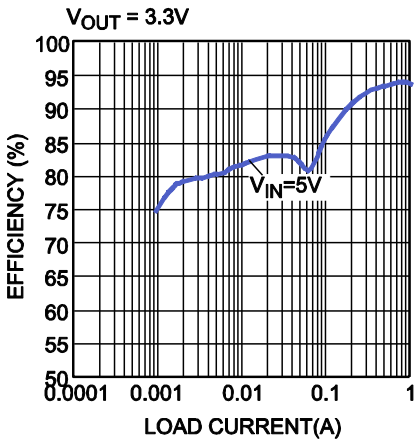
Efficiency



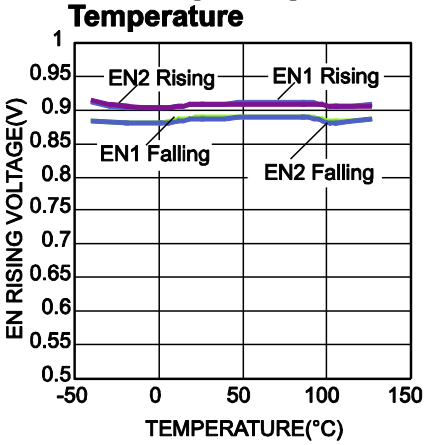
Efficiency



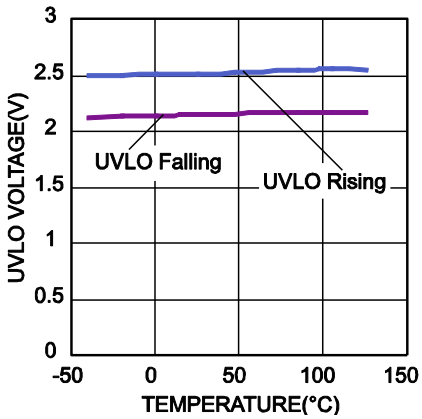
Efficiency



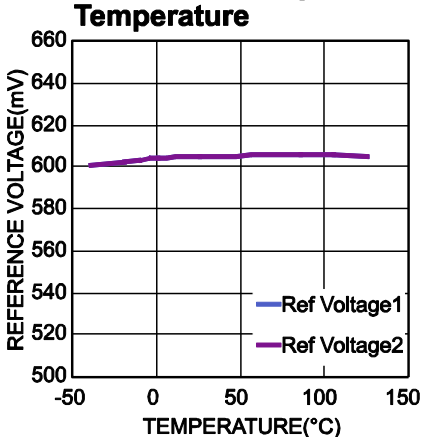
EN Rising Voltage vs. Temperature



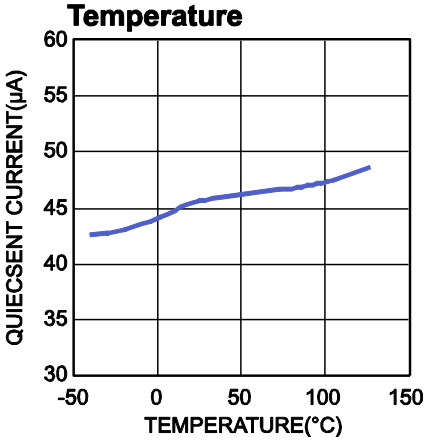
UVLO vs. Temperature



Reference Voltage vs. Temperature



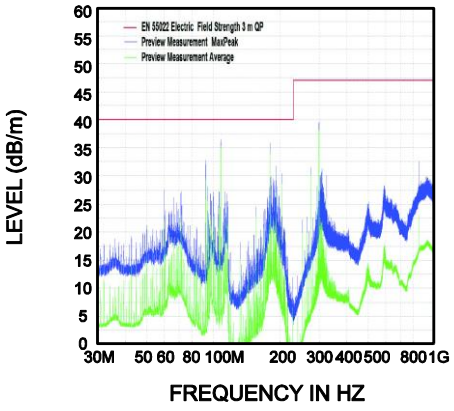
Quiescent Current vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

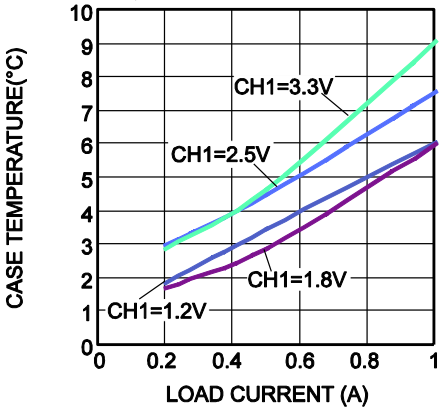
V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L = 1µH, C_{OUT1} = C_{OUT2} = 22µF, T_A = 25°C, unless otherwise noted.

Radiated EMI



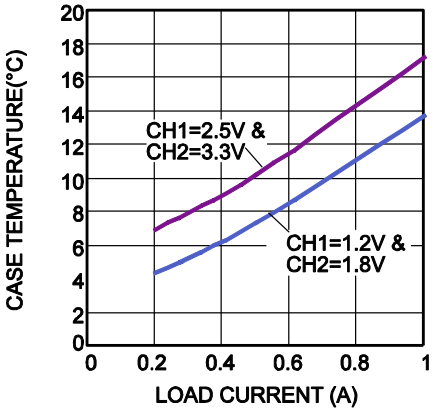
Case Temperature Rise

Single Channel

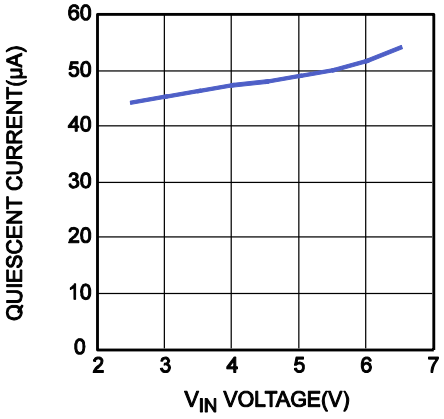


Case Temperature Rise

Both Channel

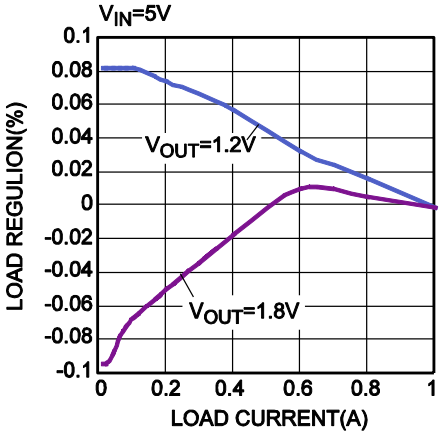


Quiescent Current vs. VIN



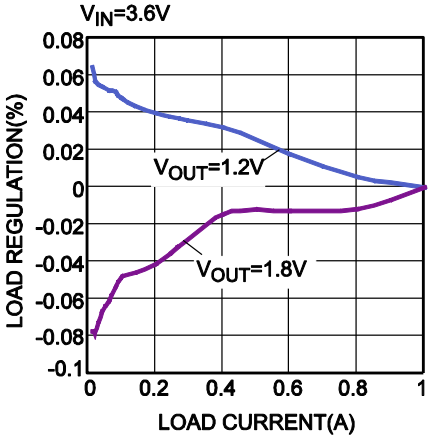
Load Regulation

V_{IN}=5V



Load Regulation

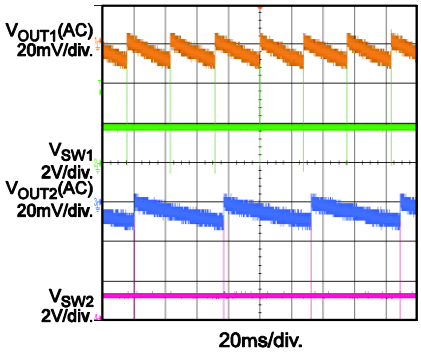
V_{IN}=3.6V



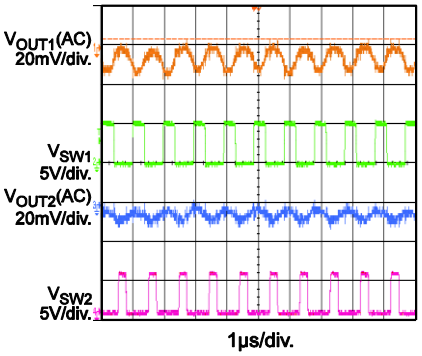
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L = 1µH, C_{OUT1} = C_{OUT2} = 22µF, T_A = 25°C, unless otherwise noted.

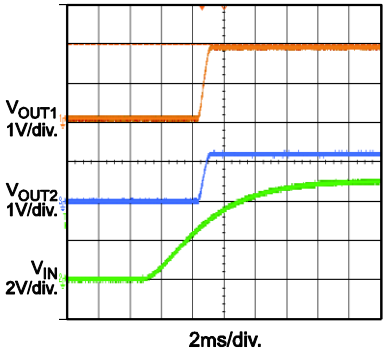
Output Ripple
I_{OUT1} =I_{OUT2} = 0A



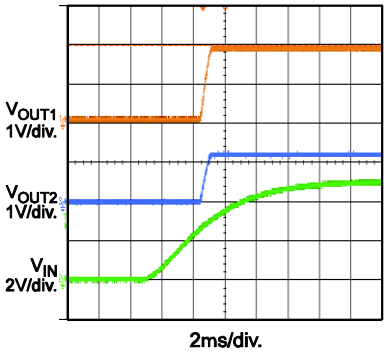
Output Ripple
I_{OUT1} =I_{OUT2} = 1A



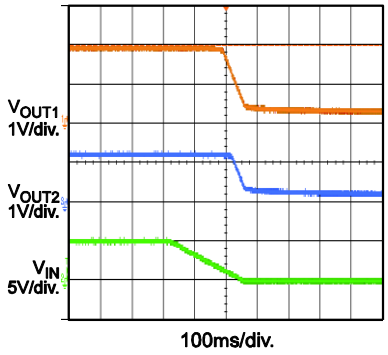
V_{IN} Power Up without Load
I_{OUT1} =I_{OUT2} = 0A



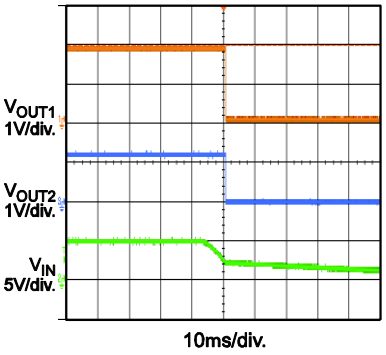
V_{IN} Power Up with 1A Load
I_{OUT1} =I_{OUT2} = 1A



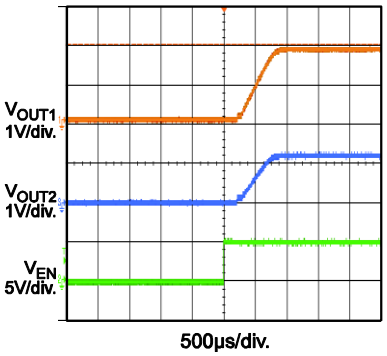
V_{IN} Power Down without Load
I_{OUT1} =I_{OUT2} = 0A



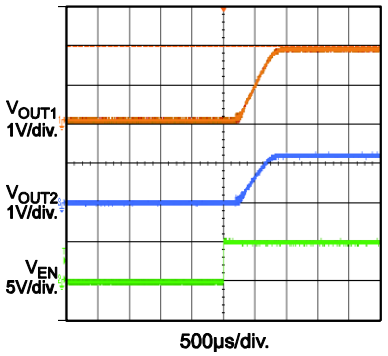
V_{IN} Power Down with 1A Load
I_{OUT1} =I_{OUT2} = 1A



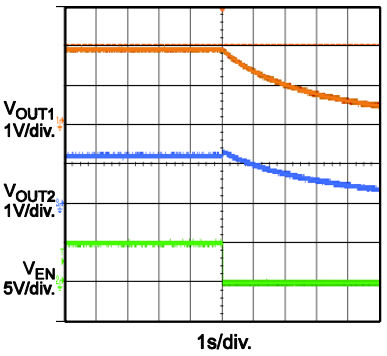
EN On without Load
I_{OUT1} = I_{OUT2} =0A



EN On with 1A Load
I_{OUT1} = I_{OUT2} =1A



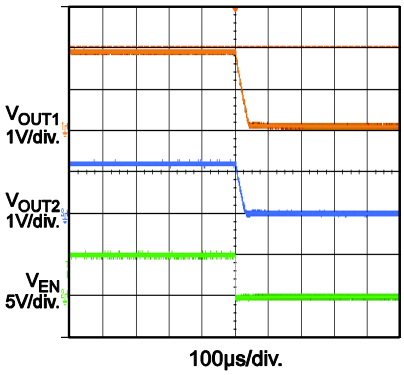
EN Down without Load
I_{OUT1} = I_{OUT2} =0A



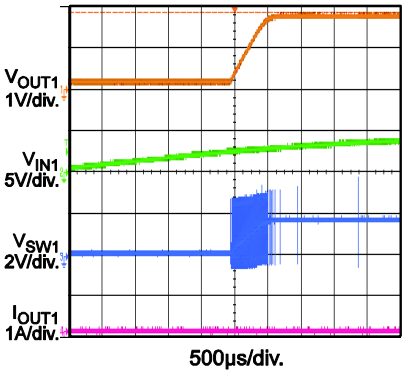
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT1} = 1.8V, V_{OUT2} = 1.2V, L = 1µH, C_{OUT1} = C_{OUT2} = 22µF, T_A = 25°C, unless otherwise noted.

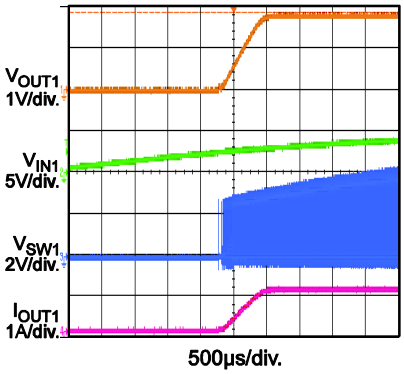
EN Down with 1A Load
I_{OUT1} = I_{OUT2} =1A



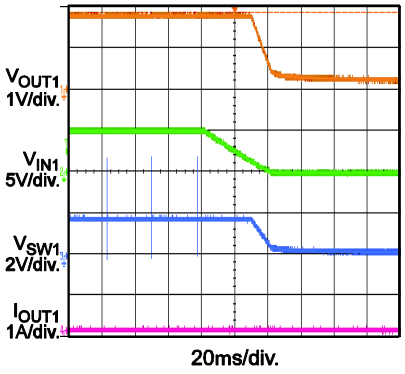
V_{IN} Power On without Load
I_{OUT1} = I_{OUT2} =0A



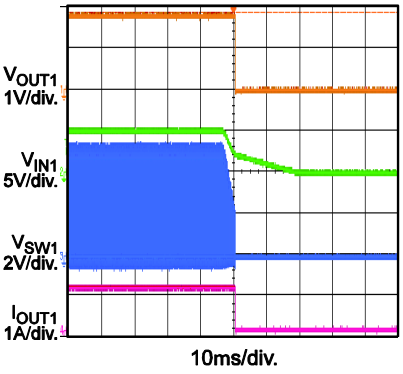
V_{IN} Power On with 1A Load
I_{OUT1} =1A, I_{OUT2} =0A



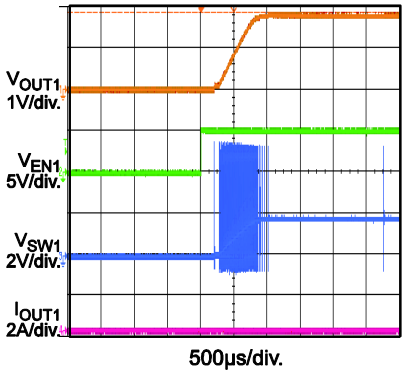
V_{IN} Power Down without Load
I_{OUT1} = I_{OUT2} =0A



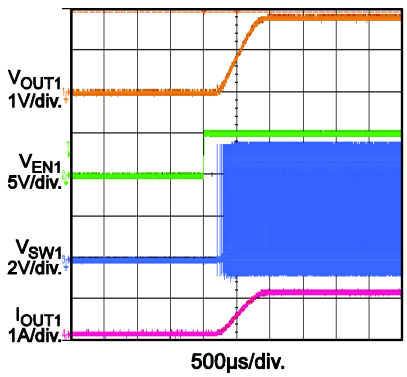
V_{IN} Power Down with 1A Load
I_{OUT1} =1A, I_{OUT2} =0A



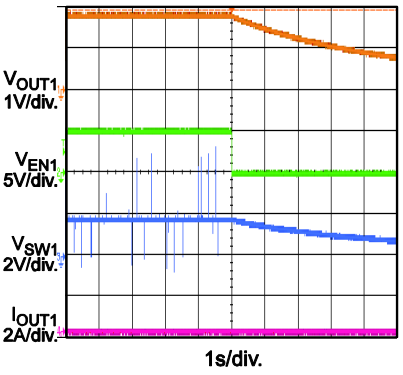
Enable On without Load
I_{OUT1} = I_{OUT2} =0A



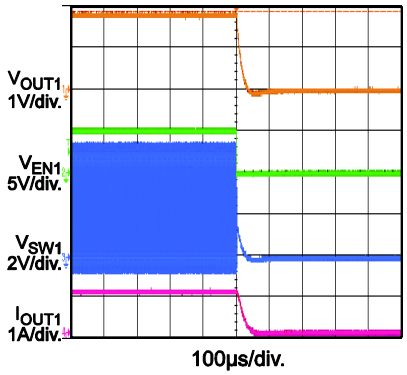
Enable On with 1A Load
I_{OUT1} =1A, I_{OUT2} =0A



Enable Down without Load
I_{OUT1} = I_{OUT2} =0A



Enable Down with 1A Load
I_{OUT1} =1A, I_{OUT2} =0A



PIN FUNCTIONS

Pin #	Name	Description
1, 2, 14	GND	**Power ground.**
3	EN1	**Channel 1 enable.**
4	SW1	**Switch node.** SW1 connects to the channel 1 internal high-side and low-side power MOSFETs. SW1 also connects to the inductor.
5, 6	OUT1	**Channel 1 power output.**
7, 8	OUT2	**Channel 2 power output.**
9	SW2	**Switch node.** SW2 connects to the channel 2 internal high-side and low-side power MOSFETs. SW2 also connects to the inductor.
10	EN2	**Channel 2 enable.**
11	FB2	**Feedback 2.** FB2 is the error amplifier input. Connect FB2 to the tap of an external resistor divider between the output and GND. FB2 sets the regulation voltage.
12	FB1	**Feedback 1.** FB1 is the error amplifier input. Connect FB1 to the tap of an external resistor divider between the output and GND. FB1 sets the regulation voltage.
13	VIN	**Input supply.** VIN requires a decoupling capacitor to ground to reduce switching spikes.

BLOCK DIAGRAM

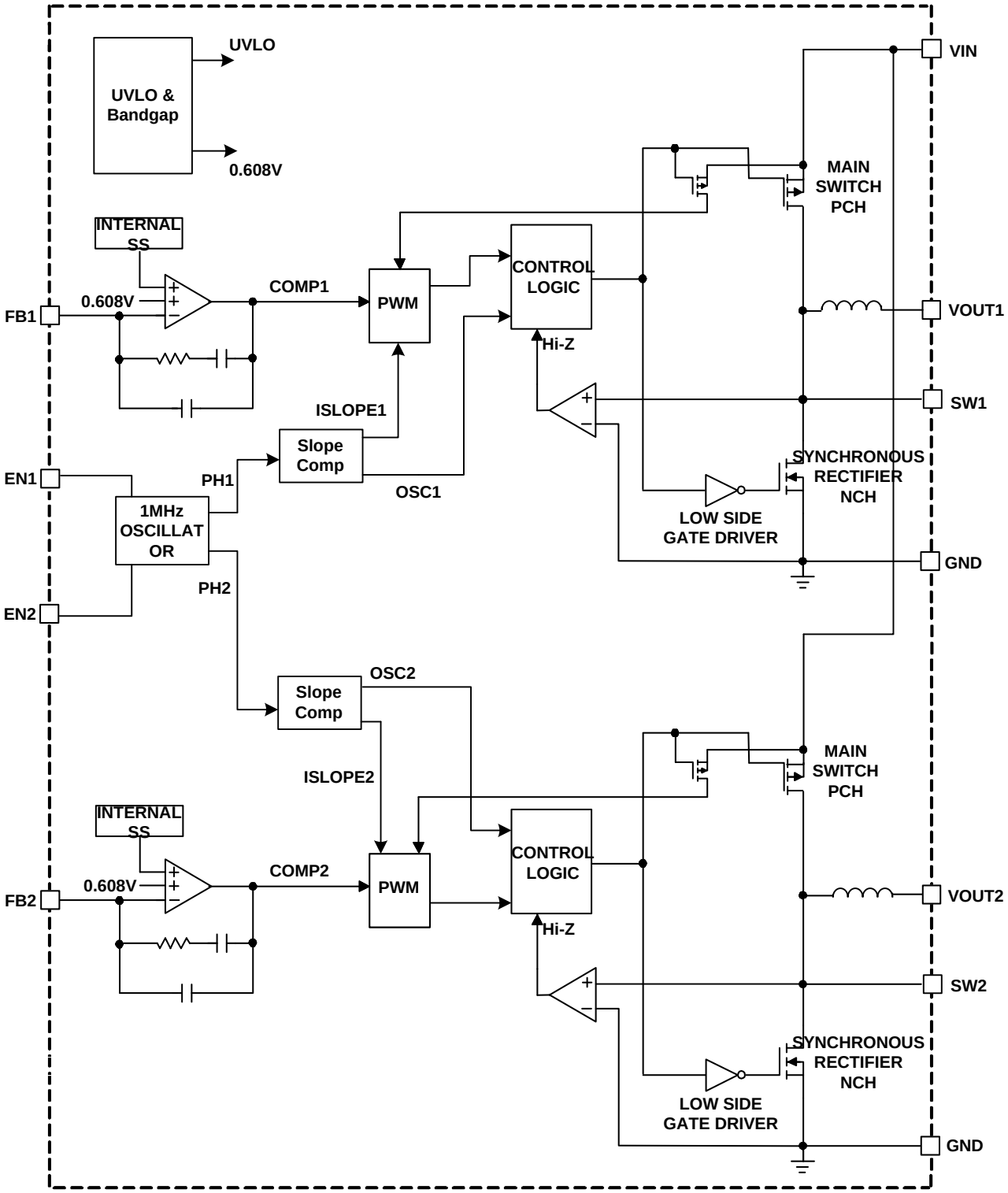


Figure 1: Functional Block Diagram

OPERATION

The MPM38111 is a dual-channel DC/DC module that includes a monolithic, step-down, switch-mode converter with built-in, internal power MOSFETs and inductors. Both channels have peak-current mode with internal compensation for faster transient response and cycle-by-cycle current limit.

The MPM38111 is optimized for low-voltage, space-constrained applications where efficiency and small size are critical.

180° Phase Shift

By default, the MPM38111's two channels operate at a 180° phase shift to reduce input current ripple (see Table 1). The smaller current ripple allows for use of a smaller input bypass capacitor. In continuous conduction mode (CCM), two internal clocks control the switching. The high-side MOSFET (HS-FET) turns on at the corresponding clock's rising edge.

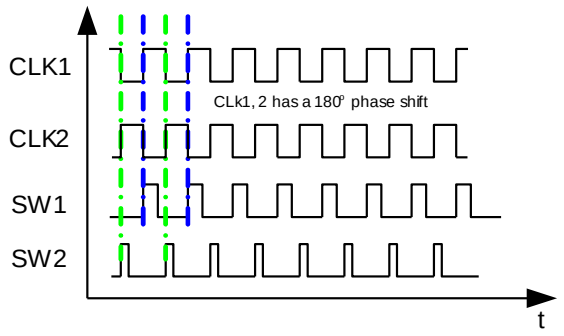


Figure 2: Clock/Switching Timing

The switching frequency drops below 1MHz with a fixed off time when operating at a low dropout voltage. Once the input voltage recovers to a high value, switching for PWM mode resumes normally and synchronizes with the master oscillator for phase-shifted operation.

Light-Load Operation

In light loads, the MPM38111 uses a proprietary control scheme to save power and improve efficiency (see Table 1). The MPM38111 turns off the low-side switch when the inductor current starts to reverse, and then works in discontinuous conduction mode (DCM) operation. When either channel enters DCM or low-dropout operation, it will not be controlled by the internal 1MHz oscillator.

Table 1: Modes of Operation

	Condition		Mode	
	CH1	CH2	CH1	CH2
1	Heavy load		1MHz CCM	1MHz CCM,180° phase
2	Light load		DCM	DCM
3	Low dropout		Fixed off time	Fixed off time
4	Heavy load	Light load	0.95MHz CCM	DCM
5	Light load	Heavy load	DCM	0.95MHz CCM
6	Heavy load	Low dropout	0.95MHz CCM	Fixed off time
7	Low dropout	Heavy load	Fixed off time	0.95MHz CCM
8	Light load	Low dropout	DCM	Fixed off time
9	Low dropout	Light load	Fixed off time	DCM

DCM occurs only after the low-side switch is turned off by the ZCD circuit. Considering the ZCD circuit propagation time, the typical delay is 50ns. This means that the inductor current continues falling after ZCD is triggered during this delay. If the inductor current falling slew rate is fast (V_{OUT} is high or close to VIN), the low-side MOSFET (LS-FET) is turned off at the moment the inductor current is negative. This prevents the MPM38111 from entering DCM operation.

If DCM operation is required, the off time of the LS-FET in CCM should be longer than 100ns. For example, if VIN is 3.4V, and V_{OUT} is 3.3V, then the off time in CCM is about 30ns. It is difficult to enter DCM at light load.

Soft Start (SS)

The MPM38111 has a built-in soft start (SS) that ramps up the output voltage at a controlled slew rate to avoid overshooting at start-up. The soft-start time is about 0.5ms.

Over-Current-Protection (OCP) and Hiccup

The MPM38111 has a cycle-by-cycle over-current limit when the inductor current peak value exceeds the set current-limit threshold. The output voltage drops until V_{FB} is below the under-voltage (UV) threshold, typically 75% below the reference. Once UV is triggered, the MPM38111 enters hiccup mode to restart the

part periodically. This protection mode is especially useful when the output is dead-shorted to ground, and reduces the average short-circuit current greatly to alleviate thermal issues and protect the regulator.

De-Rating Current Operation

Figure 3 provides guidelines for the maximum allowed power loss on the IC at a certain ambient temperature. It describes the maximum allowed IC power loss when the junction temperature reaches 125°C.

For example, the application condition is V_{IN} = 5V, V_{OUT1} = 1.8V/1A, V_{OUT2} = 1.2V/1A. From the efficiency curve, if the single-channel efficiency is about 90% at 1.8V/1A and 87% at 1.2V/1A, then the total power loss is about 0.38W. Figure 3 also shows that the maximum allowable power loss is 2.1W at a 25°C ambient temperature. Since the IC power loss is less than 2.1W, the application is safe when the two channels take a 1A load at T_A = 25°C. If the IC power loss is higher than the maximum allowable value, the junction temperature is over 125°C. It is recommended to de-rate the load current or lower the ambient temperature.

The curve is based on MPS's standard evaluation board (EVB). The junction-to-ambient thermal resistance (θ_{JA}) of the MPS EVB is 47°C/W. The thermal resistance may differ with different layouts.

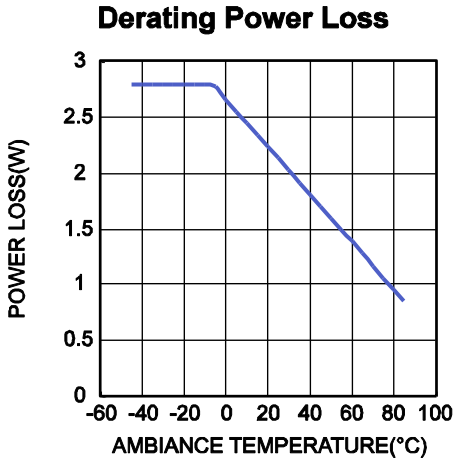


Figure 3: De-Rating Power Loss

APPLICATION INFORMATION

Output Voltage

External resistor dividers connected to the FB pins set the output voltage. The feedback resistor connected to FB1 (R1) also sets the feedback loop bandwidth (f_C).

f_C does not exceed $0.1xf_{SW}$. When using a ceramic output capacitor (C_O), set the range to 50kHz and 100kHz for optimal transient performance and good phase margin. When using an electrolytic capacitor, set the loop bandwidth no higher than a quarter of the ESR zero frequency (f_{ESR}). f_{ESR} can be calculated with Equation (1):

$$f_{ESR} = \frac{1}{2\pi \cdot R_{ESR} \cdot C_O} \quad (1)$$

Choose R1 by referring to Table 2. R2 can then be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.608V} - 1} \quad (2)$$

Table 2: Resistor Values vs. Output Voltage

V_{OUT}	R1	R2	C_{OUT} (Ceramic)
1.2V	200kΩ	200kΩ	22µF
1.5V	200kΩ	133kΩ	22µF
1.8V	200kΩ	100kΩ	22µF
2.5V	150kΩ	47.5kΩ	22µF
3.3V	120kΩ	26.7kΩ	22µF

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (3):

$$I_{C1} = I_{LOAD} x \sqrt{\frac{V_{OUT}}{V_{IN}} x (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (4):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (4)$$

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, ceramic capacitor (e.g.: 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{F_S \times C_1} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Output Capacitor

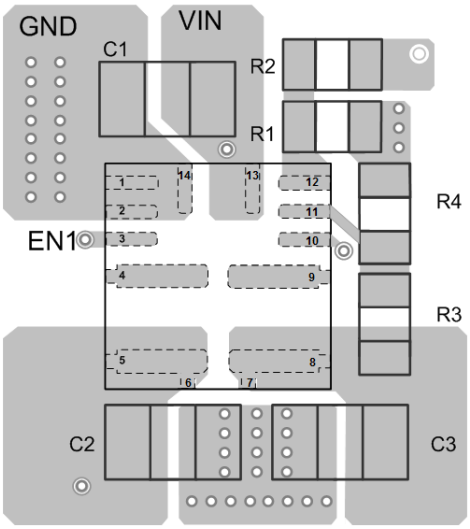
The output capacitor limits the output voltage ripple and ensures a stable regulation loop. Select an output capacitor with a low impedance at the switching frequency. Use ceramic capacitors with X5R or X7R dielectrics. Using an electrolytic capacitor may result in additional output voltage ripple thermal issues, and requires additional care when selecting the feedback resistor (R1) due to the large ESR. The output ripple (ΔV_{OUT}) can be approximated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \cdot f_{OSC} \cdot L} \cdot \left(ESR + \frac{1}{8 \cdot f_{OSC} \cdot C_O} \right) \quad (6)$$

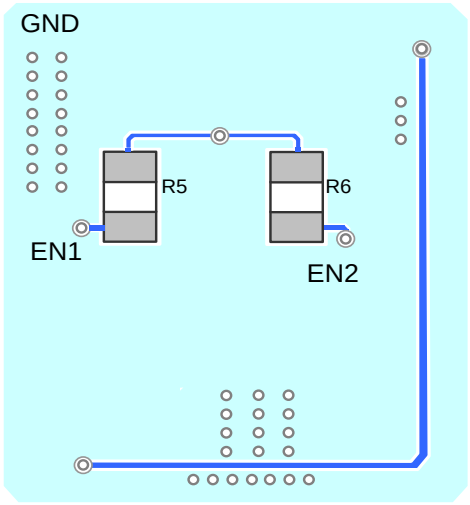
PCB Layout Guidelines

Efficient PCB layout of the switching power supplies is critical for stable operation. A poor layout design can result in poor line or load regulation and stability issues. For best results, refer to Figure 4 and follow the guidelines below.

1. Place the high-current paths (GND, VIN) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close to VIN and GND as possible.
3. Place the external feedback resistors next to FB.



Top Layer



Bottom Layer

Figure 4: Recommended Layout

Design Example

Table 3 is a design example following the application guidelines for the specifications below.

Table 3: Design Example

VIN	5V
VOUT1	1.8V
VOUT2	1.2V

The detailed application schematic is shown in Figure 5. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUIT

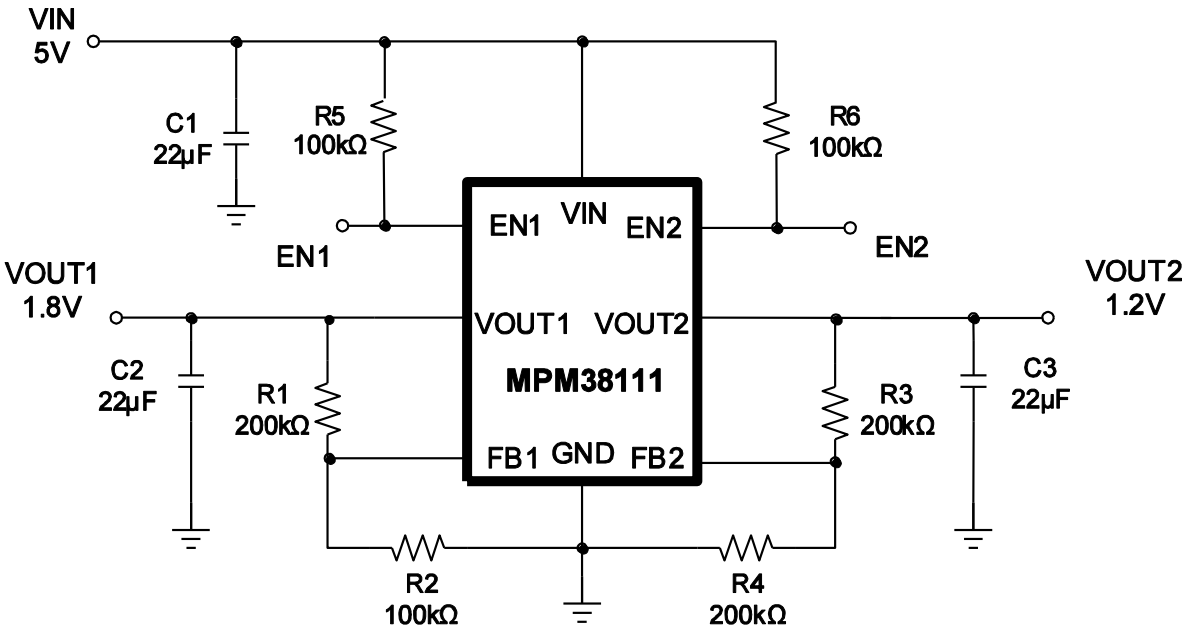
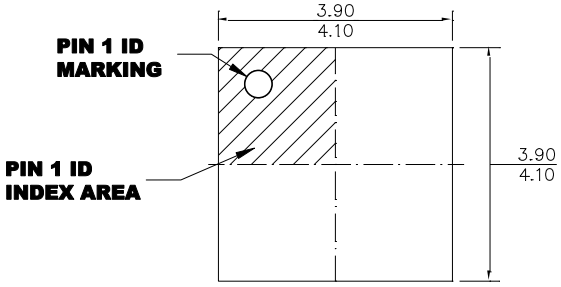


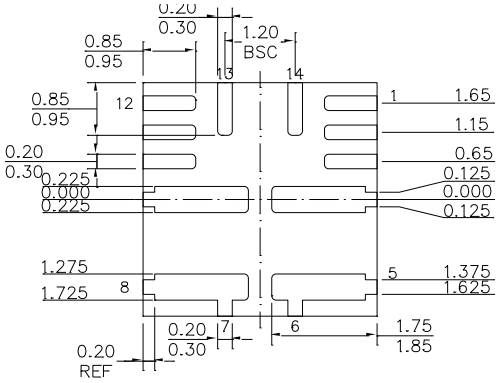
Figure 5: Typical Application Circuit

PACKAGE INFORMATION

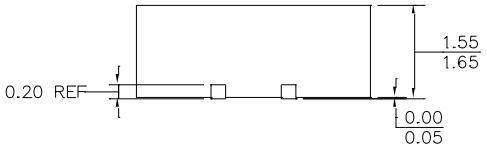
QFN-14 (4mmx4mmx1.6mm)



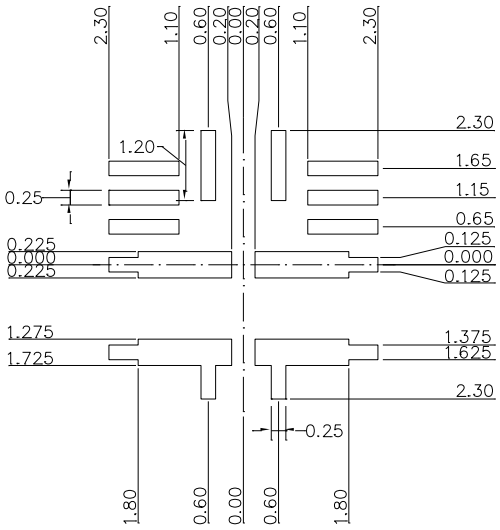
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.