NEC

MOS INTEGRATED CIRCUIT
MC-4532DC726

32 M-WORD BY 72-BIT SYNCHRONOUS DYNAMIC RAM MODULE REGISTERED TYPE

Description

The MC-4532DC726 is a 33,554,432 words by 72 bits synchronous dynamic RAM module on which 36 pieces of 64 M SDRAM: μPD4564441 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 33,554,432 words by 72 bits organization (ECC type)
- Clock frequency and Access time from CLK

	Part number	/CAS latency	Clock frequency (MAX.)	Access time from CLK (MAX.)
	MC-4532DC726FA-A80	CL = 3	125 MHz	6 ns
		CL = 2	100 MHz	6 ns
	MC-4532DC726FA-A10	CL = 3	100 MHz	6 ns
		CL = 2	77 MHz	7 ns
★	MC-4532DC726LFA-A80	CL = 3	125 MHz	6 ns
		CL = 2	100 MHz	6 ns
★	MC-4532DC726LFA-A10	CL = 3	100 MHz	6 ns
		CL = 2	77 MHz	7 ns

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Quad internal banks controlled by BA0 and BA1 (Bank Select)
- Programmable burst-length (1, 2, 4, 8 and Full Page)
- Programmable wrap sequence (Sequential / Interleave)
- Programmable /CAS latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- Single 3.3 V ± 0.3 V power supply
- LVTTL compatible
- 4,096 refresh cycles/64 ms
- Burst termination by Burst Stop command and Precharge command
- All DQs have 10 Ω ± 10 % of series resistor
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Registered type
- Serial PD
- Stacked Module

★ • PC100 registered DIMM Rev. 1.0 compliant

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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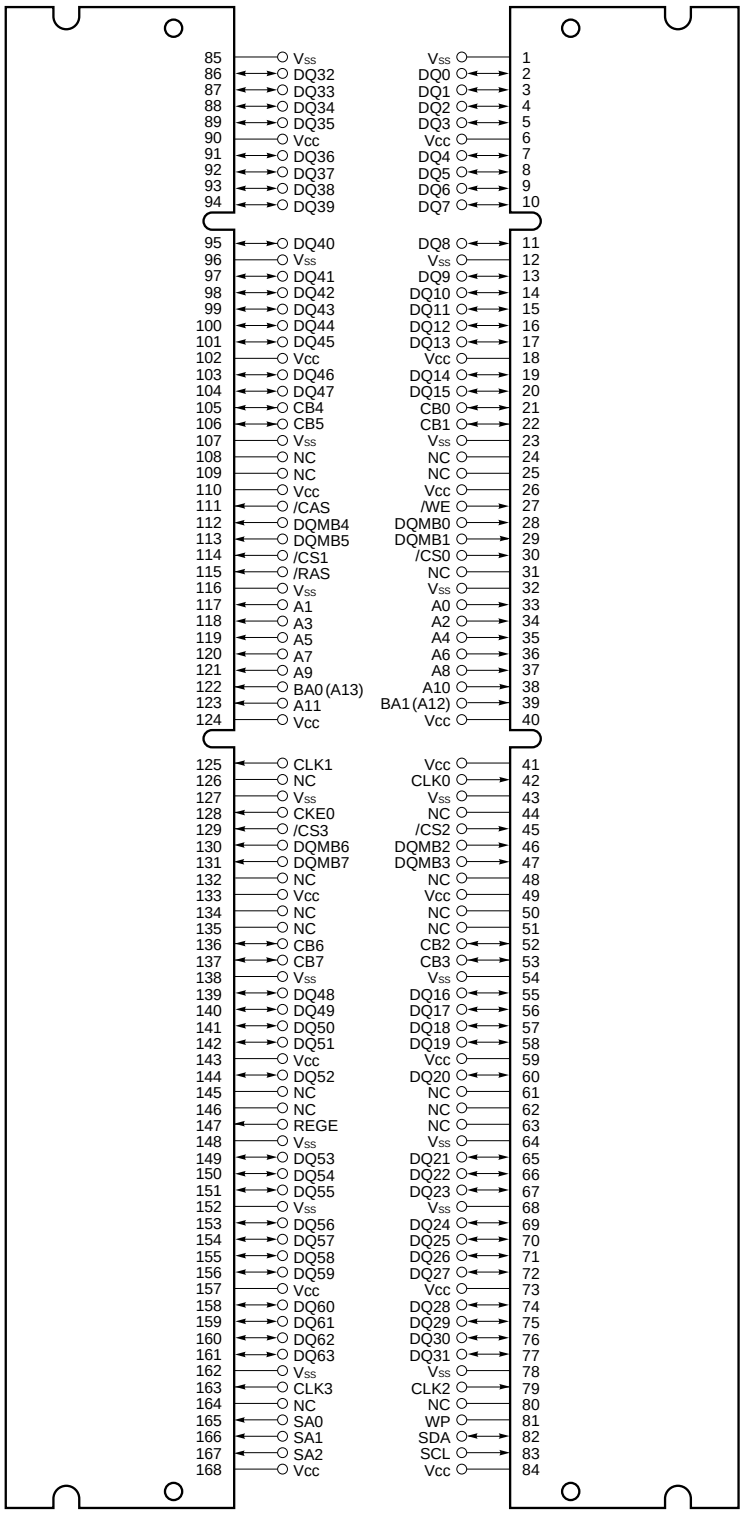
The mark ★ shows major revised points.

Ordering Information

	Part number	Clock frequency MHz (MAX.)	Package	Mounted devices
	MC-4532DC726FA-A80	125 MHz	168-pin Dual In-line Memory Module	36 pieces of μPD4564441G5 (Rev. E)
	MC-4532DC726FA-A10	100 MHz	(Socket Type)	(400 mil TSOP (II))
★	MC-4532DC726LFA-A80	125 MHz	Edge connector: Gold plated	36 pieces of μPD4564441G5 (Rev. L)
★	MC-4532DC726LFA-A10	100 MHz	43.18 mm (1.70 inch) height	(400 mil TSOP (II))

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector: Gold plated)

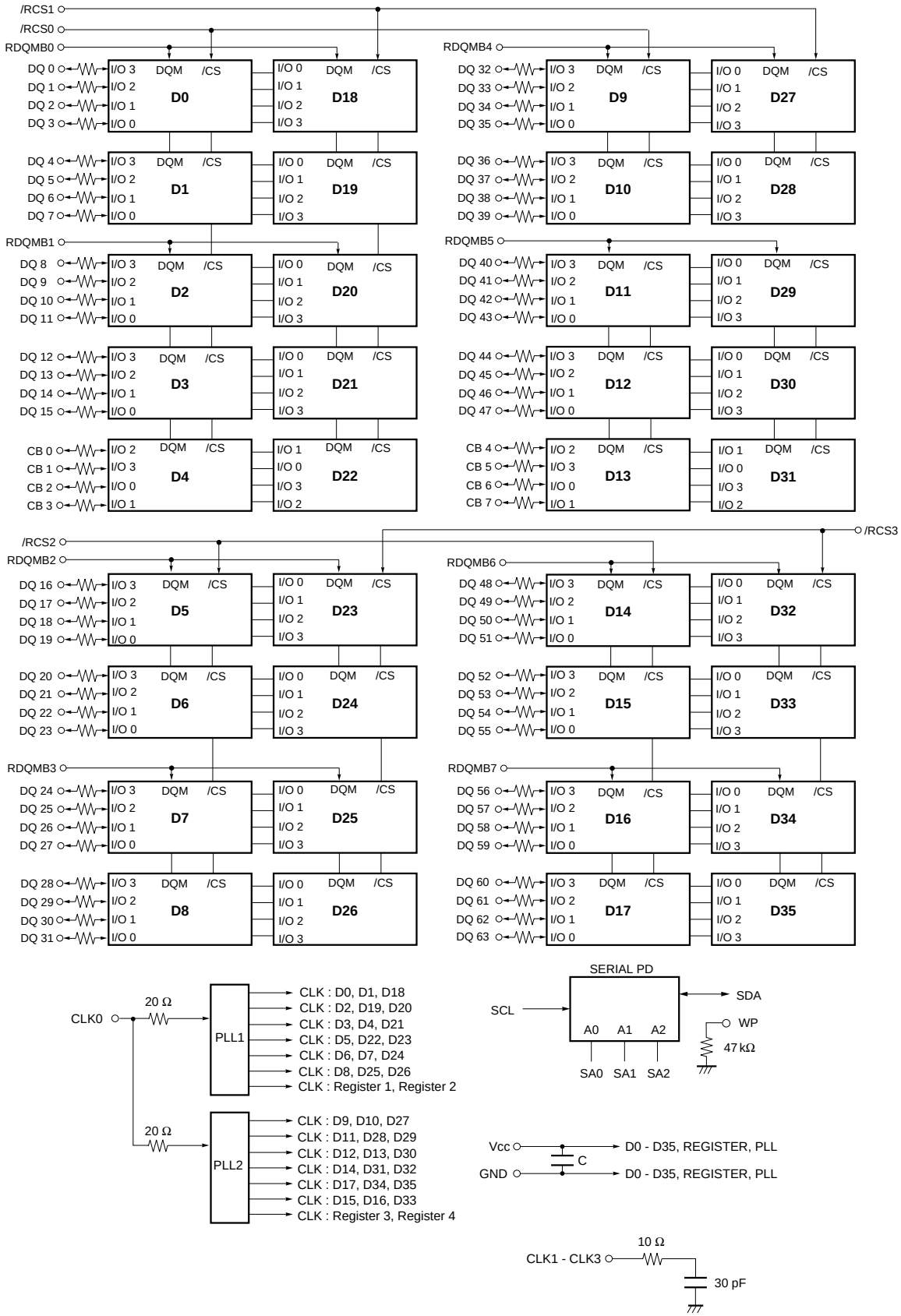


/xxx indicates active low signal.

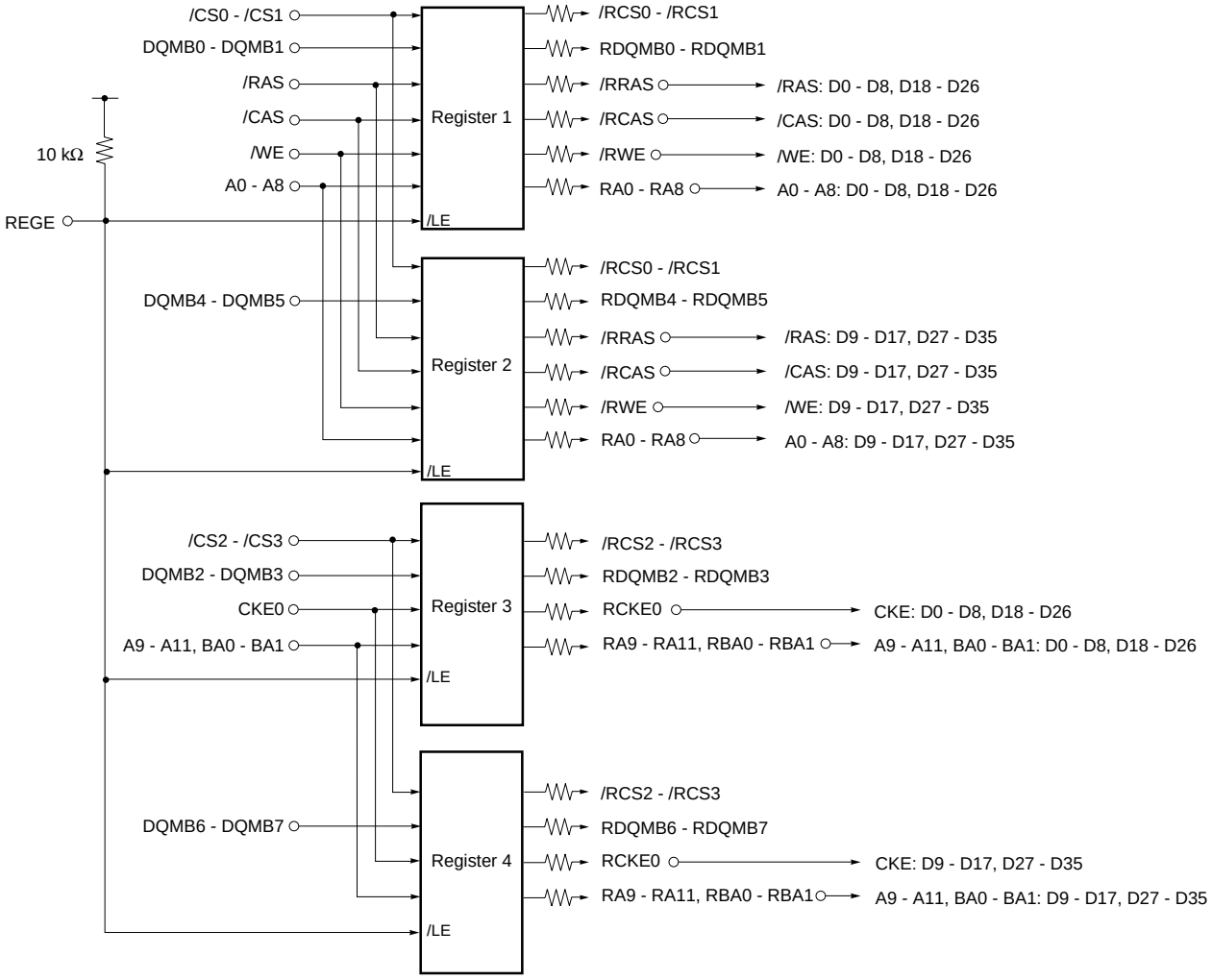
A0 - A11	:	Address Inputs
[Row : A0 - A11, Column : A0 - A9]		
BA0 (A13), BA1 (A12)	:	SDRAM Bank Select
DQ0 - DQ63, CB0 - CB7	:	Data Inputs/Outputs
CLK0 - CLK3	:	Clock Input
CKE0	:	Clock Enable Input
WP	:	Write Protect [Note]
/CS0 - /CS3	:	Chip Select Input
/RAS	:	Row Address Strobe
/CAS	:	Column Address Strobe
/WE	:	Write Enable
DQMB0 - DQMB7	:	DQ Mask Enable
SA0 - SA2	:	Address Input for EEPROM
SDA	:	Serial Data I/O for PD
SCL	:	Clock Input for PD
V_{CC}	:	Power Supply
V_{SS}	:	Ground
REGE	:	Register/Buffer Enable
NC	:	No Connection

Note WP is not used yet. It is connected to ground.

Block Diagram (1/2)



Block Diagram (2/2)



Remarks 1. The series resistor values of DQs are 10 Ω.

2. WP is not used yet. It is connected to ground.

3. D0 - D35: μPD4564441 (4M words × 4 bits × 4 banks)

4. REGE ≤ V_{IL}: Buffer Mode

REGE ≥ V_{IH}: Register Mode

5. Register: SN74ALVC16334DGG

PLL: CDC2509APW

6. D0 - D8, D18 - D26, Register 1, Register 3, and PLL 1 are assembled on main PCB.

D9 - D17, D27 - D35, Register 2, Register 4 and PLL 2 are assembled on sub PCB.

Electrical Specifications

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 1 ms and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V_{CC}		–0.5 to +4.6	V
Voltage on input pin relative to GND	V_T		–0.5 to +4.6	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		42	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC}+0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A11, BA0(A13), BA1(A12), /RAS, /CAS, /WE,	8		17	pF
	C_{I2}	CLK0 - CLK3	15		35	
	C_{I3}	CKE0	14		31	
	C_{I4}	/CS0 - /CS3,	8		17	
	C_{I5}	DQMB0 - DQMB7	5		12	
Data input/output capacitance	$C_{I/O}$	DQ0 - DQ63, CB0 - CB7	11		21	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[MC-4532DC726FA]

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC(MIN.)}$ I_O = 0 mA	/CAS latency = 2	-A80		2,350	mA	1
				-A10		2,170		
			/CAS latency = 3	-A80		2,440		
				-A10		2,260		
Precharge standby current in power down mode	$I_{CC2}P$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 15 ns				536	mA	
	$I_{CC2}PS$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = ∞				28		
Precharge standby current in non power down mode	$I_{CC2}N$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH(MIN.)}$, Input signals are changed one time during 30 ns.				1,220	mA	
	$I_{CC2}NS$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = ∞ Input signals are stable.				216		
Active standby current in power down mode	$I_{CC3}P$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 15 ns				680	mA	
	$I_{CC3}PS$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = ∞				144		
Active standby current in non power down mode	$I_{CC3}N$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH(MIN.)}$, Input signals are changed one time during 30 ns.				1,400	mA	
	$I_{CC3}NS$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = ∞ Input signals are stable.				360		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK(MIN.)}$ I_O = 0 mA	/CAS latency = 2	-A80		2,620	mA	2
				-A10		2,260		
			/CAS latency = 3	-A80		2,890		
				-A10		2,620		
CBR (Auto) refresh current	I_{CC5}	$t_{RC} \geq t_{RC(MIN.)}$	/CAS latency = 2	-A80		3,340	mA	3
				-A10		3,340		
			/CAS latency = 3	-A80		3,430		
				-A10		3,430		
Self refresh current	I_{CC6}	CKE ≤ 0.2 V				536	mA	
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V, All other pins not under test = 0 V			– 20	+ 20	μA	
Output leakage current	$I_{O(L)}$	D_{OUT} is disabled, V_O = 0 to 3.6 V			– 3	+ 3	μA	
High level output voltage	V_{OH}	I_O = – 4.0 mA			2.4		V	
Low level output voltage	V_{OL}	I_O = + 4.0 mA				0.4	V	

Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

3. I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

★ **[MC-4532DC726LFA]**

Parameter	Symbol	Test condition			MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC(MIN.)}$ I_O = 0 mA	/CAS latency = 2	-A80		2,400	mA	1
				-A10		2,220		
			/CAS latency = 3	-A80		2,490		
				-A10		2,310		
Precharge standby current in power down mode	$I_{CC2}P$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 15 ns				536	mA	
	$I_{CC2}PS$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = ∞				53		
Precharge standby current in non power down mode	$I_{CC2}N$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH(MIN.)}$, Input signals are changed one time during 30 ns.				1,220	mA	
	$I_{CC2}NS$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = ∞ Input signals are stable.				216		
Active standby current in power down mode	$I_{CC3}P$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = 15 ns				680	mA	
	$I_{CC3}PS$	CKE ≤ $V_{IL(MAX.)}$, t_{CK} = ∞				144		
Active standby current in non power down mode	$I_{CC3}N$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH(MIN.)}$, Input signals are changed one time during 30 ns.				1,400	mA	
	$I_{CC3}NS$	CKE ≥ $V_{IH(MIN.)}$, t_{CK} = ∞ Input signals are stable.				540		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK(MIN.)}$ I_O = 0 mA	/CAS latency = 2	-A80		2,670	mA	2
				-A10		2,310		
			/CAS latency = 3	-A80		2,940		
				-A10		2,640		
CBR (Auto) refresh current	I_{CC5}	$t_{RC} \geq t_{RC(MIN.)}$	/CAS latency = 2	-A80		3,390	mA	3
				-A10		3,390		
			/CAS latency = 3	-A80		3,480		
				-A10		3,480		
Self refresh current	I_{CC6}	CKE ≤ 0.2 V				536	mA	
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V, All other pins not under test = 0 V			– 20	+ 20	μA	
Output leakage current	$I_{O(L)}$	D_{OUT} is disabled, V_O = 0 to 3.6 V			– 3	+ 3	μA	
High level output voltage	V_{OH}	I_O = – 4.0 mA			2.4		V	
Low level output voltage	V_{OL}	I_O = + 4.0 mA				0.4	V	

Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

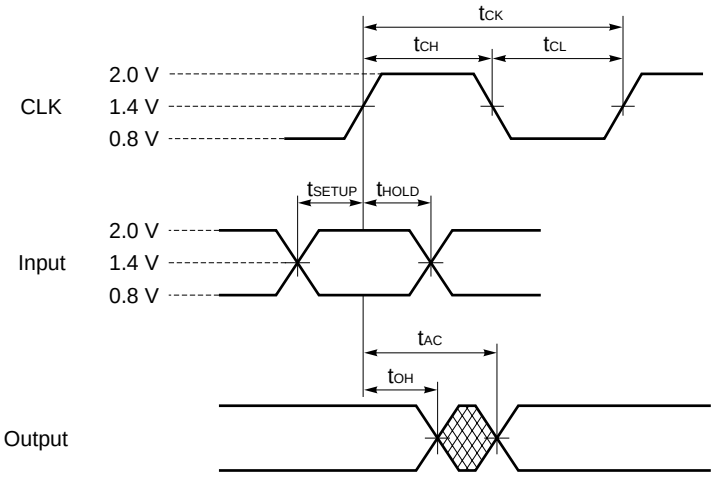
2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

3. I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK(MIN.)}$.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

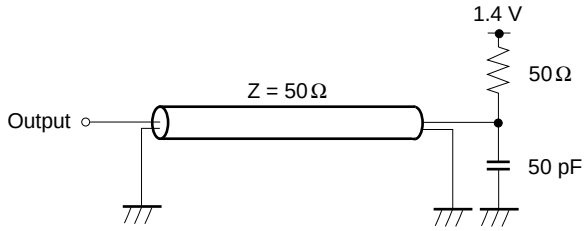
- AC measurements assume t_T = 1 ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL}.
- If t_T is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH(MIN.)}$ and $V_{IL(MAX.)}$.
- An access time is measured at 1.4 V.



Synchronous Characteristics (Registered Mode)

Parameter		Symbol	-A80		-A10		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
Clock cycle time	/CAS latency = 3	t_{CK3}	8	(125 MHz)	10	(100 MHz)	ns	
	/CAS latency = 2	t_{CK2}	10	(100 MHz)	13	(77 MHz)	ns	
Access time from CLK	/CAS latency = 3	t_{AC3}		6		6	ns	1
	/CAS latency = 2	t_{AC2}		6		7	ns	1
Input CLK duty cycle			40	60	40	60	%	
Data-out hold time	/CAS latency = 3	t_{OH3}	3		3		ns	1
	/CAS latency = 2	t_{OH2}	3		3		ns	1
Data-out low-impedance time		t_{LZ}	0		0		ns	
Data-out high-	/CAS latency = 3	t_{HZ3}	3	6	3	6	ns	
impedance time	/CAS latency = 2	t_{HZ2}	3	6	3	7	ns	
Data-in setup time		t_{DS}	2		2		ns	
Data-in hold time		t_{DH}	1		1		ns	
Address setup time		t_{AS}	1.5		1.5		ns	
Address hold time		t_{AH}	0.9		0.9		ns	
CKE setup time		t_{CKS}	1.5		1.5		ns	
CKE hold time		t_{CKH}	0.9		0.9		ns	
CKE setup time (Power down exit)		t_{CKSP}	1.5		1.5		ns	
Command (/CS0 - /CS3, /RAS, /CAS, /WE, DQMB0 - DQMB7) setup time		t_{CMS}	1.5		1.5		ns	
Command (/CS0 - /CS3, /RAS, /CAS, /WE, DQMB0 - DQMB7) hold time		t_{CMH}	0.9		0.9		ns	

Note 1. Output load



Remark These specifications are applied to the monolithic device.

Asynchronous Characteristics (Registered Mode)

Parameter		Symbol	-A80		-A10		Unit	Note
			MIN.	MAX.	MIN.	MAX.		
REF to REF/ACT command period		t_{RC}	70		70		ns	
ACT to PRE command period		t_{RAS}	48	120,000	50	120,000	ns	
PRE to ACT command period		t_{RP}	20		20		ns	
Delay time ACT to READ/WRITE command		t_{RCD}	20		20		ns	
ACT(0) to ACT(1) command period		t_{RRD}	16		20		ns	
Data-in to PRE command period		t_{DPL}	–1CLK+8		–1CLK+10		ns	
Data-in to ACT(REF) command period (Auto precharge)	/CAS latency = 3	t_{DAL3}	20		20		ns	
	/CAS latency = 2	t_{DAL2}	20		20		ns	
Mode register set cycle time		t_{RSC}	2		2		CLK	
Transition time		t_T	0.5	30	1	30	ns	
Refresh time (4,096 refresh cycles)		t_{REF}		64		64	ms	

Serial PD (1/2)

Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
0	Defines the number of bytes written into serial PD memory		80H	1	0	0	0	0	0	0	0	128 bytes
1	Total number of bytes of serial PD memory		08H	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type		04H	0	0	0	0	0	1	0	0	SDRAM
3	Number of rows		0CH	0	0	0	0	1	1	0	0	12 rows
4	Number of columns		0AH	0	0	0	0	1	0	1	0	10 columns
5	Number of banks		02H	0	0	0	0	0	0	1	0	2 banks
6	Data width		48H	0	1	0	0	1	0	0	0	72 bits
7	Data width (continued)		00H	0	0	0	0	0	0	0	0	0
8	Voltage interface		01H	0	0	0	0	0	0	0	1	LVTTL
9	CL = 3 Cycle time	-A80	80H	1	0	0	0	0	0	0	0	8 ns
		-A10	A0H	1	0	1	0	0	0	0	0	10 ns
10	CL = 3 Access time	-A80	60H	0	1	1	0	0	0	0	0	6 ns
		-A10	60H	0	1	1	0	0	0	0	0	6 ns
11	DIMM configuration type		02H	0	0	0	0	0	0	1	0	ECC
12	Refresh rate/type		80H	1	0	0	0	0	0	0	0	Normal
13	SDRAM width		04H	0	0	0	0	0	1	0	0	×4
14	Error checking SDRAM width		04H	0	0	0	0	0	1	0	0	×4
15	Minimum clock delay		01H	0	0	0	0	0	0	0	1	1 clock
16	Burst length supported		8FH	1	0	0	0	1	1	1	1	1, 2, 4, 8, F
17	Number of banks on each SDRAM		04H	0	0	0	0	0	1	0	0	4 banks
18	/CAS latency supported		06H	0	0	0	0	0	1	1	0	2, 3
19	/CS latency supported		01H	0	0	0	0	0	0	0	1	0
20	/WE latency supported		01H	0	0	0	0	0	0	0	1	0
21	SDRAM module attributes		1FH	0	0	0	1	1	1	1	1	Registered
22	SDRAM device attributes : General		0EH	0	0	0	0	1	1	1	0	
23	CL = 2 Cycle time	-A80	A0H	1	0	1	0	0	0	0	0	10 ns
		-A10	D0H	1	1	0	1	0	0	0	0	13 ns
24	CL = 2 Access time	-A80	60H	0	1	1	0	0	0	0	0	6 ns
		-A10	70H	0	1	1	1	0	0	0	0	7 ns
25-26			00H	0	0	0	0	0	0	0	0	
27	$t_{RP(MIN.)}$	-A80	14H	0	0	0	1	0	1	0	0	20 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
28	$t_{RRD(MIN.)}$	-A80	10H	0	0	0	1	0	0	0	0	16 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
29	$t_{RCD(MIN.)}$	-A80	14H	0	0	0	1	0	1	0	0	20 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
30	$t_{RAS(MIN.)}$	-A80	30H	0	0	1	1	0	0	0	0	48 ns
		-A10	32H	0	0	1	1	0	0	1	0	50 ns
31	Module bank density		20H	0	0	1	0	0	0	0	0	128M bytes

Serial PD (2/2)

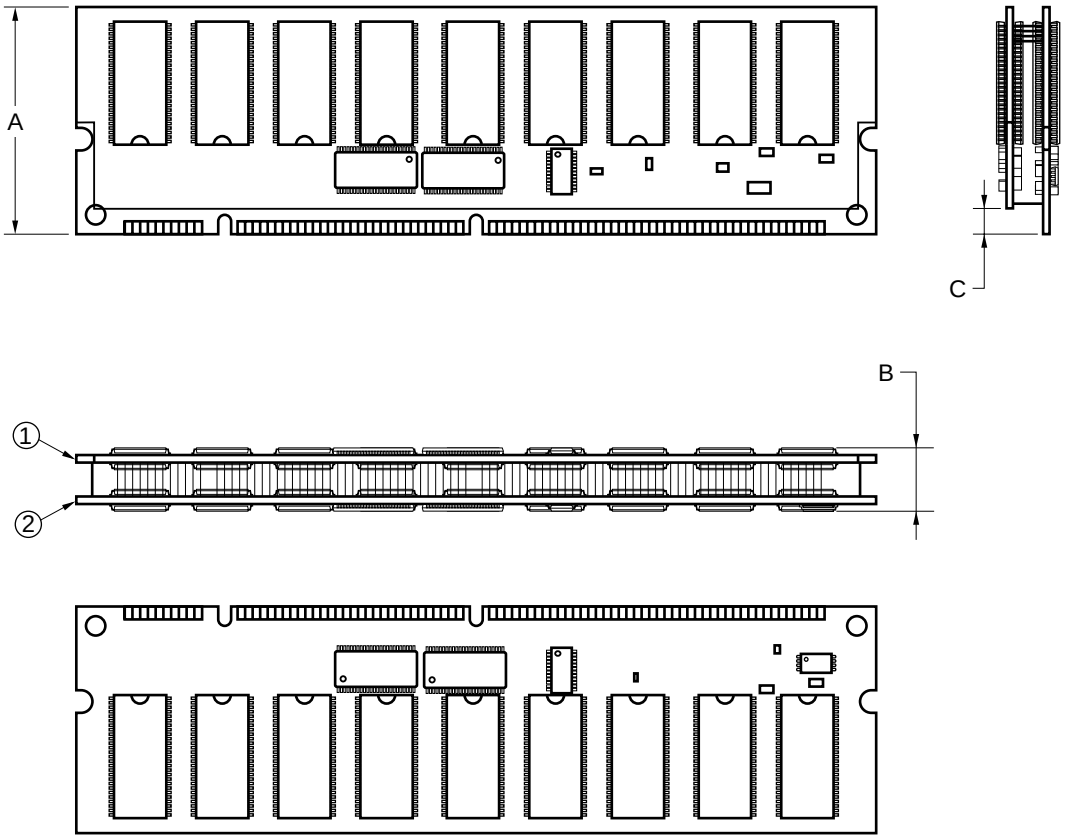
Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
32	Command and address signal input setup time		15H	0	0	0	1	0	1	0	1	1.5 ns
33	Command and address signal input hold time		09H	0	0	0	0	1	0	0	1	0.9 ns
34	Data signal input setup time		20H	0	0	1	0	0	0	0	0	2 ns
35	Data signal input hold time		10H	0	0	0	1	0	0	0	0	1 ns
36-61			00H	0	0	0	0	0	0	0	0	
62	SPD revision		12H	0	0	0	1	0	0	1	0	1.2
63	Checksum for bytes 0 - 62	-A80	08H	0	0	0	0	1	0	0	0	
		-A10	6EH	0	1	1	0	1	1	1	0	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91	Revision Code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-125	Mfg specific											
126	Intel specification frequency		64H	0	1	1	0	0	1	0	0	100 MHz
127	Intel specification /CAS	-A80	8FH	1	0	0	0	1	1	1	1	
	latency support	-A10	8DH	1	0	0	0	1	1	0	1	

Timing Chart

★ Refer to the **SYNCHRONOUS DRAM MODULE TIMING CHART Information (M13348X)**.

★ **Package Drawings**

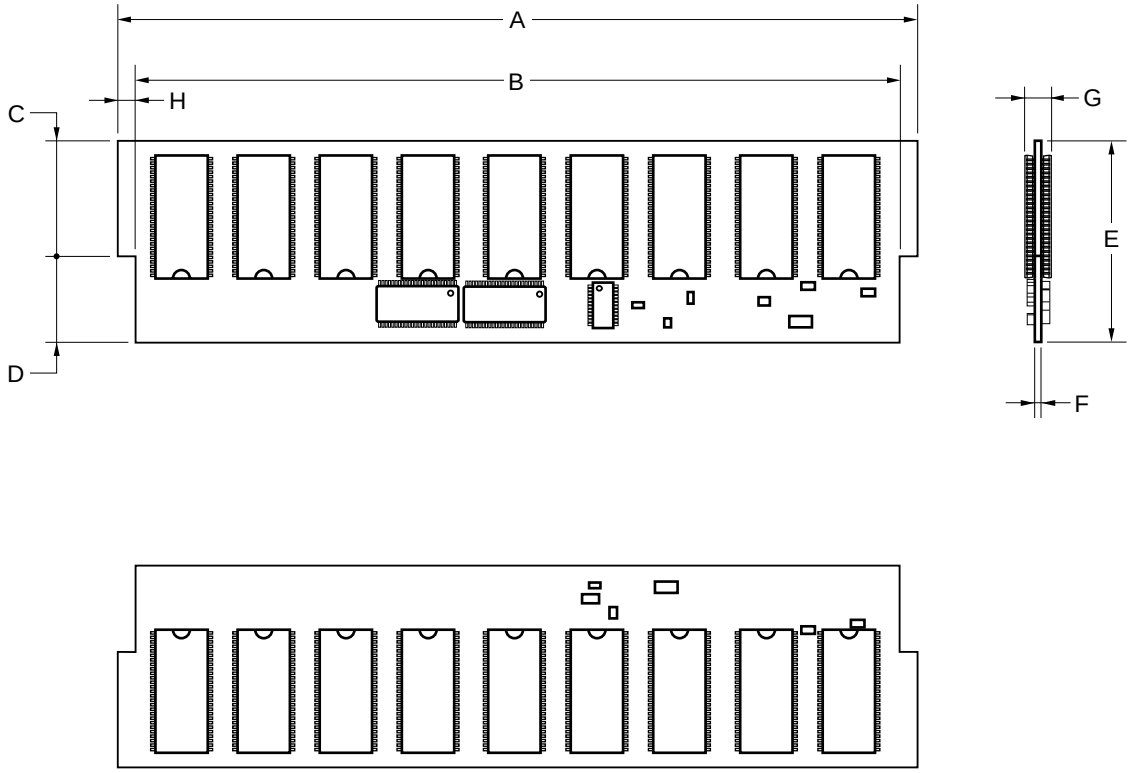
168 PIN DUAL IN-LINE MODULE (SOCKET TYPE) (1/3) [ASSEMBLY DRAWING]



ITEM	MILLIMETERS
A	43.18±0.13
B	8.10±0.25
C	4.00

M168S-50A92-1

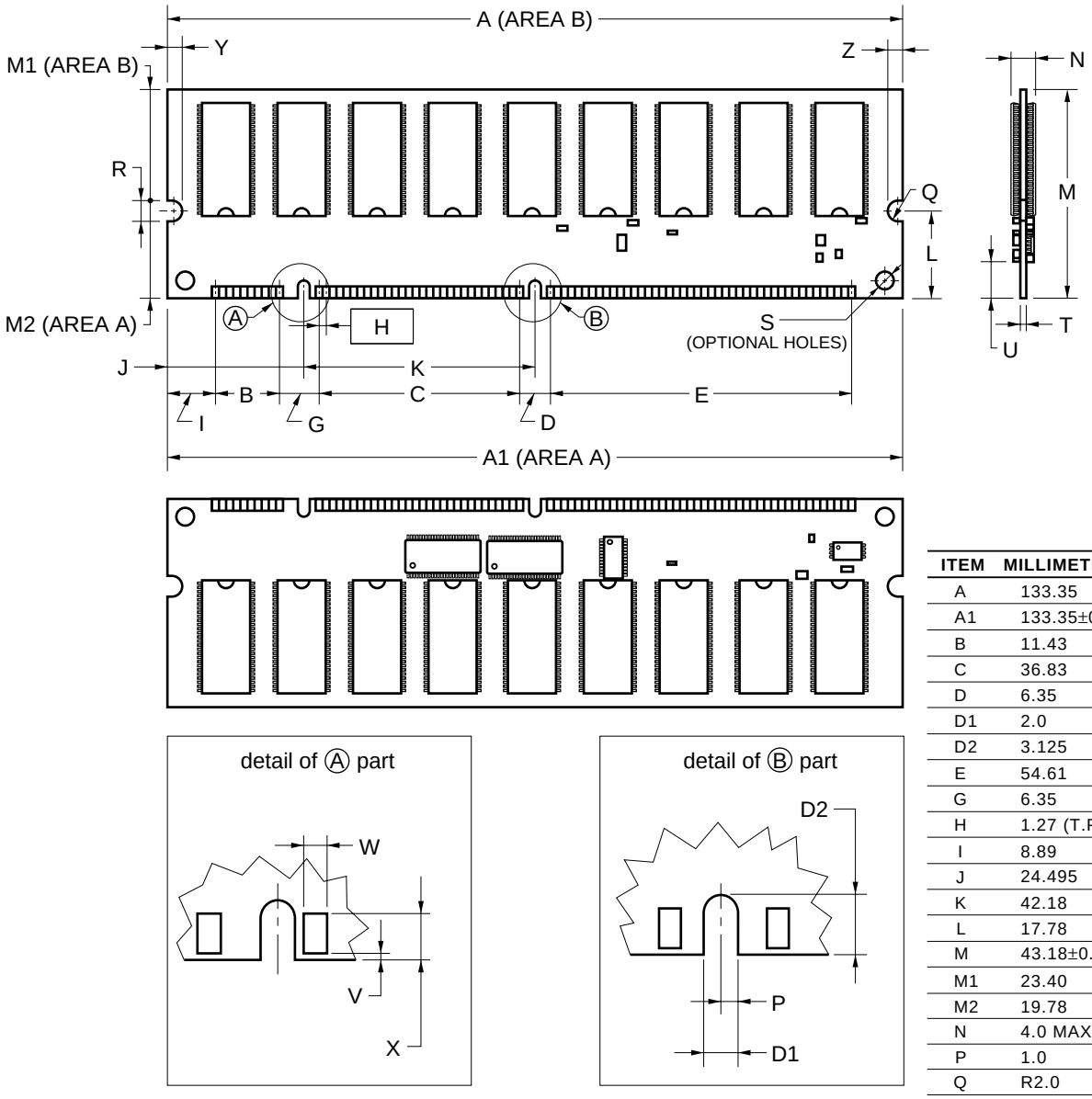
168 PIN DUAL IN-LINE MODULE (SOCKET TYPE) (2/3)
[PART DRAWING 1]



ITEM	MILLIMETERS
A	133.35
B	126.95
C	22.18
D	17.00
E	39.18
F	1.27±0.1
G	4.0 MAX.
H	3.2

M168S-50A92-1

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE) (3/3)
[PART DRAWING 2]



ITEM	MILLIMETERS
A	133.35
A1	133.35±0.13
B	11.43
C	36.83
D	6.35
D1	2.0
D2	3.125
E	54.61
G	6.35
H	1.27 (T.P.)
I	8.89
J	24.495
K	42.18
L	17.78
M	43.18±0.13
M1	23.40
M2	19.78
N	4.0 MAX.
P	1.0
Q	R2.0
R	4.0±0.10
S	ϕ3.0
T	1.27±0.1
U	4.0 MIN.
V	0.2±0.15
W	1.0±0.05
X	2.54±0.10
Y	3.0 MIN.
Z	3.0 MIN.

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[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.