PRODUCT PREVIEW

SYNCHRONOUS UP/DOWN DECADE COUNTER

DESCRIPTION

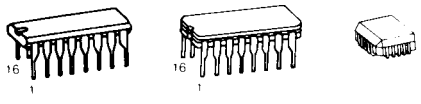
The M54/74HC192 is a high speed CMOS SYNCHRONOUS UP/DOWN DECADE COUNTER fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. This counter has two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flop are simultaneously triggered on the low to high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked.

This counter may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D input. When the LOAD input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n counters by modifying the count length with the preset inputs.

In addition the counter can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to a low level independently of either COUNT input.

Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counter can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device.

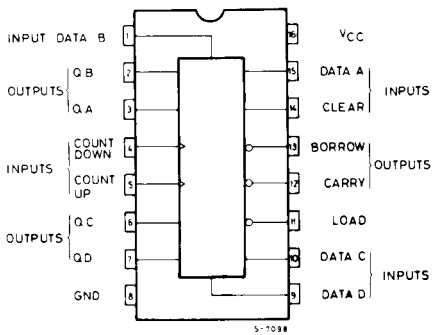
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



B1 Plastic Package | **F1** Ceramic Package | **C1** Chip Carrier

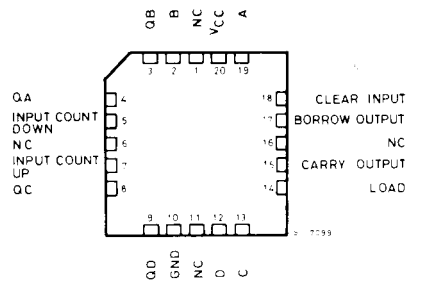
ORDERING NUMBERS: M54HC192 F1
M74HC192 B1
M74HC192 F1
M74HC192 C1

PIN CONNECTIONS
(top view)



Dual in line

CHIP CARRIER



NC = No Internal Connection

TRUTH TABLE

Count		Clear	Load	Function
Up	Down			
↑	H	L	H	Count UP
H	↑	L	H	Count Down
X	X	H	X	Clear
X	X	L	L	Load

H = High level
L = Low level
↑ = Transition from low-to-high
X = Don't care

FEATURES

- Low Power Dissipation
  I_{CC} = 4 μA (Max.) at T_A = 25°C
- High Noise Immunity
  V_{NIH} = V_{NIL} = 28% V_{CC} (Min.)
- Output Drive Capability
  10 LSTTL Loads
- Symmetrical Output Impedance
  $|I_{OH}|$ = I_{OL} = 4 mA (Min.)
- Balanced Propagation Delays
  t_{PLH} = t_{PHL}
- Wide Operating Voltage Range
  V_{CC} (opr) = 2V to 6V
- Pin and Function compatible
  with 54/74LS192

INPUT AND OUTPUT EQUIVALENT CIRCUIT