Contents

CONTROLLER FOR REFLECTING ECB COLOR LCD S-4581A

The S-4581A is a medium-sized, simple dot matrix type LCD display controller for graphics display.
It can interface with an 8-bit MPU having a READY ($\overline{\text{WAIT}}$) input pin and accesses the VRAM by the cycle steal method so that the display screen is not disturbed. It contains all address/data control circuits for cycle stealing, so it does not require any external circuits. Since it has chip select output pins for the VRAM, it can be connected directly with eight 64K SRAMs or two 256K SRAMs without using an external decoder circuit.
Since the VRAM is mapped on the MPU memory, all display data can be addressed directly by the MPU and display data processes, such as drawing, can be performed quickly and efficiently.
The S4581A provides two display modes: 4- and 8-gradation display modes. When all 64KB of the VRAM are used, the maximum number of dots for display image data is 262,144 in the 4-gradation display mode and 131,072 in the 8-gradation display mode.

■ Features

- Can be controlled by an 8-bit (Intel) MPU.
- Can interface with an MPU with a READ ($\overline{\text{WAIT}}$) signal.
- The MPU accesses the VRAM by the cycle steal method.
  ⇒It does not affect the display screen.
- VRAM
  Mapping: MPU memory space
  Capacity: 64K bytes (2^{16})
- LCD display mode
  4- and 8-gradation display modes
- LCD panel
  Single-screen drive panel (4-bit data transfer)
- Maximum horizontal display width: 1024 dots (gradation display mode)
- Maximum number of vertical lines: 1024
- Maximum display screen (4-gradation mode and frame frequency 200 Hz)
  320 × 240 dots
- Vertical smooth scrolling is possible.
- VRAM chip select output pin
- CMOS operation
- Operating power supply voltage: 5 ± 0.5 V
- S-4581AF: 80-pin QFP
  (Pin pitch: 0.8 mm)

This product is tentative yet therefore specifications may be changed without notice.

■ Cautions

1. DO NOT apply a voltage or current that exceeds the absolute maximum ratings to terminals. If applied, the IC may malfunction or be destroyed.
   The standard values are set with sufficient margins, but use the IC within the recommended operating conditions to optimize device quality.
2. Measures against static electricity
   2.1 When transporting or storing ICs, use conductive containers or metal coated boxes.
   2.2 Check that there is no current leakage in electrical facilities, and be sure to ground them. Also ensure that workbenches and people who handle ICs are grounded.
3. Excessive external noise to the power supply or I/O terminals of CMOS ICs causes latch-up, leading to faults and damage. If latch-up has occurred, immediately turn off the device, eliminate the cause, and turn on the device again.
4. Keep the IC away from mechanical vibration, shock, and sudden changes in temperature. These may cause wires to break.
5. Environment
   5.1 Use and store ICs below the absolute maximum rated temperature.
   5.2 DO NOT use or store ICs where condensation can occur.
   5.3 DO NOT use ICs where they are directly exposed to dust, salt, or acid gas such as SO_2. These may cause leaks between element leads and cause corrosion.
   5.4 To store ICs for a long time, DO NOT process them. During storage, DO NOT apply any load to ICs.

■ Pin Description

External dimensions (Unit: mm)

S-4581AF: 80-pin OFP

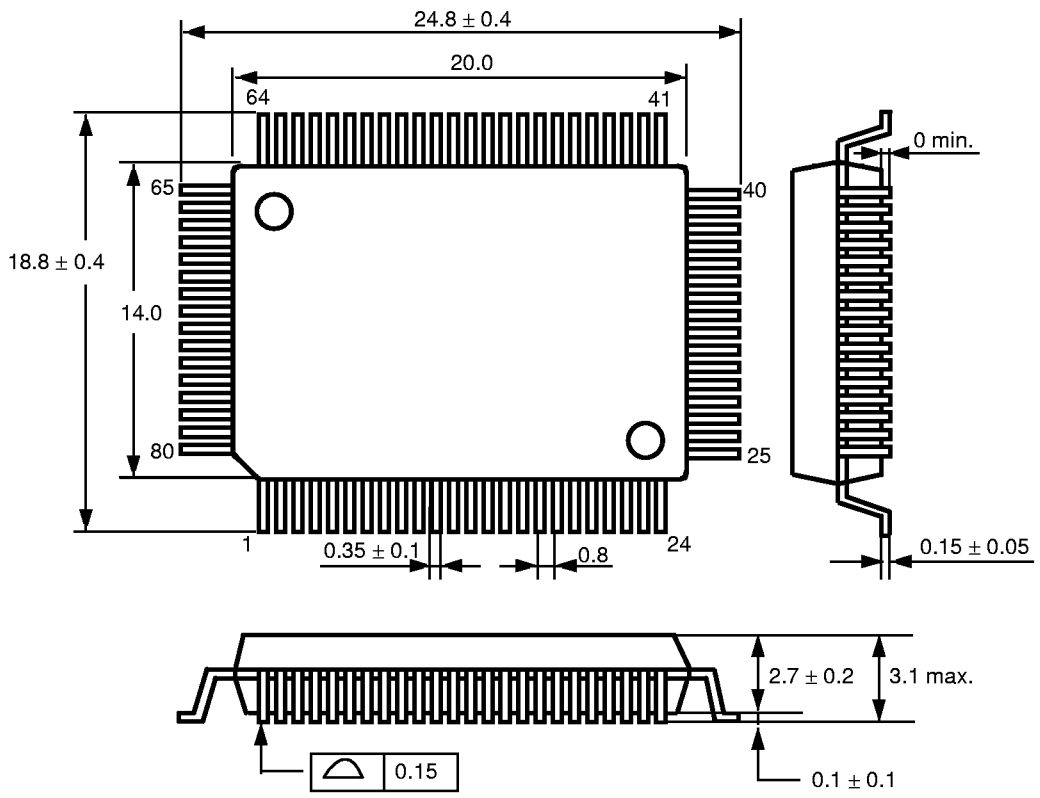


Figure 1-1 External Dimensions

■ S-4581A Pin Layout

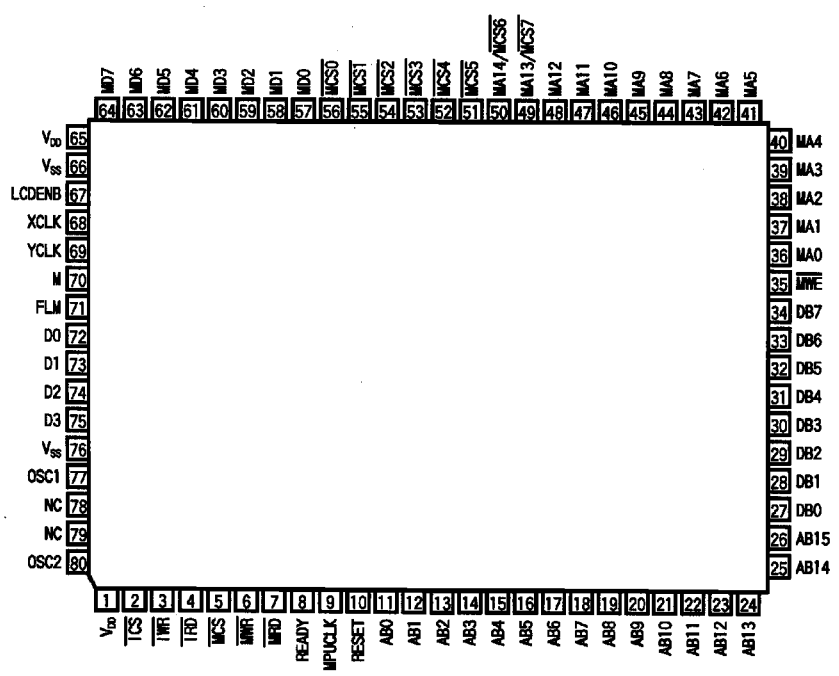


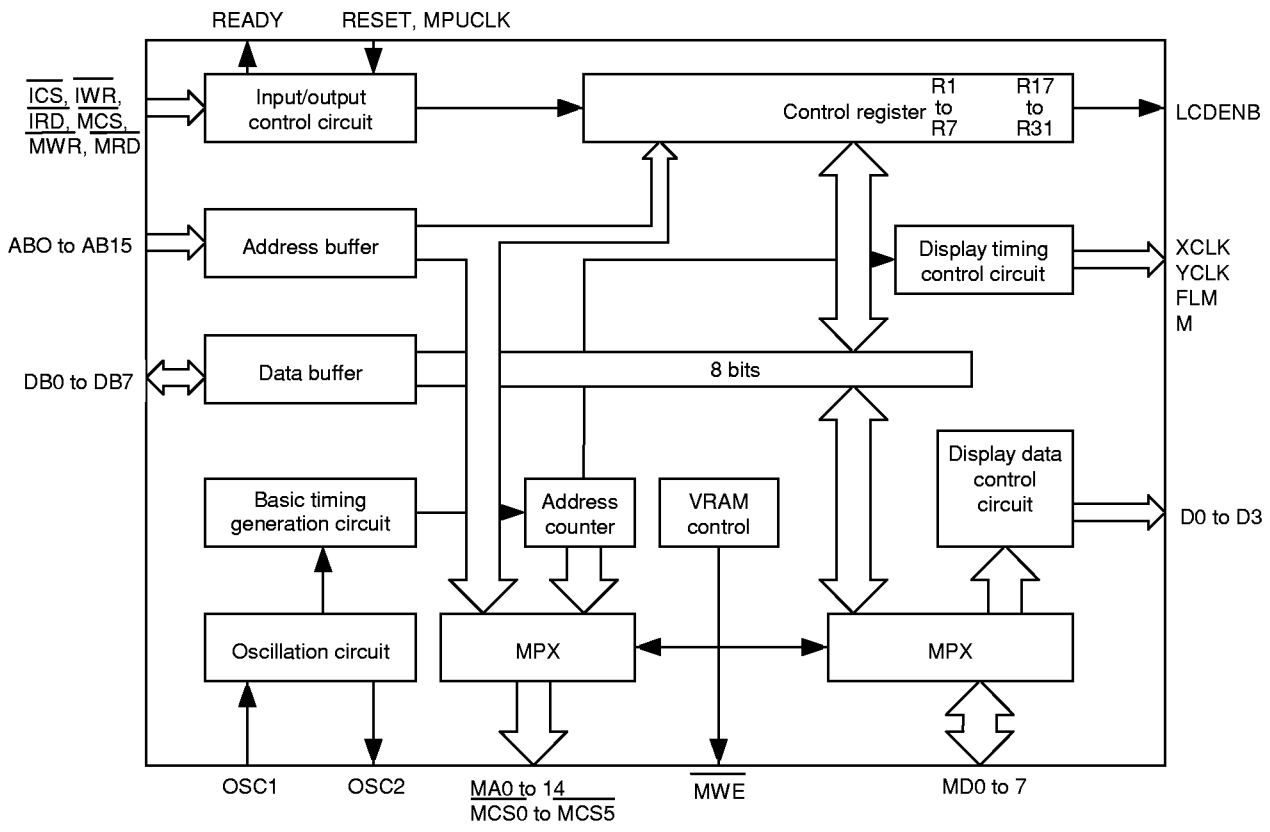
Figure 1-2 Pin Layout

■ Pin Functions

66, 76	VSS	Negative power supply pin Ground pin
1, 65	VDD	Positive power supply pin Normally connected to +5V.
2	$\overline{\text{ICS}}$	MPU interface select signal input pin Low: Active
3	$\overline{\text{IWR}}$	MPU interface write signal input pin Low: Active
4	$\overline{\text{IRD}}$	MPU interface read signal input pin Low: Active
5	$\overline{\text{MCS}}$	VRAM chip select input pin Low: Active
6	$\overline{\text{MWR}}$	VRAM write signal input pin Low: Active
7	$\overline{\text{MRD}}$	VRAM read signal input pin Low: Active
8	READY	MPU wait signal output pin CMOS output A low signal is output at a falling edge of the $\overline{\text{ICS}}$ or $\overline{\text{MCS}}$ signal. After internal processing ends, a high signal is output at a rising edge of MPUCLK. This pin may be connected directly to the $\overline{\text{WAIT}}$ pin of the MPU to wait the MPU.
9	MPUCLK	MPU clock signal input pin
10	RESET	Reset signal input pin Input the MPU RESET signal. The pulse width must to be 1μsec or more. ・ Command initialization/Internal register initialization R1: Initialization described later R2 to R7: All zeros R14, R15, R17, R18, R19: All zeros R21 to R31: All zeros R20: All ones
11 to 26	AB0 to AB15	MPU address bus input pin ・ Address setting at command input AB0=A0 : : : : AB4=A4 ・ VRAM address setting AB0=MA0 : : : : AB15=MA15 Note: If the address signal is multiplexed, latch and input it.
27 to 34	DB0 to DB7	MPU data bus input/output pin
35	$\overline{\text{MWE}}$	VRAM write enable output pin. Low: Active Output a write signal to the VRAM. Connect to the VRAM $\overline{\text{WE}}$ pin.
36 to 48	MA0 to MA12	VRAM address bus output pin
49 to 51	MA13/$\overline{\text{MCS7}}$ to MA14/$\overline{\text{MCS6}}$	VRAM address bus output VRAM chip select signal output pin ・ VRAM chip select signal output pins when 64K SRAM is selected MA13/$\overline{\text{MCS7}}$=$\overline{\text{MCS7}}$ MA14/$\overline{\text{MCS6}}$=$\overline{\text{MCS6}}$

		・ VRAM address bus output pins when 256K SRAM is selected MA13/$\overline{MCS7}$=$\overline{MA13}$ MA14/$\overline{MCS6}$=$\overline{MA14}$
52 to 56	$\overline{MCS5}$ to $\overline{MCS0}$	VRAM chip select signal output pin
		・ VRAM chip select signal output pin when 64K SRAM is selected $\overline{MCS5}$=$\overline{MCS5}$ $\overline{MCS4}$=$\overline{MCS4}$ $\overline{MCS3}$=$\overline{MCS3}$ $\overline{MCS2}$=$\overline{MCS2}$ $\overline{MCS1}$=$\overline{MCS1}$ $\overline{MCS0}$=$\overline{MCS0}$
		・ VRAM address bus output pins when 256K SRAM is selected $\overline{MCS5}$=Unused $\overline{MCS4}$=Unused $\overline{MCS3}$=Unused $\overline{MCS2}$=Unused $\overline{MCS1}$=$\overline{MCS1}$ $\overline{MCS0}$=$\overline{MCS0}$
57 to 64	MD0 to MD7	VRAM data bus input/output pins Connect these pins to the VRAM data bus.
67	LCDENB	The LCD Enable mode setting command setting specified by D6 is output. The LCD pin goes low at reset.
68	XCLK	Display data transfer clock output pin Read display data D0 to D3 into the driver at a falling edge of XCLK.
69	YCLK	Display data latch signal output pin The clock for transferring display data latch signal and operation signal is input to the LCD driver IC. The signal is output after the data for one line for the display panel is transmitted. Transfer the display latch and operation signals at a falling edge of YCLK.
70	M	AC drive signal output pin
71	FLM	Frame start line output pin The common drive IC reads a high output signal from FLM at a falling edge of the YCLK signal. The FLM output has a 2-line return line period for the specified common count of the display panel, and the time of one frame is +2 lines.
72	D0	Display data output pin. 4-bits D0 to D3 are output in parallel to the LCD drive IC.
73	D1	
74	D2	
75	D3	
77	OSC1	Oscillation input pin External clock input pin
78	NC	
79	NC	
80	OSC2	Oscillation output pin Open when an external clock is input

■ Block Diagram



VRAM Address Assignment (1) (When 64K SRAM is used)

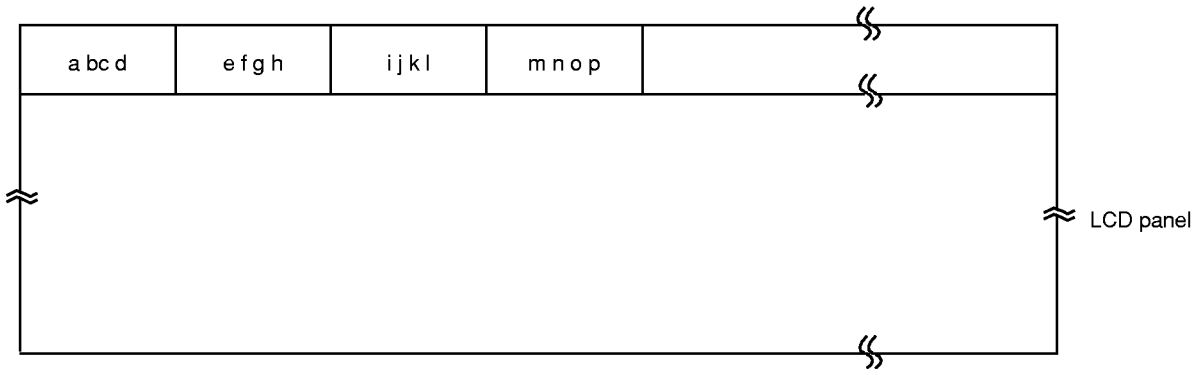
VRAM / S-4581A	VRAM pin		Memory mapping
	Address bus	Chip select	
MA0	A0		
MA1	A1		
MA2	A2		
MA3	A3		
MA4	A4		
MA5	A5		
MA6	A6		
MA7	A7		
MA8	A8		
MA9	A9		
MA10	A10		
MA11	A11		
MA12	A12		
MA13 / $\overline{MCS7}$		$\overline{MCS7}$	E000H to FFFFH
MA14 / $\overline{MCS6}$		$\overline{MCS6}$	C000H to DFFFH
$\overline{MCS5}$		$\overline{MCS5}$	A000H to BFFFH
$\overline{MCS4}$		$\overline{MCS4}$	8000H to 9FFFH
$\overline{MCS3}$		$\overline{MCS3}$	6000H to 7FFFH
$\overline{MCS2}$		$\overline{MCS2}$	4000H to 5FFFH
$\overline{MCS1}$		$\overline{MCS1}$	2000H to 3FFFH
$\overline{MCS0}$		$\overline{MCS0}$	0000H to 1FFFH

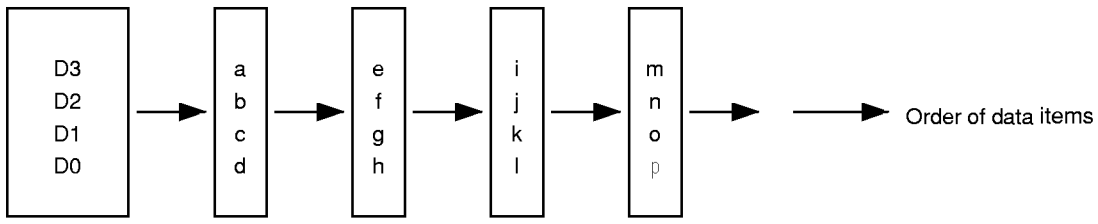
VRAM address assignment (2) (When 256K SRAM is used)

VRAM / S-4581A	VRAM pin		Memory mapping
	Address bus	Chip select	
MA0	A0		
MA1	A1		
MA2	A2		
MA3	A3		
MA4	A4		
MA5	A5		
MA6	A6		
MA7	A7		
MA8	A8		
MA9	A9		
MA10	A10		
MA11	A11		
MA12	A12		
MA13 / $\overline{MCS7}$	A13		
MA14 / $\overline{MCS6}$	A14		
$\overline{MCS5}$			
$\overline{MCS4}$			
$\overline{MCS3}$			
$\overline{MCS2}$			
$\overline{MCS1}$		$\overline{MCS1}$	8000H to FFFFH
$\overline{MCS0}$		$\overline{MCS0}$	0000H to 7FFFH

· D0 to D3

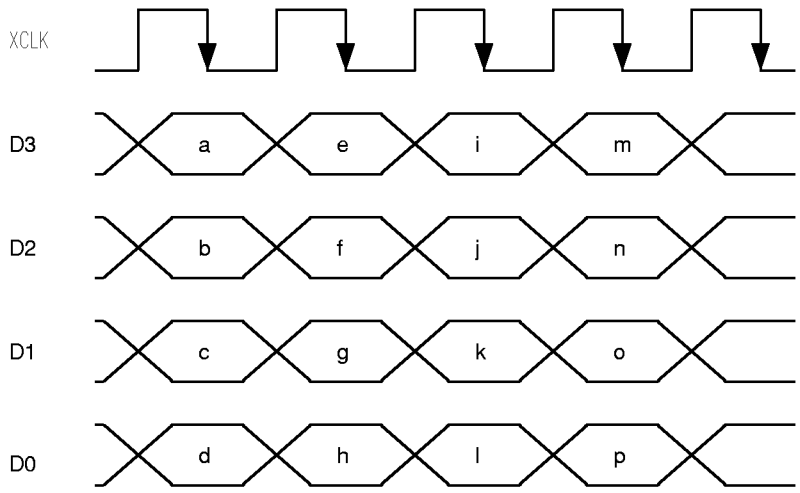
D0 to D3 are LCD display data. The following are the display data output from the D0 to D3 pins and the panel display:





· XCLK

A shift clock for display data transfer. The D0 to D3 display data is sent to the LCD at a falling edge ▼ of XCLK.



· YCLK

This clock is used to transfer display data latch pulse and scan signals. It is output when one line of LCD data is transmitted. Latch the display data at a falling edge ▼ of YCLK. Also, latch the scan signal at a falling edge ▼ of YCLK.

· M

A frame signal to drive the LCD.

· FLM

Outputs a start pulse of a scan line. The signal is active when it is high, and the scan line drive IC should read FLM at falling edge ▼ of YCLK.

- LCDENB

  Outputs data set at bit 1 (D1) of the mode register (R1), which is one of control registers.

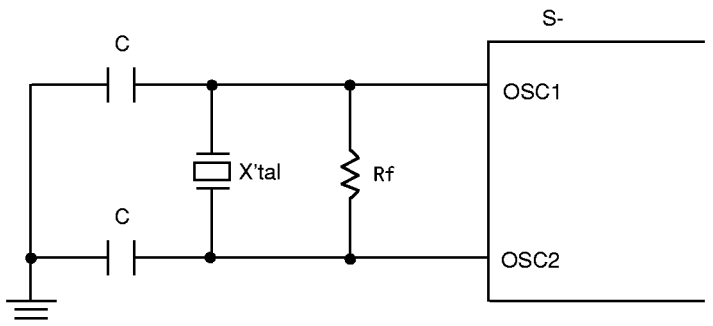
  The signal is low at reset and can be used to control the LCD power supply.

● Oscillation pins

- OSC1 and OSC2

  These pins output clocks for internal operations. OSC1 is an input pin and OSC2 is an output pin. The crystal oscillation clock can be output from OSC2 and external clocks can be input to OSC1.

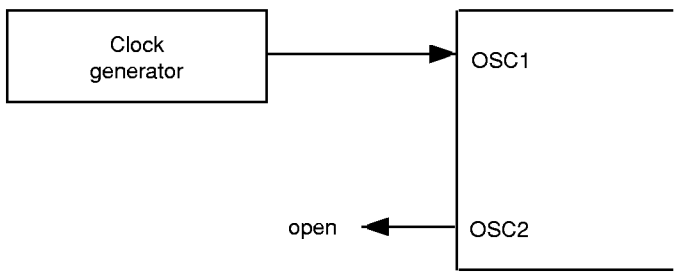
  (i) Crystal oscillation



Note: Install C, Rf, and X'tal close to the pin.

C ≅ 30pf Rf = 1MΩ

(ii) When external clocks are input



● Power supply pins

VDD, VSS

Each of the power supply pins has two pins. Supply positive power to V_{DD} and 0V to V_{SS}. Be sure to connect a capacitor near a pair of V_{DD} and V_{SS}.(4.7μF or more)

■ Control Registers

The S-4581A contains 22 registers to interface with various sizes of LCDs and display data freely.
Use $\overline{ICS}$, $\overline{IWR}$, and $\overline{IRD}$ for setting. The address of each register is defined by A0 to A4.

● Types of control registers

Register type		I/O address					Data									
No	Name	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Register function	R/W
R1	Mode register	0	0	0	0	1	DISP	REV	—	TST	GRAD	EX	LCDE	RAMS	Set the basic operation mode of the S-4581A.	W
R2	Horizontal display width register	0	0	0	1	0	← C/R →								Set the horizontal display width of each line.	W
R3	Horizontal synchronizing pulse width register	0	0	0	1	1	← YW →								Set the pulse width of the YCLK output for each line.	W
R4	Vertical line count register	0	0	1	0	0	← SLTL (Lower) →								Set the number of vertical lines of the LCD.	W
R5		0	0	1	0	1	* * * * * *						← (Upper) SLTH →		Set eight lower bits for SLTL and two upper bits for SLTH.	
R6	Screen display start address register	0	0	1	1	0	← SADL (Low order) →								Set the screen start address.	R/W
R7		0	0	1	1	1	← SADH (High order) →								Set eight lower bits for SADL and eight high-order bits for SADH.	R/W
R14 or R18	Gradation conversion code register GS1 (Note 2)	0 / 1	1 / 0	1 or 0	1 / 1	0 / 0	← GS1 →								Set gradation conversion code when gradations are displayed.	
R15 or R19	Gradation conversion code register GS2 (Note 2)	0 / 1	1 / 0	1 or 0	1 / 1	1 / 1	← GS2 →								4-gradation mode (C1, C0)=(0, 0)⇒GS0 (C1, C0)=(0, 1) ⇒GS1	
R17	Gradation conversion code register GS0	1	0	0	0	1	← GS0 →								(C1, C0)=(1, 0) ⇒GS2 (C1, C0)=(1, 1) ⇒GS3	
R20	Gradation conversion code register GS3	1	0	1	0	0	← GS3 →								8-gradation mode (C2, C1, C0)=(0, 0, 0) ⇒GS0	W
R21	Gradation conversion code register GS4	1	0	1	0	1	← GS4 →								(C2, C1, C0)=(0, 0, 1) ⇒GS1 (C2, C1, C0)=(0, 1, 0) ⇒GS2 (C2, C1, C0)=(0, 1, 1) ⇒GS3 (C2, C1, C0)=(1, 0, 0) ⇒GS4	
R22	Gradation conversion code register GS5	1	0	1	1	0	← GS5 →								(C2, C1, C0)=(1, 0, 1) ⇒GS5 (C2, C1, C0)=(1, 1, 0) ⇒GS6 (C2, C1, C0)=(1, 1, 1) ⇒GS7	
R23	Gradation conversion code register GS6	1	0	1	1	1	← GS6 →									
R24	Gradation conversion code register GS7	1	1	0	0	0	← GS7 →									
R25	FLM register	1	1	0	0	1	ENB ← FLM →								Set the number of M reversing frames when the tailing prevention circuit is activated.	W
R26	CL1 register	1	1	0	1	0	← CL1 →								Set the number of M reversing lines when the tailing prevention circuit is activated.	W
R27	SLS register	1	1	0	1	1	ENB ← SLS →								Set the number of shift lines for each frame when the tailing prevention circuit is activated.	W
R28 . . R31	Test register	1 . . 1	1 . . 1	1 . . 1	0 . . 1	0 . . 1									IC test register. If this area is accessed, the function defined in the specification document cannot be implemented. DO NOT access it.	DO NOT access it.

Remark: Only control register addresses A4 to A0 are decoded. A7 to A5 are ignored.

Note 1: R14/R18: When either the R14 or R18 address is pointed, a value can be written into the CSI register.
This also applies to R15/R19.