# VANGUARD SEMICONDUCTOR

**Division of California Micro Devices** **VN1225**

## MONOLITHIC HIGH-SPEED DUAL TRACK-AND-HOLD AMPLIFIER

### FEATURES

- Single-Chip Dual Track and Hold Amplifier
- Reduced Number of Power Supplies(±5V only)
- 25ns Acquisition Time (0.1%,1V Step)
- 20ns Track-and-Hold Settling Time
- 2ps Aperture Jitter
- 1mV pedestal Offset
- 20nV/μs Droop Rate
- 60dB Feedthrough Rejection Ratio
- ±70mA Output Current (for each output)
- Short Circuit Output Protection
- ECL Compatibility

### APPLICATIONS

- Subranging High Resolution A/D Conversion
- Flash A/D Converters
- Signal Deglitching of Video D/A Converters
- High Resolution Graphics
- High Speed Instrumentation
- Radar and Guidance Control Systems
- Medical Electronics

### GENERAL DESCRIPTION

Vanguard Semiconductor's single-chip VN1225 Dual Track-and-Hold amplifier is manufactured using a proprietary BiCMOS process technology that, combined with novel integrated circuit design techniques, provides an ideal device for high speed data acquisition applications.

The fully differential system VN1225 is a dual version of the VN1025 single-chip track-and-hold amplifier. The VN1225 contains two closed loop track-and-hold amplifiers with two gain stages per amplifier used to preserve high bandwidth with minimal phase margin degradation. A typical d.c. gain of 100dB ensures a minimum linearity of 10 bits over temperature and process variations, as well as full voltage swing. The low output impedance integrating amplifiers have been designed to minimize the overall phase margin degradation when driving 50 Ω output loads and includes short circuit output protection.

Available in 24-pin CERDIP, 24-pad LCC, and 24-pin SOIC, the VN1225 is guaranteed to operate over the commercial, industrial, and military temperature ranges.

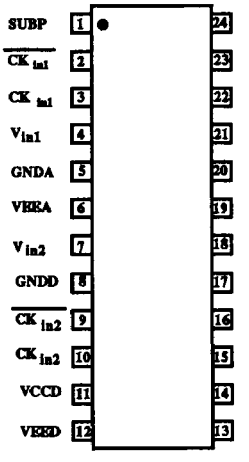
### PACKAGE OPTIONS

| Package Type | Temp. Range |
|---|---|
| 24-pin Cerdip | C, I, M |
| 24-pin SOIC | C |
| 24-pad LCC | C, I, M |

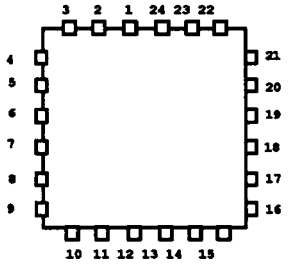
C = 0°C to +70°C
I = -40°C to +85°C
M = -55°C to +125°C

### PINOUT CONFIGURATIONS

24-PIN CERDIP



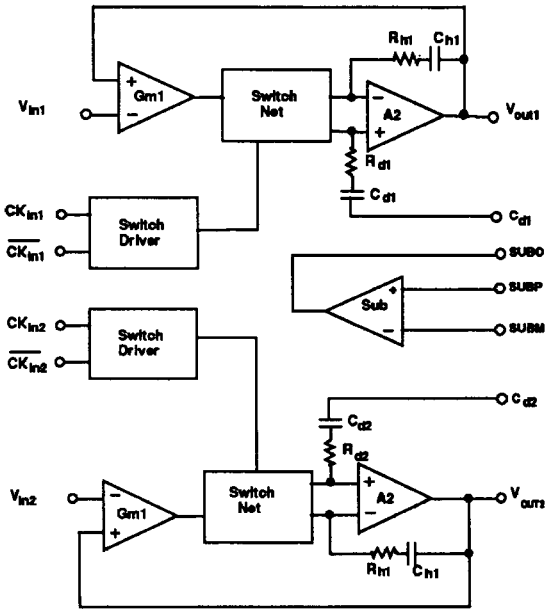

24 LCC




| | | | |
|---|---|---|---|
| 1 | VEEA | 13 | VEEAO |
| 2 | Vin2 | 14 | VOUT1 |
| 3 | GNDD | 15 | Cd1 |
| 4 | CKin2 | 16 | IADJ1 |
| 5 | CKin2 | 17 | VCCAO |
| 6 | VCCD | 18 | SUBO |
| 7 | VEED | 19 | SUBM |
| 8 | IADJ2 | 20 | SUBP |
| 9 | Cd2 | 21 | CKin1 |
| 10 | VOUT2 | 22 | CKin1 |
| 11 | GNDA | 23 | Vin1 |
| 12 | VCCA | 24 | GNDA |

**This is advance information and specifications are subject to change without notice**

### FUNCTIONAL BLOCK DIAGRAM




## ADVANCED PRODUCT INFORMATION

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## FUNCTIONAL DESCRIPTION

A full differential configuration internal to the devices balances the charge injection of the sampling switches during turn-off, while a common mode cancellation circuit provides CMRR of up to 65dB. To provide ease of interface to other system components, the VN1225 amplifiers feature a high input impedance with a low input capacitance of 1pF.

Featuring acquisition time of 25 nanoseconds, hold mode settling time of 20 nanoseconds, aperture jitter of 2 picoseconds, 1mV pedestal offset, and a very low droop rate of 20nV/µs, the VN1225 offers similar ac performance and superior dc characteristics than the more costly and less reliable hybrid solutions. The VN1225 significantly reduces board space requirement as it contains two high speed track-and-hold amplifiers on the same die, offering better performance and matching than combined hybrid devices.

The number of required bypass capacitors is also reduced since the VN1225 only requires ±5V power supplies, thus eliminating the need for additional high voltage supplies. The VN1225 outperforms other monolithic track-and-hold amplifiers by approximately two orders of magnitude, allowing designers to significantly upgrade sytem performance at minimal cost.

In addition to two independent track-and-hold amplifiers the VN1225 also includes a subtractor that can be independently used to perform arithmetic subtraction.

Compared to the VN1025, the VN1225 has four additional pins which are $C_d$, SUBN, SUBP and SUBO. All pins have ESD protection. SUBN and SUBP are inputs of the subtractor cell, while SUBO is its output. $C_d$ is used for arithmetic subtraction.

## APPLICATION DIAGRAMS

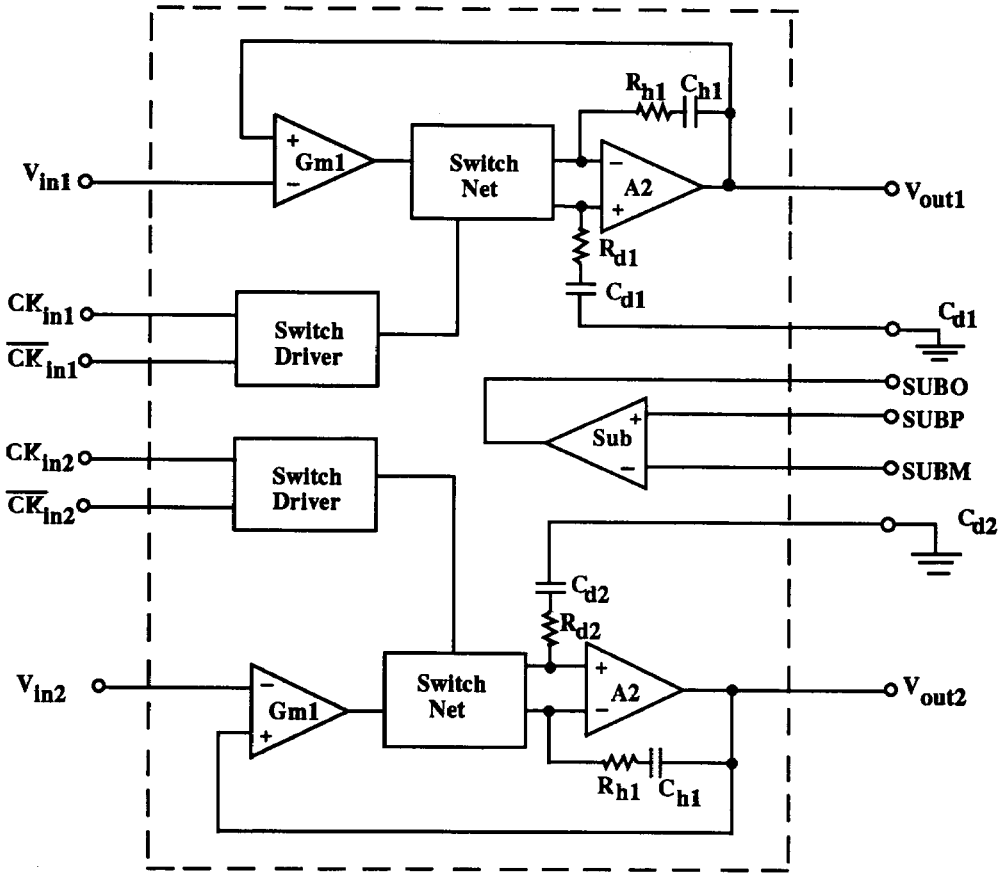


Fig.1 Two isolated and independent track and hold amplifiers with separate switch driver network and a subtractor.



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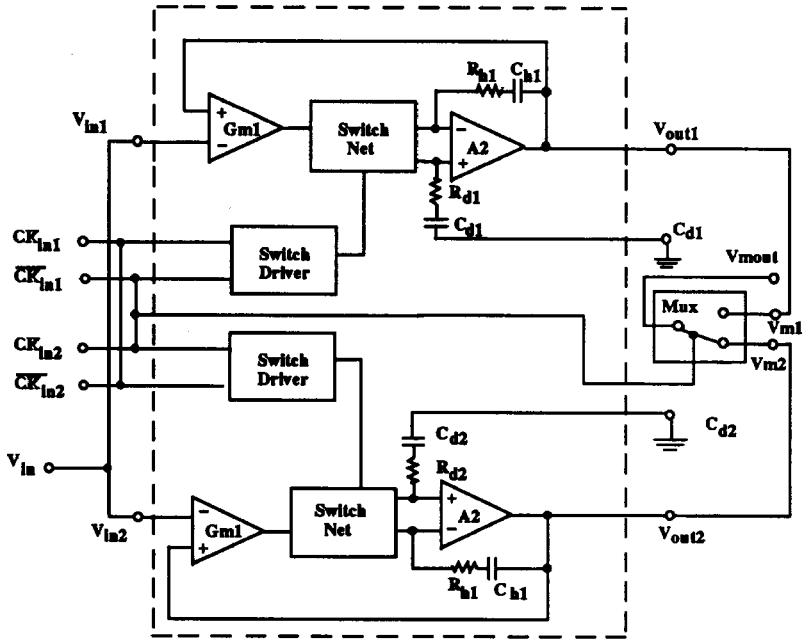


Fig.2 Multiplexed scheme to increase throughput times. When the first track-and-hold amplifier is in track mode, the other one is in hold mode.
Notes: Mux is an external device.
Subtractor cell is not displaced in this scheme.

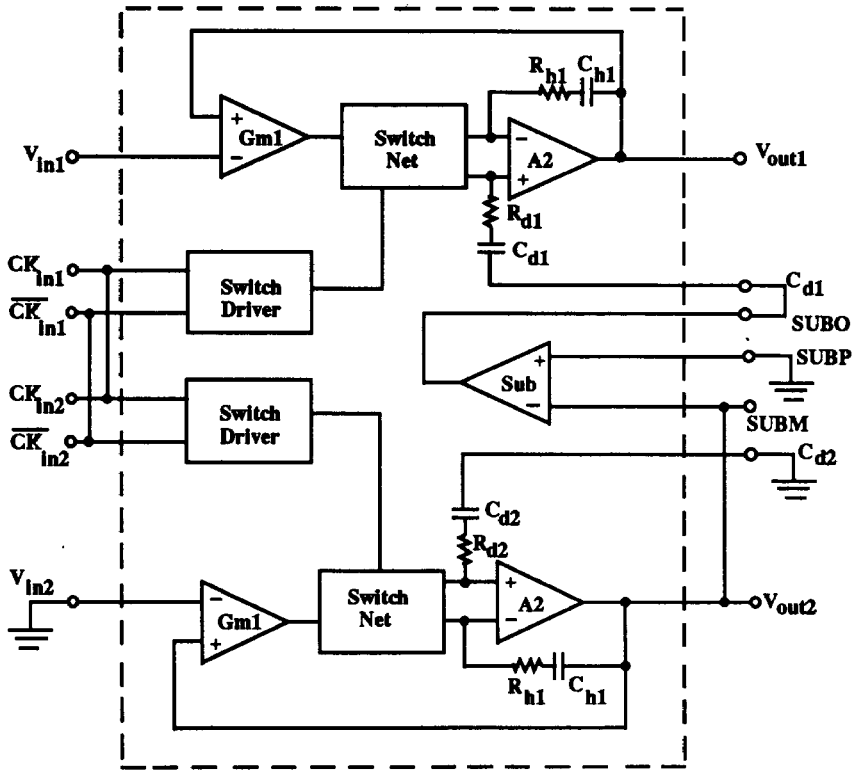


Fig.3 Two-stage single track-and-hold amplifier with 12-bit accuracy and reduced pedestal offset.


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## Absolute Maximum Ratings

| Rating | Symbol | Value |
|---|---|---|
| Supply Voltages | $V_S$ | ±7V |
| Analog Input Voltage | $V_{IN}$ | ±5V |
| Differential Input Voltage | $V_{diff}$ | ±3.5V |
| Digital Input Voltage | $V_{DIN}$ | 0V to -5V |
| Output Current | $I_O$ | ±150mA Continuous |
| Junction Temperature | $T_J$ | 150°C |
| Storage Temperature | $T_S$ | -60°C to +150°C |

**Note: Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.**

## Eletrical Characteristics

$V_S$ = ±5V, $R_L$ = 50Ω, $T_A$ = 25°C, Each Track-and-Hold Amplifier, Unless Otherwise Specified

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| ANALOG INPUT VOLTAGE | | | | | | |
| Voltage Range | $V_{IN}$ | | ±1 | ±2.5 | | V |
| Input Impedance | $R_{IN}$ | | 30 | 60 | | KΩ |
| Bias Current | $I_B$ | | | 10 | 100 | nA |
| Input Capacitance | $C_{IN}$ | | | 1 | 2 | pF |
| ECL-COMPATIBLE DIGITAL INPUT | | | | | | |
| Track Mode | $CK_{IN}$ | $CK_{IN}$=1, $CK_{INB}$=0 | -1.8 | -1.5 | | V |
| Hold Mode | $CK_{IN}$ | $CK_{IN}$=0, $CK_{INB}$=1 | | -1.1 | -0.5 | V |
| Input High Current | $I_{IH}$ | | | 3.0 | 10.0 | µA |
| Input Low Current | $I_{IL}$ | | | 3.0 | 10.0 | µA |
| ANALOG OUTPUT | | | | | | |
| Current (Short Circuit Protected) | $I_{OUT}$ | | ±50 | ±70 | | mA |
| Impedance | $R_{OUT}$ | | | 0.2 | 2.0 | Ω |
| Noise in Track Mode | $e_{TM}$ | Across Bandwidth | | 0.25 | 0.5 | mV(rms) |
| DC ACCURACY/STABILITY | | | | | | |
| Unity Gain Error | G | | | .001 | .01 | |
| Gain Non-Linearity | $G_{NL}$ | 1VNS Input | | 0.01 | | % |
| Initial Offset Voltage | $V_{os}$ | | | ±5.0 | ±10.0 | mV |
| Input Noise Voltage | $e_{IN}$ | f=1KHz | | 10 | | nV/√Hz |
| TRACK-MODE DYNAMICS | | | | | | |
| Small Signal Bandwidth | SSBW | | 100 | 300 | | MHz |
| Full Power Bandwidth | FPBW | | 60 | 80 | | MHz |
| Slew Rate | SR | | 300 | 500 | | V/µs |
| Harmonic Distortion | HD | 2Vpp @ 20 MHz | | - 44 | | dB |


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| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **TRACK-TO-HOLD SWITCHING** | | | | | | |
| Effective Aperture Delay | $t_{EAD}$ | | | 2 | | ns |
| Aperture Uncertainty | $t_{AUN}$ | | | 2 | | ps(rms) |
| Offset Step (Pedestal) | $P_{os}$ | | | 1 | 25 | mV |
| Temperature Coefficient | $\partial P_{os}/\partial T$ | | | 50 | 150 | µV/°C |
| Sensitivity to -5V | | | | 1 | 10 | mV/V |
| Switching Delay | $t_{SW}$ | | | 1.5 | | ns |
| Switching Transient | | | | | | |
| Amplitude | $TH_A$ | | | 30 | | mV |
| Settling to ±1mV | $TH_S$ | | | 20 | 30 | ns |
| **HOLD MODE DYNAMICS** | | | | | | |
| Droop Rate | DR | $T_A$=25 °C | | 20 | 50 | nV/µs |
| | | $T_A$=85°C | | 1.5 | | nV/µs |
| Temperature Variation | ∂DR/ ∂T | | | Double | | /10°C |
| Feedthrough Rejection | $FT_R$ | Vpp=2V@20MHz | 55 | 60 | | dB |
| **HOLD-TO-TRACK DYNAMICS** | | | | | | |
| Acquisition Time | $t_{AQ1}$ | Vpp=1V | | | | |
| to ±1% | | | | 15 | 20 | ns |
| to ±0.1% | | | | 25 | 35 | ns |
| Acquisition Time | $t_{AQ2}$ | Vpp=2V | | | | |
| to ±1% | | | | 20 | 27 | ns |
| to ±0.1% | | | | 30 | 40 | ns |
| **TOTAL POWER REQUIREMENTS** | | | | | | |
| $V_{CCA}$ (+5V ±0.5V) | $I_{CCA}$ | | | 40 | 60 | mA |
| $V_{EEA}$ (-5V ±0.5V) | $I_{EEA}$ | | | 40 | 60 | mA |
| $V_{CCD}$ (+5V ±0.5V) | $I_{CCD}$ | | | 10 | 15 | mA |
| $V_{EED}$ (-5V ±0.5V) | $I_{EED}$ | | | 10 | 15 | mA |
| $V_{CCAO}$ (+5V ±0.5V) | $I_{CCAO}$ | | | 50 | 75 | mA |
| $V_{EEAO}$ (-5V ±0.5V) | $I_{EEAO}$ | | | 50 | 75 | mA |
| Total Supply Current | $I_{SB}$ | | | 100 | 150 | mA |
| Total Power Dissipation | $P_D$ | | | 1 | 1.5 | W |
| Power Supply Rejection Ratio | PSRR | | | 2 | 3 | mV/V |
| **INTERCHANNEL FEATURES** | | | | | | |
| Interchannel Isolation | | $V_{IN}$ = ±1V, 100KHz | 80 | 86 | | dB |
| Interchannel Aperture Offset | | | | 10 | 30 | ps |
| Interchannel Offset Voltage | | | | 0.1 | 2 | mV |
| **SUBTRACTOR SECTION** | | | | | | |
| Current Output | $I_{OUT}$ | | | 2 | | mA |
| Input Bias Current | $I_B$ | | | 6 | | µA |
| Gain | G | | | -1 | | |
| Small Signal Bandwidth | SSBW | | 100 | 200 | | MHz |
| Noise Across Bandwidth | $e_{in}$ | | | 0.25 | | mV(rms) |
| Input Impedance | $R_{IN}$ | | | 100 | | KΩ |
| Input Capacitance | $C_{IN}$ | | | 1 | | pF |
| Offset Voltage | $V_{OS}$ | | | 1 | | mV |
| Slew Rate | SR | | 300 | 500 | | V/µs |



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## PARAMETER DEFINITION

**Initial Offset Voltage** - The output voltage in track mode when the input signal is grounded.

**Gain Non-Linearity** - The deviation from a straight line on the input versus held output transfer characteristics. This parameter is given as a percentage of the maximum analog input voltage.

**Gain Error** - The voltage gain deviation during the sample mode over the full scale voltage range. Ideal gain is assumed to be unity.

**Small Signal Bandwidth** - The frequency at which the voltage gain is 3dB below its dc value when the input signal is a sinusoidal waveform with amplitude equal to the fall scale voltage range.

**Acquisition Time** - The time required to acquire a full scale input step within a specified error range during track mode.

**Analog Delay** - The time required for an analog input signal to propagate to the analog output.

**Effective Aperture Delay Time** - The time between the propagation delays on the analog input and the digital switch control logic. This parameter indicates the point in time when input signal is actually held relative to the hold command input.

**Aperture Uncertainty** - The sample-to-sample variation in effective aperture delay time due to noise in the switch control logic. This parameter is also referred to as aperture uncertainty and causes an error in the output voltage which is dependent on the slew rate of the input signal.

**Droop Rate** - A change in the output voltage during the hold mode due to leakage currents in the holding capacitor.

**Feedthrough Rejection** - The change in the output signal during the hold mode when a full scale sinusoidal waveform is applied at the input as a funtion frequency.

**Offset Step (Pedestal)** - The output voltage offset caused by switching to hold mode. Charge injection in the storage capacitor and other internal offsets are the major contributors.

**Track-to-Hold Settling Time** - The time required for the output to settle within a specified range referenced to the hold command input signal.

**Track-to-Hold Switching delay** - The time required for the output signal to start changing as a result of a track command.

### Typical Waveforms