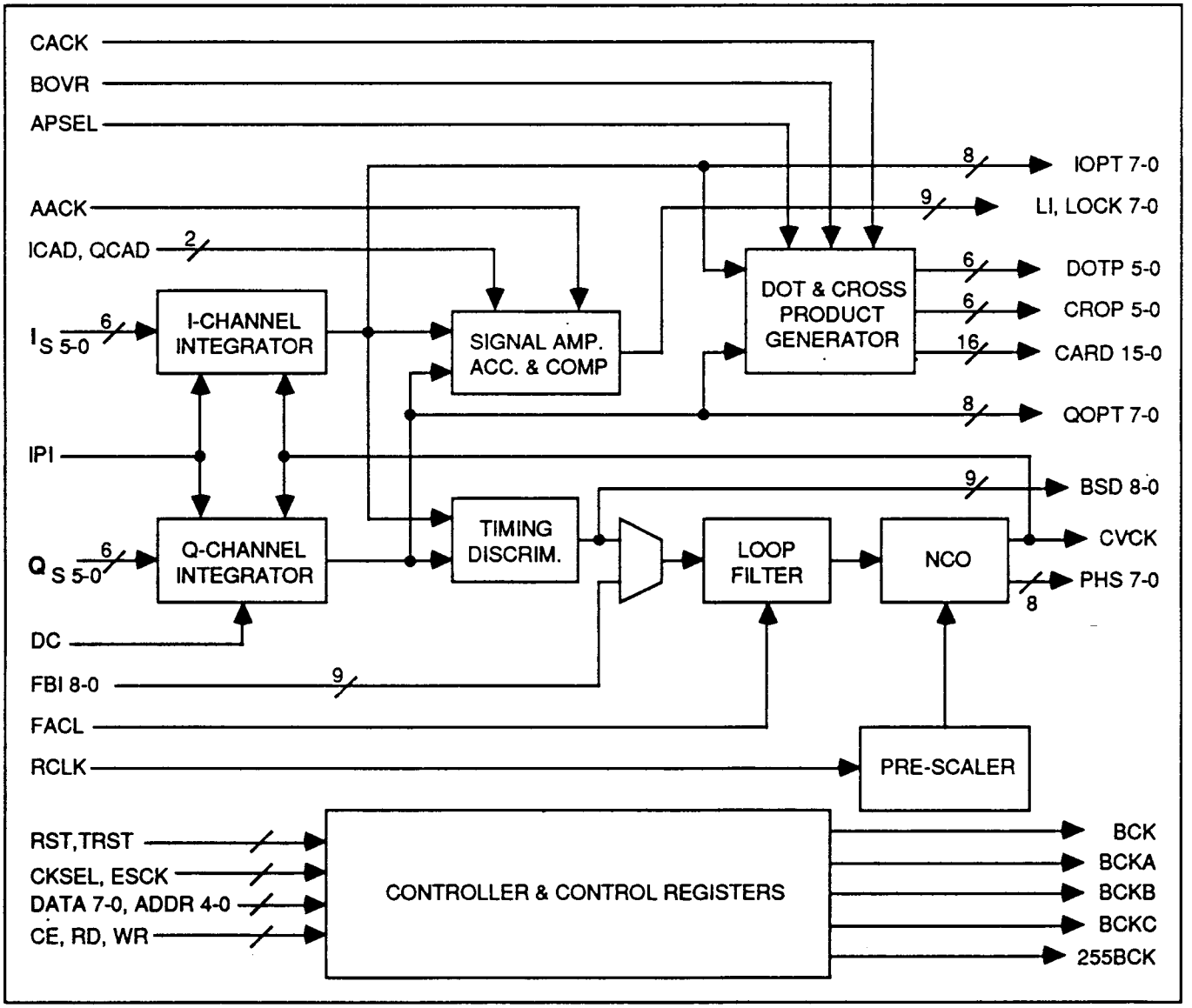
FEATURES

- UP TO 6 Mbps OPERATION IN BPSK MODE AND 12 Mbps IN QPSK MODE
- CARRIER TRACKING FEEDBACK WITH PLL OR AFC OUTPUTS
- BIT TIMING DRIVEN BY NUMERICALLY CONTROLLED OSCILLATOR
- PROGRAMMABLE 2ND ORDER LOOP
- PROGRAMMABLE DATA RATES
- DPSK OUTPUT AVAILABLE

FUNCTIONAL DESCRIPTION

The STEL-2110A Bit Synchronizer/PSK Demodulator provides bit timing to control the sampling of the signal in a receiver as well as a feedback signal to control the frequency of the local oscillator. It can be used in high speed coherent PSK, QPSK and DPSK modems in either continuous carrier or burst carrier (TDMA) environments. Soft decision output data is provided to facilitate the inclusion of Forward Error Correction (FEC) using convolutional coding and Viterbi decoding into the system.

BLOCK DIAGRAM

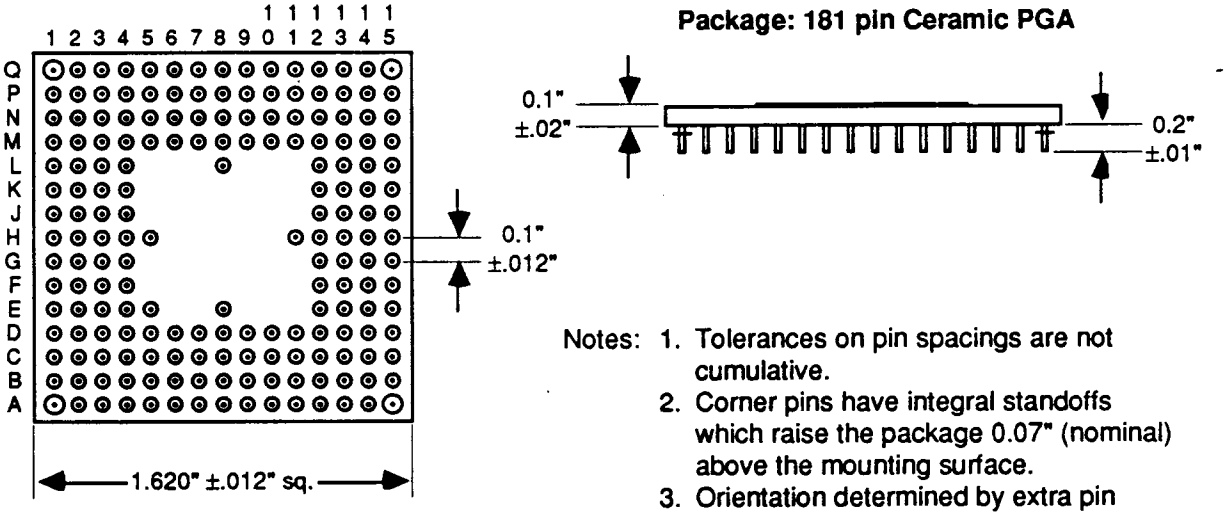


CIRCUIT DESCRIPTION

The bit synchronizer (clock recovery) portion of the STEL-2110A is a digital phase locked loop which operates by integrating the input signals in both the **I** and **Q** channels over one symbol period. This is done 3 times; in addition to the nominally "on time" integration, "quarter period early" and "quarter period late" integrations are also carried out. The difference between the last two gives an indication of the timing error, since the averaged difference will be zero when the timing is correct. This signal is used to drive a numerically controlled oscillator which produces the clock signals to drive the entire circuit as well as sampling the incoming signals. The signals can also be integrated prior to the main timing integrators, to improve the performance The number of accumulations per symbol in this section is controlled by the pre-accumulation control factor, A_1. This pre-accumulation factor can be set to one, two four, eight or sixteen times. The optimally integrated **I** and **Q** signals are used to derive a DPSK output and a feedback signal to control the local oscillator for carrier tracking. This signal can be selected to be a phase locked loop (PLL) control signal or an automatic frequency control (AFC) signal. The former is intended for coherent demodulation in continuous carrier systems, and the latter is intended for use where fast acquisition is required, e.g., in burst carrier systems, such as TDMA, where the acquisition time of a PLL would cause significant loss of data at the beginning of each burst. An STEL-2210 Block Phase Estimator can be used to compensate for the residual phase roll in burst applications. A lock indicator output is also derived from the **I** and **Q** data which gives an indication of when the clock recovery circuit is within 1/4 of a symbol of optimum timing. The STEL-2110A is designed for maximum flexibility and can be used in staggered QPSK as well as non-staggered QPSK systems.

Several options are available with the STEL-2110A. The internal bit timing can be bypassed allowing external timing to be used. This allows two or more devices to be slaved together. The timing discriminator loop filter can also be internal or external, giving the maximum flexibility for loop design.

PACKAGING INFORMATION



Notes:
1. Tolerances on pin spacings are not cumulative.
2. Corner pins have integral standoffs which raise the package 0.07" (nominal) above the mounting surface.
3. Orientation determined by extra pin at location E5.
4. See page 4 for pin connections.

PIN CONNECTIONS See Page 3 for description of layout of pins on package.

Note: I.C. denotes Internal Connection. Do not use as vias.

A1	V_{DD}	D1	BSD_1	H11	V_{SS}	N1	TRST
A2	$QOPT_7$	D2	BSD_7	H12	$DATA_2$	N2	$LOCK_3$
A3	$QOPT_6$	D3	IPI	H13	V_{DD}	N3	V_{DD}
A4	$QOPT_5$	D4	N.C.	H14	$CARD_5$	N4	PHS_3
A5	$QOPT_4$	D5	V_{DD}	H15	$CARD_{10}$	N5	PHS_2
A6	$QOPT_3$	D6	CACK			N6	PHS_1
A7	$QOPT_2$	D7	V_{DD}	J1	$LOCK_1$	N7	PHS_0
A8	$QOPT_1$	D8	V_{SS}	J2	$LOCK_7$	N8	V_{SS}
A9	$CROP_0$	D9	$CROP_5$	J3	I_{S4}	N9	RCLK
A10	$CROP_1$	D10	I.C.	J4	I_{S0}	N10	V_{SS}
A11	V_{SS}	D11	V_{DD}	J12	$DATA_1$	N11	255BCK
A12	$CROP_2$	D12	$DATA_6$	J13	$CARD_1$	N12	CVCK
A13	$CROP_3$	D13	WR	J14	V_{SS}	N13	V_{SS}
A14	$CROP_4$	D14	BOVR	J15	$CARD_{11}$	N14	$CARD_9$
A15	N.C.	D15	I.C.			N15	N.C.
				K1	$LOCK_0$		
B1	BSD_0	E1	BSD_2	K2	$LOCK_6$	P1	N.C.
B2	$QOPT_0$	E2	BSD_8	K3	I_{S5}	P2	$LOCK_2$
B3	V_{DD}	E3	QCDD	K4	I_{S1}	P3	PHS_7
B4	FBI_0	E4	Q_{S3}	K12	$DATA_0$	P4	PHS_6
B5	FBI_1	E8	V_{SS}	K13	$CARD_2$	P5	V_{SS}
B6	FBI_2	E12	$DATA_5$	K14	$CARD_6$	P6	PHS_5
B7	FBI_3	E13	RD	K15	$CARD_{12}$	P7	PHS_4
B8	FBI_4	E14	$ADDR_3$			P8	BCK
B9	I.C.	E15	I.C.	L1	V_{DD}	P9	V_{SS}
B10	I.C.			L2	$LOCK_5$	P10	BCKA
B11	I.C.	F1	BSD_3	L3	V_{SS}	P11	V_{SS}
B12	I.C.	F2	FACL	L4	I_{S2}	P12	BCKB
B13	I.C.	F3	V_{SS}	L8	V_{SS}	P13	V_{SS}
B14	I.C.	F4	Q_{S2}	L12	$CARD_0$	P14	BCKC
B15	I.C.	F12	$DATA_4$	L13	$CARD_3$	P15	$CARD_{15}$
		F13	CE	L14	$CARD_7$		
C1	N.C.	F14	$ADDR_2$	L15	$CARD_{13}$	Q1	AACK
C2	BSD_6	F15	I.C.			Q2	$IOPT_5$
C3	FBI_5			M1	CKSEL	Q3	$IOPT_4$
C4	FBI_6	G1	BSD_4	M2	$LOCK_4$	Q4	$IOPT_3$
C5	FBI_7	G2	LI	M3	ICDD	Q5	$IOPT_2$
C6	FBI_8	G3	Q_{S5}	M4	I_{S3}	Q6	$IOPT_1$
C7	I.C.	G4	Q_{S1}	M5	V_{DD}	Q7	$IOPT_0$
C8	$ADDR_4$	G12	$DATA_3$	M6	$IOPT_7$	Q8	$DOTP_0$
C9	RST	G13	$DATA_7$	M7	$IOPT_6$	Q9	V_{DD}
C10	I.C.	G14	$ADDR_1$	M8	V_{DD}	Q10	$DOTP_1$
C11	I.C.	G15	I.C.	M9	N.C.	Q11	$DOTP_2$
C12	I.C.			M10	N.C.	Q12	$DOTP_3$
C13	$ADDR_0$	H1	BSD_5	M11	V_{SS}	Q13	$DOTP_4$
C14	APSEL	H2	DC	M12	ESCK	Q14	$DOTP_5$
C15	I.C.	H3	Q_{S4}	M13	$CARD_4$	Q15	V_{DD}
		H4	Q_{S0}	M14	$CARD_8$		
		H5	V_{SS}	M15	$CARD_{14}$		

INPUT SIGNALS

I_{S5-0} (Pins J4, K4, L4, M4, J3, K3)
Six-bit sampled in-phase input signal in "offset 2's complement" format (see page 9). The signal is sampled on the rising edge of the **CVCK** output.

Q_{S5-0} (Pins H4, G4, F4, E4, H3, G3)
The quadrature-phase input signal has the same specifications as I_{S5-0}.

IPI (Pin D3)
Input Polarity Invert. When this input is high the I_S and Q_S inputs are multiplied by minus one.

ICDD (Pin M3)
I Channel Discriminator Disable. A high level on this input causes the in-phase signal to be disabled from the timing discriminator output.

QCDD (Pin E3)
Q Channel Discriminator Disable. A high level on this input causes the quadrature-phase signal to be disabled from the timing discriminator output.

DC (Pin H2)
Delay Control. A high level on this input causes the Q_S inputs to be delayed by one half of a symbol period (2 or 4 clock cycles, depending on whether the 4 or 8 clocks per symbol mode is selected) relative to the I_S inputs. This control is intended to enable the chip to be used for offset QPSK signals when coherent carrier tracking preceeds the demodulator.

RST (Pin C9)
Reset. A low level on this signal forces the demodulator to a predefined state. See the specification of the I/O bus and registers for a description of the initial conditions. The chip must then be restarted with an external clock after a reset as shown in the descriptions of **CKSEL** and **ESCK**.

TRST (Pin N1)
Timing Reset. A low level on this signal forces the timing circuits to their initial conditions, in which the timing signals are set to the first $^1/_8$ period of the symbol time. No other functions are initialized with this signal.

CKSEL (Pin M1)
Clock Select. A low level on this signal selects the **ESCK** to control demodulator timing in place of the clock generated by the NCO in the demodulator. This capability, in conjunction with the **TRST** signal, enables two or more demodulators to operate in parallel with one controlling the timing and the others slaved to this timing. This pin must be set low after power up and after any time the chip is reset with the **RST** input until a non-zero frequency has been loaded into the bit timing NCO. **CKSEL** can then be set high.

ESCK (Pin M12)
External Sample Clock. This externally generated clock should nominally be a square wave at 4 to 128 times the symbol rate, depending on S_s, the number of samples per symbol, and A_f, the Pre-Accumulation Control Factor. When **CKSEL** is low **ESCK** controls the timing of the demodulor, otherwise the **CVCK** generated by the internal NCO controls timing of the demodulator. When using an external clock, the **CVCK** signal is still valid, and should be used to sample the data at the A/D converters. The **CVCK** output will be delayed relative to the **ESCK** input by about 5 nsecs. When this capability is not being used in the system an external clock such as **RCLK** must be connected to this input to start up the chip after power-up and after a reset.

FBI_{8-0} (Pins B4-8, C3-6)
Feedback Inputs. This 9-bit input signal in "offset two's complement" format provides the input to the bit timing loop filter when Bit-1 in Address 7 is set to a logic 1. In this mode, other signals may be be connected to the loop filter for feedback applications other than bit synchronization. In this case, the **PHS** outputs of the NCO would be used as the feedback controlling elements.

APSEL (Pin C14)
AFC/PLL Select. A high level on this signal causes the carrier tracking logic to use a noncoherent AFC algorithm to perform carrier tracking. A low level causes the discriminator to use phase information to implement a phase locked loop, enabling coherent demodulation to be performed.

BOVR (Pin D14)
BPSK Override. If the received signal is modulated in QPSK format, this signal should be set low. If the modulation technique is limited to ±180° phase transitions, then the **BOVR** signal should be set high to provide improved carrier tracking performance.

AACK (Pin Q1)
Amplitude Accumulate Clock. This signal controls the number ot integrations used in the signal detection function. When this signal is low, the accumulator continues to accumulate. To end the accumulation

period, this signal should be set high for at least one full symbol period. This causes the output of the accumulator to be saved and held, while the accumulator itself is cleared. Timing output signals such as **255BCK** may be connected directly to this input. The accumulator will operate for a minimum of 256 clock cycles without overflowing, depending on the level of the signal.

CACK (Pin D6)
Carrier Accumulate Clock. This signal controls the number ot integrations used in the carrier tracking discriminator function. When this signal is low, the accumulator continues to accumulate. To end the accumulation period, this signal should be set high for at least one full symbol period. This causes the output of the accumulator to be saved and held, while the accumulator itself is cleared. Timing output signals such as **255BCK** may be connected directly to this input. The accumulator will operate for a minimum of 64 cycles without overflowing. However, under typical operating conditions the number of cycles will be several hundred, since the noise component will be uncorrelated and will not accumulate.

FACL (Pin F2)
Frequency Accumulator Clear. A low level on this input forces the frequency accumulator to zero without affecting any other registers.

RCLK (Pin N9)
Reference Clock. This nominally square wave input signal may have a frequency up to 75 MHz.

OUTPUT SIGNALS

CVCK (Pin N12)
Converter Clock. This signal is generated by the NCO within the demodulator is nominally a square wave and is used extensively within the demodulator. It is provided as an output to control the timing of A/D converters which precede the demodulator. The A/D converters should begin a new conversion on the rising edge of this signal and hold the output from that conversion stable until a new conversion is initiated.

PHS_{7-0} (Pins N7-4, P7-6, P4-3)
Phase. This 8-bit output is the phase of the bit-timing NCO which drives the **CVCK** output. It changes every cycle of the NCO clock, which is the **RCLK** divided by the pre-scaler factor, C_s. This output is provided as a secondary output to be used in applications other than bit timing; its primary use is device testing.

$IOPT_{7-0}$ (Pins Q7-2, M7-6)
The 8-bit synchronized In-phase output is provided in "offset two's complement" format. It is the integrated value of the I_S input samples. When S_s, (the number of samples per symbol) is set to eight this output is the integration of eight I_S inputs divided by two. This output is stable for one period of **CVCK** before and after the rising edge of **BCK**. There is a delay of four periods of **BCK** between a symbol entering at I_S and Q_S and that same symbol appearing at **IOPT** and **QOPT**.

$QOPT_{7-0}$ (Pins B2, A8-2)
The 8-bit synchronized quadrature-phase output has the same specifications as **$IOPT_{0-7}$**

BCK (Pin P8)
Bit Clock. This signal is synchronized to the input symbol timing and is nominally a square wave. The signal is low during the first half of the symbol.

BCKB (Pin P12)
Bit Clock B. This signal is a rectangular pulse which is synchronized to the input symbol timing. The signal goes high one cycle of **CVCK** before the beginning of the symbol period for a period of one **CVCK** cycle.

BCKA (Pin P10)
Bit Clock A. This signal is similar to **BCKB** but goes high 1/4 of a symbol period earlier.

BCKC (Pin P14)
Bit Clock C. This signal is similar to **BCKB** but goes high 1/4 of a symbol period later.

255BCK (Pin N11)
1/255 Bit Clock. This signal goes high for one symbol time once every 255 symbol periods, starting with the 255th symbol period after the falling edge of **TRST**.

LI (Pin G2)
The signal appearing at the Lock Indicator output is the sign bit of the integrated value of the **$LOCK_{7-0}$** output. This signal goes to a logic one when the system is within ±1/4 symbol of optimium timing.

BSD_{8-0} (Pins B1, D1, E1, F1, G1, H1, C2, D2, E2)
Bit Sync Discriminator. The 9-bit output of the bit sync discriminator is provided in "offset twos complement" format. It is updated once per symbol period and is intended to be connected directly to the **FBI** port in normal operation. When bit 1 in the Mode Control Register is set to zero (the reset value) this connection is made internally, and the **BSD_{8-0}** and **FBI_{8-0}** signals are not used.

$LOCK_{7-0}$ (Pins K1, J1, P2, N2, M2, L2, K2, J2)
The **$LOCK_{7-0}$** output bus is used as a **lock** indicator. It provides the value:

$$|I| + |Q| - 1/2(|I_{early}| + |Q_{early}| + |I_{late}| + |Q_{late}|)$$

This 8-bit signed number will be positive when the symbol timing is within lock (±1/4 symbol of optimium timing) and will have a maximum value at the perfect lock point.

$DOTP_{5-0}$ (Pins Q9,Q10-14)
Dot Product. The 6-bit truncated and limited dot product result is presented in "offset twos complement" format. This result is updated once per symbol period. The dot product represents the demodulated DPSK data, and is the function $I_n * I_{n-1} + Q_n * Q_{n-1}$. The 5 LSBs of the 13-bit dot product are discarded, and the 6-bit output is caused to saturate on overflow.

$CROP_{5-0}$ (Pins A9-10, A12-14, D9)
Cross Product. The 6-bit truncated and limited cross product result is presented in "offset twos complement" format. This result is updated once per symbol period. This function is used internally, and although it can be used as a discriminator, it is not normally used externally. The function $I_n * Q_{n-1} - Q_n * I_{n-1}$. The 5 LSBs of the 13-bit dot product are discarded, and the 6-bit output is caused to saturate on overflow.

$CARD_{15-0}$ (Pins L12, J13, K13, M13, H14, K14, L14, M14, N14, H15, J15, K15, L15, M15, P15)
Carrier Discriminator. The 16-bit discriminator signal is presented in "offset twos complement" format, and is updated once per **CACK** period. The maximum magnitude of this signal is a function of the signal level and the clock selected for the **CACK**. This signal can be used directly to drive a digital loop filter which in turn controls a numerically controlled oscillator (NCO) to generate the local oscillator signal. Alternatively, a subset of these bits can be connected to a D/A converter to drive an analog loop filter which in turn drives the frequency control of a VCO for the local oscillator. **$CARD_{15-0}$** can be either a phase discriminator for PLL operation or a frequency discriminator for AFC depending on the state of **APSEL**.

I/O BUS SIGNALS

$DATA_{7-0}$
(Pins K12, J12, H12, G12, F12, E12, D12, G13)
An 8-bit bidirectional data bus is used for writing and reading information to and from the demodulator.

CE (Pin F13)
Chip Enable. When this signal is high the **RD** and **WR** signals are disabled. When it is low data can be transferred to and from the chip under control of the **RD**, **WR** and **ADDR(0-3)** signals.

RD (Pin E13)
Read. When this input and **CE** are both low information can be read from the demodulator on the **DATA** bus. The state of the **ADDR** bus determines which data is available on the bus, as defined in pages 8 to 10.

WR (Pin D13)
Write. When this input and **CE** are both low information can be written to the device. The state of the **ADDR** bus determines which registers are written to, as defined in pages 8 to 10.

$ADDR_{4-0}$ (Pins C13, G14, F14, E14, C8)
Address. The 5-bit address bus defines which register will be the source or destination of I/O information, as defined in pages 8 to 10.

MISCELLANEOUS

V_{SS} (Pins A11, D8, E8, F3, H5, H11, J14, L3, L8, M11, N8, N10, N13, P5, P9, P11, P13)
Negative power supply, normally connected to ground.

V_{DD} (Pins A1, B3, D5, D7, D11, H13, L1, M5, M8, N3, Q9, Q15)
Positive power supply, normally connected to +5 volts.

N.C. (Pins A15, C1, M9-10, N15, P1)
No connection. Can be used as vias.

TEST (Pins B9-15, C7, C10-12, C15, D15, E15, F15, G15)
Used for test purposes, do NOT use as vias.

CONTROL REGISTER SPECIFICATION

Caution: Do not write to undocumented addresses. Addtional registers exist for test purposes, and writing to them can result in a malfunction.

INPUT DATA

The following information can be written into the device by selecting the appropriate address A(n) and writing bit B(m):

Address 10_H: Timing Control Register.
Reset Value: 01_H.

Bit 0: Bit 0 controls S_s, the number of samples per symbol. B(0) =1 sets $S_s = 8$ *; B(0) = 0 sets $S_s = 4$.

Bit 1: Bit 1 controls P_a, the number of accumulations of the discriminator just prior to the loop filter.
Bit 1 = 0 sets $P_a = 1$ *; Bit 1 =1 sets $P_a = 4$.
Note: This bit **must** be set to 1 when the symbol rate is greater than $1/28$ times the NCO clock frequency, f_c.

Bits 2, 3, and 4: These bits control the NCO Clock Prescale Factor, C_s. The clock provided to the NCO is divided by the following scale factors:

Bit 4	Bit 3	Bit 2	C_s
0	0	0	1 *
0	0	1	4
0	1	0	16
0	1	1	64
1	0	0	256
1	0	1	1024
1	1	0	4096
1	1	1	16384

Bits 5, 6, and 7: These bits control the Pre-Accumulation Control Factor, A_1

Bit 7	Bit 6	Bit 5	A_1
0	0	0	1 *
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16

Address 11_H: Loop Gain Control Register.
Reset Value: $B7_H$. (See section on Feedback Loop Parameters for a description of loop performance and an explanation of K_1 and K_2.)

* Default values

Bits 0, 1, 2, and 3: These bits control the Gain Control Factor K_1 as shown in the table:

Bit 3	Bit 2	Bit 1	Bit 0	K_1
0	0	0	0	2^0
0	0	0	1	2^1
0	0	1	0	2^2
0	0	1	1	2^3
0	1	0	0	2^4
0	1	0	1	2^5
0	1	1	0	2^6
0	1	1	1	2^7 *
1	0	0	0	2^8
1	0	0	1	2^9
1	0	1	0	2^{10}
1	0	1	1	2^{11}
1	1	0	0	2^{12}
1	1	0	1	2^{13}
1	1	1	0	2^{14}
1	1	1	1	2^{15}

Bits 4, 5, 6, and 7: These bits control the Gain Control Factor K_2 as shown in the table:

Bit 7	Bit 6	Bit 5	Bit 4	K_2
0	0	0	0	2^{-4}
0	0	0	1	2^{-3}
0	0	1	0	2^{-2}
0	0	1	1	2^{-1}
0	1	0	0	2^0
0	1	0	1	2^1
0	1	1	0	2^2
0	1	1	1	2^3
1	0	0	0	2^4
1	0	0	1	2^5
1	0	1	0	2^6
1	0	1	1	2^7 *
1	1	0	0	2^8
1	1	0	1	2^9
1	1	1	0	2^{10}
1	1	1	1	2^{11}

* Default values

INPUT DATA (Cont.)

Addresses 12_H, 13_H, and 14_H: Bit Rate Control Register.
Reset Value: 000000_H. The 27-bit NCO is programmed with these 3 bytes, which are loaded into the 24 MSBs of the 27-bit Δ-Phase Register. Bit 7 of Address 12_H is the MSB, and Bit 0 of Address 14_H is the LSB. The formula for N_r, the number programmed in the NCO, is as follows:

$$A_r = R_s \times S_s \times A_i$$

$$N_r = (^1/f_c) \times R_s \times S_s \times A_i \times 2^{24}$$

where:

N_r : 24 bit number which establishes the nominal A/D sample rate
f_c: NCO input clock frequency (after scaling the input clock by C_s)
A_r : A/D converter clock rate
R_s: Symbol rate of PSK information to be demodulated
S_s: Number of accumulated samples per symbol (4 or 8)
A_i: Number of front end accumulations (1,2,4,8 or 16)

CAUTION: The NCO is not double buffered and will immediately switch to the newly programmed frequency after any of the bytes are changed. **The NCO output is used internally in the NCO loading process. Do not set the 24-bit data to be 000000_H at any time as this will set the NCO output frequency to zero, causing the entire chip to freeze up, requiring CSEL to be set low in order to restart it.** If it is necessary to set any byte to zero, the other non-zero bytes should be loaded first, followed by the zero-value byte.

Addresses 15_H and 16_H: Not used.

Address 17_H: Mode Control Register.
Reset Value: 81_H. This register is used to store various control parameters, as shown :

Bit 0: Input Data Format Control. When this bit is set to a zero the I_{S5-0} and Q_{S5-0} input data must be in "Offset Two's Complement format (see figure below), and when it is set to a one (default value) the data must be in offset binary format.

Bit 1: Loop Filter Input Control. When this bit is set to a zero (default value) the output of the bit-timing discriminator is connected to the loop filter, and when it is set to a one the FBI_{S-0} inouts are connected to the loop filter.

Bit 2: Coherent DPSK Enable. When this bit is set to a one the **Q** arm of the dot product generator is disabled, permitting differential detection of the data in the I channel only. The default value is zero.

Bit 3: Freeze Data Control. On the rising edge of this bit all the data to be read out of the STEL-2110A output registers is frozen and may then be read at any time. The data latches are edge triggered, and new data will be written only after a rising edge on this bit, meaning that it must be reset to zero each time before it can be set to one again.

Bits 4, 5, and 6: Loop Offset Control. These three bits define a phase offset for the symbol tracking loop, as shown in the table:

Bit 6	Bit5	Bit4	Offset (symbols)
1	1	1	$-^3/_4$
1	1	0	$-^1/_2$
1	0	1	$-^1/_4$
X	0	0	0
0	0	1	$+^1/_4$
0	1	0	$+^1/_2$
0	1	1	$+^3/_4$

The default value is zero.

Bit 7: Software reset. When this bit set to zero a reset will occur, exactly as if the reset line was set to a logic zero. The bit will automatically clear itself after 4 cycles of the **CVCK** signal. The default value is one.

OUTPUT DATA

Address 00_H: I Data Register. The 8-bit I (in-phase) data word is stored in this byte.

Address 01_H: Q Data Register. The 8-bit Q (quadrature-phase) data word is stored in this byte.

Addresses 02_H and 03_H: Carrier Discriminator Register. The 16-bit output of the carrier discriminator ($CARD_{15-0}$) is stored in these two bytes, as well as being available directly on the CARD bus. Bit 7 in Address 02_H is the MSB and Bit 0 in Address 03_H is the LSB.

Addresses 10_H, 11_H, 12_H, and 13_H: Frequency Accumulator Register. The 27 bits of the frequency accumulator in the loop filter are available in these 4 bytes. Bit 2 in Address 10_H is the MSB and Bit 0 in Address 13_H is the LSB.

Addresses 14_H and 15_H: Signal Level Register. The 16 bits of the signal amplitude accumulator are presented in these 2 bytes. Bit 7 in Address 14_H is the MSB and Bit 0 in Address 15_H is the LSB.

Addresses 16_H and 17_H: Dot Product Register. The 13-bit dot product result is presented in these 2 bytes. Bit 4 in Address 16_H is the MSB and Bit 0 in Address 17_H is the LSB.

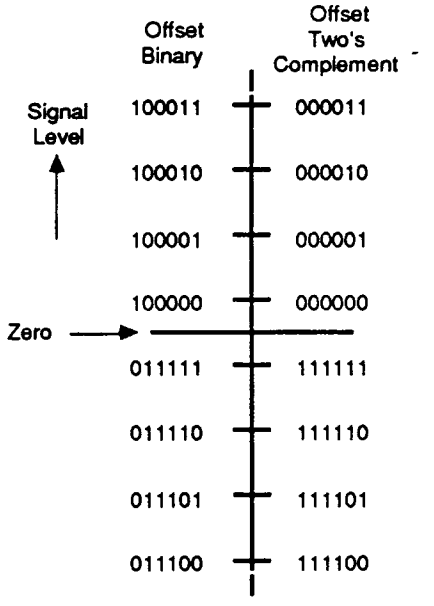
Addresses 18_H and 19_H: Cross Product Register. The 13-bit dot product result is presented in these 2 bytes. Bit 4 in Address 18_H is the MSB and Bit 0 in Address 19_H is the LSB.

Addresses $1A_H$ and $1B_H$: Carrier Discriminator Register. The 13 input bits to the carrier discriminator accumulator are presented in this byte. Bit 4 in Address $1A_H$ is the MSB and Bit 0 in Address $1B_H$ is the LSB.

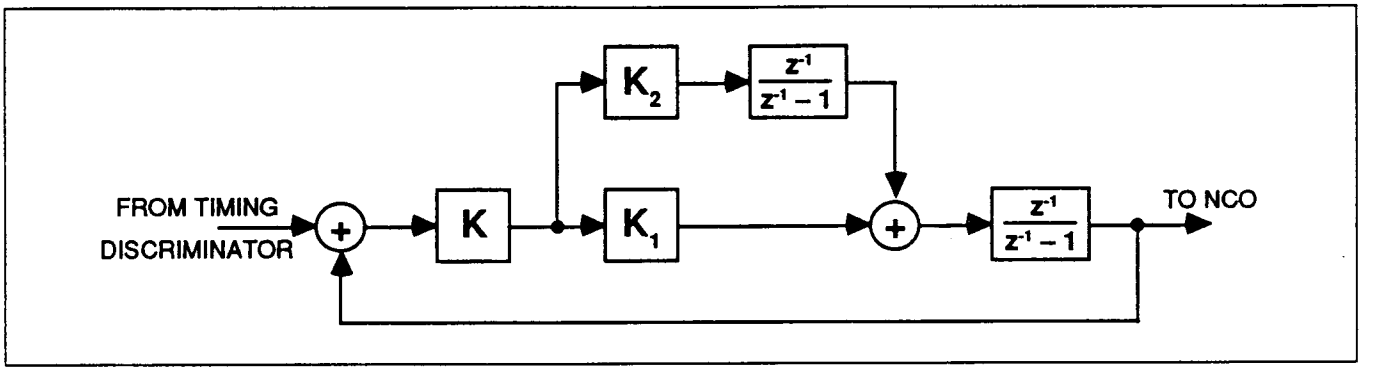
Addresses $1C_H$, $1D_H$, $1E_H$, and $1F_H$: NCO Control Word Register. The two's complement 27-bit NCO frequency control word (Δ-Phase Register) is presented in these 4 bytes. Bit 3 in Address $1C_H$ is the MSB, and Bit 0 in Address $1F_H$ is the LSB.

Input and Output Signal Representation

The input signals I_{S5-0} and Q_{S5-0} to the STEL-2110A can be in either Offset Binary or Offset Two's Complement formats, depending on the state of bit 0 in the Mode Control Register (Address 17_H). All the output signals are in Offset Two's Complement. The meaning of these formats is shown in the diagram to the right. The formats have no digital value corresponding to zero signal level; rather, the least negative and least positive values are equally spaced about zero. The significance of this is that there are the same number of positive and negative values in the formats. In conventional formats one of the values represents zero, leaving an odd number of values to represent the non-zero levels. Consequently, by using these offset formats, the input signal can be converted over the full range of the A/D converter and the sign bit of the outputs optimally represents the hard-decision data. These input data formats are easily generated by offsetting the A/D converter by half an LSB.



FEEDBACK LOOP PARAMETERS



Above is a simplified block diagram of the feedback system. The value of the loop constant K is a function of the chip set-up parameters and signal input conditions. The parameters K_1 and K_2 are controlled by the data stored in Address11_H. The most simple model of the loop is a second order sampled data feedback system. In reality, there are several additional delays within the loop, due to pipelining, which are not shown, and which may affect loop performance in high loop bandwidth conditions. This is taken into account in the table below which relates loop gain to loop bandwidth.

LOOP GAIN COMPUTATION (CONSTANT NOISE)

$$K = \frac{T_d \times Q \times S_s^{3/2} \times A_i^{3/2} \times P_a^2 \sqrt{E_s/N_0}}{8 \times N_r \times b}$$

where:

T_d = Transition density of data. If the phase changed at every symbol transition, then T_d would be 1.0. In normal operation for a BPSK signal, T_d is 0.5.

Q = Quantization. This number is the standard deviation of the 6 bit input sample caused by thermal noise. The value of Q should be 2 states or greater to avoid significant losses (2 dB worst case) due to quantization effects. The value of Q should be less than 16 to avoid losses due to limiting when signal plus noise exceeds the range of the six bit A/D converter.

S_s = Number of accumulated samples per symbol (4 or 8)

A_i = Number of front end accumulations (1,2,4,8 or 16)

P_a = Number of Discriminator Accumulations (1 or 4)

E_s/N_0 = Ratio of energy per symbol to noise density. This quantity is usually expressed in logarithmic form, but for this purpose it is expressed as be a linear ratio.

N_r = 24 bit number which establishes the nominal A/D sample rate clock generated by the NCO.

b = 1 when A_i = 1
b = 2 when A_i = 2 or 4
b = 4 when A_i = 8 or 16

The loop bandwidth (B_L) may be controlled by varying K_1 and K_2, given K as computed above. The loop bandwidth (normalized to the data rate) may be determined from the following table.

$K*K_2$	$K*K_1$	B_L ($^1/_{R_s}$)
1×2^{-3}	1×2^{-8}	.13
1×2^{-4}	1×2^{-10}	.05
1×2^{-5}	1×2^{-12}	.02
1×2^{-6}	1×2^{-14}	.01
1×2^{-7}	1×2^{-16}	.005
1×2^{-8}	1×2^{-18}	.0025
1×2^{-9}	1×2^{-20}	.0012

For example, assume:

E_s/N_0 = 2.5 (4 dB)
S_s = 8
A_i = 1
Q = 2
T_d = 0.5
P_a = 1
$N_r = 2^{22}$

From these numbers and the above formula, the value of K is determined to be 1.12×2^{20}. By letting $K2 = 2^6$ and $K1 = 2^{14}$, the loop bandwidth is determined from the above table to be approximately 1% of the symbol rate.

LOOP GAIN COMPUTATION (SIGNAL ONLY)

For the case when an AGC controls the level of the input signal, an alternative formula for K can be used. In this case, assume a noiseless input and define A to be the magnitude of the digitized signal into the bit synchronizer.

$$K = \frac{A \times T_d \times S_s^2 \times A_i^2 \times P_a^2}{8 \times N_r \times b}$$

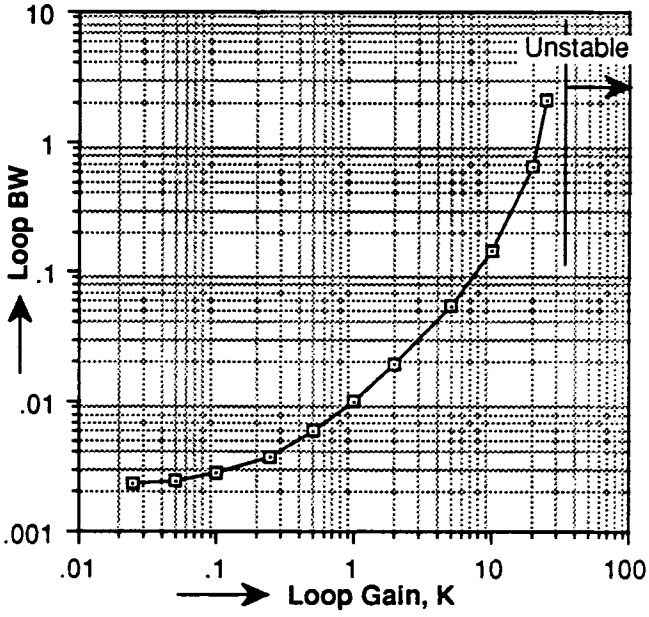
For example, assume the following

$A = 8$
$S_s = 8$
$A_i = 1$
$T_d = 0.5$
$P_a = 1$
$N_r = 2^{22}$

In this case, $K = 2^{-17}$, and the loop bandwidth is deterimined as before with the table.

VARIATION IN LOOP PERFORMANCE AS A FUNCTION OF LOOP GAIN

In determining the value for K_1 and K_2 it is important to consider the effect of loop gain variation due to factors such as signal level variation. Below is a graph illustrating a loop which was designed for a bandwidth of 1 % with K=1. As K increases, the loop gain increases eventually resulting in loop instability for values of K greater than 25. As K is reduced, the loop gain approaches a value of about 0.2%, but stability is maintained. The best region to operate the feedback loop, from the standpoint of transient response characteristics, is in the center, where bandwidth and gain are almost linearly related.



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Note: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability.

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–65 to +150	°C
T_a	Operating Temperature	–40 to +85	°C (Plastic package)
		–55 to +125	°C (Ceramic package)
V_{CCmax}	Max. voltage between V_{CC} and V_{DD}	+7 to –0.7	volts
$V_{I/O(max)}$	Max. voltage on any input or output pin	V_{DD}+0.7	volts
$V_{I/O(min)}$	Min. voltage on any input or output pin	V_{SS}–0.7	volts

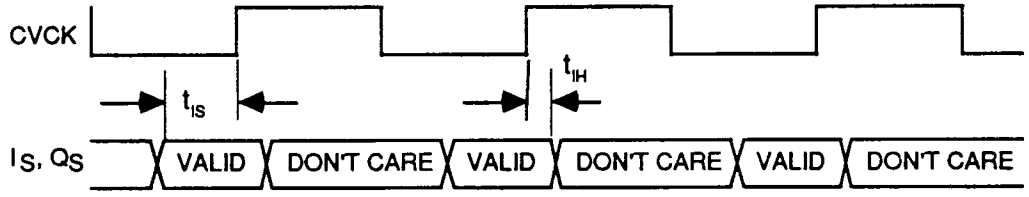
RECOMMENDED OPERATING CONDITIONS

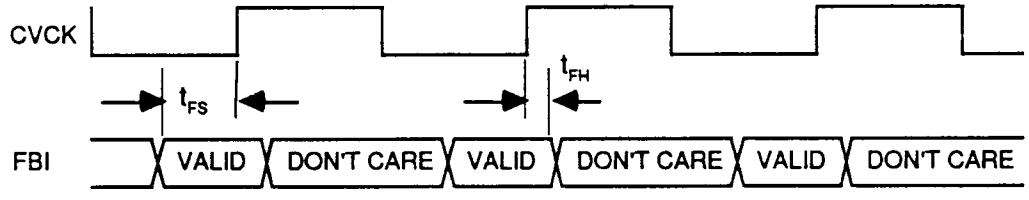
Symbol	Parameter	Range	Units
V_{DD}	Supply Voltage	+5 ± 10%	volts
T_a	Operating Temperature (Ambient)	0 to +70	°C (Plastic package)
		–55 to +125	°C (Ceramic package)

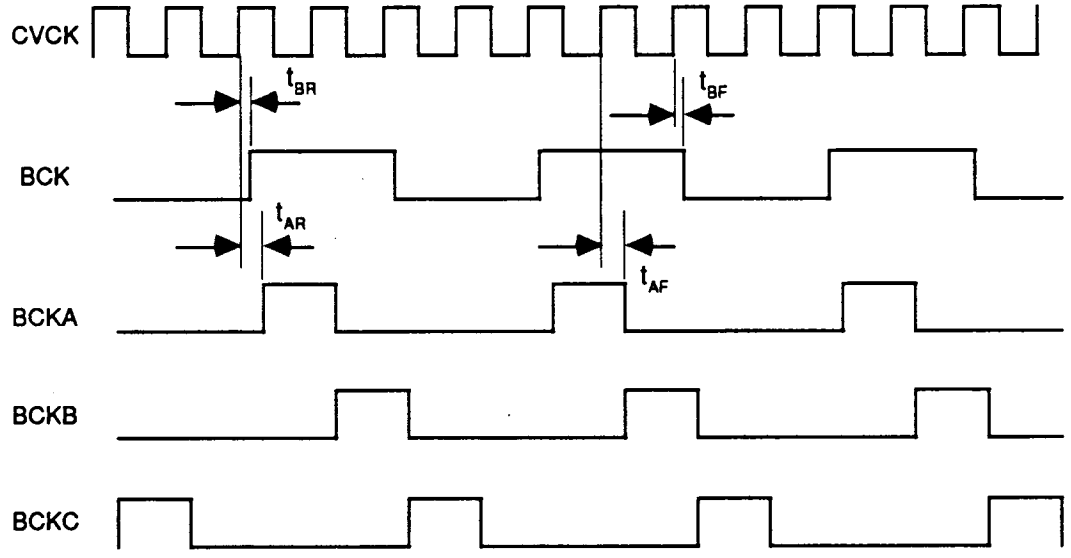
D.C. CHARACTERISTICS (Operating Conditions: V_{DD}=5.0 volts ± 5%, V_{SS}=0 volts, T_a=0° to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational			2.5	mA/MHz	75 MHz, 1 Mbps
$V_{IH(min)}$	Min. High Level Input Voltage	2.0			volts	Guaranteed Logic '1'
$V_{IL(max)}$	Max. Low Level Input Voltage			0.8	volts	Guaranteed Logic '0'
$V_{OH(min)}$	Min. High Level Output Voltage	2.4			volts	I_O = –4.0 mA
$V_{OL(max)}$	Max. Low Level Output Voltage			0.4	volts	I_O = 4.0 mA
$I_{IH(max)}$	Max. High Level Input Current			10	µA	V_{IN} = +5.0 volts
$I_{IL(max)}$	Max. Low Level Input Current			–10	µA	V_{IN} = 0 volts

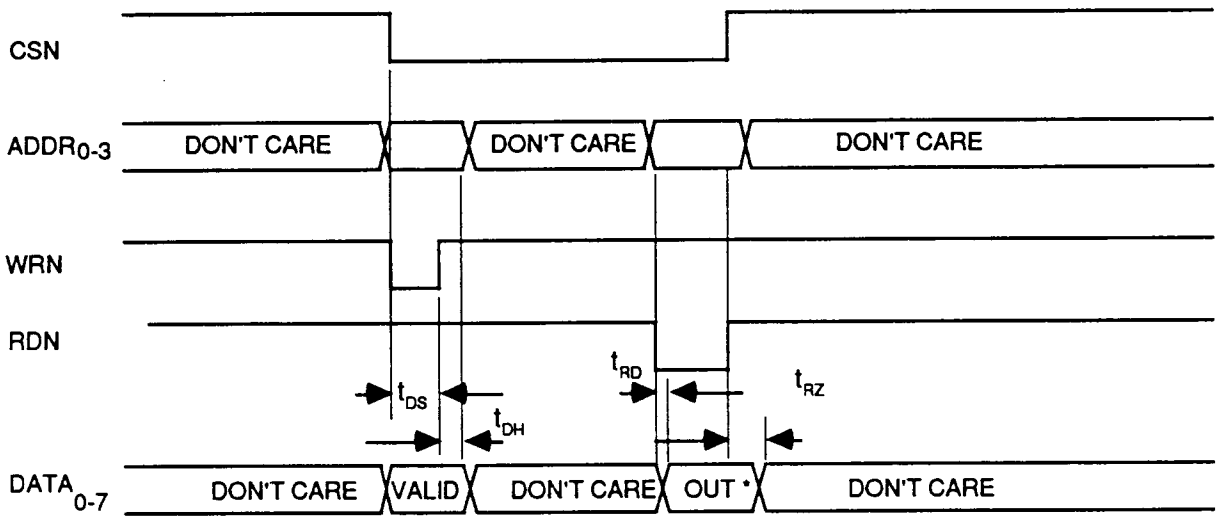
I/O TIMING DIAGRAMS







BUS TIMING DIAGRAMS



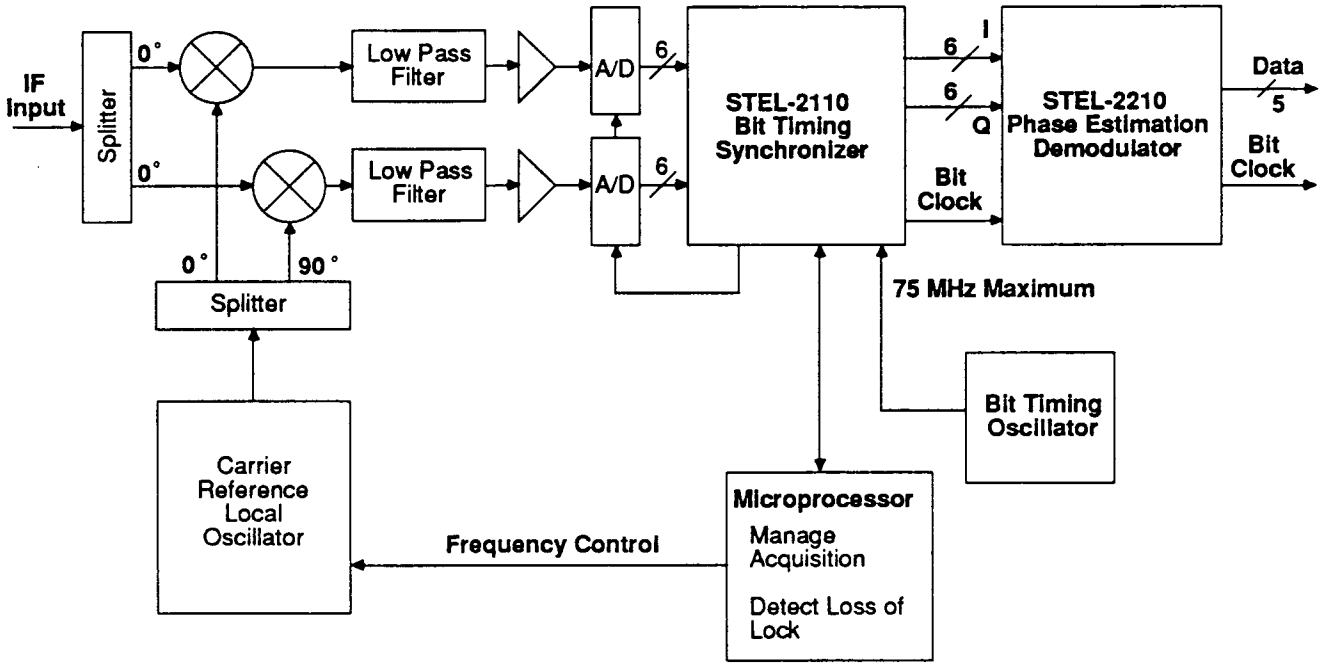
* Data is read out at this time, while **RD** is low. Bus is in a high-impedance state at all other times.

A.C. CHARACTERISTICS (Operating Conditions: V_{DD}=5.0 volts ± 5%, V_{SS}=0 volts, T_a=0° to 70°C)

Symbol	Parameter	Min.	Max.	Units	Conditions
t_{IS}	I_e and Q_e Data Setup time	15		nsec.	
t_{IH}	I_e and Q_e Hold time	0		nsec.	
t_{FS}	**FBI**$_{0-8}$ Setup time	23		nsec.	
t_{FH}	**FBI**$_{0-8}$ Hold time	0		nsec.	
t_{BR}	Rising edge of **BCK** delay from **CVCK**		10	nsec.	
t_{BF}	Falling edge of **BCK** delay from **CVCK**		10	nsec.	
t_{AR}	Rising edge of **BCKA*** delay from **CVCK**		10	nsec.	
t_{AF}	Falling edge of **BCKA*** delay from **CVCK**		10	nsec.	
t_{DS}	Data Setup time from **CSN**, **ADDR** or **DATA** to Rising edge of **WRN**	10		nsec.	
t_{DH}	Data Hold time	5		nsec.	
t_{RD}	Read Delay time		8	nsec.	Load = 20 pF
t_{RZ}	Read Hold time (to Hi Z state)		10	nsec.	Load = 20 pF

* Also applies to **BCKB** and **BCKC**

TYPICAL APPLICATION
COHERENT PSK DEMODULATOR



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ASIC & Custom Products Group
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