MF1167-03

EPSON

LCD Controller ICs

S1D13305 Series

Technical Manual

SEIKO EPSON CORPORATION

ENERGY SAVING EPSON

✻ In this manual, Zilog's Z80-CPU or its equivalent shall be called Z80, Intel's 8085A or its equivalent shall be called 8085 and Motorola's MC6809 and MC6802 or their equivalents shall be called 6809 and 6802, respectively.
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Configuration of product number

- Devices

S1 D 13706 F 00A0 00

- 00 — Packing specification
- 00A0 — Specification
- F — Package (B: CSP, F: QFP)
- 13706 — Corresponding model number
- D — Model name (D: driver, digital products)
- S1 — Product classification (S1: semiconductor)

- Evaluation Board

S5U 13705 P00C0 00

- 00 — Packing specification
- P00C0 — Specification
- 13705 — Corresponding model number (13705: for S1D13705)
- S5U — Product classification (S5U: development tool for semiconductor)

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1 OVERVIEW

The S1D13305 Controller displays text and graphics on a midsize, dot-matrix liquid crystal display (LCD). A very flexible, low-power display system can be configured using the S1D13305 in combination with various LCD modules. The character code or bitmap display data from the microprocessor is temporarily stored in frame buffer memory, then periodically read out and converted into LCD module signals for output to the LCD. The various command functions make it possible to overlay text and graphics screens, scroll the screen in any direction, and split the screen for multi-window display. Moreover, the external memory timing circuit, built-in LCD module control circuit, and high-speed character generator allows you to build an LCD control block using only a few external circuits.

1.1 Features

- Number of display dots:........................... Text display mode
80 columns x 32 rows + graphics screen overlay
Graphic display mode
(640 dots x 256 dots) x three-screen overlay
- Three display modes:............................... Text display mode, graphic display mode, and text/ graphic overlay mode (Layered display functions)
- Automatic cursor shift function:.............. For shifting in four directions
Up/down and left/right
- Flexible scroll function:........................... The text/graphics display screen can be easily moved and smoothly scrolled horizontally.
- Frame buffer: .... Up to 64 KB of SRAM, virtual screen configuration
- Internal character generator:.................... 160 characters (mask programmable 5 x 7 dots)
- External character generator capacity:..... CGRAM .... (8 dots x 16 dots) x 64 characters
CGROM .... (8 dots x 16 dots) x 256 characters
- Drive duty cycle:..................................... Can be set without any required increments from 1/2 up to 1/256 duty cycles.
- 80 or 68-series MPU interface (selectable)
- Single power supply: .... 2.7 to 5.5 V
- Package:.. 60-pin QFP (plastic)
QFP5-60pin ... S1D13305F00A

1.2 *System Overview*

Positioned midway between the MPU and LCD panel, the S1D13305 transfers the control commands and data for display to and from the MPU, making it possible to control up to 64 Kbytes of display memory (VRAM) as shown in the system configuration diagram below.

Moreover, because the S1D13305 has a built-in a control circuit for LCD units, it is possible to take full advantage of the features of midsize, dot-matrix liquid crystal display units without using any external circuit.

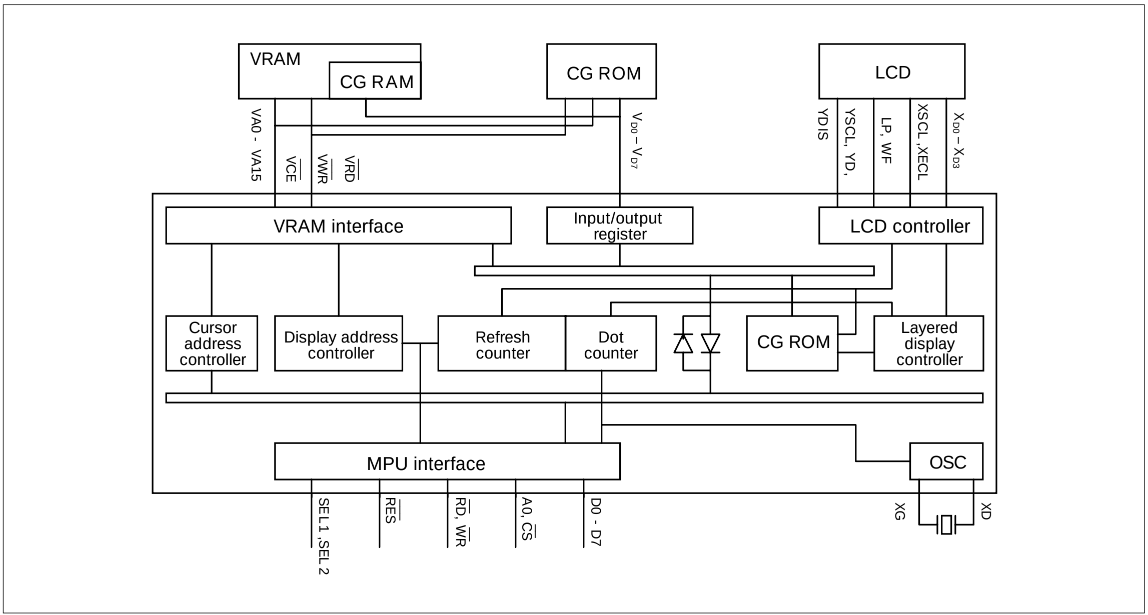


Figure 1-1 Block diagram of the S1D13305

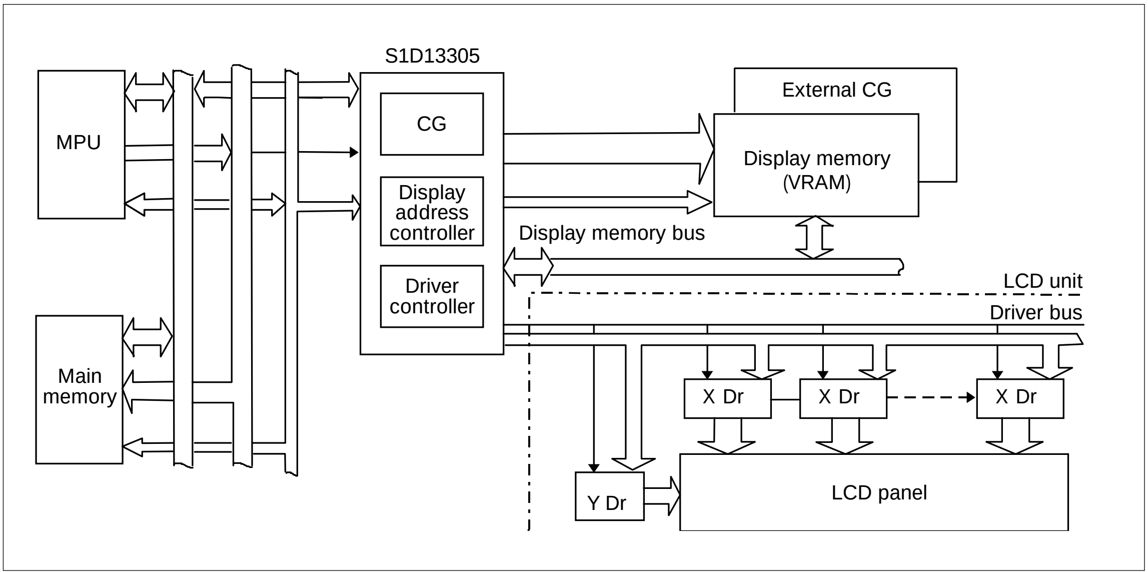


Figure 1-2 Example of system configuration

The S1D13305 divides the display memory space into the four areas shown below. When this configuration is combined with the layered (overlaid) display and flexible scroll functions of the S1D13305, it is possible to greatly reduce the MPU load when inverting or underlining text, displaying graphs with text, or creating simple animation.

The S1D13305 uses the display memory space by dividing it into the four areas shown below to realize the layered display functions using only a single controller.

Example of display memory mapping by the S1D13305

(1) Character code table

- A memory area to store character code when displaying text
- 1 character = 8 bits
- Variable table mapping (by altering the scroll start address)

(2) Graphic data table

- A memory area to store bitmap data
- 1 word = 8 bits
- Variable table mapping

(3) CG RAM table (for external characters)

- A character generator whose character patterns can be altered by the MPU as desired
- Maximum 8 x 16 bits (16 bytes per character)
- Maximum 64 discrete characters
- Usable in combination with internal or external CG ROM
- Variable table mapping

(4) CG ROM table

- An area to be set up when another CG is needed separately from the internal CG
- Combined use with the internal CG not possible; combined use with the CG ROM possible
- Maximum 8 x 16 bits (16 bytes per character)
- Maximum 256 discrete characters
- Mapped into a fixed #F000H–#FFFFH area

To make the most of the above-mentioned functions of the S1D13305, a high-speed interfacing method is used to enable pipelined command processing between the MPU and S1D13305. Most commands of the S1D13305 are processed so that the controller completes the processing of any input command before the next command is issued from the MPU. Therefore, the MPU does not need to frequently check the status of the S1D13305, and is not kept waiting by the S1D13305. Thus, the high-speed interfacing method adopted for the S1D13305 helps minimize possible reduction in the MPU's processing capability.

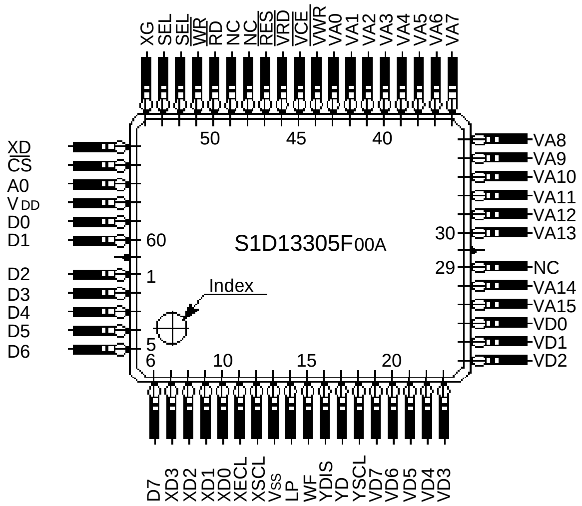
1.3 List of Abbreviations

Abbreviation	Meaning
• A	Address
• AP	Address pitch
• C	Text display mode (Denotes a command in command code descriptions.)
• CD	Cursor movement direction
• CG	Character generator
• CGRAM ADR	Character generator memory offset address
• CM	Cursor shape
• C/R	Number of characters per line
• CRX	Cursor size in the X direction
• CRY	Cursor size in the Y direction
• CSRDIR	Direction of cursor movement
• CSRFORM	Cursor shape
• CSRR	Cursor address read
• CSRW	Cursor address write
• DM	Display mode
• FC	Flashing cursor
• fFR	Frame frequency
• fOSC	Oscillation frequency
• FP	Layer flashing
• FY	Character field in the Y direction
• G	Graphic display mode
• GLC	Graphic liquid crystal unit controller
• HDOT SCR	Smooth scrolling in horizontal direction
• IV	Inverse
• L	Layer
• L/F	Number of lines per screen
• MREAD	Display memory readout
• MX	Screen composition method
• MWRITE	Display memory write
• OV	Screen overlay
• OVRAY	Screen overlay
• P	Parameter
• R	Row
• RAM	Random access memory
• ROM	Read-only memory
• SAD	Display start address
• SL	Number of scanning lines
• TC/R	Total number of characters per line
• VRAM	Display memory
• WF	AC drive waveform
• W/S	Double common/single common
• XDr	X direction driver
• YDr	Y direction driver

2 PINS

2.1 Pin Connection

2.1.1 Pin Assignments



2.1.2 Pin Description

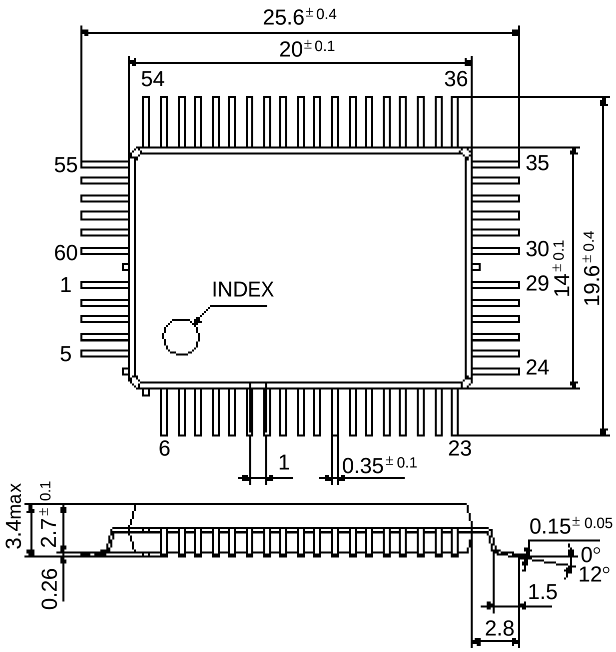
Pin Name	Pin No. S1D13305F00A	I/O Type	Description
XG XD	54 55	I O	Oscillator pins
V_{DD}	58	V_{CC}	Power supply (V_{CC})
V_{SS}	13	GND	Power supply (GND)
SEL1, 2	53 · 52	I	80/68-series bus switching
D0–D7	59–60 1–6	I/O	System-side data bus
A0	57	I	Data bus signal discriminating signal
$\overline{RD}$	50	I	80 series ... Read signal 68 series .... E clock
$\overline{WR}$	51	I	80 series .... Write signal 68 series .... R/$\overline{W}$ signal
$\overline{CS}$	56	I	Chip select input signal
$\overline{RES}$	47	I	Reset signal input
VA0–VA15	27 · 28 30–43	O	VRAM address bus

Pin Name	Pin No. S1D13305F00A	I/O Type	Description
VD0–VD7	19–26	I/O	VRAM data bus
$\overline{VWR}$	44	O	VRAM write signal
$\overline{VRD}$	46	O	VRAM read signal
$\overline{VCE}$	45	O	VRAM chip enable
XD0–XD3	7–10	O	X driver data bus
XSCL	12	O	X driver shift clock
XECL	11	O	X driver enable chain clock
LP	14	O	Latch pulse
WF	15	O	Frame signal
YSCL	18	O	Scan shift clock
YD	17	O	Scan start pulse
YDIS	16	O	LCD power-down output

NC: Non Connection

2.1.3 Package Dimensions

- S1D13305F00A



2.2 Pin Functions

2.2.1 Power Supply Pins

Pin Name	Function
V_{DD}	This pin connects to the V_{CC} power supply (and is shared with MPU power supply pin V_{CC}). Note 1
V_{SS}	This is the 0V grounding pin connected to system GND.

Note 1: Because the spike power supply current in the S1D13305 could reach levels that are several tens higher than the average amount of dynamically consumed current, measures must be taken to minimize the power supply impedance of the S1D13305. For example, use thick power supply wiring from the power supply to the S1D13305 or insert a capacitor of 0.47 µF or more (with good frequency characteristics) between V_{DD} and V_{SS} close to the S1D13305. These measures will help to reduce power supply impedance.

2.2.2 Oscillator Pins

XG XD	These pins are used to connect a crystal resonator for the internal clock-generating oscillator. For details, see Section 4.2, “Oscillator Circuit” on page 51. When operating with an external clock, use XG as the input pin and leave XD open. Note 2

Note 2: The external clock EXTϕ0 supplied from XG must satisfy the oscillation characteristics stipulated in Section 5.3.6, “External Clock Input Characteristics” on page 71, because it is used to internally generate the basic timing in the S1D13305.

2.2.3 System Bus Connecting Pins

D0–D7	Tristate input/output, active high These pins comprise an 8-bit bidirectional data bus, which is connected to the 8-bit or 16-bit MPU data bus.
SEL1 SEL2	Input, active high A combination of SEL1 and SEL2 allows the MPU interface format to be changed so that the S1D13305 can be connected directly to the 80-series MPU (Z80® or 8085) bus or the 68-series MPU (6809 or 6802) bus.

SEL1	SEL2	Mode	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	D0	D1	D2	D3	D4	D5	D6	D7
0	0	80 series	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
1	0	68 series	↑	E	R/$\overline{W}$	↑	↑	↑	↑	↑	↑	↑	↑	↑
0	1	*	*	*	*	*	*	*	*	*	*	*	*	*
1	1	*	*	*	*	*	*	*	*	*	*	*	*	*

*: Inhibited

Note 3

Note 3: SEL1 and SEL2 must normally be connected directly to either side of the power supply (V_{DD} or V_{SS}) so as not to prevent noise impact. If noise gets mixed in, insert a capacitor between SEL1/SEL2 and V_{SS} as close to the IC pins as possible. This will effectively prevent noise from impacting SEL1 and SEL2.

<table>
<tr><td>A0</td><td>Input, active high
Normally, the least significant bit of the MPU address is connected to this pin. In combination with the $\overline{RD}$ and $\overline{WR}$ signals or R/$\overline{W}$ and E signals, this pin discriminates the data bus signal as shown in the table below.

<For the 80-series interface>
<table>
<tr><th>A0</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Status flag read</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Data (VRAM, CG, or cursor address) read</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Data (VRAM or register) write</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Command write (code only)</td></tr>
</table>
<For the 68-series interface>
<table>
<tr><th>A0</th><th>R/$\overline{W}$</th><th>E</th><th>Function</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Status flag read</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Data (VRAM, CG, or cursor address) read</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Data (VRAM or register) write</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Command write (code only)</td></tr>
</table>
Notes 4</td></tr>
</table>

Note 4: Register write refers to writing parameters.

<table>
<tr><td>$\overline{RD}$ (E)</td><td>• When an 80-series MPU is connected
Input, active low
This strobe signal is used by the MPU as it reads data or status flags from the S1D13305. The data bus of the S1D13305 remains in the output state while this signal is low.
• When a 68-series MPU is connected
Input, active high
This pin functions as a clock-enable input pin for the 68-series MPU.</td></tr>
<tr><td>$\overline{WR}$ (R/$\overline{W}$)</td><td>• When an 80-series MPU is connected
Input, active low
This strobe signal is used by the MPU as it writes data or parameters to the S1D13305. The S1D13305 receives the data bus signal at the rising edge of $\overline{WR}$.
• When a 68-series MPU is connected
Input
This pin functions as a R/$\overline{W}$ control signal input pin for the 68-series MPU.
R/$\overline{W}$ = high: Read
R/$\overline{W}$ = low: Write</td></tr>
<tr><td>$\overline{CS}$</td><td>Input, active low
This chip select signal is used by the MPU to activate the S1D13305 before accessing it, and is normally derived by decoding the address bus signal.</td></tr>
<tr><td>$\overline{RES}$</td><td>Input, active low
This input signal is used to reset the S1D13305 to initialize it in hardware. Note 5</td></tr>
</table>

Note 5: Although this pin is a Schmitt trigger input to prevent the S1D13305 from being inadvertently reset by noise, care must be taken when intentionally lowering the power supply voltage.

2.2.4 *Display Memory Control Pins*

The S1D13305 can directly access static RAM and 2176 or 2732-type PROM. Therefore, these different types of memory can be used in combination, allowing the most suitable mix of memory to be selected by considering the amount of current consumed by and the cost of display memory.

VA0–15	Output This 16-bit address bus is connected to display memory. When accessing CG RAM or external CG ROM, the four low-order bits of the S1D13305 line counter are output in VA0–VA3.
VD0–VD7	Tristate input/output This 8-bit data bus is connected to display memory. The data bus is in the output state while $\overline{\text{VWR}}$ is low.
$\overline{\text{VWR}}$	Output, active low This write control signal for display memory goes low when data to be stored in display memory exists in VD0–7.
$\overline{\text{VRD}}$	Output, active low This read control signal for display memory is used to enable data output from display memory.
$\overline{\text{VCE}}$	Output, active low This signal is used to place display memory in sleep mode or in the standby state during the period of per-line frequency division adjustment (blanking interval).

2.2.5 LCD Driver Control Pins

The S1D13305 can directly control both the X and Y drivers based on an enable chain, which is a method of effectively reducing the amount of current consumption needed to drive dot-matrix liquid crystal display elements.

XD0–XD3	Output, active high This 4-bit dot data bus for the X driver (column driver) is connected to the data input pins of the X driver.
XSCL	Output, falling edge triggered This signal causes the dot data bus signals (XD0–XD3) to be stored in the X driver at the signal's falling edge, and thus functions as a shift clock for the internal shift register of the X driver. To reduce power consumption, this clock is turned off until the MPU starts sending data for the next display line after outputting the LP signal. (For details, see Section 5.3.7, "LCD Control Signal Timing Characteristics" on page 72.)
XECL	Output, falling edge triggered XECL is a dedicated clock signal for the X drivers cascaded by an enable chain. It causes the enable signal to be successively passed to the next X driver every 16 XSCL periods.
LP	Output, falling edge triggered For the liquid crystal display elements to be successively driven, the X driver contains a circuit to latch each output bit of the internal shift register at the falling edge of LP. This signal is output for every display line.
WF	Output This signal provides a one-frame interval for the X and Y drivers to determine the AC drive waveform for the LCD panel. Two types of cyclic signals are output depending on how the System Set command parameters are set.
YSCL	Output, active high, rising edge triggered This signal is a clock for the Y driver, and is equivalent to XSCL for the X driver. The Y data signal (YD) is stored in the Y driver at the beginning of a frame, and YSCL is used as an internal shift clock.
YD	Output, active high YD is data for the Y driver, and is a cyclic signal output at the first display line interval of a frame. The electrodes on the common side of liquid crystal display elements are sequentially scanned as the YD signal is sequentially shifted inside the Y driver synchronously with the YSCL signal.
YDIS	Output, active high This signal is used to power down the LCD unit and is held high during the display period. Note 6

Note 6: The YDIS signal goes low at a time equivalent to one to two frames after the sleep command is written. When the YDIS signal goes low, all Y driver outputs are forcibly brought to an intermediate level (unselected), thus causing display to turn off. Therefore, to power off the LCD unit, the liquid crystal drive power supply (with relatively large steady-state current) must be turned off at the same time display is turned off by using the YDIS signal.

3 COMMANDS

3.1 Types of Commands

Purpose	Command	Code											HEX	Command description	Parameters following the command		Remark
		$\overline{RD}$	$\overline{WR}$	A0	D7	D6	D5	D4	D3	D2	D1	D0			Number of parameters	See pages	
					BIN												
Operation control	SYSTM SET	1	0	1	0	1	0	0	0	0	0	0	40	Resets the device, sets window size, and controls sleep.	8	15	
	SLEEP IN	1	0	1	0	1	0	1	0	0	1	1	53		0	24	Note 1
Display control	DISP ON/OFF	1	0	1	0	1	0	1	1	0	0	D	58 • 59	Turns display on or off and makes display blink.	1	24	Note 1
	SCROLL	1	0	1	0	1	0	0	0	1	0	0	44	Sets the display start address and display area.	10	26	
	CSRFORM	1	0	1	0	1	0	1	1	1	0	1	5D	Sets the cursor shape, etc.	2	32	
	CGRAM ADR	1	0	1	0	1	0	1	1	1	0	0	5C	Sets the CG RAM start address.	2	35	
											CD	CD					
	CSRDIR	1	0	1	0	1	0	0	1	1	1	0	4C–4F	Sets the direction of cursor movement.	0	33	
	HDOT SCR	1	0	1	0	1	0	1	1	0	1	0	5A	Sets the dotwise scroll position in horizontal direction.	1	36	
	OVLAY	1	0	1	0	1	0	1	1	0	1	1	5B	Specifies screen overlay mode.	1	33	
Drawing control	CSRW	1	0	1	0	1	0	0	0	1	1	0	46	Sets the cursor address.	2	37	Note 1
	CSRR	1	0	1	0	1	0	0	0	1	1	1	47	Reads the cursor address.	2	37	Note 1
Memory control	MWRITE	1	0	1	0	1	0	0	0	0	1	0	42	Writes to display memory.	—	39	Note 1
	MREAD	1	0	1	0	1	0	0	0	0	1	1	43	Reads display memory data.	—	40	

Note 1: As a rule, a command is executed each time a parameter for the command is input to the S1D13305, and completed before the next parameter (P) or command (C) is input. Therefore, the MPU can stop sending parameters in the middle and send the next command. In this case, the parameters already sent are effective and other parameters not input to the S1D13305 retain their original values. However, two-byte parameters are handled in the manner described below. (Note 2)

1. CSRW and CSRR commands: The parameter is executed one byte at a time. Therefore, the MPU can only alter or check the low-order byte.
2. Commands other than CSRW and CSRR: The parameter is not executed until its second byte is input.

SYSTEM SET
SCROLL
CGRAM ADR

Note 2: Two-byte parameters consist of two bytes of data (as in the case of APL and APH). Because the value of each register after power-on is indeterminate, make sure all command parameters are set.

3.2 Command Description

3.2.1 Operation Control Commands

SYSTEM SET

This command and the parameters that follow specify initial reset of the device, set the window size, and the method of connecting with the LCD unit. This command determines the fundamental operation of the S1D13305. Therefore, if this command is incorrectly set, the functions of other commands may not work normally.

	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
C	0	10		00		000		
P1	0	0	IV	1	W/S	M2	M1	M0
P2	WF	00		00		← FX →		
P3	00		00		← FY →			
P4	← C/R →							
P5	← TC/R →							
P6	← L/F →							
P7	← APL →							
P8	← APH →							

● C The command alone has the following initial reset functions:

- Resets the internal timing circuit.
- Turns display off.
- Deactivates sleep mode (internal operation stopped state) (thus starting the oscillator).

To deactivate sleep mode, make sure the command and one parameter (P1) are input.

[Parameter P1]

- M0 — Specifies the CG ROM to be used for display. Although internal CG ROM can generate 160 discrete character fonts (each consisting of 5 x 7 dots as shown in Section 4.4.1, "Character Fonts (Internal CG)" on page 62), external CG ROM may be used when different character fonts or more characters (up to 256) are needed.

  M0 0: Internal CG ROM (160 characters)
  1: External CG ROM (up to 256 characters)

  Note: When the CG area is mapped in the display memory space, the memory area available to store display data is reduced by the amount of CG area mapped.

- M1 — Selects the CG RAM definition area where the user can define any desired character pattern. The CG RAM code may be selected from the 64 discrete codes assigned in Section 4.4.2, "Relationship between Character Codes and Those Usable as CG RAM (for combined use with internal CG ROM)" on page 63.

M1	0: Without bit D6 correction	The CG RAM1 and CG RAM2 areas are noncontiguous. Only CG RAM1 is handled as CG RAM, with CG RAM2 handled as CG ROM.
	1: With bit D6 correction	The CG RAM1 and CG RAM2 areas are contiguous. Both CG RAM1 and RAM2 are handled as CG RAM.

- M2 — Selects the CG size in the Y direction in order for the economical use of external CG ROM and CG RAM. CGs whose sizes in the Y direction are 17 dots or more cannot be handled with the character codes of the S1D13305. In such case, characters may be decomposed into bit images and displayed in graphic display mode of the S1D13305.

  M2 0: 8 dots (using 2716 or equivalent ROM)
  1: 16 dots (using 2732 or equivalent ROM)

- W/S — Selects the LCD unit drive method.

  W/S 0: Single-screen drive method
  1: Dual-screen drive method

- DR2 — Selects the number of horizontal pixels for adjustment of the driver's output count and shift clock needed for the enable chain when using the dual-screen drive method.

  DR 0: Other than the above (This value is usually set.)
  1: The number of horizontal pixels is 2n + 1 times 32 (n = 0, 1, 2, ...)

Table 3-1 W/S Related Registers

Parameter	W/S = 0		W/S = 1	
	IV = 1	IV = 0	IV = 1	IV = 0
C/R	C/R	C/R	C/R	C/R
TC/R	TC/R	TC/R	TC/R	TC/R
L/F	L/F	L/F	L/F	L/F
SL1	00H–L/F	00H–L/F + 1	(L/F)/2	(L/F)/2
SL2	00H–L/F	00H–L/F + 1	(L/F)/2	(L/F)/2
SAD1	First screen block	First screen block	First screen block	First screen block
SAD2	Second screen block	Second screen block	Second screen block	Second screen block
SAD3	Third screen block	Third screen block	Third screen block	Third screen block
SAD4	Invalid	Invalid	Fourth screen block	Fourth block screen
Cursor	Successively movable on all screens		Upper/lower screen configuration: Successively movable on all screens	

Note: 1. For details on how to set C/R and TC/R when using the HDOT SCR command, see Section 4.1.6, “Determining Various Parameters” on page 45.

2. The SL value for IV = 0 is the SL value for IV = 1 plus 1.

● IV

Corrects the screen origin during inverse display. Normally set IV = 1.
The most effective way to display characters in inverse video is to use a unique function of the S1D13305 that allows the text screen and graphics back-layered screen to be exclusive OR’d.
However, because the character origin is at the upper-left corner of the screen when characters are mapped on the screen by the S1D13305, the uppermost line and leftmost column on the display screen do not have dots to draw the outline of characters, thus making the displayed characters illegible. Therefore, the S1D13305 uses the IV specification and horizontal direction dot scroll function (HDOTSCR command) to shift the origin of the text screen for correction with respect to the graphics back-layered screen, allowing characters to be displayed in inverse video anywhere on the screen. For details, see Section 4.1.7, “Scrolling” on page 46.

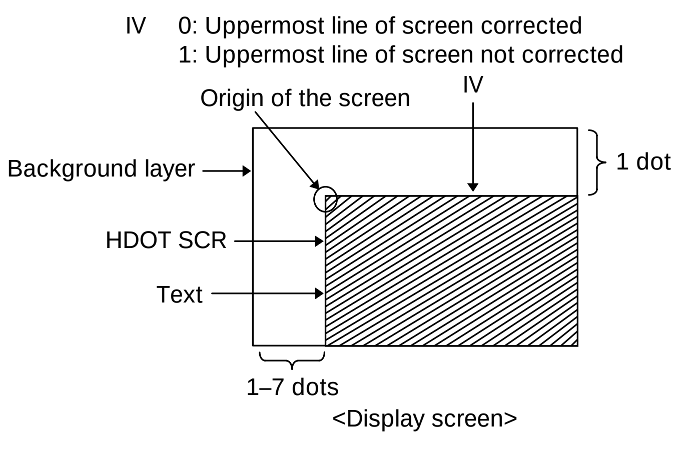


Figure 3-1 Combination of IV and HDOTSCR

Note: If the leftmost column must also be corrected, shift dots in the horizontal direction.

[Parameter P2]

● FX Defines the size of the character field in the X direction (i.e., size of one character including a space).

HEX	D4 D3 D2 D1 D0					Number of dots [FX]
	BIN					
00	0	0	0	0	0	1
01	0	0	0	0	1	2
.	.	.	.	.	.	.
.	.	.	.	.	.	.
07	0	0	1	1	1	8

Structure of the character field

1. Because the S1D13305 processes the display data in 8-bit units, if the character font exceeds 8 bits, the text screen must configure one character with two or more display memory addresses as normally practiced. In this case, odd-numbered bits less than a unit of 8 bits are not displayed as shown below. Odd-numbered bits less than a unit of 8 bits are also not displayed on the back-layered screen as shown below.
2. In graphic display mode, the character field must normally be 8 bits long. For other character fields, odd-numbered bits less than a unit of 8 bits are not displayed.

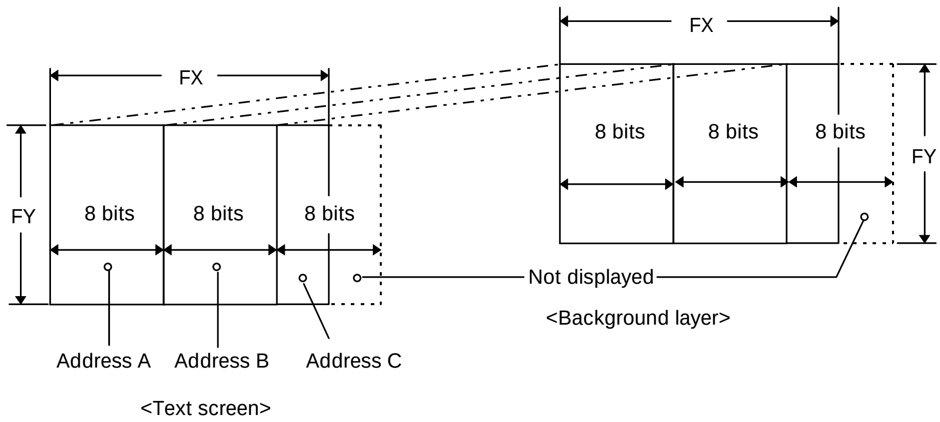


Figure 3-2 Typical relationship between FX/FX and display addresses

● WF Specifies the AC drive method of the liquid crystal.

WF 0: Line inversion drive method
1: Two-frame AC drive method (method B)

The two-frame AC drive method is an AC drive method in which the half period of the WF signal constitutes a one-frame interval. Normally, set WF = 1.

The line inversion drive method is a modified AC drive method in which the WF signal has its waveform inverted every 16 Y lines.

Note: Although the LCD may look better when WF is set to 0, stripes in the X direction will appear when the LCD drive voltage is high or viewing angle large.

[Parameter P3]

- FY Defines the size of the character field in the Y direction.

HEX	D3	D2	D1	D0	Number of dots [FX]
	BIN				
00	0	0	0	0	1
01	0	0	0	1	2
.	.	.	.	.	.
.	.	.	.	.	.
07	0	1	1	1	8
.	.	.	.	.	.
.	.	.	.	.	.
0E	1	1	1	0	15
0F	1	1	1	1	16

[Parameter P4]

- C/R Defines the display interval in the X direction by indicating the number of display characters counted in address units, as described in the section on parameter FX. When [FX] = 10 dots, for example, two memory addresses are counted per character. For details on how to calculate the [C/R] value, see Section 4.1.6, “Determining Various Parameters” on page 45. The value set for this parameter cannot be greater than the calculated [C/R] value, but can be equal to or less than the calculated [C/R] value. In that case, excess display sections are left blank.

HEX	D7	D6	D5	D4	D3	D2	D1	D0	Characters per line [C/R]
	BIN								
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
4F	0	1	0	0	1	1	1	1	80
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
EE	1	1	1	0	1	1	1	0	239
EF	1	1	1	0	1	1	1	1	240

Note: Make sure the number of dots in excess display sections is within 64.

[Parameter P5]

● TC/R The condition [TC/R] ≥ [C/R] + 4 must always be met.
To minimize the amount of current consumed by the S1D13305 and LCD unit for a given display capacity, the S1D13305's oscillation frequency (fosc) must be adjusted.

Moreover, because the one-frame time (1/fFR) must be made constant to prevent flicker, define [TC/R] according to the equation to calculate [TC/R] as described in Chapter 4 and adjust the S1D13305's divide-by-n ratio.

HEX	D7	D6	D5	D4	D3	D2	D1	D0	[TC/R]
	BIN								
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
52	0	1	0	1	0	0	1	0	83
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

[Parameter P6]

● L/F Defines the display interval in the Y direction by indicating the number of display lines per screen.

HEX	D7	D6	D5	D4	D3	D2	D1	D0	Number of lines per screen
	BIN								
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
7F	0	1	1	1	1	1	1	1	128
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

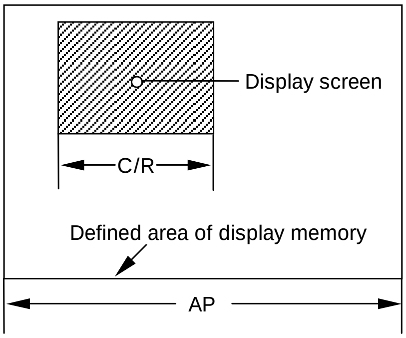
Note: When W/S = 1, [L/F] must be defined as an even number because dual-screen display is assumed.

[Parameters P7, P8]

● AP Defines the number of memory addresses in the X direction of a virtual screen.

APL	AP7	AP6	AP5	AP4	AP3	AP2	AP1	AP0
APH	AP15	AP14	AP13	AP12	AP11	AP10	AP9	AP8

APH	APL	Number of memory addresses per line [AP]
HEX		
0 0	0 0	0
0 0	0 1	1
. .	. .	.
. .	. .	.
0 0	5 0	80
. .	. .	.
. .	. .	.
F F	F E	2^{16}-2
F F	F F	2^{16}-1



SLEEP IN

● C When this command is input, the S1D13305 blanks the display for at least a one-frame period, then stops all internal operations including clock oscilllation before entering sleep mode. At this time, the LCD unit sends OFF data to the X driver while simultaneously sending the YDIS signal to the Y driver to turn the bias voltage off. Therefore, in no case will unexpected display remain on the screen when the liquid crystal is powered off by the YDIS signal.

In sleep mode, the S1D13305 registers retain the original state before entering sleep mode. Moreover, the display memory control pins are fixed high or low to maintain the integrity of data stored in display memory.

To restore the S1D13305 from sleep mode, write the command and one parameter (P1) of the SYSTEM SET to the S1D13305 once to immediately wake up the S1D13305. To restore display, execute the DISP ON instruction immediately after that.

	MSB							LSB
C	0	1	0	1	1	0	0	D

Note:

1. The YDIS signal goes low at a time equivalent to one to two frames after the sleep command is written. When the YDIS signal goes low, all Y driver outputs are forcibly brought to an intermediate level (unselected), causing display to turn off. Therefore, for the LCD unit to be powered down, the liquid crystal drive power supply (with relatively large steady-state current) must be turned off at the same time display is turned off by using the YDIS signal.
2. If the drive power supply of the liquid crystal remains on in sleep mode, a DC component may be applied to the LCD panel because all internal operations of the S1D13305 have been stopped in that mode. When priority is placed on reliability, however, the liquid crystal drive power supply must be turned off before writing the sleep command to prevent DC components from being applied to the LCD panel.
3. Although the bus is placed in the high-impedance state during sleep mode, some voltage may be supplied to the bus line for a bus with pull-up/pull-down resistors.

3.2.2 Display Control Commands

DISP ON/OFF

This command turns display of the entire screen on or off.

The parameters that follow this command turn the cursor and each layered screen on or off individually, and select the cursor blink rate and screen flashing rate. Setting a blink rate and flashing rate makes area flashing possible (i.e., flashing one entire line) instead of flashing just one character by means of cursor display.

	MSB							LSB
C	0	1	0	1	1	0	0	D
P1	FP5	FP4	FP3	FP2	FP1	FP0	FC1	FC0

● C

D 0: Disables entire screen display.
1: Restores entire screen display.

Note: Parameter D (to disable entire screen display) has priority over parameter FP.

[Parameter P1]

● FC Selects turning the cursor on or off and defines a blink rate.

FC1	FC0	Cursor display	
0	0	OFF (blank)	
0	1	ON	Blinking off
1	0	ON	Blink at fFR/32 Hz (approx. 2 Hz)
1	1	ON	Blink at fFR/64 Hz (approx. 1 Hz)

Cursor blink on/off ratio
ON:OFF = 7:3

Note: As the MWRITE command always enables the cursor, the cursor position can be checked, even when performing consecutive writes to display memory while the cursor is flashing.

● FP

FP1, FP0 FP3, FP2 FP5, FP4		First screen block (SAD1) Second screen block (SAD2, SAD4) Note Third screen block (SAD3)	
0	0	Screen display off (blank)	
0	1	Display on	Screen flashing off
1	0	Display on	Flash at fFR/32 Hz (approx. 2 Hz)
1	1	Display on	Flash at fFR/4 Hz (approx. 15 Hz)

Screen flashing on/off ratio
ON:OFF = 7:3

Note: Although SAD4 is assumed when W/S = 1, the screens specified by SAD2 and SAD4 cannot be made to flash independently of each other due to simultaneous control by parameters FP2 and FP3.

SCROLL

● C	Defines the scroll start address (SAD) and number of lines per block to be scrolled (SL). Parameters P1 through P10 can be omitted when not required. However, the parameters must be set sequentially as shown below.

	MSB							LSB	
C	0	1	0	0	0	1	0	0	
P1	A7	A6	A5	A4	A3	A2	A1	A0	(SAD1L)
P2	A15	A14	A13	A12	A11	A10	A9	A8	(SAD1H)
P3	L7	L6	L5	L4	L3	L2	L1	L0	(SL1)
P4	A7	A6	A5	A4	A3	A2	A1	A0	(SAD2L)
P5	A15	A14	A13	A12	A11	A10	A9	A8	(SAD2H)
P6	L7	L6	L5	L4	L3	L2	L1	L0	(SL2)
P7	A7	A6	A5	A4	A3	A2	A1	A0	(SAD3L)
P8	A15	A14	A13	A12	A11	A10	A9	A8	(SAD3H)
P9	A7	A6	A5	A4	A3	A2	A1	A0	(SAD4L) Note
P10	A15	A14	A13	A12	A11	A10	A9	A8	(SAD4H) Note

Note: Parameters P9 and P10 must be set only when the dual-screen drive method (W/S = 1) and two-layered configuration are selected. SAD4 defines the fourth screen block display start address.

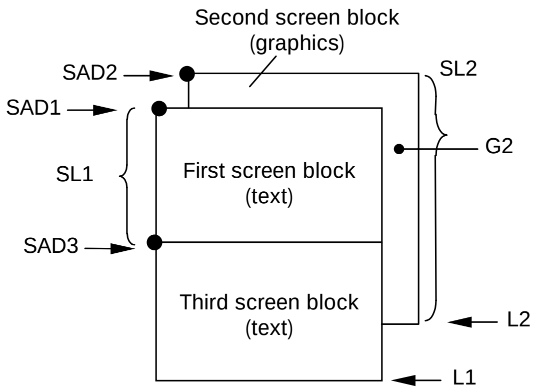
HEX	L7	L6	L5	L4	L3	L2	L1	L0	Number of lines [SL]
	BIN								
00	0	0	0	0	0	0	0	0	1
01	0	0	0	0	0	0	0	1	2
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
7F	0	1	1	1	1	1	1	1	128
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
FE	1	1	1	1	1	1	1	0	255
FF	1	1	1	1	1	1	1	1	256

The next page shows the relationship between display modes and SAD and SL.

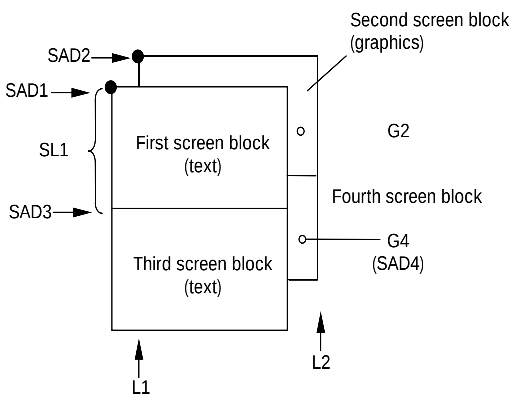
[Display modes]

(1) Text display mode

W/S		First screen block	Second screen block
0	First layer Second layer	SAD1 SL1	SAD2 SL2
	Third screen block (split)	SAD3 Note 1	
	When not using split screens, set both SL1 and SL2 to L/F + 1. <Example of screen configuration> Note 3		

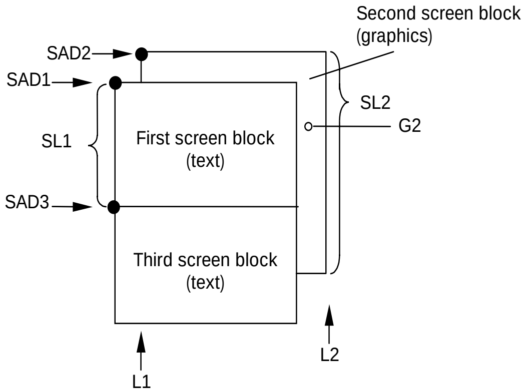


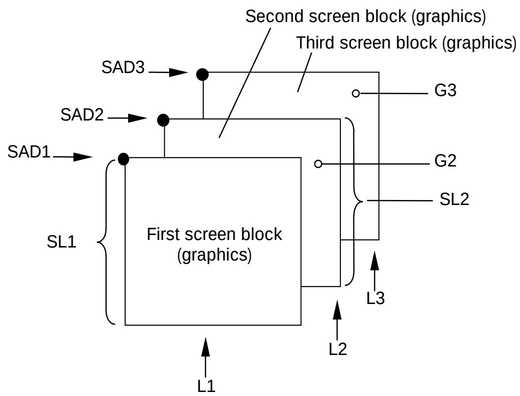
W/S		First layer	Second layer
1	Upper screen	SAD1 SL1	SAD2 SL2
	Lower screen	SAD3 Note 2	SAD4 Note 2
	Set both SL1 and SL2 to $\frac{L/F}{2} + 1$ <Example of screen configuration> Note 3		



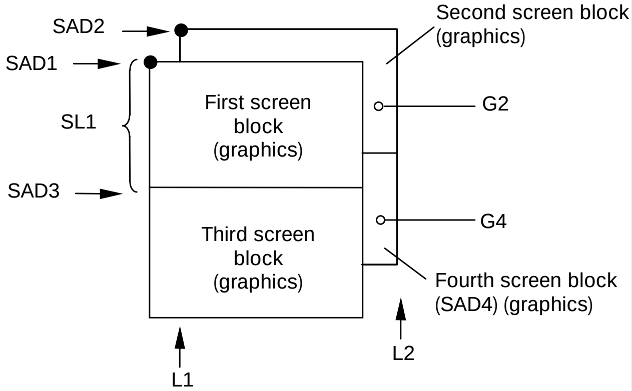
(2) Graphic display mode

<table>
<tr><th>W/S</th><th></th><th>First layer</th><th>Second layer</th></tr>
<tr><td rowspan="3">0</td><td rowspan="2">Two-layer composition</td><td>SAD1
SL1</td><td>SAD2
SL2</td></tr>
<tr><td colspan="2">SAD3 Note 1</td></tr>
<tr><td colspan="3">When not using split screens, set both SL1 and SL2 to L/F + 1.

<Example of screen configuration>

</td></tr>
</table>

<table>
<tr><th>W/S</th><th></th><th>First layer</th><th>Second layer</th><th>Third layer</th></tr>
<tr><td rowspan="2">0</td><td>Three-layer composition</td><td>SAD1
SL1</td><td>SAD2
SL2</td><td>SAD3
—</td></tr>
<tr><td colspan="4"><Example of screen configuration>

</td></tr>
</table>

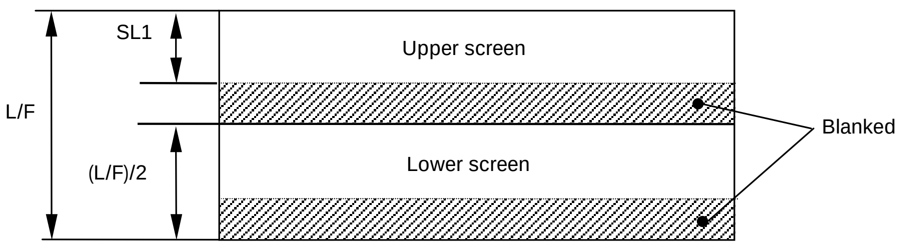
W/S		First layer	Second layer
1	Upper screen	SAD1 SL1	SAD2 SL2
	Lower screen	SAD3 Note 2	SAD4 Note 2
	Set both SL1 and SL2 to $\frac{L/F}{2} + 1$ <Example of screen configuration> Note 3		



Note 1: SAD3 is added to SL1 or SL2 (whichever has the fewest lines).

Note 2: Parameters corresponding to SL3 and SL4 are determined by L/F, and thus need not be set.

Note 3: When W/S = 1, the differences between SL1 and (L/F) / 2 and between SL2 and (L/F) / 2 are blanked.



CSRFORM

Defines the size and shape of the cursor displayed.

Although the cursor is normally used in text display mode, the S1D13305 can also display the cursor in graphic display mode to display kanji and other special characters.

	MSB							LSB
C	0	1	0	1	1	1	0	1
P1	0	0	0	0	X3	X2	X1	X0
P2	CM	0	0	0	Y3	Y2	Y1	Y0

[Parameter P1]

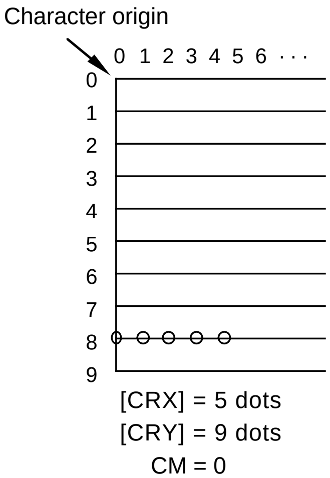
● CRX Defines the size of the cursor in the X direction by the number of dots counted from the character origin. Always make sure that CRX ≤ FX.

HEX	X3 X2 X1 X0 (BIN)	Number of dots [CRX]
0	0 0 0 0	1
1	0 0 0 1	2
·	· · · ·	·
·	· · · ·	·
4	0 1 0 0	5
·	· · · ·	·
·	· · · ·	·
E	1 1 1 0	15
F	1 1 1 1	16

[Parameter P2]

● CRY Defines the display line position of an underscored cursor in a character field by the number of dots counted from the character origin, or the size of a block cursor in the Y direction by the number of dots counted from the character origin.

HEX	Y3 Y2 Y1 Y0 (BIN)	Number of dots [CRY]
0	0 0 0 0	Illegal
1	0 0 0 1	2
·	· · · ·	·
·	· · · ·	·
8	1 0 0 0	9
·	· · · ·	·
·	· · · ·	·
E	1 1 1 0	15
F	1 1 1 1	16



● CM Defines the cursor shape.

CM 0: Underscore cursor
1: Block cursor

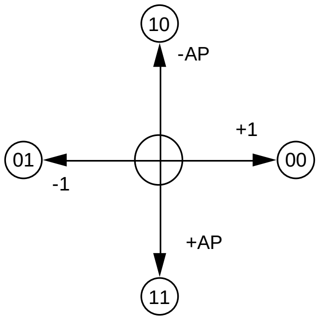
For the graphics screen, set CM = 1.

CSRDIR

● C Specifies the direction in which the cursor address counter is automatically shifted. When horizontal screen movement is specified, the cursor address is shifted -1 or +1 by the S1D13305 internal arithmetic/logic circuit. When vertical screen movement is specified, the cursor address is made to jump as many as the number of memory addresses defined by the address pitch (AP). Therefore, when accessing display memory successively in a given direction, it is only necessary to set the start address first. Then the cursor address need not be set by the MPU from the next data on.

	MSB							LSB
C	0	1	0	0	1	1	CD1	CD2

HEX	CD1 CD2 (BIN)		Shift direction
4C	0	0	Right
4D	0	1	Left
4E	1	0	Up
4F	1	1	Down



Note: Because the cursor moves in address units even if $FX \geq 9$, the cursor address must be preset for movement in character units. (See Section 4.1.4, “Cursor” on page 41.)

OVLAY

● C Specifies the method of composing layered screens and text or graphic display mode for each screen.

	MSB							LSB
C	0	1	0	1	1	0	1	1
P1	0	0	0	OV	DM2	DM1	MX1	MX0

[Parameter P1]

- MX0 Specifies the method of composing layered screens.
- MX1 Selects the method of screen composition from OR, AND, Exclusive OR, and Prioritized OR as listed in the table below. Because screens are composed in units of layers, different composition methods cannot be used for individual screen blocks, even if a layer is divided into two screen blocks.

  Prioritized OR is the same as simple OR unless the flashing of individual screens is used in combination with it.

MX1	MX0		Composition method	Application example
0	0	$L1 \cup L2 \cup L3$	Simple overlay (OR)	Underlining, rules, mixed text, and graphic display
0	1	$(L1 \oplus L2) \cup L3$	Black & white reverse overlay (EXOR)	Characters in inverse video, area flashing, underlining
1	0	$(L1 \cap L2) \cup L3$	Selective overlay (AND)	Simple animation, three-dimensional appearance
1	1	L1 > L2 > L3	Prioritized overlay	

Note: L1: First layer (text or graphics)
L2: Second layer (graphics only)
L3: Third layer (graphics only)

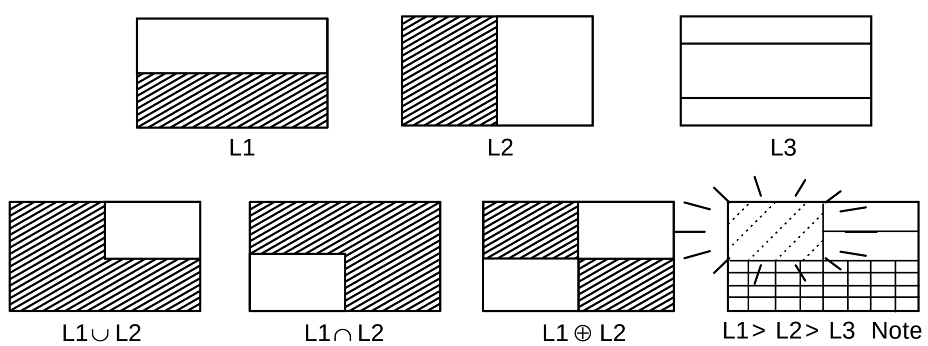


Figure 3-3 Example of screen compositions

Note: L1: Not flashing
L2: Flashing at 17 Hz (as specified by DISP ON/OFF command)
L3: Flashing at 2 Hz

● DM1 Specifies the display mode of the first screen block.

● DM2 Specifies the display mode of the third screen block.

DM1, DM30: Text mode
1: Graphics mode

Note: 1 The second and fourth screen blocks are limited to graphics mode.

2 When W/S = 1, DM1 and DM2 can only be set to (0, 0) or (1, 1).
Even when W/S = 0, DM1 and DM2 should be set to (0, 0) or (1, 1).

● OV Specifies a two-layer or three-layer composition in graphics mode.

OV 0: Two-layer composition
1: Three-layer composition

Note: Set OV = 0 for mixed text and graphics mode.

CGRAM ADR

● C Defines the offset address of CG RAM in the display memory space.

	MSB							LSB	
C	0	1	0	1	1	1	0	0	
P1	A7	A6	A5	A4	A3	A2	A1	A0	(SAGL)
P2	A15	A14	A13	A12	A11	A10	A9	A8	(SAGH)

Note: For details on how to define CG RAM, see Section 4.1.2, “Character Generator (CG)” on page 33.”

HDOT SCR

Although the screen can be scrolled left or right only in units of characters using the SCROLL command alone, the combined use of this command allows the screen to be scrolled in units of dots.

The scrolling on individual layers, however, cannot be controlled.

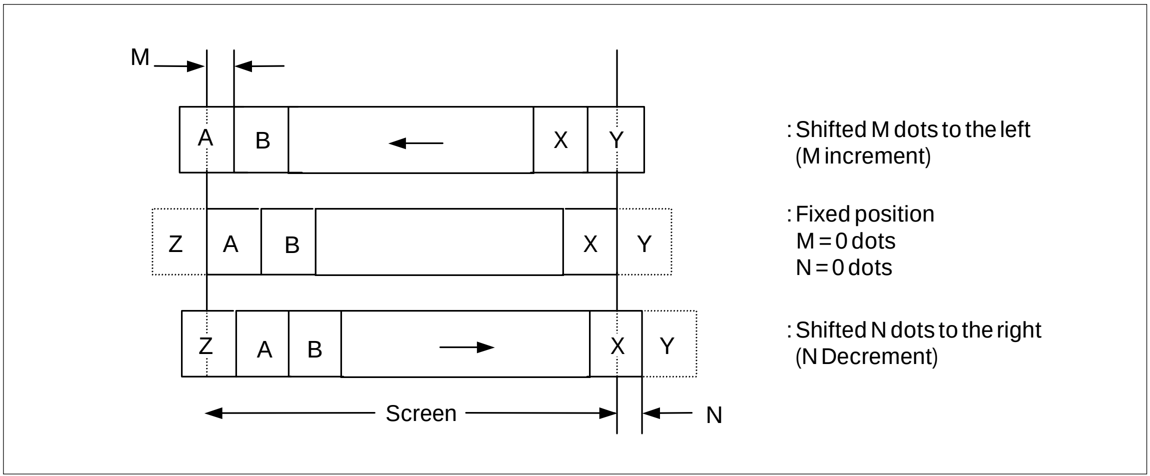
This command defines the number of dots to be shifted from the character origin.

	MSB							LSB
C	0	1	0	1	1	0	1	0
P1	0	0	0	0	0	D2	D1	D0

[Parameter P1]

● D0–D2 The C/R value must be set to one more than the number of display characters before using HDOT SCR to scroll the screen in units of dots. Smooth scrolling (dotwise scrolling) is possible when the MPU resends the HDOT SCR command to the S1D13305 at given time intervals for setting the number of dots to be shifted from the character origin.

HEX	D2	D1	D0	Number of dots to be shifted
	BIN			
00	0	0	0	0
01	0	0	1	1
02	0	1	0	2
.	.	.	.	.
.	.	.	.	.
06	1	1	0	6
07	1	1	1	7



Note: See Section 4.1.7, “Scrolling” on page 46, for more information about this function.

3.2.3 *Drawing Control Commands*

CSRW

● C

This command is used to write the cursor address to the cursor register.
Because the S1D13305 has only one address input bit, only two addresses in the address space of the MPU can be specified at a time. Therefore, the MPU cannot directly access display memory. To compensate for this inconvenience, the S1D13305 has a 16-bit cursor register that serves the purpose of MPU addresses.

	MSB						LSB	
C	0	1	0	0	0	1	1	0
P1	A7	A6	A5	A4	A3	A2	A1	A0	(CSRL)
P2	A15	A14	A13	A12	A11	A10	A9	A8	(CSRH)

The cursor address is set in the S1D13305 before display memory (VRAM, CG RAM, or CG ROM) is automatically accessed. If this address is not set, display starts from the address set last or an automatically shifted address. (The cursor address register can only be modified by other than the CSRW command by executing a memory control command.)

The cursor address is not affected by scrolling display because it is managed by the absolute display memory addresses fixed in hardware. Note also that the cursor address points to the absolute display memory address where data for the origin part of the character field is stored.

CSRR

● C

This command is used to read a cursor address from the cursor register. When this command is written to the S1D13305, the low-order byte of the cursor address (CSRL) is set in the output buffer. Therefore, the high-order byte of the cursor address (CSRH) also can be read out by entering the RD signal following this command.

	MSB						LSB	
C	0	1	0	0	0	1	1	0
P1	A7	A6	A5	A4	A3	A2	A1	A0	(CSRL) Note
P2	A15	A14	A13	A12	A11	A10	A9	A8	(CSRH) Note

Note: This is the read data.

3.2.4 *Memory Control Commands*

MWRITE

This command is used by the MPU to place the S1D13305 in the data input state before writing data to display memory. Each time the $\overline{WR}$ signal is input following this command, the S1D13305 automatically modifies the cursor address at which to write display memory according to the CSRDIR value. This allows the MPU to write two or more consecutive items of data to display memory.

	MSB							LSB	
C	0	1	0	0	0	0	1	0	
P1									
P2									
⋯									
Pn									n ≥ 1

P1, P2, · · · , Pn: Display data

MREAD

This command is used to place the S1D13305 in the data output state and store the contents of display memory (specified by the cursor address) in the data bus buffer before reading data from display memory. Each time the $\overline{RD}$ signal is input following this command, the read cursor address of display memory is automatically modified according to the CSRDIR value, and read data is stored in the data bus buffer. Because the command is executed in a manner similar to pipelined processing, high-speed readout limited only by the MPU cycle time is possible.

When the cursor is displayed, the read data and cursor positions do not match (with the cursor two positions ahead).

	MSB							LSB	
C	0	1	0	0	0	0	1	1	
P1									Read data
P2									Read data
⋯									
Pn									n ≥ 1, Read data

4 FUNCTION DESCRIPTION

4.1 Display Functions

4.1.1 Screen Management

(1) Character configuration

The S1D13305 can display characters using a row-scanning type of character generator that defines character patterns in the fourth quadrant with respect to the character origin as shown below. Although the character generator used determines the size of the character font area, the size of the character field can be varied in both the X and Y directions.

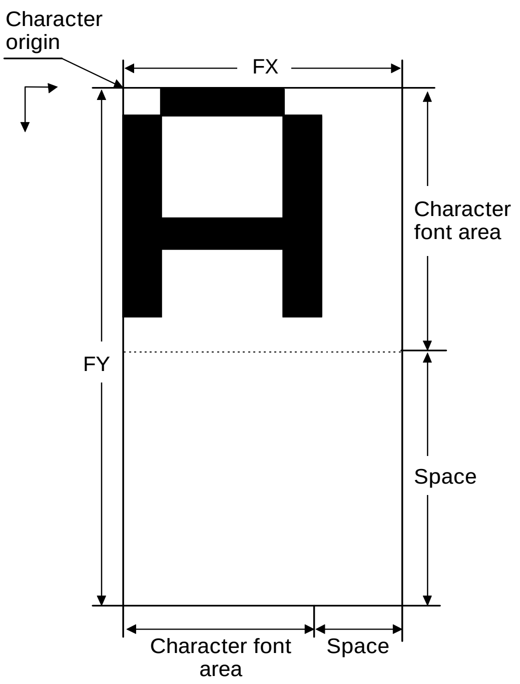


Figure 4-1 Character display ([FX] ≤ 8 dots).

	D7 MSB							D0 LSB
R0	0	1	1	1	0	0	0	0
R1	1	0	0	0	1	0	0	0
R2	1	0	0	0	1	0	0	0
R3	1	0	0	0	1	0	0	0
R4	1	1	1	1	1	0	0	0
R5	1	0	0	0	1	0	0	0
R6	1	0	0	0	1	0	0	0
R7	0	0	0	0	0	0	0	0
R8	0	0	0	0	0	0	0	0
R9	0	0	0	0	0	0	0	0
R10	0	0	0	0	0	0	0	0
R11	0	0	0	0	0	0	0	0
R12	0	0	0	0	0	0	0	0
R13	0	0	0	0	0	0	0	0
R14	0	0	0	0	0	0	0	0
R15	0	0	0	0	0	0	0	0

Figure 4-2 Example of character generator definition

Character font area: An area in which the character pattern is drawn
Character field: Character font area + space

To alter the character field, leave any portions other than the character font area set to 0 and increase FX or FY to enlarge the size of space as desired.

Even when one character requires two or more memory addresses, the character field can be set to any desired size.

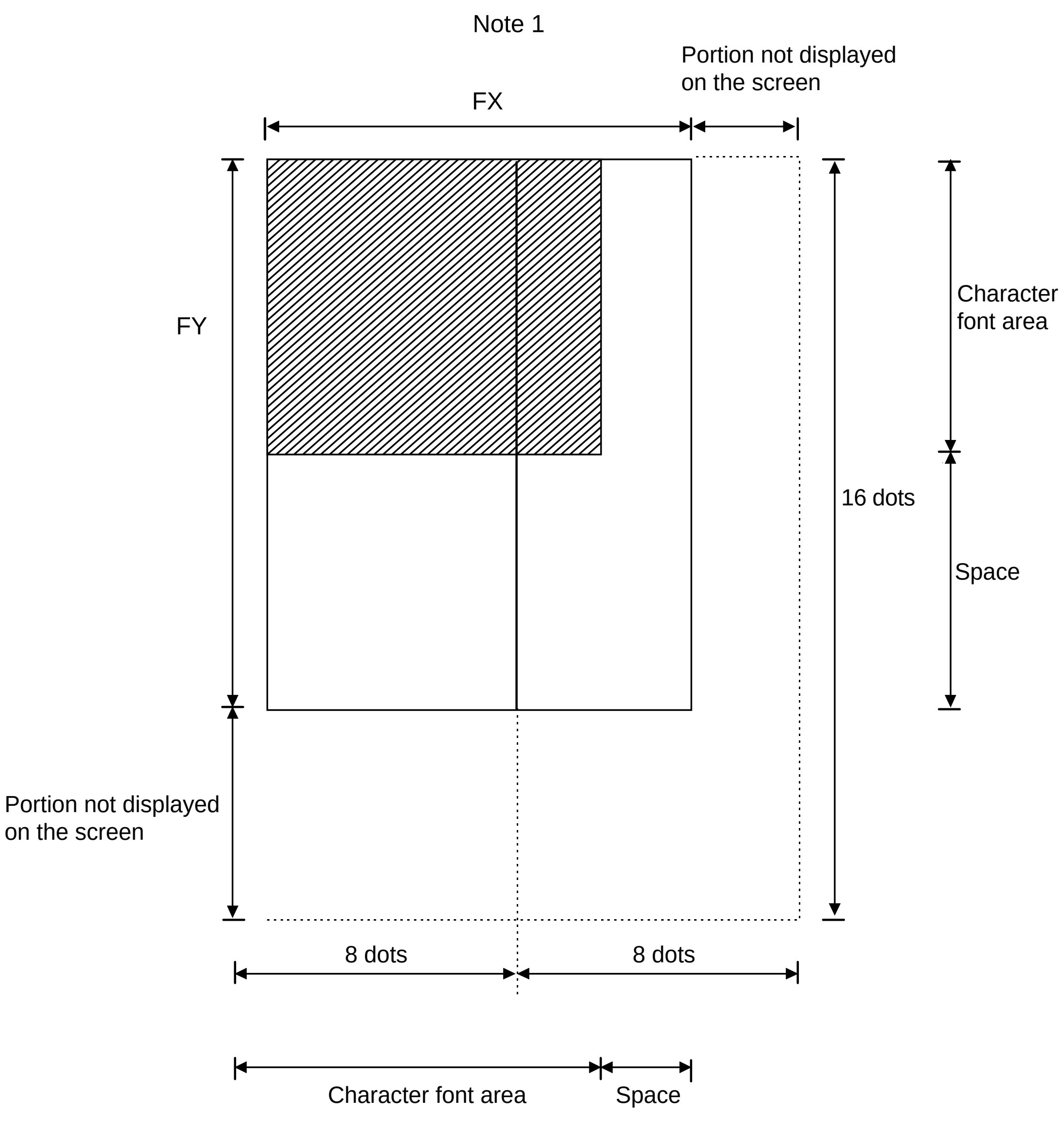


Figure 4-3 Example of character configuration consisting of two or more memory addresses (when [FX] = 9)

Note 1: The S1D13305 does not automatically insert character spaces. If the character field is greater than or equal to 9 dots, two memory addresses are required to configure one character even when the character font area may be within 8 dots.

4.1.2 Character Generator (CG)

(1) Features of each character generator

① Internal character generator

The internal character generator is effective for a minimum display system consisting of the S1D13305, display memory (data RAM), LCD unit, single-chip MPU, and a power supply. Moreover, because the internal character generator includes CMOS mask ROM, it is very advantageous when low power consumption is desired.

- Character font
  - 5 x 7 dots (See Section 4.4.1, “Character Fonts (Internal CG)” on page 62.)
- Number of characters
  - 160 JIS-compliant characters
- Combined use with CG RAM possible (up to 64 characters)
- Processing of the character field space part
  - The S1D13305 automatically sets spaces in the range of 8 x 16 dots maximum.

② External character generator

External CG ROM may be used when character fonts other than those provided by the internal character generator are desired. Data can be stored in external CG ROM in the same way as in CG RAM. (See (3) Method of determining the CG address.)

- Character font
  - 8 x 8 dots maximum <M2 = 0>
  - 8 x 16 dots maximum <M2 = 1>
- Number of characters
  - Up to 256 characters (or 192 characters when used in combination with CG RAM)
- Mapped addresses in the display space
  - F000H–F7FFH <M2 = 0>
  - F000H–FFFFH <M2 = 1>
- Processing of the character field space part
  - Spaces (data “0”) must be stored in ROM in the range of 8 x 16 dots maximum.

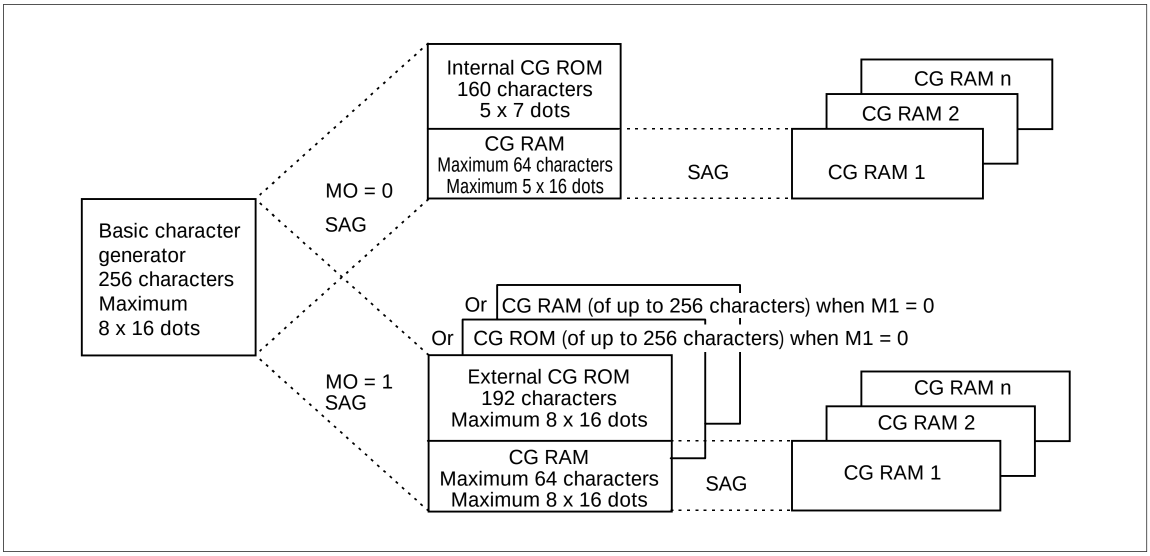
③ CG RAM

CG RAM as a graphic generator allows any desired character font to be defined by the user. Moreover, because the MPU can alter address mapping in the display memory space can be altered as required, unused portions of display memory can be effectively utilized.

- Character font
  - 8 x 8 dots maximum <M2 = 0>
  - 8 x 16 dots maximum <M2 = 1>
- Number of characters
  - Up to 64 characters when used in combination with CG ROM
  - Up to 256 characters when used only in F000H to FFFFH
- Defined area of CG RAM in the display memory space
  - CG RAM (maximum 64 characters) that can be used in combination with CG ROM can be allocated to any desired contiguous addresses.
  - CG RAM (maximum 65 characters or more) that cannot be used in combination with CG ROM must be allocated to fixed addresses F000H through FFFFH. When 193 characters or more must be defined in this fixed address area, set SAG = F000H and M1 = 0.

(2) Concept of how character generator banks are set

Because the character codes handled by the S1D13305 consist of 8 bits, the number of discrete characters that can be displayed simultaneously is limited to a maximum of 256. The CGRAM ADR command can be used to switch banks, however, thus extending the number of usable characters as shown below.



Note: Up to 64 characters can be used in one bank. Note that the relationship between patterns and codes of the character generator varies when banks are switched over.

Table 4-1 Various Settings Made to the Character Generator

CG Select Item		Parameter	Remark
Switch between internal CG and external CG		M0	
Range of character field size in Y direction	1 to 8 dots 9 to 16 dots 16 dots or more	M2 = 0 M2 = 1 Graphics mode processing (8 dots x 1 line)	
Switch between internal CG ROM and CG RAM Switch between external CG ROM and CG RAM		Automatic processing	Character code determined by the S1D13305
Correct D6 bit in CG RAM character code		M1	
CG RAM data stored address		Specified by CG RAM ADR command	Can be moved to any place in the display memory space
Defined area of external CG ROM	192 characters or less 193 characters or more	Other than the CG RAM-defined areas in Table 4-4 Set SAG = F000H and place SAG over the CG ROM table.	

(3) Method of determining the CG address

The addition shown below is performed to generate CG RAM addresses. Therefore, note that CG RAM data is not mapped from addresses set in the SAG register to the VRAM space, but are mapped based on the SAG + character code + row select address.

① When number of lines that comprise the character font is equal to or less than 8 (M2 = 0, M1 = 0)

SAG	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character code	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0
+ row select address	0	0	0	0	0	0	0	0	0	0	0	0	0	R2	R1	R0
CG RAM address	VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

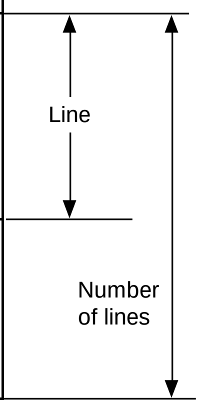
② When number of lines that comprise the character font is from 9 to 16, including both ends (M2 = 1, M1 = 0)

SAG	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Character code	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0	0	0	0	0
+ row select address	0	0	0	0	0	0	0	0	0	0	0	0	R3	R2	R1	R0
CG RAM address	VA15	VA14	VA13	VA12	VA11	VA10	VA9	VA8	VA7	VA6	VA5	VA4	VA3	VA2	VA1	VA0

Note: Only the addressing above is supported.

Table 4-2 Row Select Addresses

	R3	R2	R1	R0
ROW0	0	0	0	0
ROW1	0	0	0	1
ROW2	0	0	1	0
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
ROW7	0	1	1	1
ROW8	1	0	0	0
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
ROW14	1	1	1	0
ROW15	1	1	1	1



Note: Line count l ... when character font consists of 8 lines or less
Line count 2 ... when character font consists of 9 lines or more

③ When M1 = 1

For the character codes defined in CG RAM2, the S1D13305 automatically changes the D6 bit in the character code from 1 to 0. This ensures that the data storage area in CG RAM corresponds to contiguous addresses in the display memory space. Therefore, the CG RAM addresses to which to write data must be calculated as follows:

- Add addresses the same way as described above (M1 = 0).
- Change bit D6 in one character code from 1 to 0 when adding addresses.

Example of CG RAM definition (method of storing data) (See Figure 4-10, “Example of display memory mapping” on page 44.)

- Conditions
  - The pattern to define: Pattern A (8 x 16 dots per font) shown in Figure 4-2, “Example of character generator definition” on page 31.
  - Start address of the CG RAM table: 4800H
  - Character code of defined pattern: 80H (first character code in CG RAM area)

- Setting list

CG RAM ADR	5CH	Set SAG after calculating it by performing the method of CG RAM address calculation in reverse.
P1	00H	
P2	40H	
CSRDIR	4CH	Shift to the right
CSRW	46H	CG RAM area from 4800H
P1	00H	
P2	48H	
MWRITE	42H	
P1	70H	Write data for row 0
P2	88H	Write data for row 1
P3	88H	Write data for row 2
P4	88H	Write data for row 3
P5	F8H	Write data for row 4
P6	88H	Write data for row 5
P7	88H	Write data for row 6
P8	00H	Write data for row 7
P9	00H	Write data for row 8
.	.	.
.	.	.
.	.	.
P16	00H	Write data for row 15

4.1.3 Screen Configuration

(1) Screen configuration

The basic screen configuration of the S1D13305 consists of a text or graphics screen and an overlapping graphics screen. The graphics screen uses at least eight times as much display memory as the text screen.

Figure 4-4 schematically shows the relationship between the virtual and physical screens.

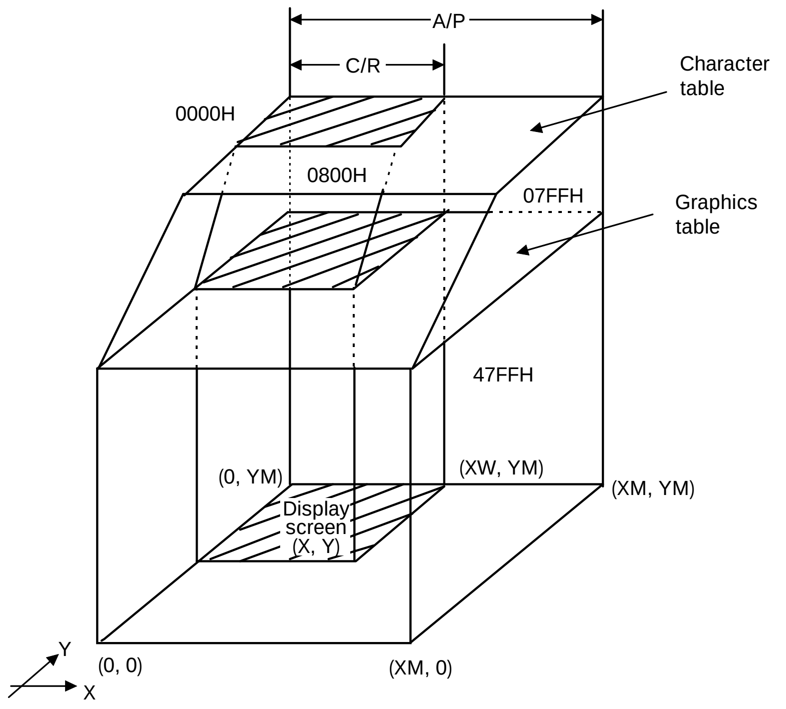


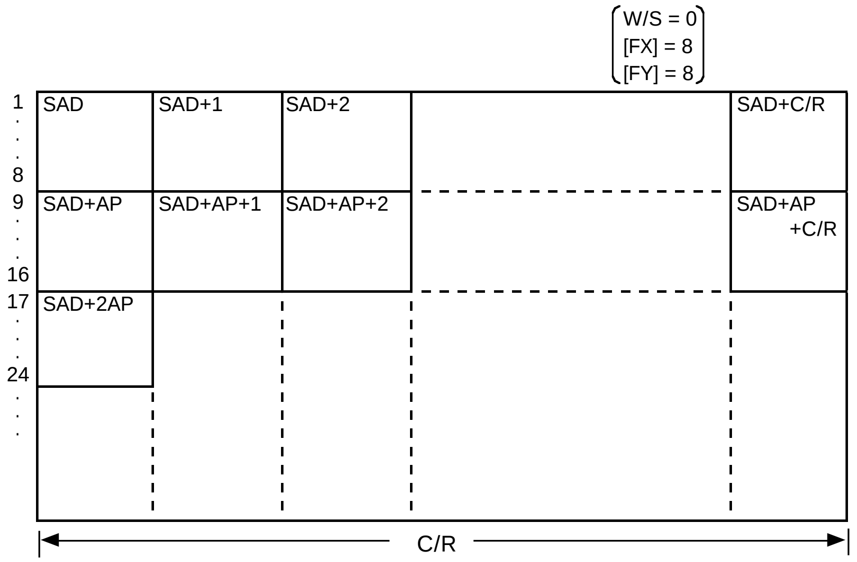
Figure 4-4 Relationship between virtual and physical screens

(2) Display address incrementation

The S1D13305 sequentially increments the display address in the X direction from the screen origin (home position) in the same way as a raster scan CRT. When the display address is incremented until the number of addresses equals C/R, one line of data is read from display memory. Next, to read the second line of data when in graphics mode, the S1D13305 starts from the address incremented by the distance equal to the address pitch (AP) from the address of the screen origin (SAD), then repeats the same operation as described above for the first line.

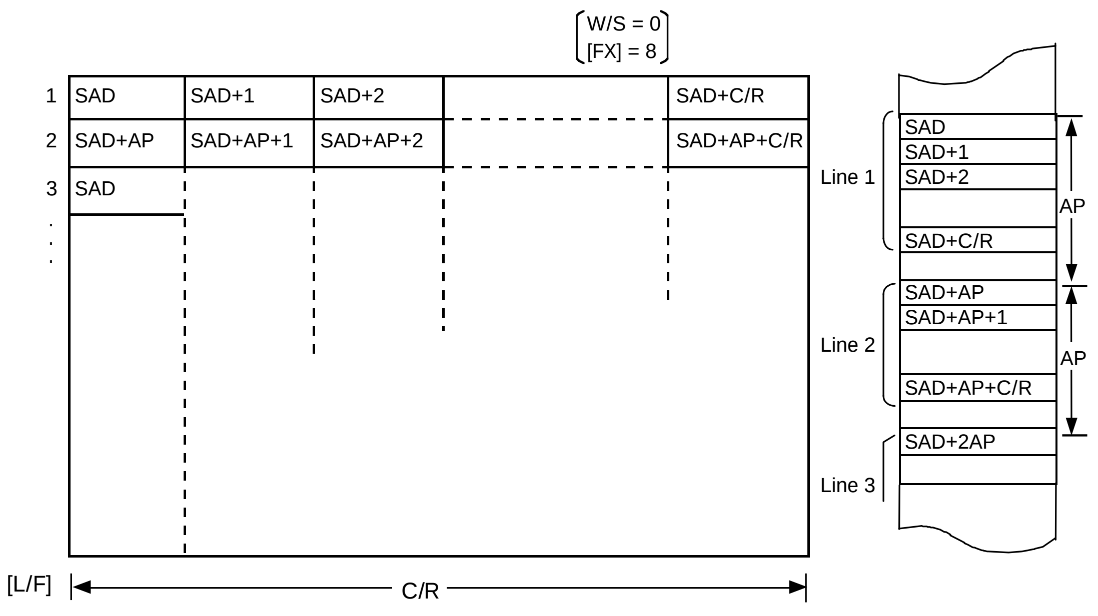
Conversely, in text mode the S1D13305 repeats the same operation as described above for the first line until the display address for one character is completed. (Character code is read from the same area, and data is read out in order of R0–R15 of the character generator.) (See Figure 4-2, “Example of character generator definition” on page 31.)

① Display address incrementation on text screen[Note]



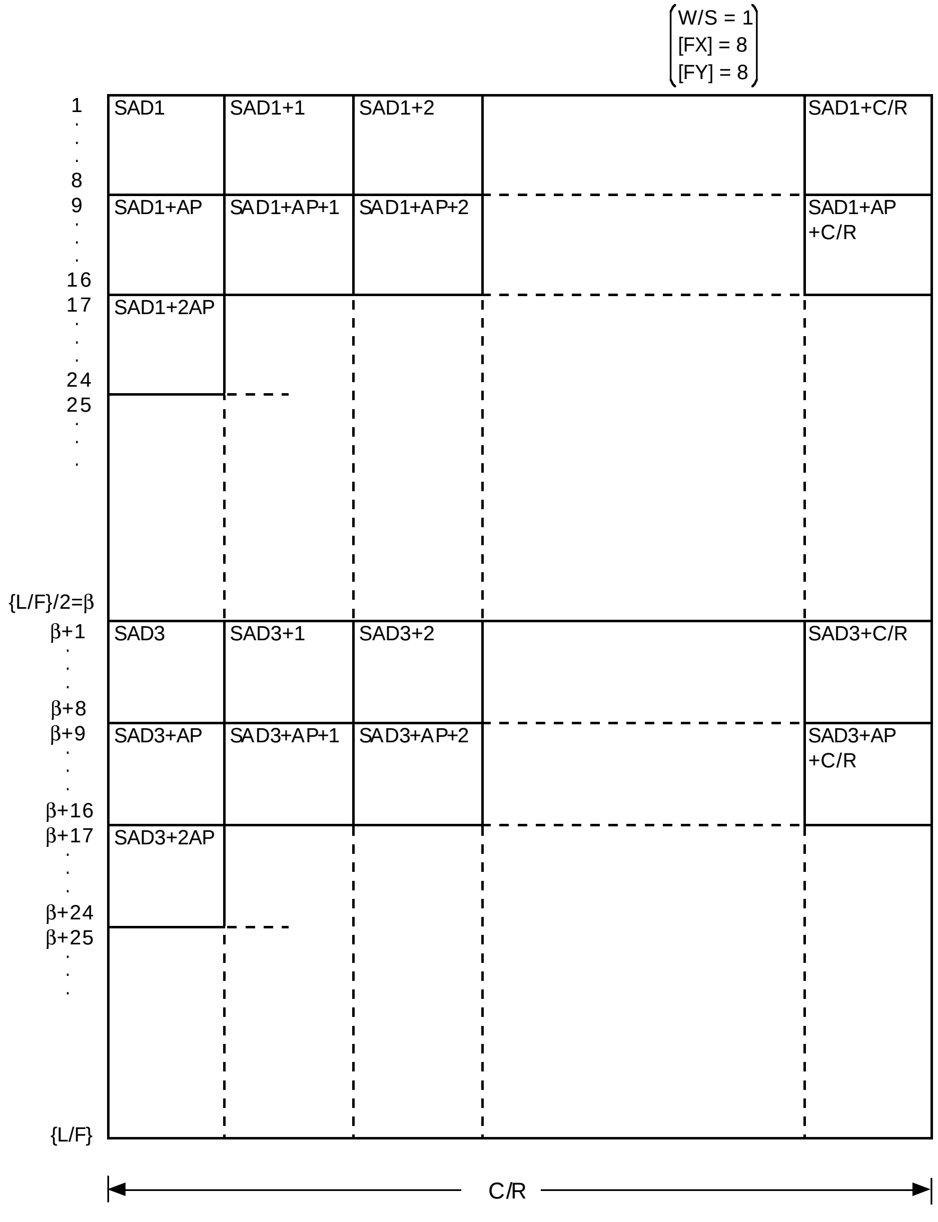
Note: One byte of display memory corresponds to one character.

② Display address incrementation on graphics screen[Note]



Note: One bit of display memory corresponds to one dot.

③ Display address incrementation during dual-screen drive (text screen)



Note: During dual-screen drive, the S1D13305 reads line 1 and line (β + 1) in succession. This constitutes one cycle, and the data for the upper and lower screens are read out alternately for each line.

(3) Basic timing

One display read cycle consists of nine ϕ0 (fosc) clock periods as shown below. This constitutes the basic display memory read cycle in the S1D13305. Therefore, the basic cycle is repeated C/R times to read one line of display data.

The period for which memory read pauses for each line is determined by the difference between TC/R and C/R, thus providing a means for fine tuning the frame frequency. The LCD drive waveform is output even during this pause period. Therefore, TC/R can be set to any value (no matter how large), provided that the limitations imposed by C/R, fosc, fFR, and the LCD unit's display capacity are satisfied. This pause time also enables the MPU to directly access display memory data (cycle steal). LP is the primary screen control signal.

Note: Even when W/S = 1, the upper and lower screens each have time R (frequency division adjustment period). In this case, the LP signal is active only at the end of the lower screen display period.

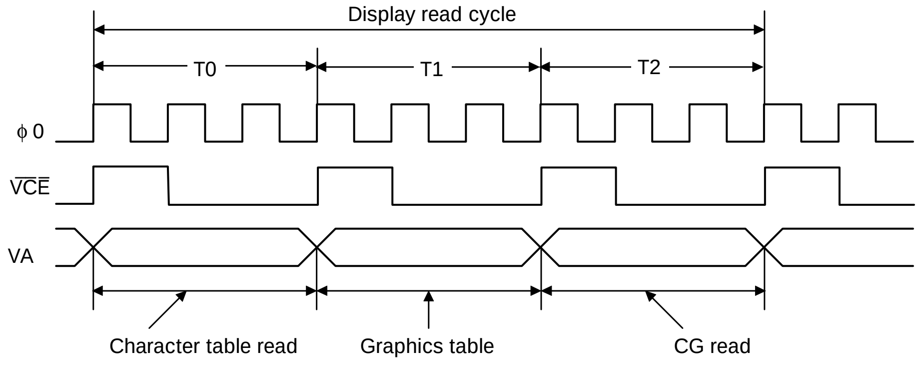


Figure 4-5 Basic display memory read cycle

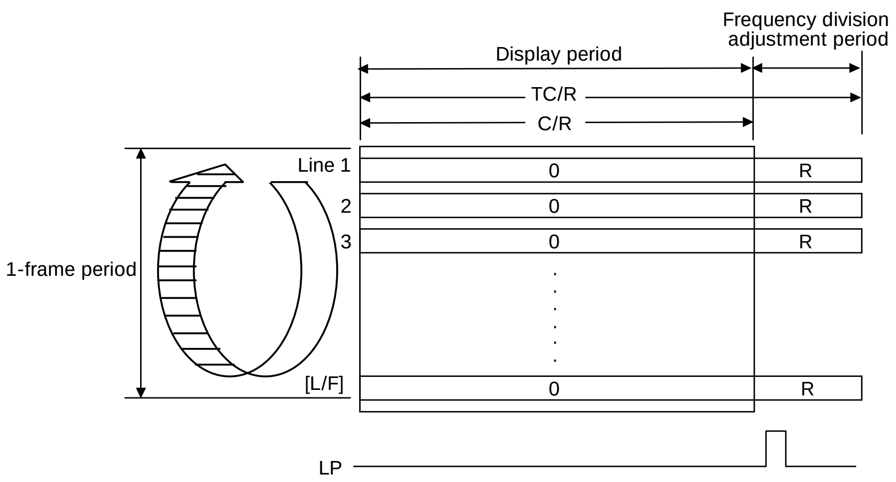


Figure 4-6 Relationship between TC/R and C/R

In this case, LP is active only at the end of the lower screen's display interval.

4.1.4 Cursor

(1) Cursor register function

The cursor register in the S1D13305 serves dual purposes as a cursor address register required to display the cursor on the screen, and as an address pointer to be referenced when accessing display memory.

Cursor register
- Cursor display address register
- Address pointer

To access any display memory area other than the screen while displaying the cursor, the cursor address must be preset before attempting such access and restored to the previous value after access is completed.

Note: The cursor will disappear if the cursor address is moved to any area other than the screen for more than several 100 ms.

(2) Direction of cursor movement

The cursor address is automatically shifted in the specified direction from the value preset by a memory control command.

(3) Cursor display layer

Although the S1D13305 can display up to three overlaid layers, the cursor can be displayed in only one of those layers. In other words, the cursor-attribute layer (or layer in which the cursor can be displayed) is:

First layer (L1) during two-layer composition, or
Third layer (L3) during three-layer composition.

The cursor will not appear if moved to other than those cursor-attribute layers. If the cursor must be displayed, change the layers or move the cursor-attribute layer to the cursor address location.

Although the cursor is generally displayed in text mode, the S1D13305 can also display a dummy cursor in graphics mode. This is accomplished by using the graphics screen as a display plane while not displaying the text screen, but using it to only generate addresses for cursor control.

Example: DISP ON/OFF

D = 1
FC1 = 0
FC0 = 1 } Cursor ON

FP1 = 0
FP0 = 0 } First screen block (text screen) OFF

FP3 = 0
FP2 = 1 } Second screen block (graphics screen) ON

To display the cursor, preset the cursor address in the first screen block area. To write display data, preset it in the second screen block area.

One conceivable application of this would be cursor display for graphically displayed kanji characters. In this case, the cursor displayed must be moved by presetting addresses from the MPU since the cursor is shifted automatically in units of display addresses, not characters.

Conversely, only a bar cursor can be displayed at the display address if the text screen is unavailable (i.e., during graphics-only screen configuration).

Moreover, when the first layer consists of a mixed text and graphics screen and the cursor changes shape into a block cursor, the S1D13305 automatically adjusts cursor display to display a block cursor on the text screen and a bar cursor on the graphics screen.

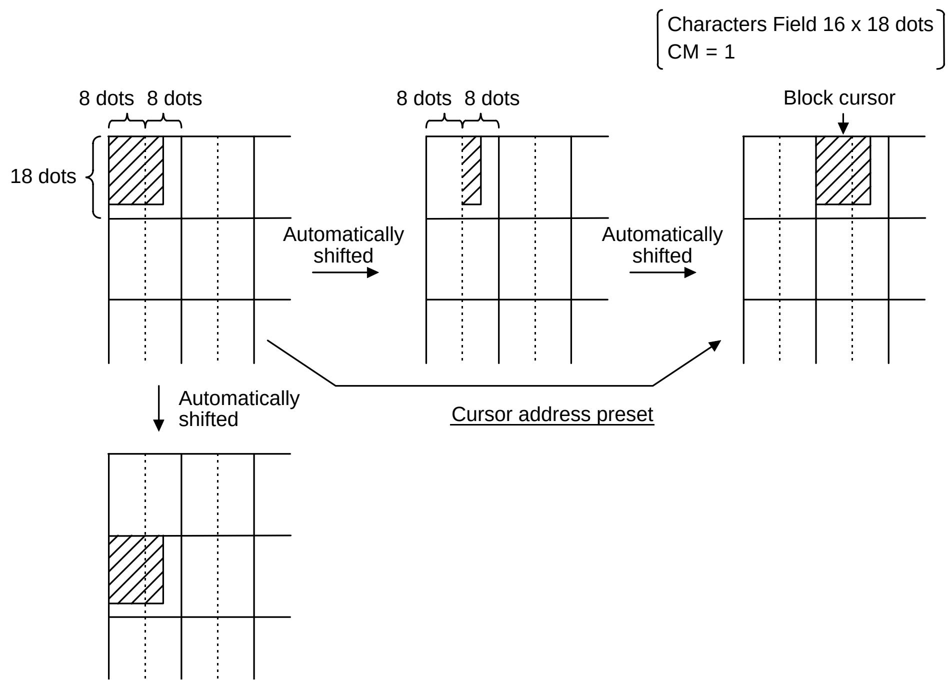


Figure 4-7 Example of cursor automatic shifting when CRX > 8

4.1.5 Relationship between Display Memory and Screens

The display memory of the S1D13305 may be used as a virtual screen of greater width than the physical size of the LCD panel address range (C/R). One layer of the S1D13305 may be considered a window through which to look at the part of display memory that comprises a virtual screen. This window can be divided into two blocks that may correspond to independent areas on the virtual screen. Therefore, it is possible to use one block as a dynamically scrollable data area and the other as a stationary message area. (See Figure 4-8 and Figure 4-9.)

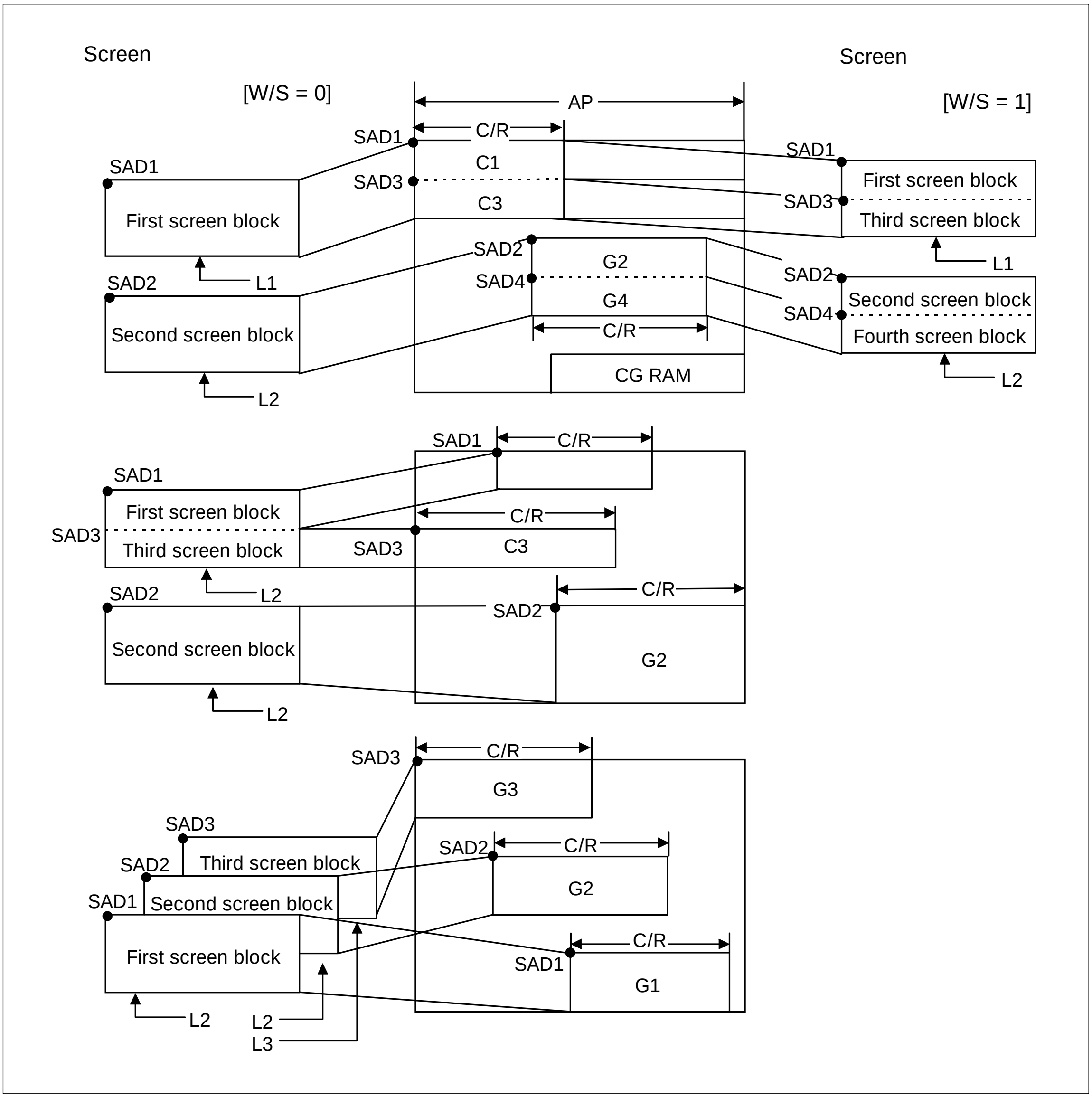


Figure 4-8 Relationship between display memory and screens

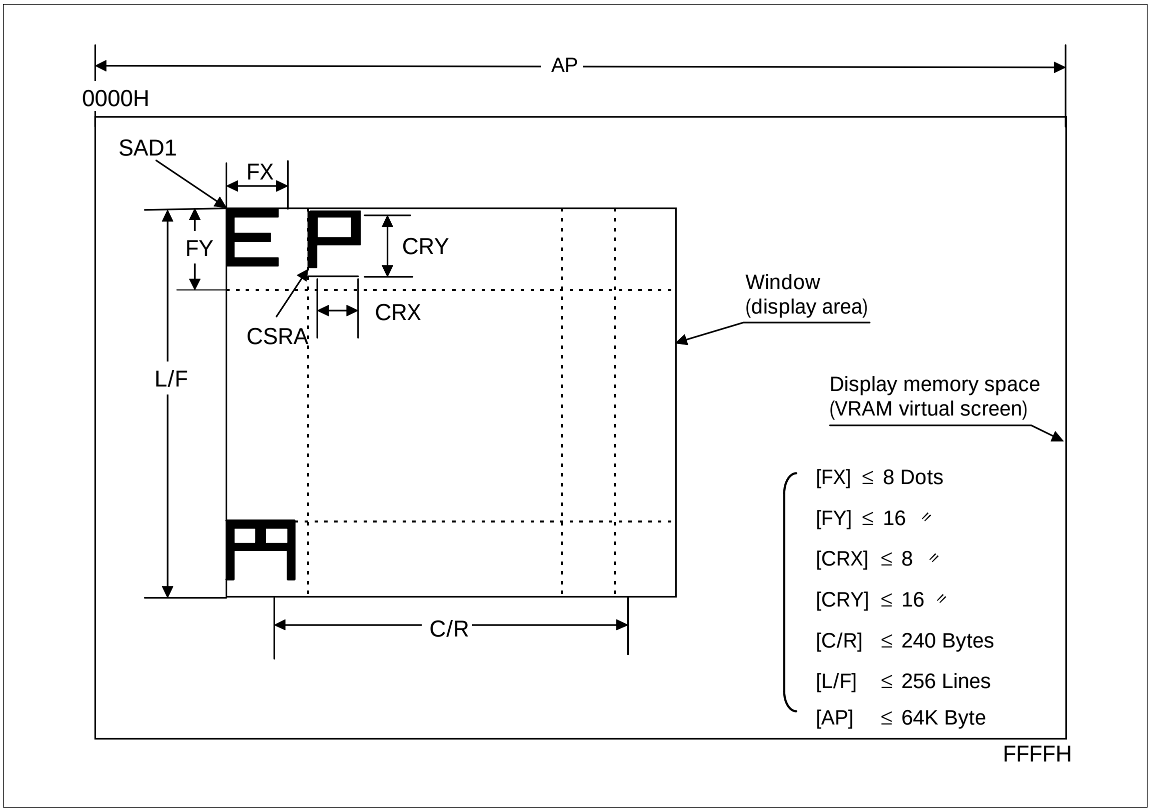


Figure 4-9 Window and display memory settings

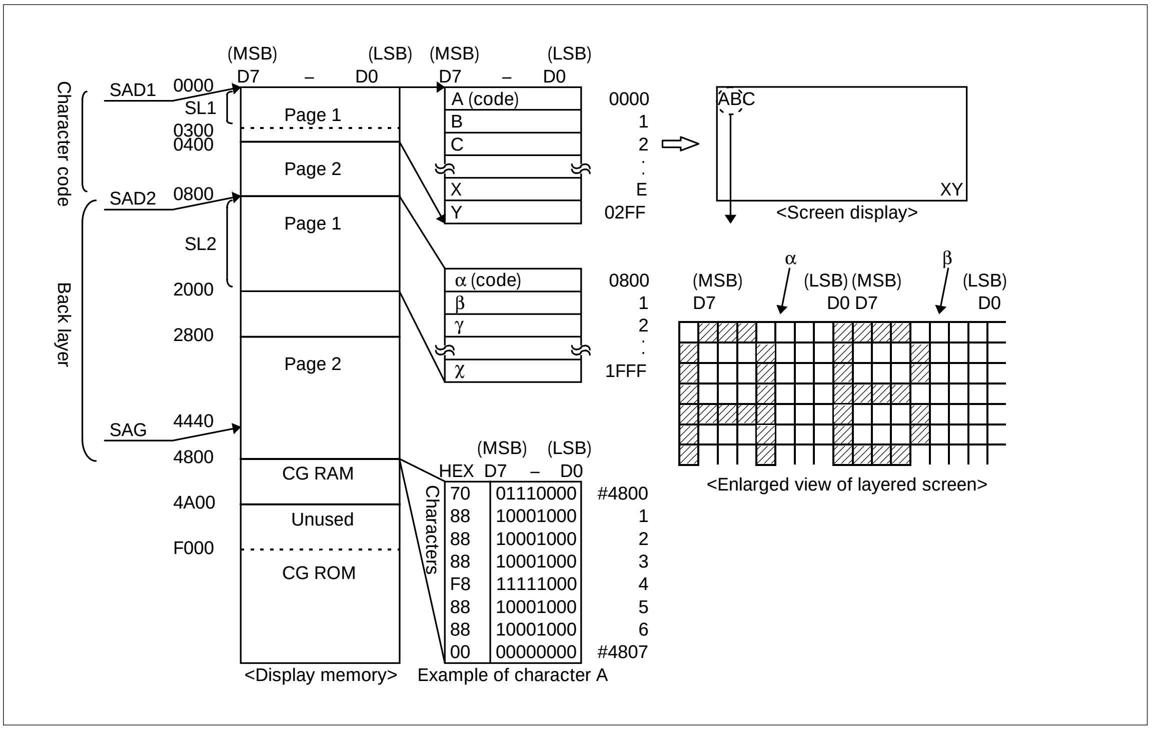


Figure 4-10 Example of display memory mapping

4.1.6 *Determining Various Parameters*

(1) Determining FX

Determine the character field size in the X direction [FX] from the number of dots in the X direction of display [VD] and the number of characters in the X direction [VC].

[VD] / [VC] ≤ [FX]

The brackets [ ] denote an integral value beginning with 1, and [FX] indicates the number of dots.

(2) Determining C/R

Next, determine a value for [C/R] from the values of [VC] and [FX].

[C/R] = | [FX] / 8 | rounded up ≤ [VC]

Note: [C/R] indicates the number of characters obtained in units of addresses.

(3) Determining TC/R

TC/R must maintain the relationship [TC/R] ([C/R] + 4.

(4) Relationship between f_{OSC} and f_{FR}

Once TC/R has been determined, the lower-limit value of the oscillation frequency (f_{OSC}) can be obtained from the equation below because the frame frequency (f_{FR}) and number of display lines [L/F] are predetermined,.

$f_{OSC} \geq \{[TC/R] \times 9 + 1\} \times [L/F] \times f_{FR}$

Note:
1. If standard crystals close to f_{OSC} thus obtained are unavailable, determine the appropriate f_{OSC} value for crystals with higher oscillation frequencies than the obtained value. To do so, reverse the calculation of the [TC/R] value in the equation above.
2. For the f_{FR} value of Epson LCD units, refer to the LCD unit specifications.

(5) Symptoms observed when TC/R is set incorrectly

- Scanning of display in the Y direction stops, with horizontal lines displayed in high contrast.
- All pixels go on or go off.
- The LP pin output signal is incomplete or inactive.
- The display of graphics or text becomes unstable.

Should any of the symptoms above be observed, even though the S1D13305's other signals connected to the LCD unit are normal, check whether the TC/R value is correct. If the TC/R value is the cause of the problem, simply set a larger TC/R value to restore normal operation.

Table 4-3 Example of Parameters for the LCD Unit

Number of pixels (X x Y)	[FX]	[FY]	[C/R]	TC/R	X'tal (MHz)
320 x 240	e.g., [FX] = 8 dots 320 ÷ 8 = 40··0 No blank dots	From a practical point of view, 8, 16, etc. are suitable.	[CR] = 40 = address → 27H During HDOT SCR, [C/R] = 41 addresses	2BH	5.72
	e.g., [FX] = 6 dots 320 ÷ 6 = 53··2 Two blank dots	↑	[CR] = 53 = address → 34H During HDOT SCR, [C/R] = 54 addresses	38H	7.40

Note: 1. Because the number of display dots varies with each LCD unit, there will be some fractional display dots depending on the value set for FX. In such case, the S1D13305 automatically blanks fractional parts at the right edge of the panel, and thus eliminates the need to manipulate display memory for adjustment.

2. Calculations are made assuming f_{FR} = 60 Hz.

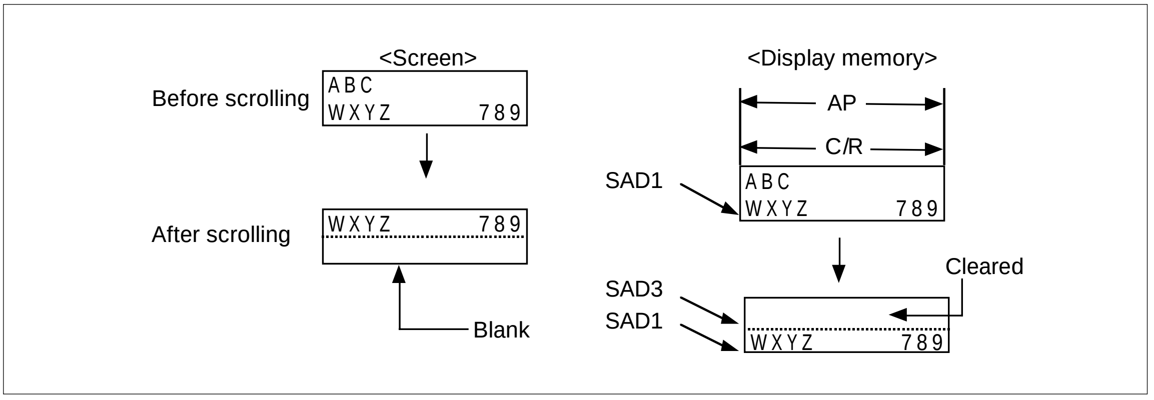
4.1.7 Scrolling

The MPU dynamically rewrites the scroll address registers (SAD1-SAD4) that provide the read start address in the S1D13305's display memory, thereby allowing various scroll modes to be set. In this case, the MPU manages all operations to execute scrolling, select scroll mode, and set a scroll rate.

(1) Intra-page scrolling

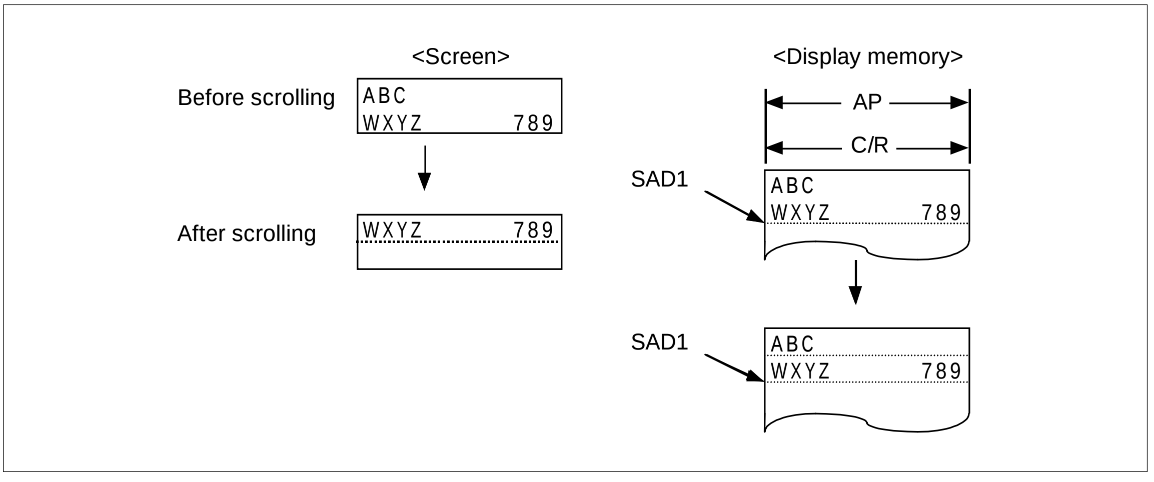
This refers to a mode of scroll operation whereby scrolling is performed within display memory space equivalent to one screen.

All lines are scrolled one line up and the bottom line is deleted as shown below. Since the S1D13305 does not automatically delete the bottom line, the MPU must rewrite the scroll address registers and simultaneously write blank data to the S1D13305.



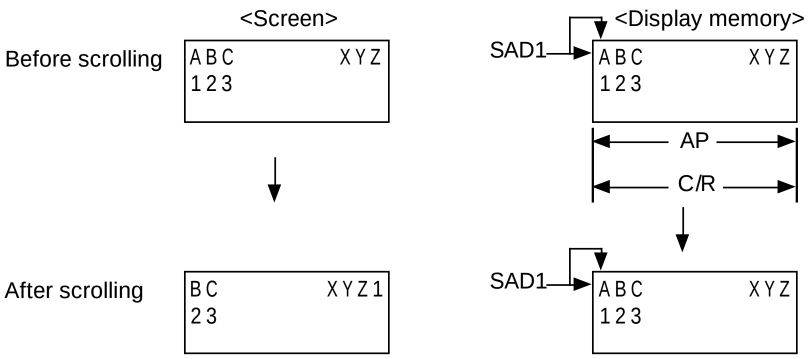
(2) Inter-page scrolling and page switching

Scrolling between pages and page switching can be performed only when display memory has more than one-screen equivalent capacity.



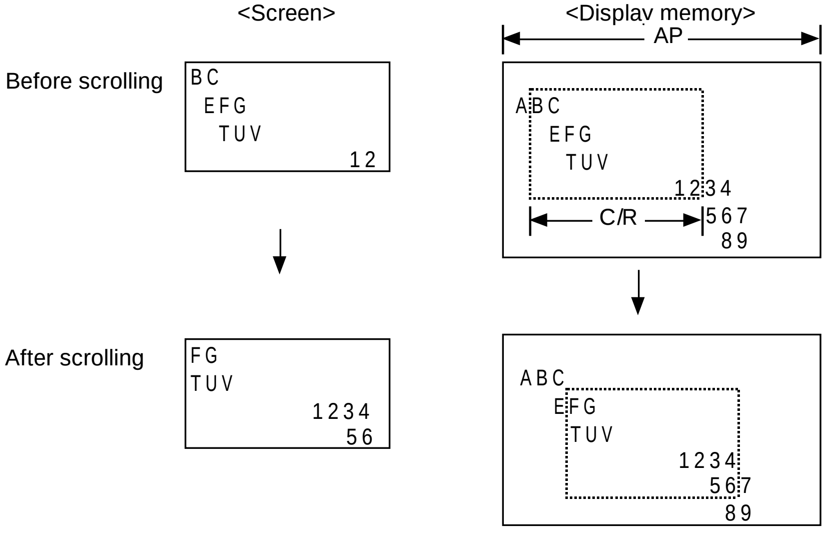
(3) Scrolling in the X direction

This refers to scrolling display in the X direction one character at a time, regardless of display memory size.



(4) Omnidirectional scrolling

This mode of scrolling is available when display memory has ample capacity larger than one screen in both the X and Y directions. Although display is normally scrolled one character at a time, the HDOT SCR command can be used to scroll display in the X direction one dot at a time.Note 1



(5) Scroll units

	Y direction	X direction
Text mode	Characters	Dots or characters
Graphics mode	Dots	Dots

Note 2

Note 1: Omnidirectional scrolling in units of dots is possible by using the SCROLL and HDOT SCR commands in combination.

Note 2: On a split screen, individual screen blocks cannot be independently scrolled in the X direction in dot units.

(6) Dotwise scrolling in the X direction (HDOT SCR)

Figure 4-11 shows the relationship between commands and display when a display pattern is smoothly scrolled to the left. In this case, the screen (window) moves to the right on a virtual screen. Therefore, the MPU only needs to sequentially increment the value of the HDOT SCR command parameter (number of dots to be shifted) without modifying the display start address (SAD) in the S1D13305 to shift display leftward one dot at a time. Then when display has been dot-shifted a distance equal to the character field, the MPU should reset the value of the HDOT SCR command parameter to 00H and simultaneously increment SAD by one address. Thus, smooth scrolling in the X direction is possible by performing this series of operations at appropriate time intervals.

To scroll the display pattern to the right, change the display dot address by reversing the order above. Should the window reach either edge of the virtual screen, use the MPU to manage the screen. Note that when smooth scrolling continues, the screen is not affected.

Also note that when scrolling display dotwise in the X direction using the HDOT SCR command, scrolling cannot be controlled separately in each layer because all layers are scrolled at the same time.

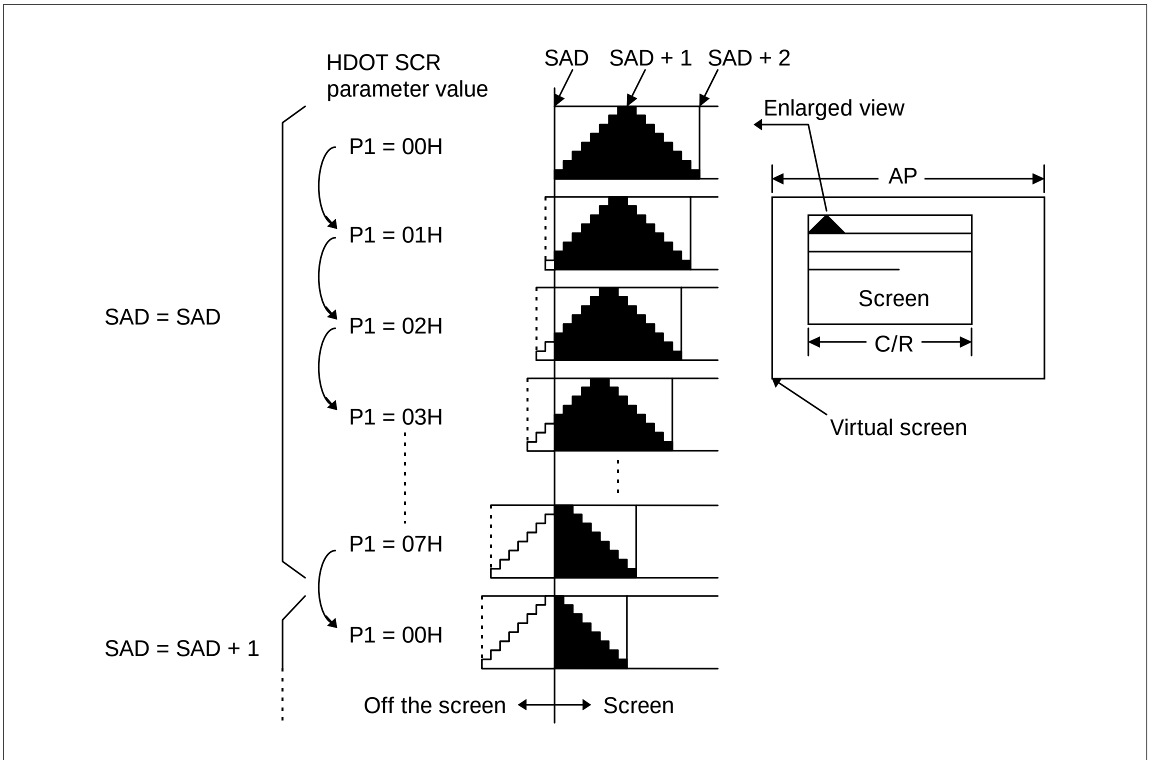


Figure 4-11 Example of using HDOT SCR ([FX] = 8)

Note: Because the speed at which the LCD responds to instructions varies with temperature, smooth scrolling at low temperatures in particular may not easily be recognized.

4.1.8 *Attribute Display using the Layered Function*

The S1D13305 provides a means of increasing the ability of expression on a monochrome liquid crystal display. More specifically, it uses the OVLAY and DISP ON/OFF commands to display characters in inverse video, produce halftone menu pads, and flash a given screen area for various highlighting effects as shown below.

Highlighting effects	MX1	MX0	Screen	First layer, single screen	Second layer, single screen
Inverse	0 1	1 1	IV EPSON	IV EPSON	
Halftone display	0 1	0 1	ME Yes, No	ME Yes, No	
Area flashing display	0 0	0 1	BL Error	BL	Error
Rules and underlining	0 0 1	0 1 1	RL LINE LINE	RL LINE LINE	

Use of the S1D13305's layered function will efficiently accomplish the highlighting effects above. The following describes a few examples of using this function to realize highlighting effects. Not all such effects can be used within the same screen block, however.

(1) Inverse

① Using the layered function

[Exclusive OR'ing of first layer (text) and second layer (graphics)]

①-1	CSRW CSDIR MWRITE	Write turn-on data "1" to the entire graphic area where characters are to be displayed in inverse video.
①-2	OVLAY MX0= "1" MX1= "0"	Specify an overlay method using the OVALY command so that the first and second layers will be exclusive OR'd.
①-3	DISP ON/OFF FP0= FP2 = "1" FP1= FP3 = "0"	Turn display of the first and second layers on using t he DISP ON/OFF command. → Characters are displayed in inverse video.

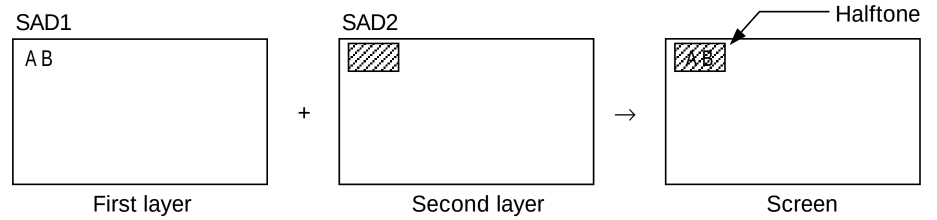
(2) Halftone display

The S1D13305 uses the DISP ON/OFF command's FP parameter to produce halftone display. This is accomplished by flashing the screen at 15 Hz. However, because this method of display may cause display to flicker, characteristics of the LCD module used must be carefully considered.

① Menu pad display

[OR'ing by the layered function]

OVLAY P1 = 00H DISP ON/OFF P1 = 34H	Disable flashing of the first layer and enable flashing of the second layer at 17 Hz, then overlay the first and second layers by OR'ing.



② Graph display

[OR'ing by the layered function]

OVLAY P1 = 00H DISP ON/OFF P1 = 34H	Disable flashing of the first layer and enable flashing of the second layer at 15 Hz, then overlay the first and second layers by OR'ing.

When displaying various data in the form of a graph for comparison purposes, this method of display is very effective because two types of diagrams distinguishable by differences in contrast can be displayed.

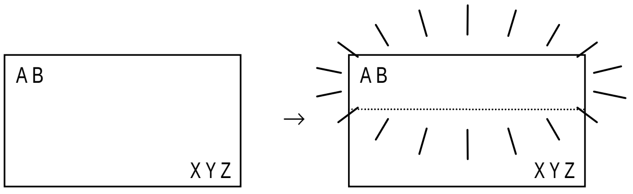
(3) Area flashing

① For flashing a few characters

Because the S1D13305 has a high-speed interface circuit, alternately rewriting the character and blank codes from the MPU to flash characters is an appropriate method. In this case, the MPU rewrites display data at intervals of 0.5 to 1.0 second as regulated by its internal timer.

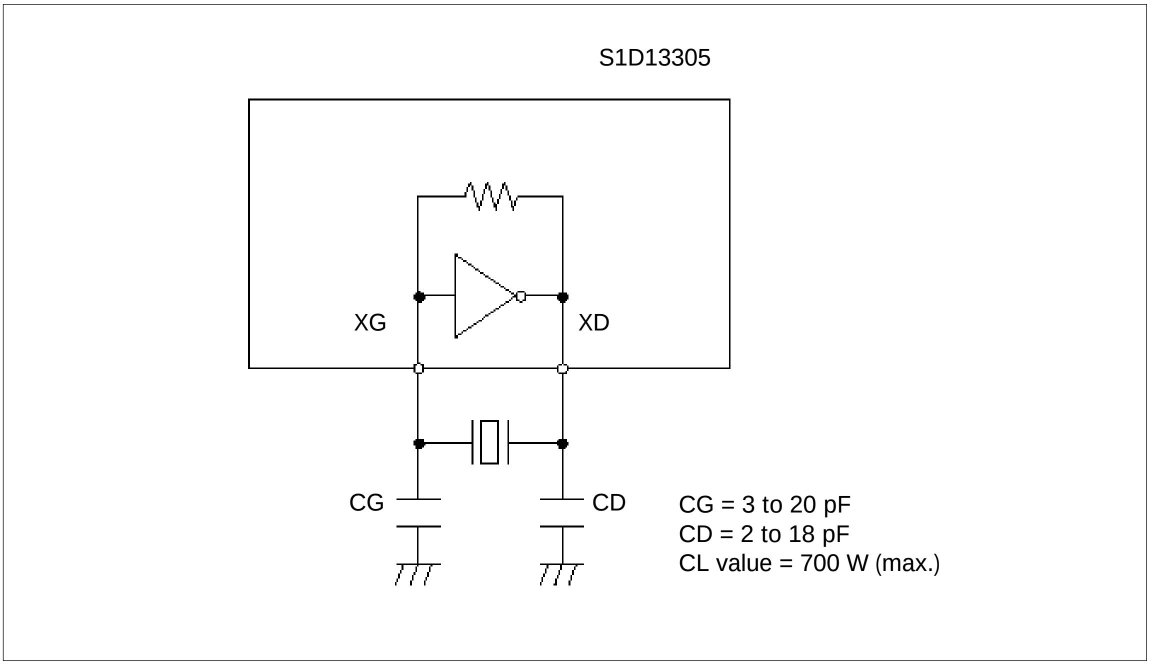
② For flashing a large area

SCROLL DISP ON/OFF OVLAY	Divide the first or second layer into halves with only the area required made to flash at 2 Hz, and overlay the halved layer blocks by OR'ing.



4.2 Oscillator Circuit

The S1D13305 features a built-in oscillator circuit, with a resonator connected to the XG and XD pins to generate oscillation. The resonator used here is usually a commercially available AT-cut quartz crystal resonator. Because the S1D13305 contains a built-in feedback resistor, the user need only connect this resonator and capacitors CG and CD externally to the chip. Note that the higher the oscillation frequency, the smaller the CG and CD values.

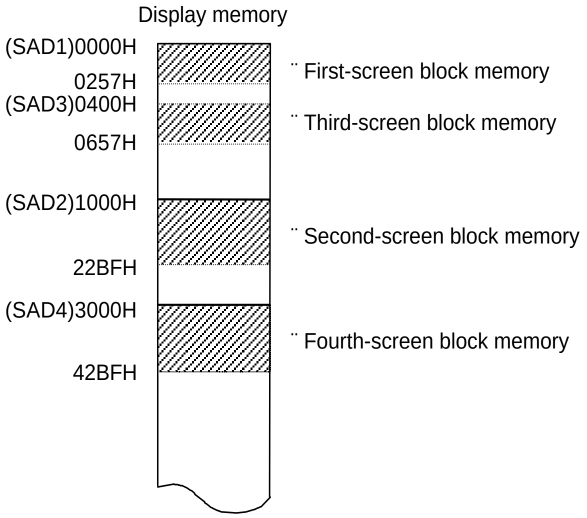
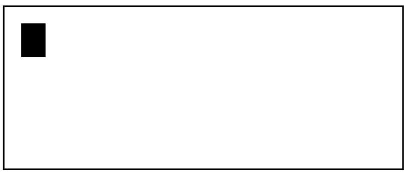


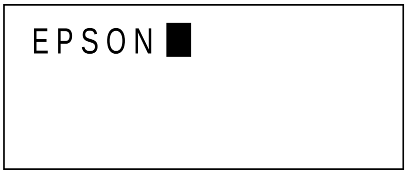
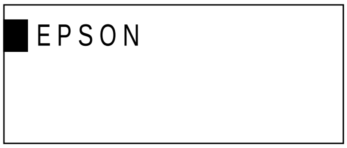
Note: XG and XD must be wired in the shortest distance possible so that the wiring capacitance does not increase oscillation frequency fluctuation or current consumption.

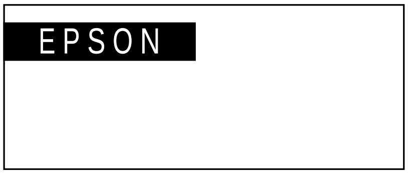
4.3 Example of Initial Settings

8-bit bus interface
LCD unit, 320 x 240 dots

No	Command	Operation
1	Power on	
2	Waits until power supply stabilizes.	Waits at least 3 ms after $V_{DD} \geq 4.5$ V and external reset are deasserted.
3	SYSTEM SET C = 40H P1 = 38H	Initializes the S1D13305. M0: Internal CG ROM M1: CG RAM (up to 32 characters) M2: Y-direction character field range (8 lines) W/S: Dual-screen drive method IV: Uppermost line not corrected
	P2 = 87H	FX: X-direction character field (8 dots) WF: Two-frame AC drive
	P3 = 07H	FY: Y-direction character field (8 dots)
	P4 = 27FH	C/R: Display address range (40 columns per line)
	P5 = 2DH	TC/R: Total display address time in X direction (46 addresses per line) f_{OSC} = 6.0 MHz, fFR = 60 Hz
	P6 = EFH	L/F: Number of display lines (240)
	P7 = 28H	AP: Virtual screen size in X direction (41 addresses)
	P8 = 00H	
4	SCROLL C = 44H	
	P1 = 00H P2 = 00H	Sets start address of the first screen block to 0000H.
	P3 = 7FH	Sets number of display lines in the first screen block to 120.
	P4 = 00H P5 = 10H	Sets start address of the second screen block to 1000H.
	P6 = 7FH	Sets number of display lines in the second screen block to 120.
	P7 = 00H P8 = 04H	Sets start address of the third screen block to 0400H.
	P9 = 00H P10 = 30H	Sets start address of the fourth screen block to 3000H.

No	Command	Operation
		
5	HDOT SCR C = 5AH P1 = 00H	Sets number of dots to be shifted in the X direction to 0.
6	OVLAY C = 5BH P1 = 01H	MX1, MX0: Overlaid for inverse display DM1: First screen block in text mode DM2: Third screen block in text mode
7	DISP ON/OFF C = 58H P1 = 56H	D: Entire screen display disabled FC1, FC0: Cursor made to blink at 2 Hz FP1, FP0: Display of first screen block turned on FC3, FP2: Display of second and fourth screen blocks turned on FP5, FP4: Display of third screen block turned on
8	CSRW C = 46H P1 = 00H P2 = 00H	Sets cursor address to the first screen block's start address (home position).
9	Clears the first layer display data.	Writes 20H (space character code) to memory location corresponding to the first layer (text screen).
10	Clears the second layer display data.	Writes 00H (dot turn-off data) to memory location corresponding to the second layer (graphics screen).
11	CSR FORM C = 5DH P1 = 04H P2 = 86H	CRX: Cursor size in X direction (5 dots) CRY: Cursor size in Y direction (7 dots) CM: Block cursor
12	DISP ON/OFF C = 59H	Restores entire screen display. Screen 

No	Command	Operation
13	CSR DIR C = 4CH	Sets direction of cursor movement so that the cursor shifts to the right.
14	MWRITE C = 42H P1 = 20H P2 = 45H P3 = 50H P4 = 53H P5 = 4FH P6 = 4EH	Sets space code. Sets character code for the letter “E.” Sets character code for the letter “P.” Sets character code for the letter “S.” Sets character code for the letter “O.” Sets character code for the letter “N.” 
15	CSRW C = 46H P1 = 00H P2 = 10H	Presets cursor address to the second screen block’s start address.
16	CSR DIR C = 4FH	Sets direction of cursor movement so that the cursor shifts downward.
17	MWRITE C = 42H P1 = FFH P9 = FFH	Fills the left side of displayed letter E with dots by entering character code to 9 lines of the second screen block that corresponds to the first column on the first line. 
18	CSRW C = 46H P1 = 01H P2 = 10H	Presets the cursor address to address 10001H.
19	MWRITE C = 42H P1 = FFH P9 = FFH	Fills the second screen block that corresponds to the second column on the first line with dots.

No	Command	Operation
20	CSRW	Repeats steps 18 and 19 until the background screen of the EPSON character string is filled with dots as shown below.
29	MWRITE	Inverse display 
30	CSRW C = 46H P1 = 00H P2 = 04H	Presets the cursor address to the first column on the first line of the third screen block.
31	CSR DIR C = 4CH	Sets direction of cursor movement so that the cursor shifts to the right.
32	MWRITE C = 42H	
	P1 = 44H	Sets character code for the letter “D.”
	P2 = 6FH	Sets character code for the letter “o.”
	P3 = 74H	Sets character code for the letter “t.”
	P4 = 20H	Sets character code for the letter “ ”
	P5 = 4DH	Sets character code for the letter “M.”
	P6 = 61H	Sets character code for the letter “a.”
	P7 = 74H	Sets character code for the letter “t.”
	P8 = 72H	Sets character code for the letter “r.”
	P9 = 69H	Sets character code for the letter “i.”
	P10 = 78H	Sets character code for the letter “x.”
	P11 = 20H	Sets character code for the letter “ ”
	P12 = 4CH	Sets character code for the letter “L.”
	P13 = 43H	Sets character code for the letter “C.”
	P14 = 44H	Sets character code for the letter “D.”

Example of display mode settings [1]

[1] For overlaying text and graphics

1. Conditions

(1) 320 x 240 dots: Single-screen drive method (1/240 duty cycle)

(2) First layer: Text display

(3) Second layer: Graphic display

(4) Character font: 8 x 8 dots

(5) CG RAM unused

2. Display memory allocation

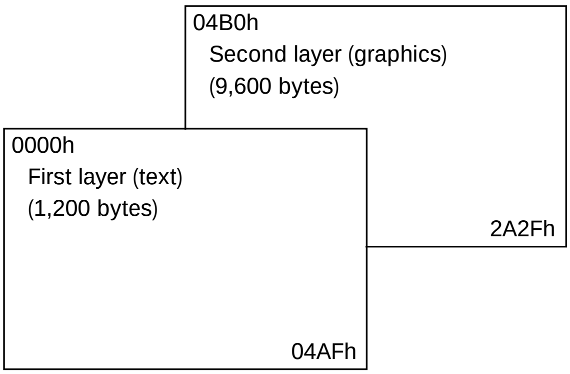
(1) First layer (text display)
Number of characters in horizontal direction = 320 / 8 = 40
Number of characters in vertical direction = 240 / 8 = 30

Therefore, the required size of memory is 40 x 30 = 1,200 bytes.

(2) Second layer (graphic display)
Number of characters in horizontal direction = 320 / 8 = 40
Number of characters in vertical direction = 240 / 1 = 240

Therefore, the required size of memory is 40 x 240 = 9,600 bytes.

[Relationship between display and memory]



3. Example of basic register settings

SYSTEM SET	Determination of TC/R
C = 40H	
P1 = 30H	Assuming f_{FR} = 60 Hz
P2 = 87H	when f_{OSC} = 6 MHz,
P3 = 07H	
P4 = 27H	6 MHz = {[TC/R] x 9 + 1} x 240 x 60
P5 = 2DH	Therefore, [TC/R] = 46
P6 = EFH	TC/R = 2DH
P7 = 28H	
P8 = 00H	

SCROLL
C = 44H
P1 = 00H
P2 = 00H
P3 = F0H
P4 = B0H
P5 = 04H
P6 = F0H
P7 = *H
P8 = *H
P9 = *H
P10 = *H

*: don’t care

CSRFORM
C = 5DH
P1 = 04H
P2 = 86H

HDOT SCR
C = 5AH
P1 = 00H

OVLAY
C = 5BH
P1 = 00H

DISP ON/OFF
C = 59H
P1 = 16H

Example of display mode settings [2]

[2] For overlaying two graphic screens

1. Conditions

(1) 320 x 240 dots: Single-screen drive method (1/240 duty cycle)

(2) First layer: Graphic display

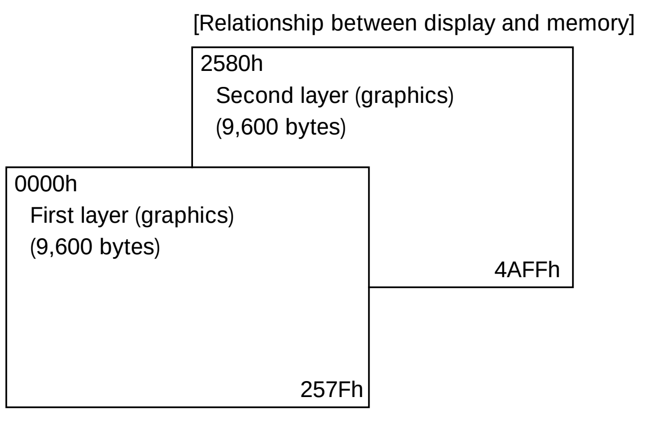
(3) Second layer: Graphic display

2. Display memory allocation

(1) First layer (graphic display)
Number of characters in horizontal direction = 320 / 8 = 40
Number of characters in vertical direction = 240 / 1 = 240

Therefore, the required size of memory is 40 x 240 = 9,600 bytes.

(2) Second layer (graphic display)
For the first layer, the required size of memory is 40 x 240 = 9,600 bytes.



3. Example of basic register settings

SYSTEM SET	Determination of TC/R
C = 40H	
P1 = 30H	Assuming f_{FR} = 60 Hz
P2 = 87H	when f_{OSC} = 6 MHz,
P3 = 00H	
P4 = 27H	6 MHz = {[TC/R] x 9 + 1} x 240 x 60
P5 = 2DH	Therefore, [TC/R] = 46
P6 = EFH	TC/R = 2DH
P7 = 28H	
P8 = 00H	
SCROLL	
C = 44H	
P1 = 00H	
P2 = 00H	
P3 = F0H	
P4 = 80H	
P5 = 25H	
P6 = F0H	
P7 = *H	
P8 = *H	
P9 = *H	
P10 = *H	*: don’t care
CSRFORM	
C = 5DH	
P1 = 04H	
P2 = 86H	
HDOT SCR	
C = 5AH	
P1 = 00H	
OVLAY	
C = 5BH	
P1 = 00H	
DISP ON/OFF	
C = 59H	
P1 = 16H	

Example of display mode settings [3]

[3] For overlaying three graphic screens

1. Conditions

   (1) 320 x 240 dots: Single-screen drive method (1 / 240 duty cycle)

   (2) First layer: Graphic display

   (3) Second layer: Graphic display

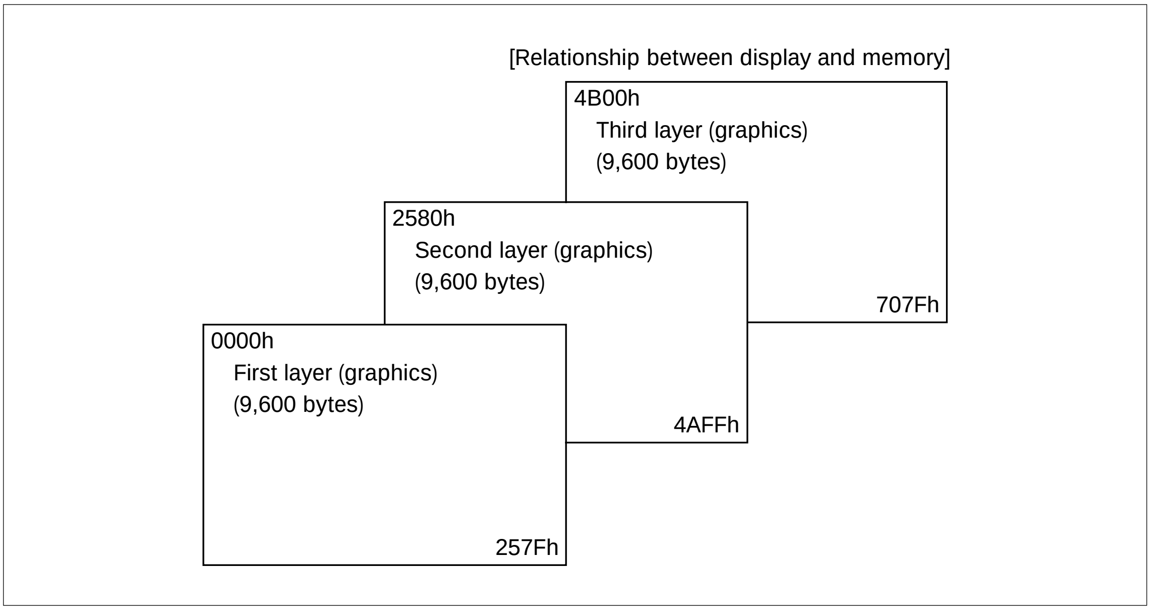
   (4) Third layer: Graphic display

2. Display memory allocation

   (1) First layer (graphic display)
   Number of characters in horizontal direction = 320 / 8 = 40
   Number of characters in vertical direction = 240 / 1 = 240

   Therefore, the required size of memory is 40 x 240 = 9,600 bytes.

   (2) Second and third layers (graphic display)
   For the first layer, the required size of memory is 40 x 240 = 9,600 bytes each.



3. Example of basic register settings

SYSTEM SET	Determination of TC/R
C = 40H	
P1 = 30H	Assuming f_{FR} = 60 Hz
P2 = 87H	when f_{OSC} = 6 MHz,
P3 = 00H	
P4 = 27H	6 MHz = {[TC/R] x 9 + 1} x 240 x 60
P5 = 2DH	Therefore, [TC/R] = 46
P6 = EFH	TC/R = 2DH
P7 = 28H	
P8 = 00H	

SCROLL
C = 44H
P1 = 00H
P2 = 00H
P3 = F0H
P4 = 80H
P5 = 25H
P6 = F0H
P7 = 00H
P8 = 4BH
P9 = *H
P10 = *H   *: don't care

CSRFORM
C = 5DH
P1 = 04H
P2 = 86H

HDOT SCR
C = 5AH
P1 = 00H

OVLAY
C = 5BH
P1 = 00H

DISP ON/OFF
C = 59H
P1 = 16H

4.4 Character Fonts and Character Codes

4.4.1 Character Fonts (Internal CG)

Note: ■ represents a 6 x 8-dot entirely black pattern.

4.4.2 Relationship between Character Codes and Those Usable as CG RAM (for combined use with internal CG ROM)

Table 4-4 Character Codes

8-bit series															
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

YS3 LS3

D7	D6	D5	D4	D3	D2	D1	D0	4 low-order bits \ 4 high-order bits		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
				0	0	0	0		0				0	@	P	`	p				ー	タ	ミ		
				0	0	0	1		1			!	1	A	Q	a	q			。	ア	チ	ム		
				0	0	1	0		2			“	2	B	R	b	r			「	イ	ツ	メ		
				0	0	1	1		3			#	3	C	S	c	s			」	ウ	テ	モ		
				0	1	0	0		4			$	4	D	T	d	t			、	エ	ト	ヤ		
				0	1	0	1		5			%	5	E	U	e	u			・	オ	ナ	ユ		
				0	1	1	0		6			&	6	F	V	f	v			ヲ	カ	ニ	ヨ		
				0	1	1	1		7			‘	7	G	W	g	w			ァ	キ	ヌ	ラ		
				1	0	0	0		8			(	8	H	X	h	x			ィ	ク	ネ	リ		
				1	0	0	1		9			)	9	I	Y	I	y			ゥ	ケ	ノ	ル		
				1	0	1	0	A	10			*	:	J	Z	j	z			ェ	コ	ハ	レ		
				1	0	1	1	B	11			+	;	K	[	k	{			ォ	サ	ヒ	ロ		
				1	1	0	0	C	12			,	<	L	¥	l	¦			ャ	シ	フ	ワ		
				1	1	0	1	D	13			.	=	M	]	m	}			ュ	ス	ヘ	ン		
				1	1	1	0	E	14			-	>	N	^	n	→			ョ	セ	ホ	゛		
				1	1	1	1	F	15			/	?	O	_	o	←			ッ	ソ	マ	゜		

CG RAM1 CG RAM2

M1=0

M1=1

5 SPECIFICATIONS

5.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Power Supply Voltage	V_{DD}	-0.3–7.0	V	
Input Voltage	V_{IN}	-0.3–V_{DD} + 0.3	V	
Operating Temperature	T_{opr}	-20–75	°C	
Storage Temperature	T_{stg}	-65–150	°C	
Soldering Temperature and Time	T_{solder}	260 · 10	°C · sec	Note 1
Power Dissipation	P_D	300	mW	

Note 1: The resistance to moisture of semiconductor products in flat packages is adversely affected when dipped in solder. When mounting the chip on a circuit board, be careful not to expose the plastic part of the package to thermal stress.

1. When using a power supply with high impedance, a large potential difference between the chip's internal power supply voltage and the input voltage may occur, thus making the power supply susceptible to latch-up. Therefore, pay particular attention to the power supply and its wiring.
2. All voltages are based on V_{SS} = 0 V.

5.2 Electrical Characteristics

[V_{SS} = 0V, V_{DD} = 4.5–5.5V, T_a = -20–75°C]

Parameter		Symbol	Test Condition	Rated Value			Unit	Applicable Pins
				Min.	Typ.	Max.		
Operating Supply Voltage Register Retention Voltage		V_{DD} V_{HO}		4.5 2.0	5.0 —	5.5 6.0	V	V_{DD}
TTL	High Level Input Voltage Low Level Input Voltage High Level Output Voltage Low Level Output Voltage	V_{IHT} V_{ILT} V_{OHT} V_{OLT}	 I_{OH} = -5.0 mA I_{OL} = 5.0 mA	0.5 xV_{DD} V_{SS} 2.4 —	— — — —	V_{DD} 0.2 x V_{DD} — V_{SS} + 0.4	V V V V	D_0–D_7, A_0 $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ VD_0–VD_7, VA_0–VA_{15} $\overline{VCE}$, $\overline{VRD}$, $\overline{VWR}$
CMOS	High Level Input Voltage Low Level Input Voltage High Level Output Voltage Low Level Output Voltage	V_{IHC} V_{ILC} V_{OHC} V_{OLC}	 I_{OH} = -2.0 mA I_{OL} = 2.0 mA	0.8 x V_{DD} V_{SS} V_{DD} - 0.4 —	— — — —	V_{DD} 0.2 x V_{DD} — V_{SS} + 0.4	V V V V	SEL1, NT/PL, YD, XD_0–XD_3 XSCL, YDIS, LP, WF, CLO
SM	Rising Edge Threshold Voltage Falling Edge Threshold Voltage	V_{T+} V_{T-}	Note 2	0.5 V_{DD} 0.2 V_{DD}	0.7 V_{DD} 0.3 V_{DD}	0.8 V_{DD} 0.5 V_{DD}	V V	$\overline{RES}$
Input Leakage Current Output Leakage Current		I_{LI} I_{LO}	V_{IN} = V_{DD}/V_{SS} Note 3	— —	0.05 0.10	2.0 5.0	µA µA	
Operating Supply Current		I_{opr}	f_{OSC} = 10 MHz Nonloaded 256 x 200 dots	—	11	15	mA	V_{DD}
Quiescent Supply Current		I_Q	Sleep mode XG, $\overline{CS}$, $\overline{RD}$ = V_{DD}	—	0.05	20	µA	V_{DD}
Oscillator Frequency External Clock Frequency Oscillator Feedback Resistance		f_{OSC} f_{CL} R_f	AT quartz crystal 47.5% duty cycle	1.0 1.0 0.5	— — 1.0	8.0 8.0 3.0	MHz MHz MΩ	XG, XD

Note:

1. Iopr denotes the current consumed in the chip when using the internal CG. Current is measured in a nonloaded state (without display memory). To further reduce current consumption, write the SYSTEM SET command (without parameters) and DISP ON/OFF command to the chip after initialization. This causes the CLO pin to stop operating, thus enabling a powering down of approximately 1 mA at 6.1 MHz operation.
2. The pulse applied to the $\overline{RES}$ pin must be held low for at least 200 µs to be effective. However, avoid keeping the input pulse active for more than several seconds because LCD DC drive capability may deteriorate.
3. VThe VD_0–VD_7 and D_0–D_7 pins come with a feedback circuit, so that even when input becomes high impedance, the pins retain the state held immediately before. Therefore, an intermediate level of input voltage allows input current to flow to the pin.

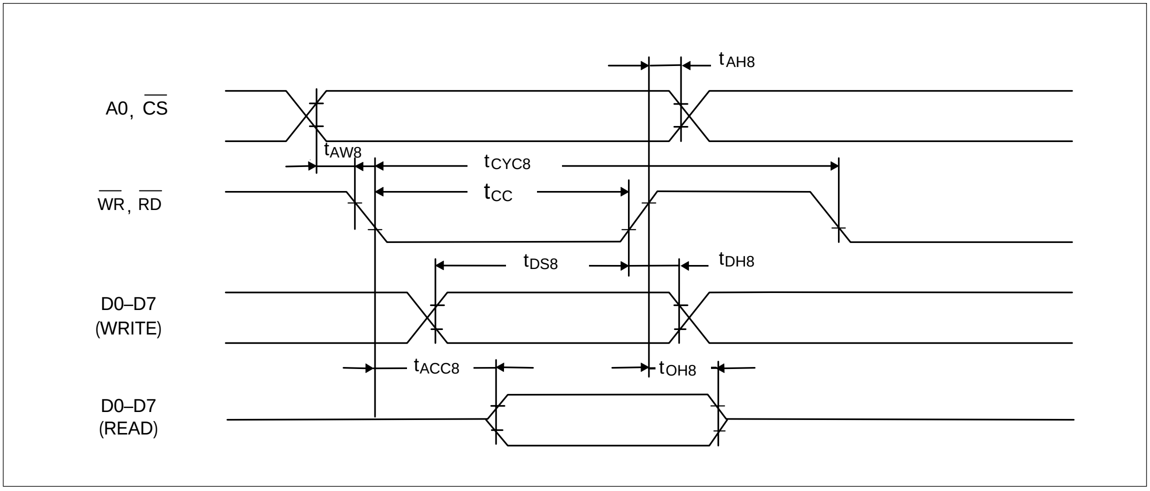
[V_{SS} = 0V, V_{DD} = 2.7–4.5V, T_a = -20–75°C]

Parameter		Symbol	Test Condition	Rated Value Min.	Rated Value Typ.	Rated Value Max.	Unit	Applicable Pins
Operating Supply Voltage Register Retention Voltage		V_{DD} V_{HO}		2.7 2.0	3.5 —	4.5 6.0	V	V_{DD}
TTL	High Level Input Voltage Low Level Input Voltage High Level Output Voltage Low Level Output Voltage	V_{IHT} V_{ILT} V_{OHT} V_{OLT}	 I_{OH} = -3.0 mA I_{OL} = 3.0 mA	0.8 x V_{DD} V_{SS} V_{DD} - 0.4		V_{DD} 0.2 xV_{DD} V_{SS} + 0.4	V V V V	D_0–D_7, A_0 $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ VD_0–VD_7, VA_0–VA_{15} $\overline{VCE}$, $\overline{VRD}$, $\overline{VWR}$
CMOS	High Level Input Voltage Low Level Input Voltage High Level Output Voltage Low Level Output Voltage	V_{IHC} V_{ILC} V_{OHC} V_{OLC}	 I_{OH} = -1.0 mA I_{OL} = 1.0 mA	0.8 x V_{DD} V_{SS} V_{DD} - 0.4		V_{DD} 0.2 x V_{DD} V_{SS} + 0.4	V V V V	SEL1, NT/PL, YD, XD_0–XD_3 XSCL, YDIS, LP, WF, CLO
SM	Rising Edge Threshold Voltage Falling Edge Threshold Voltage	V_{T+} V_{T-}		0.5V_{DD} 0.2V_{DD}	0.7 V_{DD} 0.3 V_{DD}	0.8V_{DD} 0.5V_{DD}	V V	$\overline{RES}$
Input Leakage Current Output Leakage Current		I_{LI} I_{LO}	V_{IN} = V_{DD}/V_{SS}		0.05 0.10	2.0 5.0	µA µA	
Operating Supply Current		I_{opr}	f_{OSC} = 6.1 MHz Nonloaded 256 x 200 dots		3.5 (V_{DD} = 3.5 V)	15	mA	V_{DD}
Quiescent Supply Current		I_Q	Sleep mode XG,$\overline{GS}$, $\overline{RD}$ = V_{DD}		0.05	20	µA	V_{DD}
Oscillator Frequency External Clock Frequency Oscillator Feedback Resistance		f_{OSC} f_{CL} R_f	AT quartz crystal 47.5% duty cycle Note 4	1.0 1.0 0.7		8.0 8.0 4.0	MHz MHz MΩ	XG, XD

Note: 4. The XG pin is only biased with several µA. When designing a circuit board, take the measures necessary to prevent leakage.

5.3 Timing Characteristics

5.3.1 System Bus Read/write characteristics I (80-series MPU)



(T_a = -20–75°C)

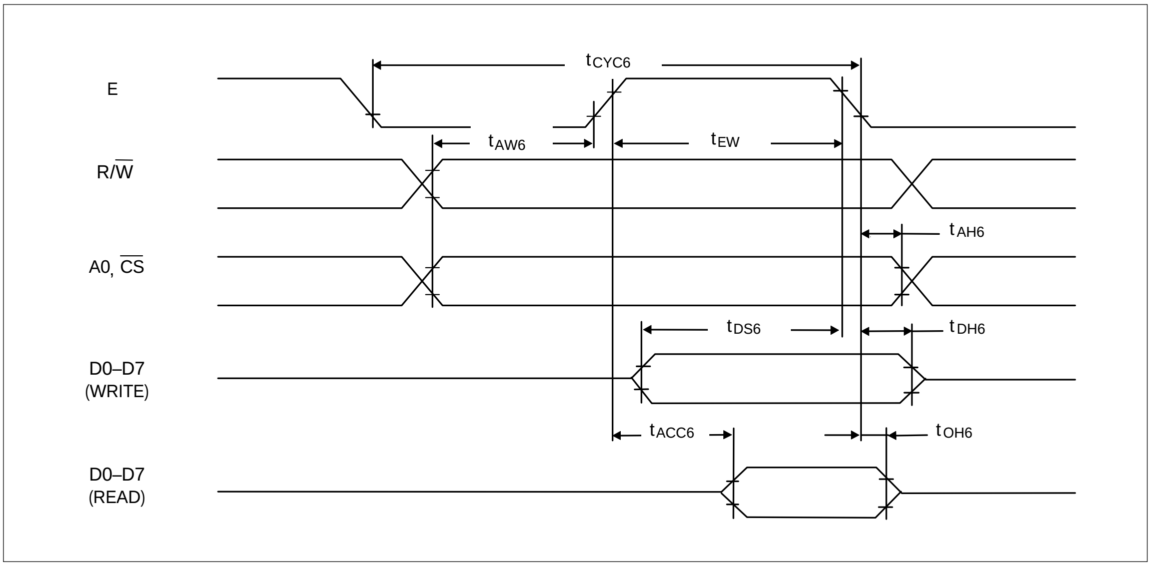
Signal	Symbol	Parameter	V_{DD} = 4.5–5.5V		V_{DD} = 2.7–4.5V		Unit	Test Condition
			Min.	Max.	Min.	Max.		
A_0, $\overline{CS}$	t_{AH8} t_{AW8}	Address Hold Time Address Setup Time	10 0	— —	10 0	— —	ns ns	C_L = 100pF
$\overline{WR}$, $\overline{RD}$	t_{CYC8} t_{CC}	System Cycle Time Control Pulse Width	[1] 120	— —	[1] 150	— —	ns ns	
D_0–D_7	t_{DS8} t_{DH8} t_{ACC8} t_{OH8}	Data Setup Time Data Hold Time $\overline{RD}$ Access Time Output Disable Time	120 5 — 10	— — 50 50	120 5 — 10	— — 80 55	ns ns ns ns	

[1] For memory control and operation control commands:

$$t_{CYC8} = 2t_C + t_{CC} + t_{CEA} + 75 > t_{ACV} + 245$$

For all other commands: $t_{CYC8} = 4t_C + t_{CC} + 30$

5.3.2 System Bus Read/write characteristics II (68-series MPU)



(T_a = -20–75°C)

Signal	Symbol	Parameter	V_{DD} = 4.5–5.5V		V_{DD} = 2.7–4.5V		Unit	Test Condition
			Min.	Max.	Min.	Max.		
A_0, $\overline{CS}$ R/$\overline{W}$	t_{CYC6}	System Cycle Time	[1]	—	[1]	—	ns	C_L = 100pF
	t_{AW6}	Address Setup Time	0	—	10	—	ns	
	t_{AH6}	Address Hold Time	0	—	0	—		
D_0–D_7	t_{DS6}	Data Setup Time	100	—	120	—	ns	
	t_{DH6}	Data Hold Time	0	—	0	—		
	t_{OH6}	Output Disable Time	10	50	10	75	ns	
	t_{ACC6}	Access Time	—	85	—	130	ns	
E	t_{EW}	Enable Pulse Width	120	—	150	—		

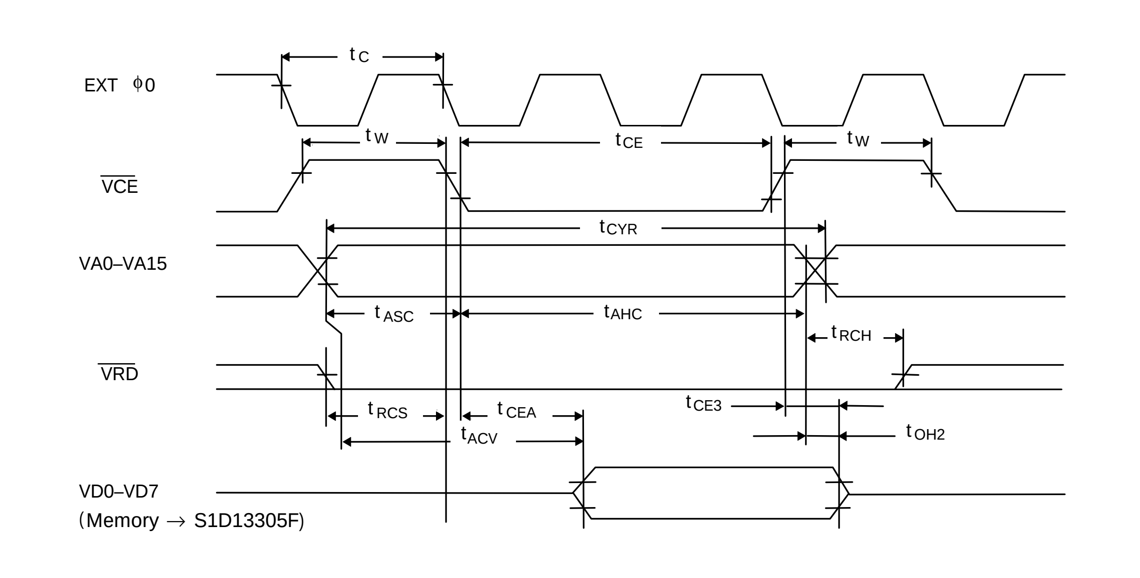
[1] For memory control and operation control commands:

$$t_{CYC6} = 2t_C + t_{EW} + t_{CEA} + 75 > t_{ACV} + 245$$

For all other commands: $t_{CYC6} = 4t_C + t_{EW} + 30$

Note: Note that t_{CYC6} defines the time period of the E signal only in designated cases where CS and E = high.

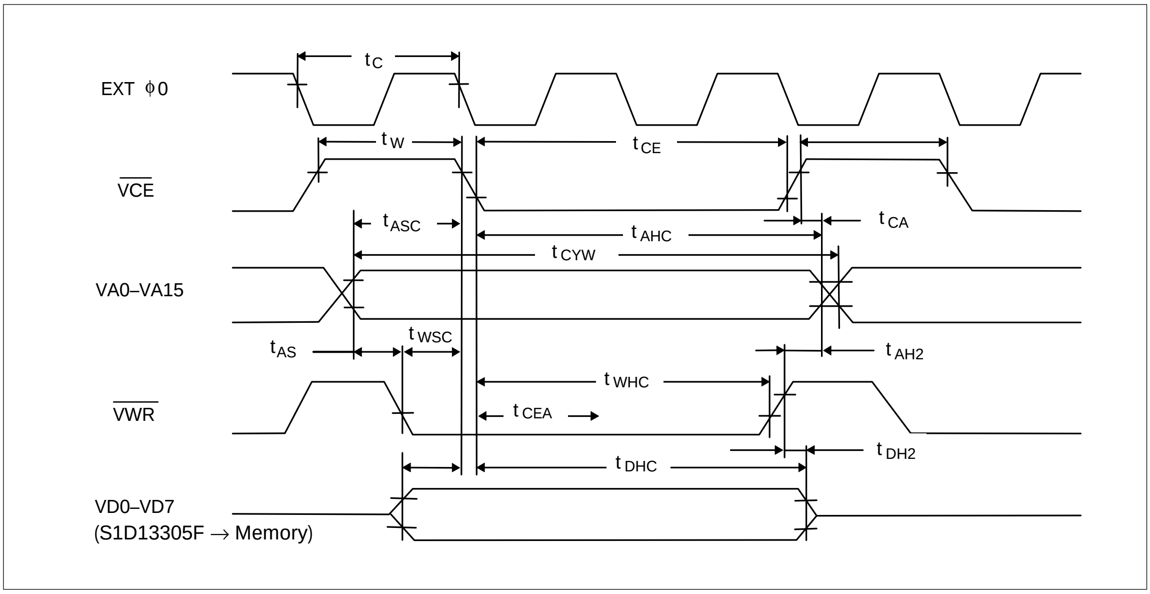
5.3.3 Display Memory Read Characteristics



(T_a = -20–75°C)

Signal	Symbol	Parameter	V_{DD} = 4.5–5.5V		V_{DD} = 2.7–4.5V		Unit	Test Condition
			Min.	Max.	Min.	Max.		
EXT ϕ0	t_C	Clock period	125	—	125	—	ns	C_L = 100pF
$\overline{VCE}$	t_W t_{CE}	VCE high-level pulse width VCE low-level pulse width	t_C - 50 $2t_C$ - 30	— —	t_C - 50 $2t_C$ - 30	— —	ns ns	
VA_0–VA_{15}	t_{CYR} t_{ASC} t_{AHC}	Read cycle time Address setup time relative to VCE fall Address hold time relative to VCE fall	$3t_C$ t_C - 70 $2t_C$ - 30	— — —	$3t_C$ t_C - 110 $2t_C$ - 40	— — —	ns ns ns	
$\overline{VRD}$	t_{RCS} t_{RCH}	Read cycle setup time relative to VCE fall Read cycle hold time relative to VCE rise	t_C - 45 $1/2t_C$	— —	t_C - 60 $1/2t_C$	— —	ns ns	
VD_0–VD_7	t_{ACV} t_{CEA} t_{OH2} t_{CE3}	Address access time VCE access time Output data hold time VCE data off time	— — 0 0	$3t_C$ - 100 $2t_C$ - 80 — —	— — 0 0	$3t_C$ - 15 $2t_C$ - 90 — —	ns ns ns ns	

5.3.4 *Display Memory Write Characteristics (at MWRITE Command Execution)*

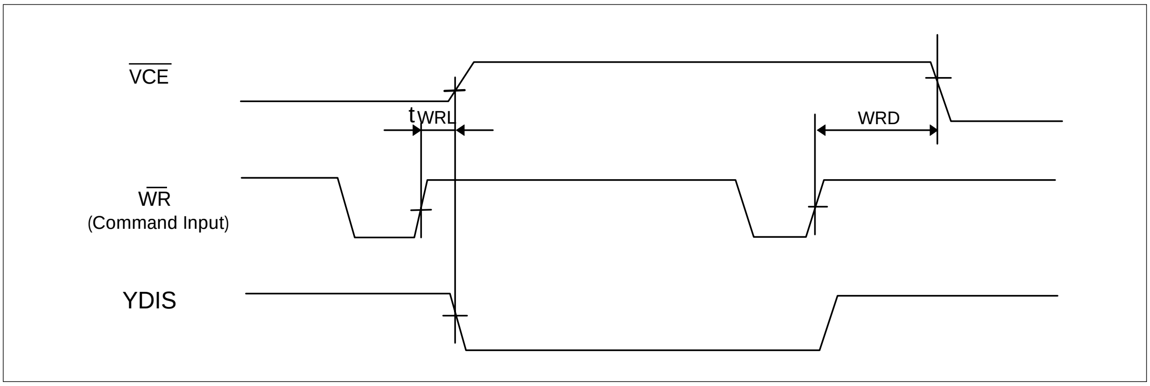


(T_a = -20–75°C)

Signal	Symbol	Parameter	V_{DD} = 4.5–5.5V		V_{DD} = 2.7–4.5V		Unit	Test Condition
			Min.	Max.	Min.	Max.		
EXT φ0	t_C	Clock period	125	—	125	—	ns	C_L = 100pF
$\overline{VCE}$	t_W	VCE high-level pulse width	t_C - 50	—	t_C - 50	—	ns	
	t_{CE}	VCE low-level pulse width	$2t_C$ - 30	—	$2t_C$ - 30	—	ns	
VA_0–VA_{15}	t_{CYW}	Write cycle time	$3t_C$	—	$3t_C$	—	ns	
	t_{AHC}	Address hold time relative to VCE fall	$2t_C$ - 30	—	$2t_C$ - 40	—	ns	
	t_{ASC}	Address setup time relative to VCE fall	t_C - 70	—	t_C - 110	—	ns	
	t_{CA}	Address hold time relative to VCE rise	0	—	0	—		
	t_{AS}	Address setup time relative to VWR fall	0	—	0	—		
	t_{AH2}	Address hold time relative to VWR fall	10	—	10	—		
$\overline{VWR}$	t_{WSC}	Write setup time relative to VCE fall	t_C - 80	—	t_C - 115	—	ns	
	t_{WHC}	Write hold time relative to VCE fall	$2t_C$ - 20	—	$2t_C$ - 20	—	ns	
VD_0–VD_7	t_{DSC}	Data input setup time relative to VCE fall	t_C - 85	—	t_C - 125	—	ns	
	t_{DHC}	Data input hold time relative to VCE fall	$2t_C$ - 30	—	$2t_C$ - 30	—	ns	
	t_{DH2}	Data input hold time relative to VWR fall	5	50	5	50	ns	

Note: The VD_0–VD_7 pins have a built-in latch so that when a VD_0–VD_7 bus enters a high-impedance state, the write data is retained until the read data from memory is placed on the bus.

5.3.5 Output Signal Characteristics (at SLEEP IN Command Execution)



(T_a = -20–75°C)

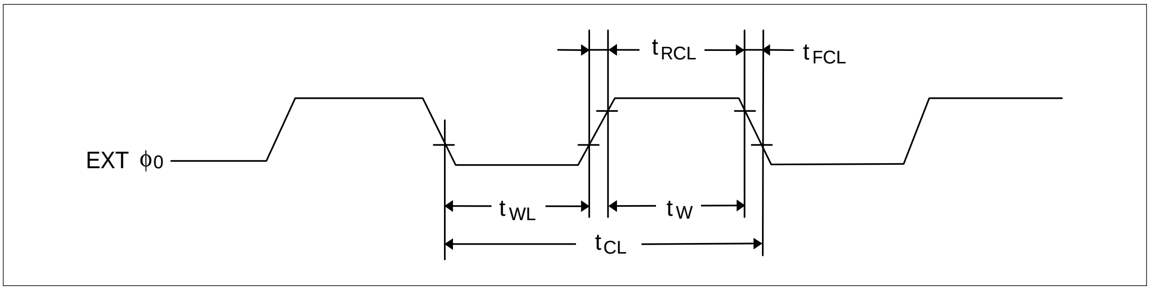
Signal	Symbol	Parameter	V_{DD} = 4.5–5.5V		V_{DD} = 2.7–4.5V		Unit	Test Condition
			Min.	Max.	Min.	Max.		
$\overline{WR}$	t_{WRD}	VCE fall delay time	[1]		[1]		ns	C_L = 100pF
	t_{WRL}	YDIS fall delay time		[2]		[2]	ns	

t_{OSS}: Oscillation start time

[1] $t_{WRD} = 18t_C + t_{OSS} + 40$

[2] $t_{WRL} = 36t_C\ [TC/R] \cdot [L/F] + 70$

5.3.6 External Clock Input Characteristics



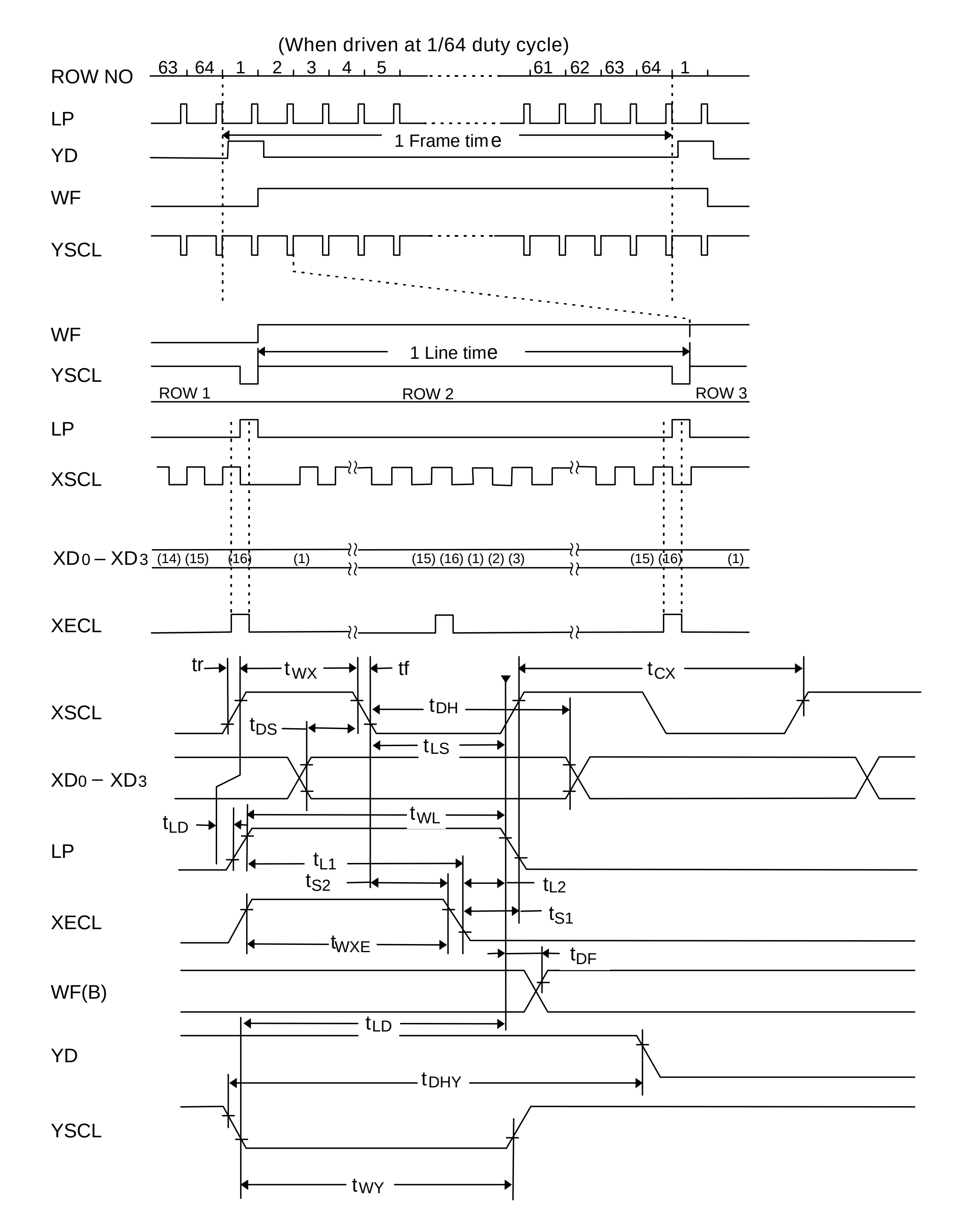
(T_a = -20–75°C)

Signal	Symbol	Parameter	V_{DD} = 4.5–5.5V		V_{DD} = 2.7–4.5V		Unit	Test Condition
			Min.	Max.	Min.	Max.		
EXT φ0	t_{RCL}	External clock rise time		15		15	ns	
	t_{FCL}	External clock fall time		15		15	ns	
	t_{WH}	External clock high-level pulse width	[1]	[2]	[1]	[2]	ns	
	t_{WL}	External clock low-level pulse width	[1]	[2]	[1]	[2]	ns	
	t_{CL}	External clock period	125				ns	

[1] $(t_C - t_{RCL} - t_{FCL}) \times \frac{475}{1000} < t_{WH}, t_{WL}$

[2] $(t_C - t_{RCL} - t_{FCL}) \times \frac{525}{1000} > t_{WH}, t_{WL}$

5.3.7 LCD Control Signal Timing Characteristics



(T_a = -20–75°C)

Signal	Symbol	Parameter	V_{DD} = 4.5–5.5V		V_{DD} = 2.7–4.5V		Unit	Test Condition
			Min.	Max.	Min.	Max.		
	t_r t_f	Rise time Fall time		30 30		40 40	ns ns	C_L = 100pF
XSCL	t_{CX} t_{WX}	Shift clock cycle time XSCL clock pulse width	$4t_C$ $2t_C$ - 60		$4t_C$ $2t_C$ - 70		ns ns	
XD_0–XD_3	t_{DH} t_{DS}	Display data hold time Display data setup time	$2t_C$ - 50 $2t_C$ - 100		$2t_C$ - 50 $2t_C$ - 105		ns ns	
LP	t_{LS} t_{WL} t_{LD}	Latch data setup time LP signal pulse width XSCL to LP delay time	$2t_C$ - 50 $4t_C$ - 80 0		$2t_C$ - 50 $4t_C$ - 120 0		ns ns ns	
WF	t_{DF}	Permissible WF delay time		50		50	ns	
YD	t_{DHY}	Scan start pulse hold time	$2t_C$ - 20		$2t_C$ - 20		ns	
YSCL	t_{WY}	YSCL clock pulse width	$4t_C$ - 80		$4t_C$ - 120		ns	

Note: When the S1D13305 displays a screen equivalent to one frame, it starts from the address corresponding to the upper-left corner of the screen (home position). Then while incrementing the address, the S1D13305 reads the necessary amount of data for up to the address corresponding to the lower-right corner (end) of the screen from display memory. This data is then converted into display data before being sent to the X driver. Therefore, each line of data for the X driver is sent out beginning with the dot data at the left edge of the screen.

6 MPU INTERFACE

6.1 Connection to the System Bus

The S1D13305 uses a combination of SEL1, SEL2, A0, $\overline{RD}$, $\overline{WR}$, and CS to discriminate the information supplied to it via the system data bus as described in Section 2.2, “Pin Functions” on page 7.

A0 normally is connected to the least significant bit of the system address bus.

SEL1 and SEL2 are provided for changing the functions of S1D13305 pins 50 and 51 to enable direct chip connection to the 80 or 68-series MPU bus. When in use, SEL1 and SEL2 are pulled high or low through a resistor. For the 80-series MPU, the S1D13305 should normally be mapped in I/O space.

6.1.1 80-series MPU

SEL1 = 0
SEL2 = 0

A0	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	Status flag read
1	0	1	Data (VRAM, CG, cursor address) read
0	1	0	Data (VRAM, register) write
1	1	0	Command write (code only)

6.1.2 68-series MPU

SEL1 = 1
SEL2 = 0

A0	$\overline{RD}$	$\overline{WR}$	Function
0	1	1	Status flag read
1	1	1	Data (VRAM, CG, cursor address) read
0	0	1	Data (VRAM, register) write
1	0	1	Command write (code only)

6.2 Synchronization with the MPU

SThe S1D13305 has a high-speed interface processing function so as not to impair the processing capability of high-speed MPUs. This allows chips to be handled just like memory devices that satisfy the rated system bus and read/write timing requirements. Therefore, when the MPU accesses the S1D13305, there is no need for polling to check for busy or handshaking status with the S1D13305. This is because the S1D13305 can execute any command within the cycle time (t_{CYC}). However, successive attempts at accessing the S1D13305 that are intolerable with respect to the one-frame time may result in noticeable screen flickering. In such case, the MPU should access the S1D13305 intermittently or check the status flag (D6) to confirm that it is cleared before accessing. This helps to minimize display effects on LCD.

The following shows the difference in interface processing performed by the S1D13305 when accessing its internal registers and when accessing display memory.

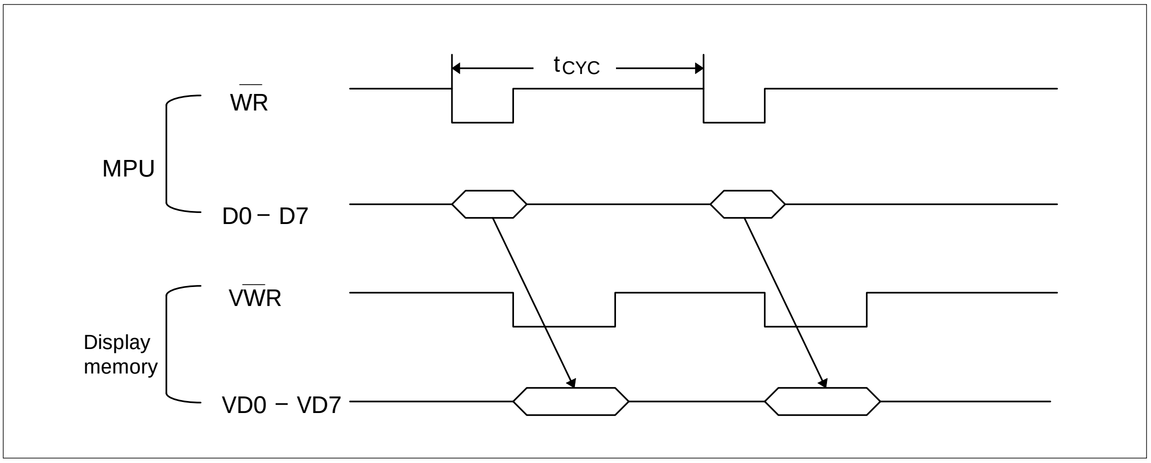
6.2.1 Internal Register Access

For the SYSTEM SET and SLEEP IN commands, input to and output from the internal registers are processed asynchronously, and not dependent on oscillator frequency. All other commands cannot be used while the system is in sleep mode.

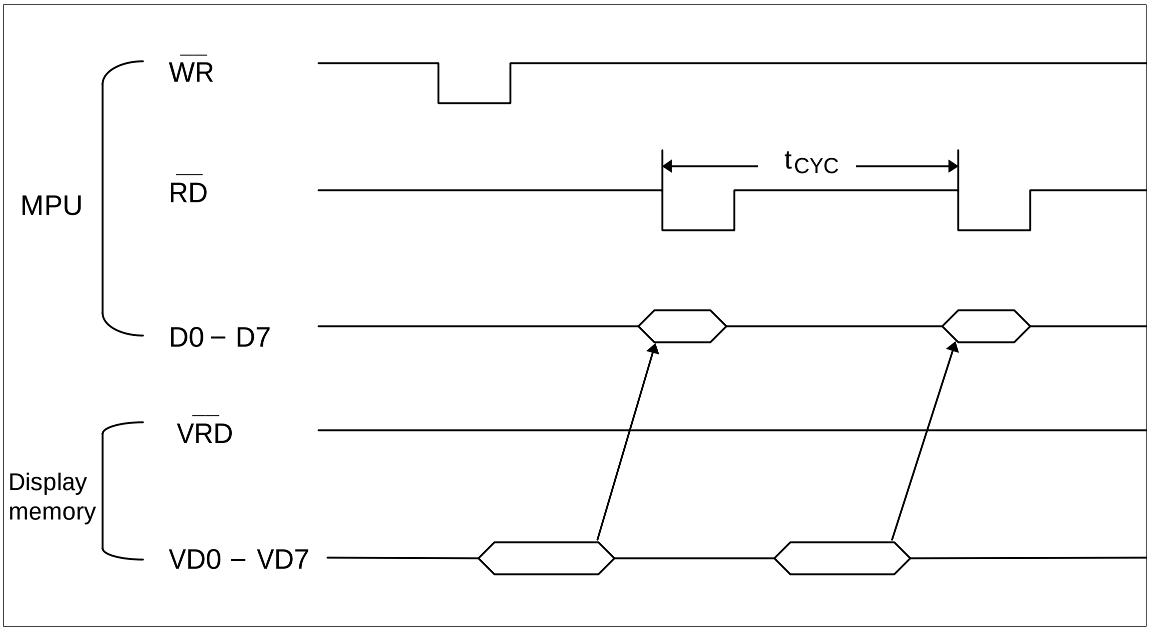
6.2.2 Display Memory Access

Display memory access is synchronized with the fundamental clock of the S1D13305. To ensure that operating frequencies of the MPU and display memory match, the S1D13305 processes operations between the chips via input/output registers in a manner similar to pipelined instruction processing, as shown below. Therefore, even if the access time of any display memory is slower than that required by the MPU, the MPU can access display memory without any problem, provided that the $\overline{RD}$ and $\overline{WR}$ signal cycle times (t_{CYC}) satisfy rated timing requirements.

(1) Write to display memory



(2) Read from display memory

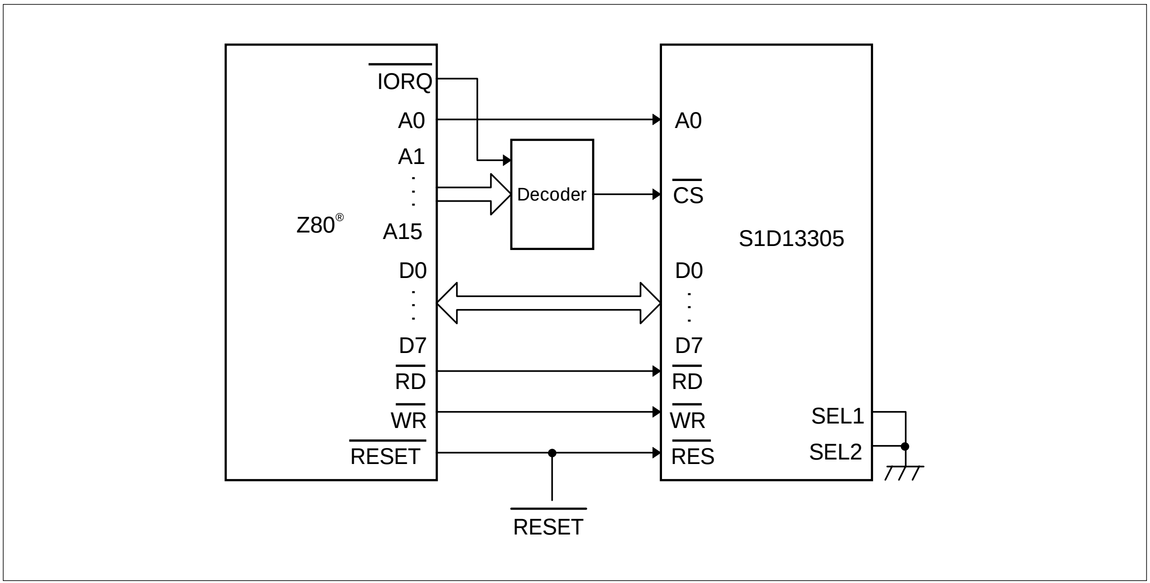


Note: The access time viewed from the system side (t_{ACC}), which often causes a problem when the MPU reads data from display memory, is not affected by the access time of display memory (t_{ACV}).

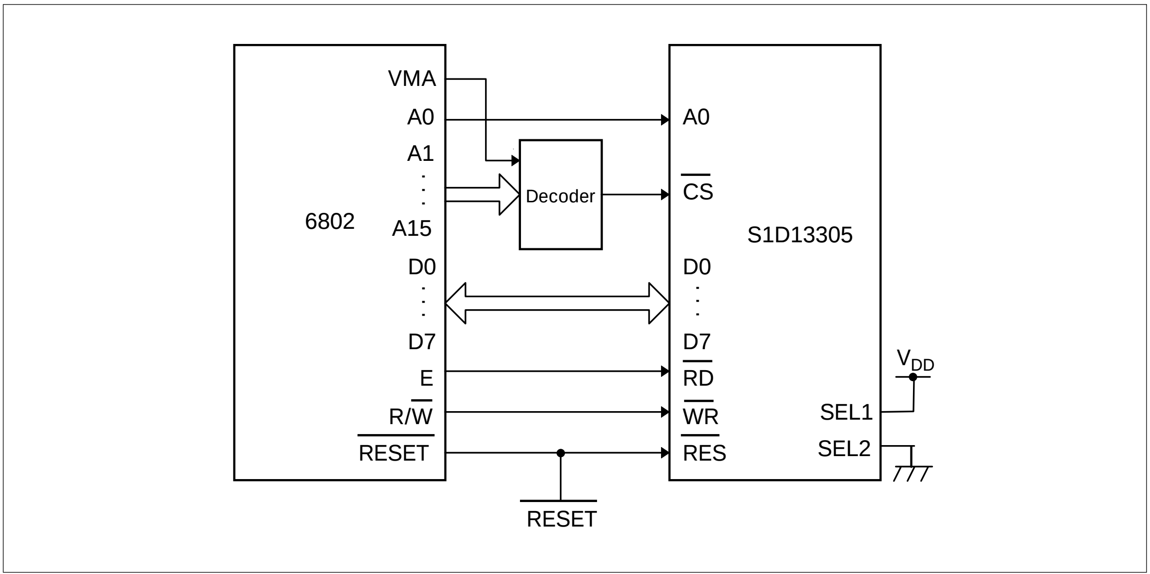
Whether the MPU can read from display memory depends on whether the access time (t_{CYC}) is guaranteed. If not, timing requirements can only be met by inserting one or more NOP instructions, which apparently has the same effect as inserting wait states.

6.3 Interfacing with the MPU (Example of Application)

6.3.1 80-series MPU



6.3.2 68-series MPU



Note: Z80 is a registered trademark of Zilog, Inc. of the U.S.

6.4 Status Flag

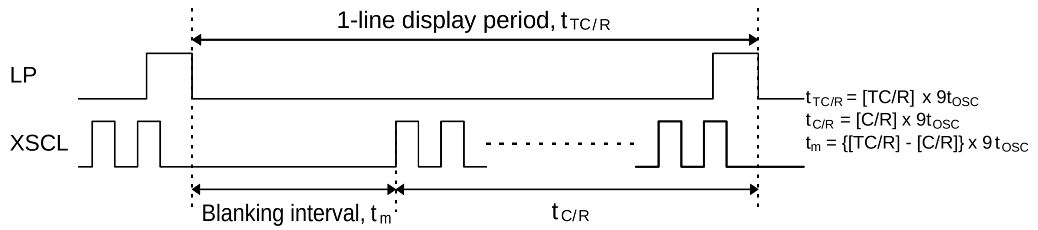
The S1D13305 has a 1-bit status flag.

D7							D0
*	D6	*	*	*	*	*	*

*: Don't Care

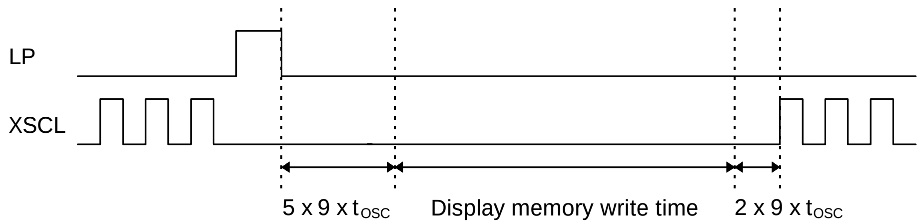
- X line standby (D6)

  The S1D13305 stops reading data from display memory after each line for the time equal to the difference between C/R and TC/R. The status flag (D6) is cleared to 0 during the blanking interval.



t_m: Time difference between C/R and TC/R (D6 is cleared to 0 during t_m period.)

Reference: Timing to avoid write noise
Timing precaution to be taken when writing to VRAM



The display memory write time is defined as:

$$\{(TC/R) - (C/R) - 7\} \times 9\ t_{OCS}$$

(where t_{OSC} = 1/f_{OSC}: oscillator frequency cycle) "5 x 9 t_{OCS}" after the fall of LP.

Given the method currently used to read the D6 status flag, it is impossible to know when the flag was cleared (D6 = low). To solve this problem, use the falling edge of LP as an interrupt signal to the CPU, and confirm that data is written to display memory within the time shown above.

Accessing display memory outside this write time may cause the screen to flicker. (When rewriting the entire screen, simply turn the display off.)

7 DISPLAY MEMORY INTERFACE

7.1 Static RAM

The diagram below shows an example of an interface for static RAM (asynchronous type) that is pin-compatible with the 2764 (made by Intel Corporation) and the S1D13305.

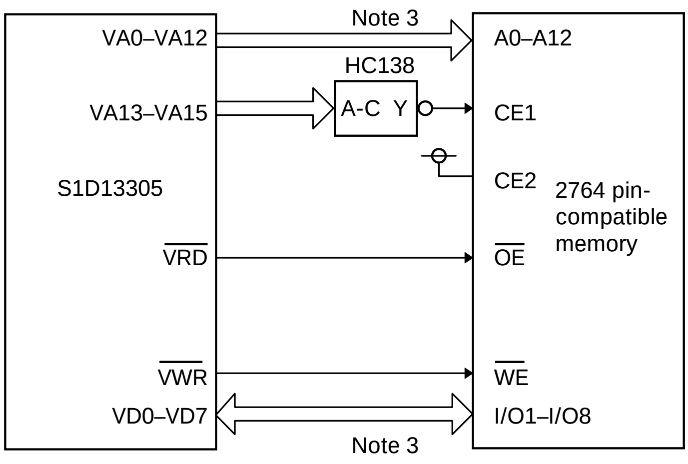


Figure 7-1 Example of interface for static RAM and the S1D13305

Note: Use a bus buffer when large load is placed on the bus.

7.2 Current Consumption during Display Memory Access

The S1D13305 has a total of 24 data and address bus lines to access display memory. These bus lines operate at one-third the oscillator frequency of the S1D13305 (f_{OSC}). The equation below defines the charging/discharging current consumed in these bus lines (IVOP), and suggests that it will exceed the average dynamic current consumption in the S1D13305 (IOPR).

$$I_{OPR} \propto C \cdot V \cdot f$$

where C = display memory bus capacitance
V = operating voltage
f = operating frequency

Applying this equation where Vopr = 5.0 V, f = 1.0 MHz, and C = 1.0 pF per display memory bus line, the following results:

$$I_{VOP} \leq 120\ \mu A/MHz \cdot pF$$

To reduce current consumption in the S1D13305 during display memory access, it is therefore necessary to reduce memory chip counts and the parasitic capacitance of the display memory bus, and not just by using memory devices with small dynamic current consumption. This will prove beneficial for low-power consumption and high-speed operation.

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