1.0 Key Features

- Technology: High voltage BICMOS (HBIMOS)
- Line interface circuit for Controller Area Network (CAN - ISO/DIS 11898)
- Up to 500 Kbit/s data rates
- Integrated protection against automotive disturbances, including Load-dump
- Optimal design of transmitter with programmable slope minimizes RFI emission, eliminating need for screened cables
- Fully compatible with CAN controller interface standards
- Tri-stateable driver
- 16 Pin SOP package
- Suitable for 12 V or 24 V vehicle systems

General Description

The MTC-3054 is the implementation of the CAN physical layer, used for serial data interchange between electronic units in automotive applications. The MTC-3054 was developed by AMI Semiconductor in co-operation with WABCO Westinghouse Fahrzeugbremsen GmbH.

The parameters for the circuit are specified under the special consideration of ISO/DIS 11898 "Road vehicles – Interchange of digital information – Controller Area Network (CAN) for high speed communication".

The circuit consists of the following blocks:

- a differential line transmitter
- a differential line receiver
- interface to the CAN protocol handler
- fault handling features

Normal Operation Mode

The IC is especially designed to provide the link between the protocol IC (Controller Area Network IC) and a physical bus line installed in the vehicle. Data interchange between the bus line and the protocol IC is realized via the interface.

The bus line can have two logical states, dominant or recessive. The bus is in the recessive state when the driving sections of all transceivers connected to this bus are passive. The differential voltage between the two wires is approximately zero. If at least one driver is active the bus changes into the dominant state. This state is represented by a differential voltage greater than a minimum threshold and therefore by a current flow through the terminating resistors of the bus line. The recessive state is overwritten by the dominant state.

The transceiver includes a bus driving section D. The driving section will be active if the transmission of a dominant bit is required. This is defined by a low level at input TX0A or TX0B. If, as usual, only one of these inputs is used, the common name will be TX0.

The transmitter is implemented as a push (at CanH) and a pull (at CanL) voltage driver, with a matched (but opposite) slew rate, which can be adjusted externally.

The bus receiving section R senses the state of the bus lines. The reception of a dominant state causes a low level at RX0.

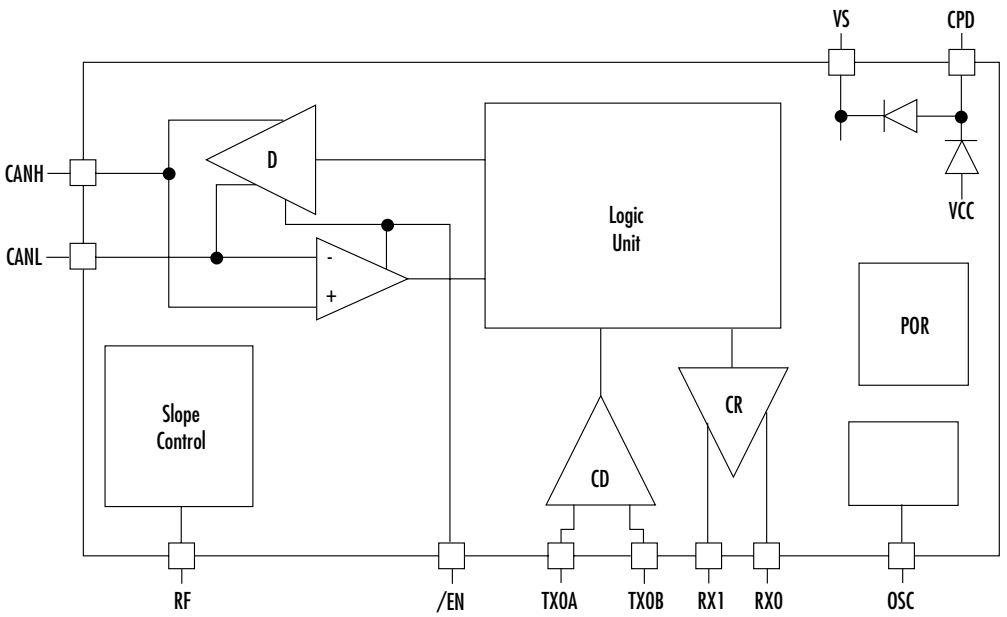


Fig.1: **Circuit Block Diagram**

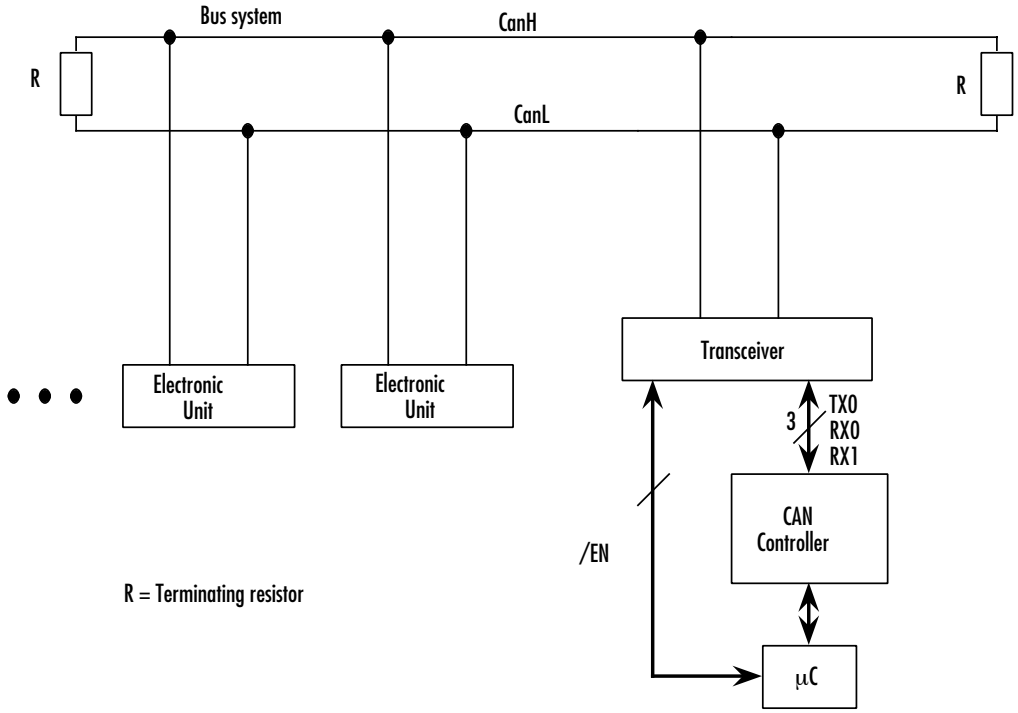


Fig.2: **CAN Bus System**

A low level on TX0 and a low level on RX0 correspond to a dominant state on the bus lines. To provide an independent switch-off of the transceiver by a third device (e.g. the µC) an enable input is included.

In the disabled state the driving section behaves as in the recessive state and does not depend on the input voltage at TX0. The output of the receiving section is forced to the recessive state and does not depend on the bus voltage. RX0 still outputs the data corresponding to the input signal at TX0A or TX0B. This is realized by an internal logical connection.

In the enabled state the driving section behavior depends on the input voltage at TX0. The output of the receiving section depends on the bus voltage. RX0 only represents the data of the receiver output. The internal logical connection between TX0 and RX0 is interrupted.

The enable input has an internal pull up resistor to ensure a disabled state when the input is not connected.

Pin VS is an additional supply pin. This pin is used to supply the control stage of the bus driver with a voltage that is higher than the normal supply voltage. This is needed to guarantee proper functioning of the bus driver. The pin VS can be supplied with a DC voltage source, or with a voltage generated with a charge pump. For this purpose a square wave generator is integrated on chip. The output is a push pull CMOS output stage at pin OSC. With the aid of two capacitors and two (external or internal) diodes a charge pump can be build to transform the supply voltage VCC to a higher level at VS.

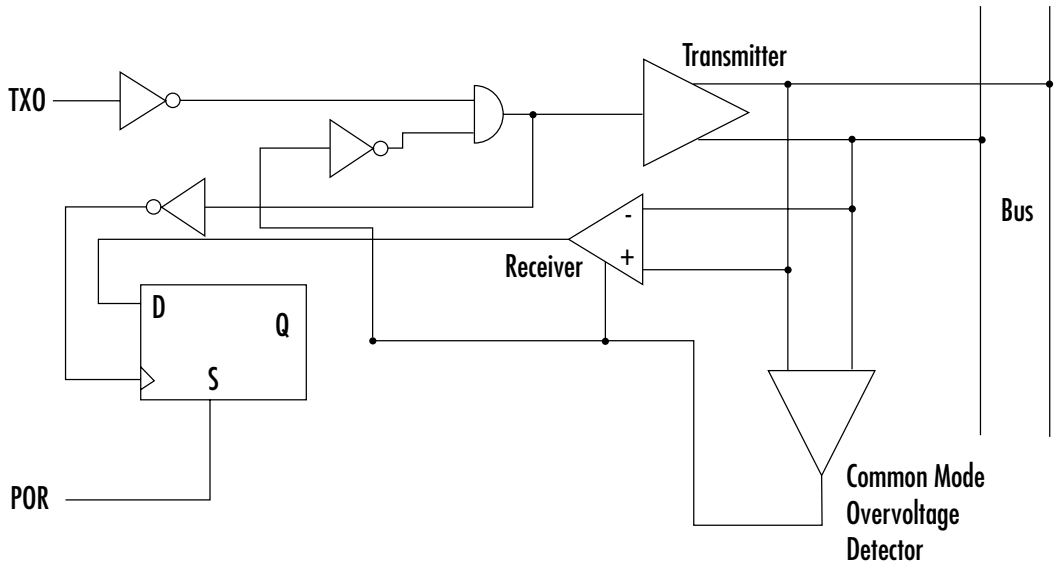


Fig.3: **Power-on Reset**

2.0 Fault Behaviour

Error Condition Handling

When the voltage at the bus lines moved out of the normal operating range, the receiver is not allowed to erroneously detect a dominant state. To ensure this, an 'out of range' signal is generated which will force the receiver to receive a recessive state. This error condition will also prohibit the driver from transmitting a dominant bit on the bus as long as the 'out of range' condition is present. Note that, due to the limited speed of the 'out of range' comparator, the receiver still can erroneously detect (and transfer) a dominant state within the period defined by the reaction time needed by the 'out of range' comparator.

To detect a short between the two bus lines, the receiver will check the state of the bus every time a dominant bit is sent by the transmitter. This check will be done at the end of the dominant pulse. The transmitter is fully self protected. It has a built in current limitation to protect against short circuits. When the voltage at the bus lines moves out of the normal operating range, the transmitter will put itself in a high impedant state to avoid excessive dissipation and to prevent breakdown.

Power-on Reset

Until Vcc reaches the voltage level VPORH, the bus connections CanH and CanL are high impedant. When Vcc is above this level the bus connections CanH and CanL are controlled. If the voltage level at Vcc drops below VPORL, the bus connections CanH and CanL become high impedant. The power-on reset comparator has a well defined hysteresis.

Note that during power on reset, the bus connections CanH and CanL are high impedant for the voltage range from -40 to +7 V. Outside this region, protection circuits can be activated.

Short Circuits

As specified in the maximum ratings, short circuits of the bus wires CanH and CanL to the positive supply voltage Vbat or to ground must not destroy the transceiver. To provide sufficient safety for automotive applications the voltage range for permanent short circuits is extended to 65 V dc. A short circuit between CanH and CanL must not destroy the IC as well. The maximum transient voltages are specified on page 5. These conditions must be fulfilled even in case of missing voltage supply and/or ground.

Faulty Supply

In case of a faulty supply (missing connection of the electronic unit or the transceiver to ground, missing connection of Vbat of the electronic unit, missing connection of Vcc of the transceiver) the power supply module of the electronic unit will operate such that the transceiver is not supplied, i.e. the voltage (Vcc - Vground) is below the power-on reset level. In this condition the bus connections of the transceiver must be in the high impedant state.

If the ground line of the electronic unit is interrupted, Vbat may be applied to the Vcc pin (measured relative to the original ground potential, to which the other units on the bus are connected).

Reverse ECU Supply

If the connections for ground and supply voltage of an electronic unit (ECU) (max. 40 V) which provides Vcc for the transceiver are exchanged this transceiver has a ground potential which may be up to 40 V higher than that of the other transceivers. In this case no transceiver must be destroyed even if several of them are connected via the bus system.

Any exchange among the four connections CanH, CanL, ground and supply voltage of the electronic unit at the connector of the unit must never lead to a destruction of any transceiver of the bus system.

Exchange possibilities	
CanH	CanL
CanH	Ground
CanH	Supply voltage Vbat
CanL	Ground
CanL	Supply voltage Vbat
Ground	Supply voltage (Vbat)

The use of an inverse current protection diode at the supply voltage input of the electronic unit is recommended.

3.0 ElectroMagnetic Compatibility (EMC)

The supply voltage Vcc is provided by the electronic unit in which the interface is located. It can be estimated, therefore, that Vcc is sufficiently filtered.

Disturbances in accordance with DIN 40839 part 2/3

The interface ports CanH and CanL withstand pulses specified in DIN 40839 parts 2 and 3. The voltages are listed below.

Vp varies from -1 to 32 V.
The definitions of the parameters are quoted from DIN 40839.

DIN 40893	Parameter		Part 2	Part 3
Pulse 1	Vs	>=	- 40 V	- 30 V
Pulse 2	Vp+Vs	<=	+80 V	+30 V
Pulse 3a	Vp+Vs	>=	-150 V	- 90 V
Pulse 3b	Vp+Vs	<=	+100 V	+60 V

Requirement	Frequency range	Signal level at CanH or CanL
No influence on IC function	1 MHz ... 400 MHz	0.1 W
No destruction of the IC	1 MHz ... 400 MHz	1 W

Disturbances in accordance with DIN 40839 part 4

The whole design is made under the special consideration of the EMC requirements which are specified in DIN 40893 part 4. Therefore, the following requirements must be met.

Note that these requirements cannot be verified in final test by AMI Semiconductor at the component level.

4.0 Printout and Packaging

Pinout

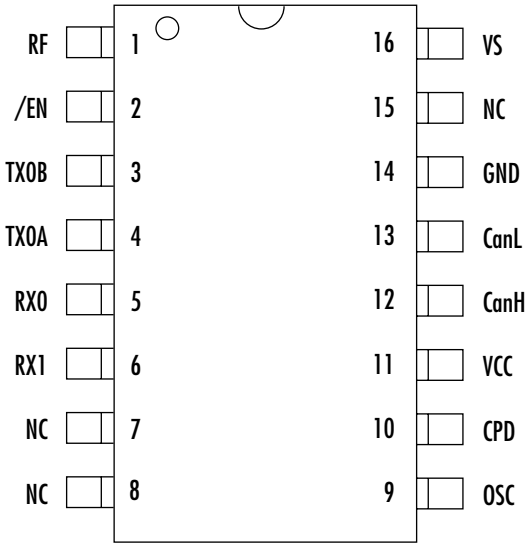


Fig.4: **Pin Configuration (SO16-B)**

Pin Description

Nr	Name	Type	Description
1	RF	Analog in	Slope control (rise-fall) of transmitters
2	/EN	Digital in	Enable input
3	TX0B	Digital in	Transmitter input B
4	TX0A	Digital in	Transmitter input A
5	RX0	Digital out	Receiver output
6	RX1	Analog out	Receiver output
7	NC		Not connected
9	OSC	Digital out	Oscillator output for charge pump
10	CPD	Analog I/O	Diode connection for charge pump
11	VCC	Supply	Positive supply voltage
12	CANH	Analog I/O	CANH transceiver I/O
13	CANL	Analog I/O	CANL transceiver I/O
14	GND	Supply	Ground connection
16	VS	Supply	Output driver secondary supply
8	NC		Not connected
15	NC		Not connected

Packaging

Package Name	Package Code	AMI Semiconductor Drawing no	JEDEC Outline DWG
16 pins PSOP 300 mils	SO16 B	87-0034	MS-013

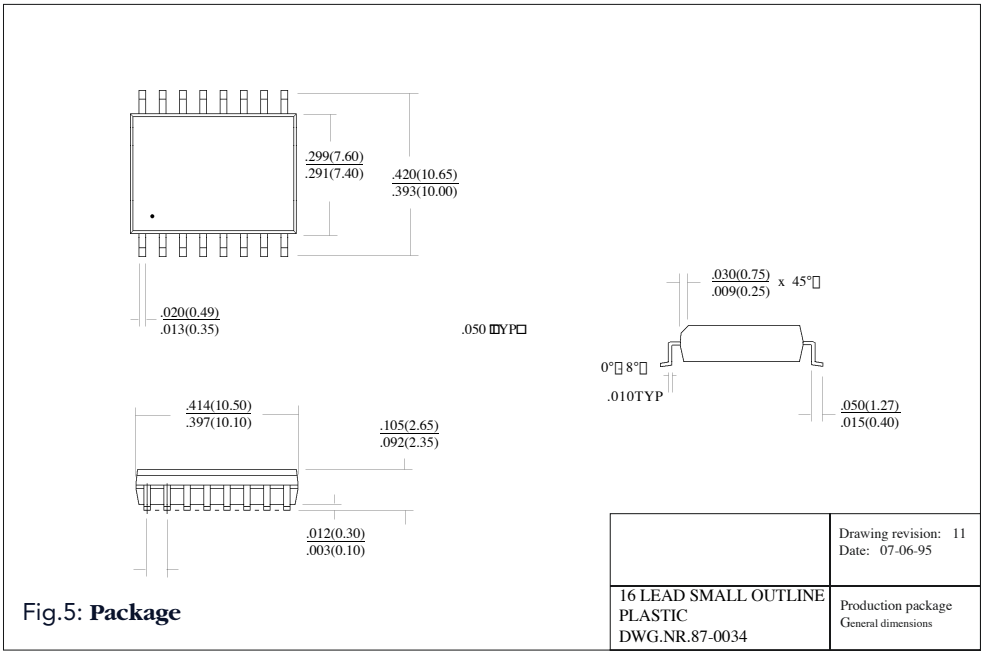


Fig.5: **Package**

Marking

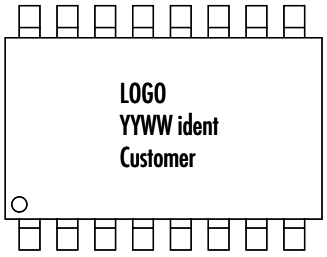


Fig.6: **Topside Marking**

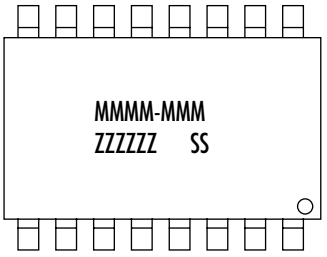


Fig.7: **Backside Marking**

LOGO: Micro-signature Alcatel
YYWW: assembly year and week
SS: Assembly source code

MMMM-MMM: AMI Semiconductor product name
ZZZZZZZ: wafer lot identification

Delivery

Delivered in tubes
44 devices per tube

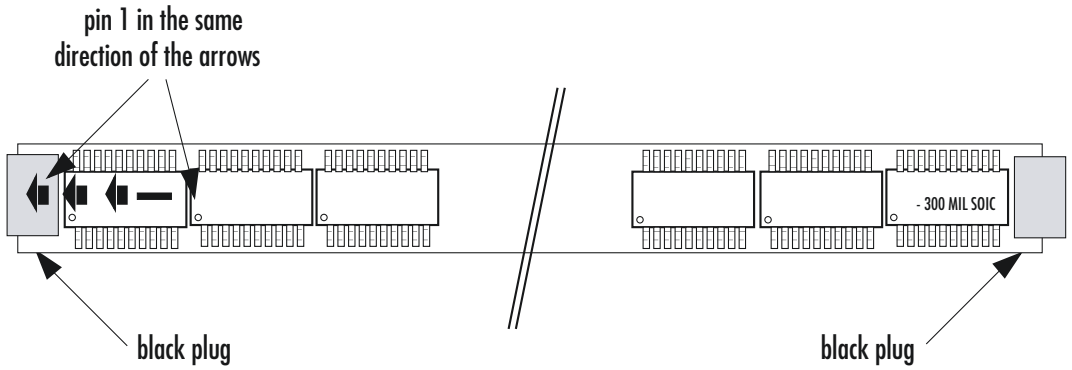


Fig.8: **SOIC Tube**

Delivered tape on reel

The plastic small outline (SO), can be placed in tape on reel, eventually in combination with dry pack.

All used materials and procedures are in line with the related EIA, IEC documents.

IEC 286-3 - packing of components for automatic handling

EIA-481-2 - 16 and 24 mmembossed carrier taping of surface mount components for automatic handling

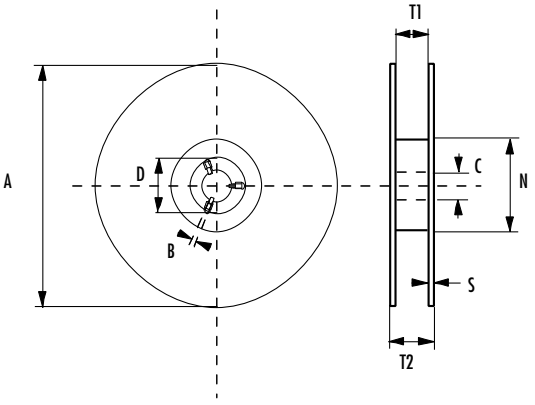


Fig.9

Reels (Fig.9) Tape width	A	N	T1	T2	D	B	C	S
	-0.5	-0.5	-1.6	-0.6	-0.2	-0.5	-0.2	
16	330	62	18	22	30.0	2	13	2.0

(All figures in mm)

Carrier tapes

Carrier tapes with width of 12, 16, 24, 32 or 44 mm are used.

- Material: Conductive polystyrene - black
- Thickness: 200 - 400um
- Tensile strenght: 19 - 25 Mpa
- Elongation at break: 40 - 45%
- Surface resistance: 10E4 - 10E6 ohms/sq
- Vicat softening point: 90 - 98°C

Dimensions for 12, 16 or 24 mm tape
(All dimensions in mm) (Fig 10).

- W: 12 +/- 0.3 or 16 +/- 0.3 or 24 +/- 0.3
- D1min: 1.5
- E1: 1.75 +/-0.10
- P0: 4.0 +/-0.10
- S1min: 0.6

Cover tape

Cover tapes with width of 9.3, 13.5, 21.5, 25.5, 37.5 mm are used in relation to the tape width.

- Material: static dissipative polyester temperature sensitive tape
- First layer: Transparent polyester
- Second layer: Polyethylene
- Total thickness: 0.060 mm
- Tensile strength: 110 N/cm
- Surface resistivity: 1.2x10E12 ohm/SQ
- Elongation at break: 91%

The clearance between the ends of the terminals or body of the component to the sides and depth of the cavity (A0, B0, C0) must be within 0.05 mm min and 0.50 mm max for 12 mm tape, or within 0.15 mm min and 0.9 mm max for 16 mm tape, or within 0.15 mm min and 1.0 mm max for 24, 32 or 44 mm tape.

General

All components are located in the cavity with pin 1 adjacent to the round sprocket holes.

The components are packed with the terminations facing the bottom of the embossed carrier.
There is a leader (start) of 230 mm minimum which may consist of carrier and/or cover tape followed by a minimum of 160 mm of empty carrier tape sealed with cover tape.

There is a tailer (End) of 160 mm minimum of empty carrier tape sealed with cover tape. The entire carrier tape must release from the reel hub as the last portion of the tape unwinds from the reel without damage to the carrier tape and the remaining components in the cavities.

More details can be found in the AMI Semiconductor document spec 16665 and spec 9210.

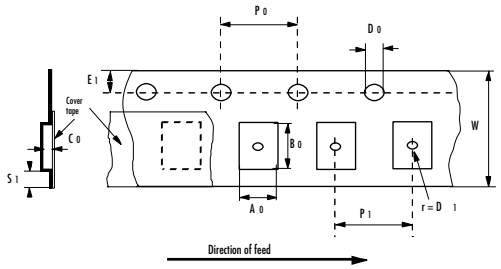


Fig.10

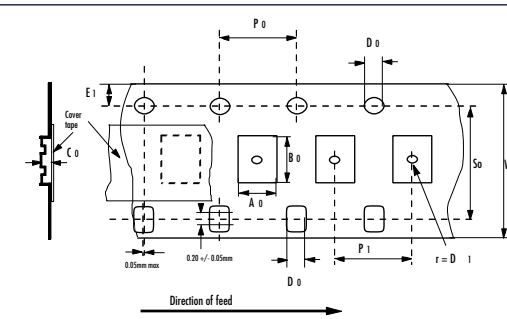


Fig.11

Tooling list for carrier tape:

Package Type	Tape width (W)	Pitch mm (P1)	A0 mm	B0 mm	C0 mm	Standard Qty/reel	Meters /reel	Cavity /reel
SO16 B	16 mm	12	10.7	10.7	3.1	1000	13.0	1083

5.0 Soldering Information

All components meet the minimum requirments of the two requirements outlined below.

- Solder wettability: test Mil STD 883 D method 2003 (95 % solder wetting of the leads)

- Wetting balance solderability test: Mil SRTD 883 D method 2022 (5 sec 245°C)

Through hole devices
These devices can be soldered with most industry standard soldering processes.
The devices withstand the resitance to soldering test IEC 68 - 2 - 20 (2 cycles).

Surface mount devices
Take into account the dry pack recommendatinos as stated on the label applied.

All SMD components can be soldered with the standard infra red, vapour phase and double wave soldering processes. Recommended profiles can be found in fig.12, 13 and14.

IR surface mountable components meet the following test sequence storage 85°C, 85 % RH, 168 hrs followed by 2 cycles of infra red solder heat application (CECC00802) and 100 thermal cycles -55°C/+125°C (Mil STD 883 D method 1010).

Double wave mountable components meet the following test sequence storage 85°C, 85 % RH, 168 hrs followed by 1 cycles of double wave solder heat application (CECC00802) and 100 thermal cycles -55°C/+125°C (Mil STD 883 D method 1010).

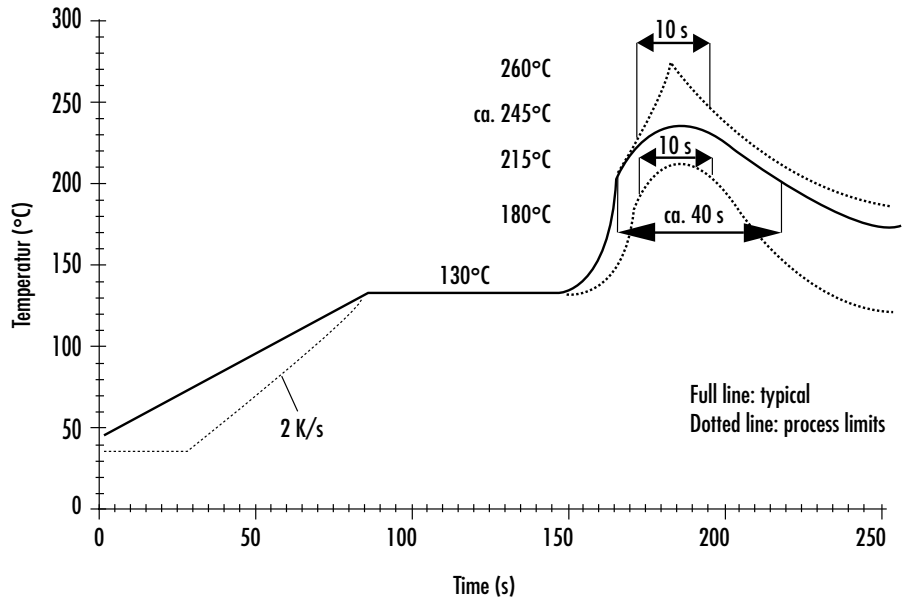
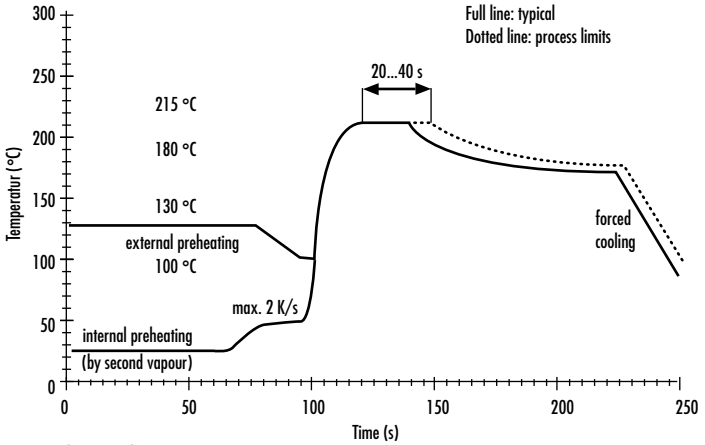


Fig.12: **Infra Red Soldering**



Vapour phase; batch system with pre heating

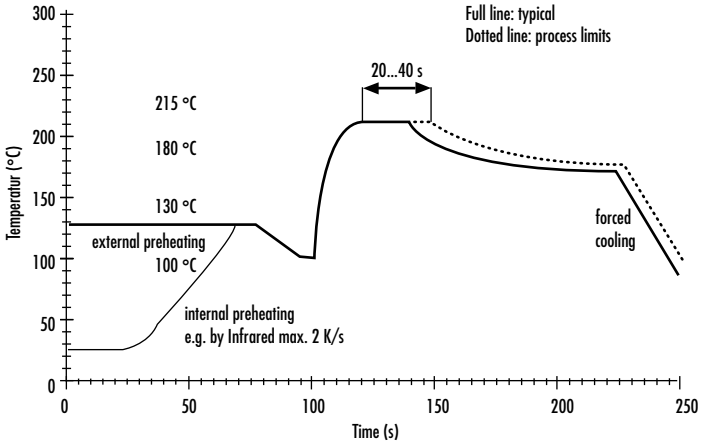


Fig.13: **Vapour phase; in line system with pre heating**

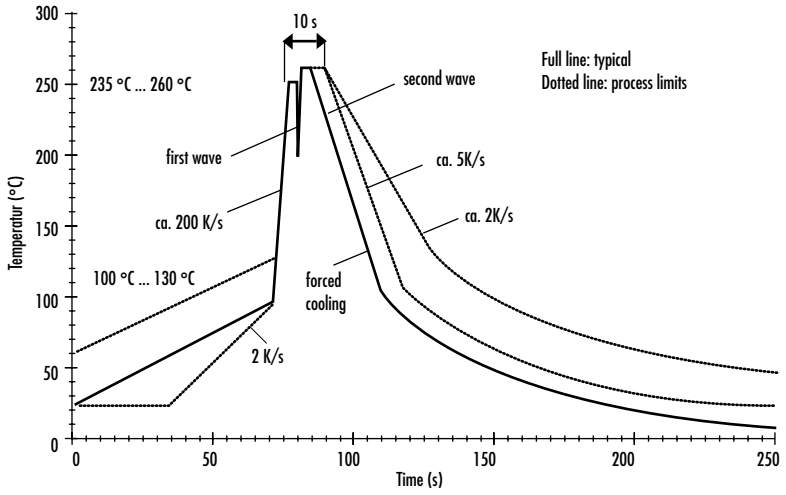


Fig.14: **Double Wave Soldering**

6.0 Electrical Characteristics

Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
TB	Storage temperature	- 55	150	°C
VCC	Power supply voltage	- 0.5	6.0	V
VS	Power supply voltage	- 0.5	65	V
Vid	Voltage at digital input pins	- 0.5	VCC + 0.5	V
Via	Voltage at analog input pins	- 0.5	VCC + 0.5	V
VBUS	Voltage at bus pins CanH and CanL	- 3	65	V
VBAT	Supply voltage for the module	8	32	V
Ibus	Current through the bus pins CanH and CanL	- 300	300	mA

Note:
Although VBAT is not directly connected to the chip, it defines the voltage range applied to the interface pins in the case of a faulty supply.

Operating Ranges

Symbol	Description	Min	Max	Unit
TA	Ambient temperature	- 40	125	°C
VCC	Power supply voltage	4.75	5.25	V
ICCR	Supply current during recessive state		14	mA
ICCD	Supply current during dominant state		110	mA
VS	Power supply voltage	6	40	V
IVSR	Supply current during recessive state		300	µA
IVSD	Supply current during dominant state (VS < 40 V)		4	mA

Note:
The current consumption will be measured:
- without any loads at the digital
- outputs
- with DC conditions at all input pins
- with 60 Ω between CanH and CanL
- with Rrf = 5 KΩ

During Schaffner pulses VS can increase up to 65 V for a maximum duration of 1 s without damaging the chip.

DC-Parameters

All characteristics are valid under the full operating range of temperature and supply voltage, mentioned above, unlessotherwise noted.
All voltages are with respect to ground, unless otherwise noted.
Characteristics marked with § are not tested in production.

Bus Drivers

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VCHR	Output voltage at CanH in recessive state	2	2.5	3	V	no load between CanH and CanL
VCLR	Output voltage at CanL in recessive state	2	2.5	3	V	no load between CanH and CanL
VCDR	= VCHR - VCLR	- 500	0	50	mV	
VCHD	Output voltage at CanH in dominant state	3.0	3.5	4.5	V	60 Ω between CanH and CanL note 1
VCLD	Output voltage at CanL in dominant state	0.5	1.5	2.0	V	60 Ω between CanH and CanL note 1
VCDD	= VCHD - VCLD	1.5	2.0	3.0	V	
VCM1	Difference between common mode voltage in dominant and recessive state (DC measurements)		1	1.5	V	note 2
VCM2	Variation in common mode voltage during transients			2	V	note 2

Note 1:
Considering a maximum of 30 units connected to a bus the voltage specifications must also be fulfilled for a load of 50 Ω between CanH and CanL.

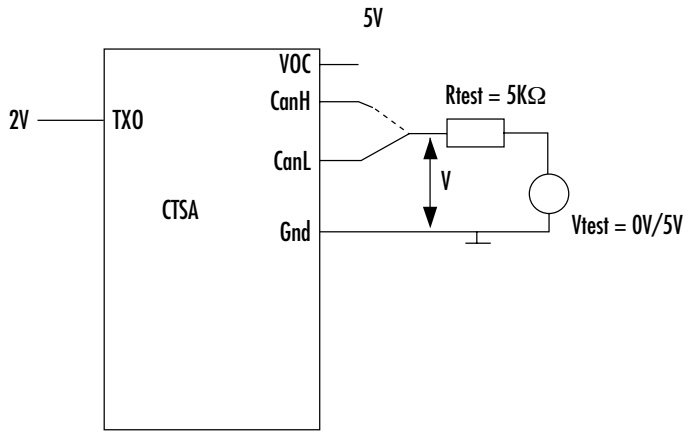
Note 2:
The common mode voltage is defined as the sum
CMj = (VCanH + VCanL) j with j
= {D, R}
= {dominant, recessive}

VCM1 = ABS (CMD - CMR) as a DC measurement
VCM2 = (CMmax - CMmin) as an AC measurement
Measurement conditions:
60 Ω between CanH and CanL
200pF between CanH and ground
200pF between CanL and ground
VCC = 5 V
VS = 7 V
Rrf = 5 KΩ
bitrate = 500 Kbit/s (only applicable for VCM2)

Bus Interface Impedances

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
RCH	Bus input resistance at CanH during recessive state	7		30	kΩ	see Fig.15
RCL	Bus input resistance at CanL during recessive state	7		30	kΩ	see Fig.15
RCD	Differential input resistance between CanH and CanL	10		100	kΩ	see Fig.16
RCM	Matching of RCH and RCL			3	%	note 1
ICZ	Input current at CanH and CanL during POR	-350		350	µA	0<VCC<VPORL note 2°

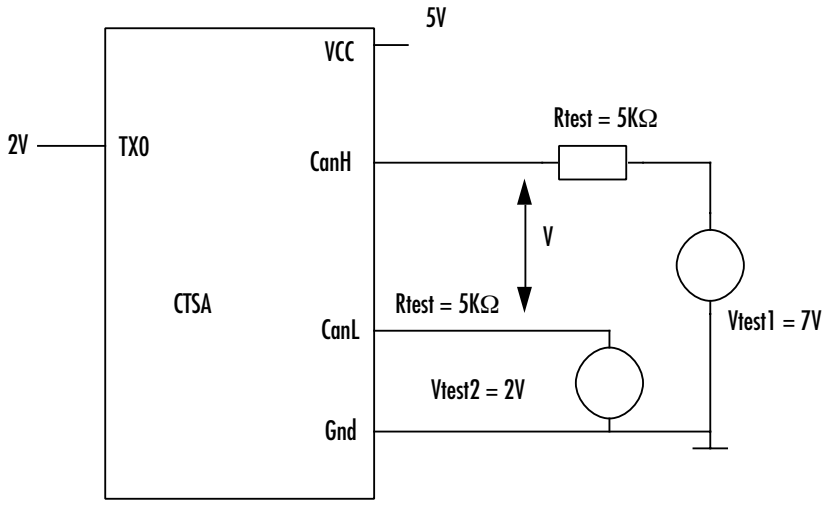
Note 1:
Matching of RCH and RCL is defined as:
ABS[(RCH - RCL) / (RCH + RCL)]*100
Note 2:
Valid for voltages at CanH and CanL
in the range from - 40 to +7 V.
For supply voltages in the range of
-0.5 V<Vcc<0 the input current will increase but will be
limited to a level that will not destroy the device.



$$ROH = \frac{Rtest * (V - VOHR)}{Vtest - V}$$

$$ROL = \frac{Rtest * (V - VOLR)}{Vtest - V}$$

Fig.15: **Definition of Rin**



$$RCD = \frac{Rtest * (V - VCDR)}{(Vtest1 - Vtest2) - V}$$

Fig.16: **Definition of Rdif**

VCHR, VCLR and VCDR are the open circuit voltages defined in the table on page 13. All measurements are DC measurements.

Bus Receiver

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VDR	Differential voltage which ensures the reception of a recessive state			0.5	V	
VDD	Differential voltage which ensure the reception of a dominant state	0.9			V	
VHYS	Built in hysteresis of the comparator	100		200	mV	
VCM	Input voltage range	-2.0		7.0	V	note 1

Note 1:
This parameter indicates that the reception of a dominant and recessive state must be possible over the referred input voltage range. (The voltage of both bus lines must be in this range).

When going outside this region the out-of-range comparator will eventually be activated. The exact levels of this comparator will not be measured in production, the functionality however is verified when measuring the speed of this detection circuit (parameter TDCMO).

Digital Interface

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
TTLVH	High level input voltage at TTL compatible input pin	2.0			V	
TTLVL	Low level input voltage at TTL compatible input pin			0.8	V	
TTLRU	Pull up resistance at TTL compatible input pin	10		40	kΩ	
CMVH	High level output voltage at CMOS compatible output pin	2.7			V	Iout = - 4 mA note 1
		VCC-1			V	Iout = - 2 mA note 1
CMVL	Low level output voltage at CMOS compatible output pin			0.4	V	Iout = 4 mA note 1

Note 1:
This parameter is applicable for all CMOS compatible outputs RX0, OSC.

AC - Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
TDRI	Central driving delay time			100	ns	baudrate = 500 Kbit/s note 1 see fig.17
TREC	Central receiving delay time			130	ns	baudrate = 500 Kbit/s note 1, 2 see fig.18
TDTR	Delay from TX0 to RX0			100	ns	baudrate = 500 Kbit/s note 3 see fig.19
TEN	Enable/disable delay time		100	200	ns	baudrate = 500 Kbit/s note 1
TDEL	Bus driver recovery time after schaffner pulse			20	us	note 4
Cin §	Input capacitance for pins CanH and CanL	3	10	30	pF	
Cdiff §	Differential input capacitance between CanH and CanL		5	15	pF	
Cload §	Max. external load capacitance	5			nF	
Fosc	Oscillation frequency at pin OSC	0.2		1	MHz	
Ccp1	Charge pump charge capacitance	10			nF	
Ccp2	Charge pump storage capacitance	100			nF	

Note 1:
60 Ω between CanH and CanL
200 pF between CanH and ground 200 pF between CanL and ground.
In production only the sum of the respective delay time TDRI and the rise or fall time will be measured, as indicated in Fig.17, 18. The limits are:

t1,2 = TDRI + TF(TR)
= 100 + 1.3*80 = 204ns
for Rrf = 5 KΩ
t1,2 = TDRI + TF(TR)
= 100 + 1.3*320 = 516ns
for Rrf = 20 KΩ

Note 2:
The input signal on the bus has a rise and fall time of 80 ns ± 20 %

Note 3:
This delay is only valid when /EN is high (disabled transceiver). Under this condition the input TX0 is transferred directly to the output RX0.
When /EN is low, the data at TX0 is passed to the bus via the transmitter, and is returned to RX0 via the receiver. This delay is therefore much larger and is dependant on the bus load.

Note 4:
TDEL is measured using a voltage step from 25 V to 2.5 V on the outputs CanH and CanL.

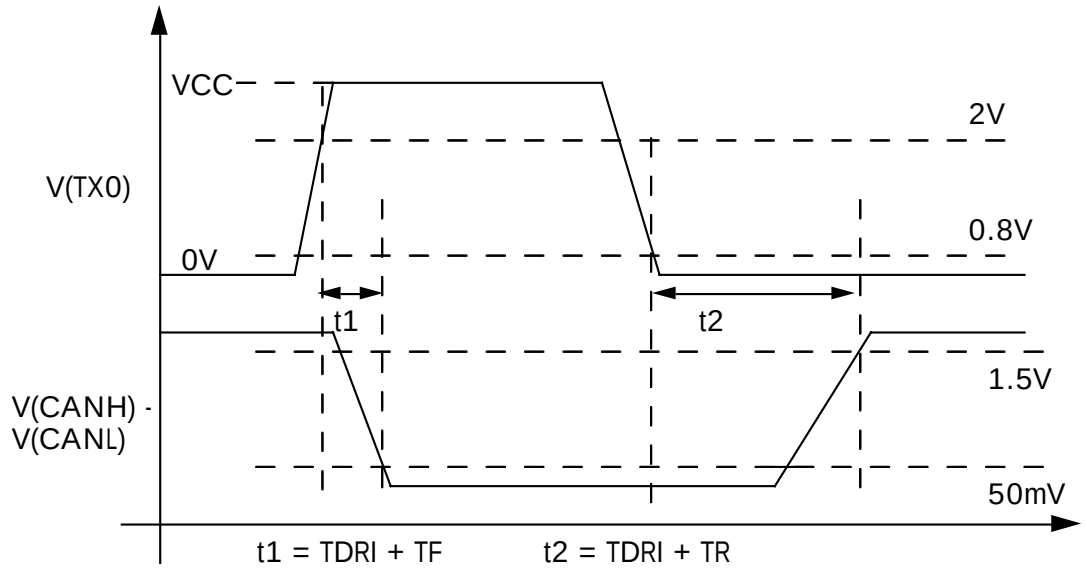


Fig.17: **Definition of tdri**

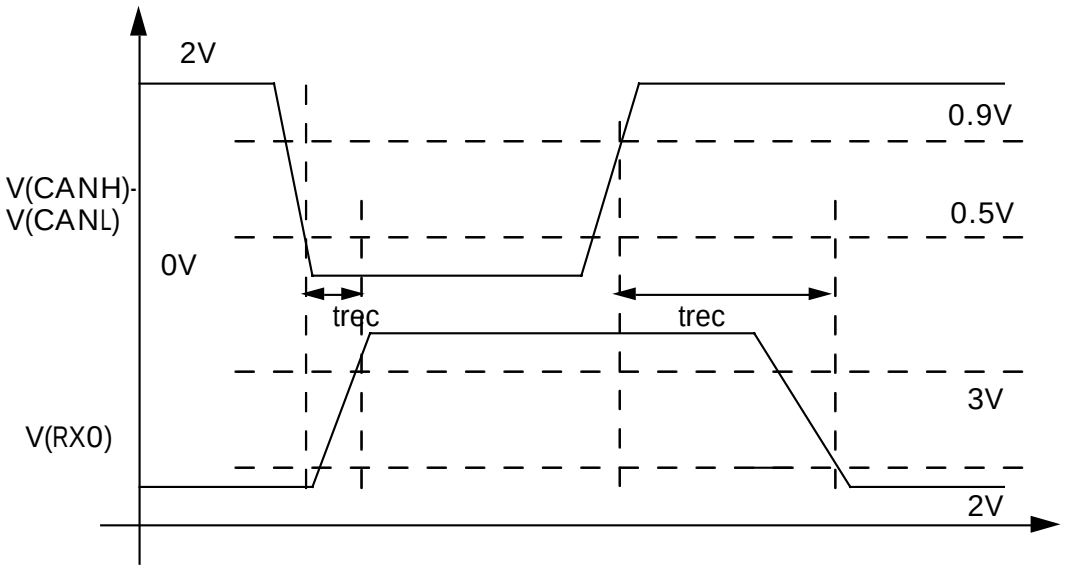


Fig.18: **Definition of trec**

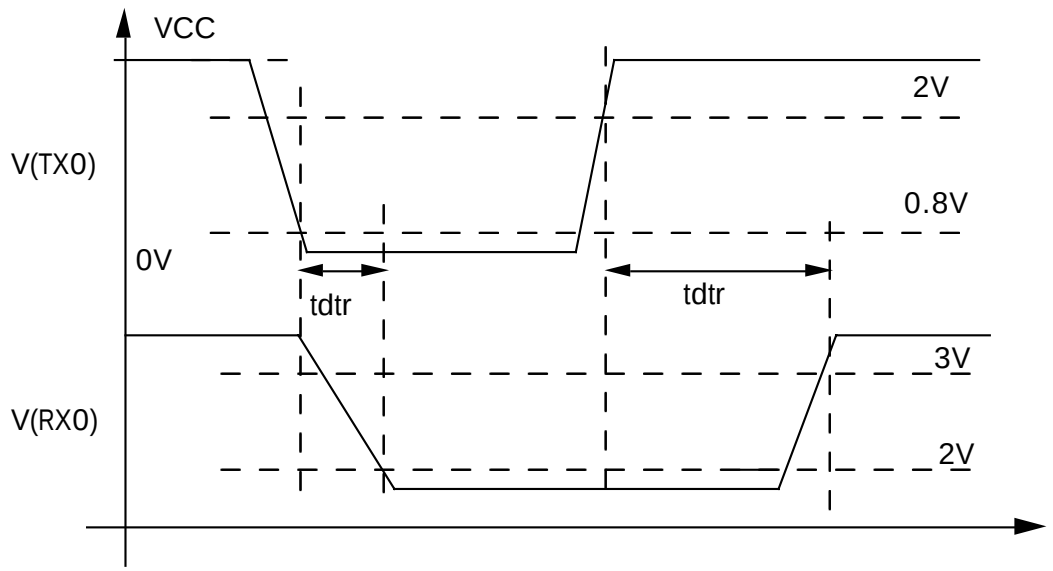


Fig.19: **Definition of tdtr**

Miscellaneous Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
SRT	Tolerance on slew rate	- 40		+35	%	note 1
Rrf	External driver slope control resistor	5		20	kΩ	
VRX1	Output voltage on pin RX1	0.47 VCC		0.53 VCC	V	
RRX1	Output impedance of pin RX1			10	kΩ	
TDCMO	Delay time for the common mode overvoltage detection comparator			20	µs	
VPORH	High level of the power-on reset comparator	3.7		4.5	V	note 2
VPORL	Low level of the power-on reset comparator	3.2		4.0	V	note 2
VPORD	Hysteresis of the power-on reset comparator	0.3		0.8	V	note 2

Note 1:
The rise time and fall time of the transmitter signal are defined by connecting a resistor Rrf between pin RF and ground.

- TR = TF = 16 E -12 * Rrf
- Δ V= 1.45 V, Ta = 25°C, Vcc = 5 V

This relationship is valid for
- Rrf = 5 kΩ ... 20 kΩ

Measurement conditions:
- 60 Ω between CanH and CanL
- 200 pF between CanH and ground
- 200 pF between CanL and ground

This parameter is not measured directly in production. The sum of the delay time and rise/fall time is guaranteed as shown under AC parameters.

Note 2:
To guarantee proper functioning of the power-on reset comparator, the slew rate of the power supply Vcc should be limited to 0.2 V/µs maximum.
Only the power-on reset levels are guaranteed at these supply voltages. All other parameters in this document are only guaranteed for the operating range power supply voltage.