4M×4 CMOS EDO DRAM

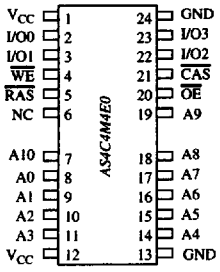
Advance information

Features

- Organization: 4,194,304 words × 4 bits
- High speed
  - 50/60/70 ns $\overline{RAS}$ access time
  - 25/30/35 ns column address access time
  - 10/12/15 ns $\overline{CAS}$ access time
- Low power consumption
  - Active: 908 mW max
  - Standby: 5.5 mW max, CMOS I/O
- Extended data out
- 2048 refresh cycles, 16 ms refresh interval
- $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh
- TTL-compatible, three-state I/O
- JEDEC standard package
  - 400 mil, 24/26-pin SOJ
- 5V power supply (4C4M4E0)
- 3V power supply (4LC4M4E0)
- Latch-up current ≥ 200 mA
- ESD protection ≥ 2000 mA

Pin arrangement

SOJ



Pin designation

Pin(s)	Description
A0 to A10	Address inputs
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
I/O0 to I/O3	Input/output
$\overline{OE}$	Output enable
V_{CC}	Power
GND	Ground

DRAM

Selection guide

	Symbol	4C4M4E0-50 4LC4M4E0-50	4C4M4E0-60 4LC4M4E0-60	4C4M4E0-70 4LC4M4E0-70	Unit
Maximum $\overline{RAS}$ access time	t_{RAC}	50	60	70	ns
Maximum column address access time	t_{CAA}	25	30	35	ns
Maximum $\overline{CAS}$ access time	t_{CAC}	10	12	15	ns
Maximum output enable ($\overline{OE}$) access time	t_{OEA}	8	10	12	ns
Minimum read or write cycle time	t_{RC}	85	100	120	ns
Minimum fast page mode cycle time	t_{PC}	25	30	35	ns
Maximum operating current	I_{CC1}	195	180	165	mA
Maximum CMOS standby current	I_{CC5}	1.0	1.0	1.0	mA

Functional description

The AS4C4M4E0 and AS4LC4M4E0 are high performance 16-megabit CMOS Dynamic Random Access Memories (DRAM) organized as 4,194,304 words × 4 bits. The AS4C1M16E0 is fabricated using advanced CMOS technology and innovative design techniques resulting in high speed, extremely low power and wide operating margins at component and system levels. The Alliance 16Mb DRAM family is optimized for use as main memory in PC, workstation, router and switch applications.

The AS4C4M4E0 features a high speed page mode operation where read and write operations within a single row (or page) can be executed at very high speed (12 ns from $\overline{CAS}$ or 30 ns from address for the 4C4M4E0-60 device) by toggling column addresses within that row. Row and column addresses are alternately latched into input buffers using the falling edge of $\overline{RAS}$ and $\overline{CAS}$ inputs respectively. Also, $\overline{RAS}$ is used to make the column address latch transparent, enabling application of column addresses prior to $\overline{CAS}$ assertion.

Extended data out (EDO) read mode enables 60MHz operation using 60ns devices. In contrast to 'fast page mode' devices, data remains active on outputs after $\overline{CAS}$ is de-asserted high, giving system logic more time to latch the data. Use $\overline{OE}$ and $\overline{WE}$ to control output impedance and prevent bus contention during read-modify-write and shared bus applications. Outputs also go to high impedance at the last occurrance of $\overline{RAS}$ and $\overline{CAS}$ going high.

Refresh on the 2048 address combinations of A0 to A10 must be performed every 16 ms using:

- $\overline{RAS}$-only refresh: $\overline{RAS}$ is asserted while $\overline{CAS}$ is held high. Each of the 2048 rows must be strobed. Outputs remain high impedence.
- Hidden refresh: $\overline{CAS}$ is held low while $\overline{RAS}$ is toggled. Refresh address is generated internally. Outputs remain low impedence with previous valid data.
- $\overline{CAS}$-before-$\overline{RAS}$ refresh (CBR): At least one $\overline{CAS}$ is asserted prior to $\overline{RAS}$. Refresh address is generated internally. Outputs are high-impedence ($\overline{OE}$ and $\overline{WE}$ are don't care).
- Normal read or write cycles refresh the row being accessed.

The AS4C4M4E0 and AS4LC4M4E0 are available in the standard 24-pin plastic SOJ package. The 4C4M4E0 device operates with a single power supply of 5V ± 0.5V and the 4LC4M4E0 operates at 3.3V ± 0.3V. Both provide TTL compatible inputs and outputs.

DRAM

Logic block diagram