

MT5C1608
2K x 8 SRAM

T-46-23-12

SRAM

2K x 8 SRAM

5 VOLT SRAM

FEATURES

- High speed: 8*, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with \overline{CE} and \overline{OE} options
- All inputs and outputs are TTL compatible

OPTIONS

• Timing

8ns access	- 8*
10ns access	-10
12ns access	-12
15ns access	-15
20ns access	-20
25ns access	-25

• Packages

Plastic DIP (300 mil)	None
Plastic SOJ (300 mil)	DJ

NOTE: Available in ceramic packages tested to meet military specifications. Please refer to Micron's *Military Data Book*.

• 2V data retention

L

• Temperature

Industrial (-40°C to +85°C)	IT
Automotive (-40°C to +125°C)	AT
Extended (-55°C to +125°C)	XT

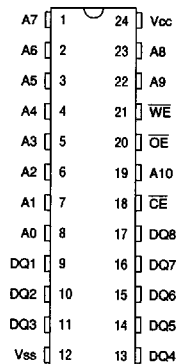
• Part Number Example: MT5C1608DJ-8 L IT

*Preliminary

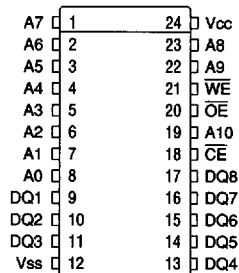
MARKING

PIN ASSIGNMENT (Top View)

24-Pin DIP (SA-3)



24-Pin SOJ (SD-1)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable (\overline{CE}) and output enable (\overline{OE}) with this organization. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable (\overline{WE}) and \overline{CE} inputs are both LOW. Reading is accomplished when \overline{WE} remains HIGH and \overline{OE} and \overline{CE} go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

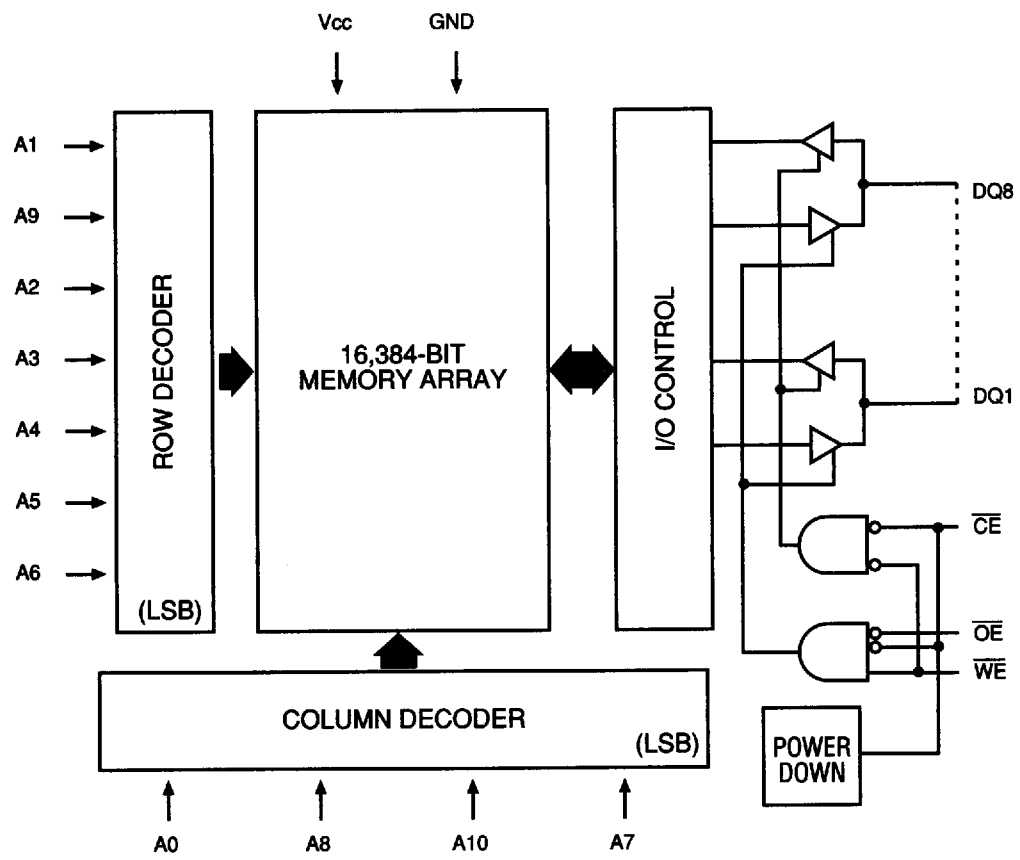
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FUNCTIONAL BLOCK DIAGRAM

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TRUTH TABLE

MODE	\overline{OE}	\overline{CE}	\overline{WE}	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss -1V to +7V
 Storage Temperature (Plastic) -55°C to +150°C
 Power Dissipation 1W
 Short Circuit Output Current 50mA
 Voltage on any pin relative to Vss -1V to Vcc +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ TA ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.2	V _{CC} +1	V	1
Input Low (Logic 0) Voltage		V _{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}	I _{LI}	-5	5	μA	
Output Leakage Current	Output(s) Disabled 0V ≤ V _{OUT} ≤ V _{CC}	I _{LO}	-5	5	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V	1
Supply Voltage		V _{CC}	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX						UNITS	NOTES
				-8*	-10	-12	-15	-20	-25		
Power Supply Current: Operating	CE ≤ V _{IL} ; V _{CC} = MAX f = MAX = 1/'RC Outputs Open	I _{CC}	65	170	155	140	120	110	110	mA	3, 14
Power Supply Current: Standby	CE ≥ V _{IH} ; V _{CC} = MAX f = MAX = 1/'RC Outputs Open	I _{SB1}	20	60	50	45	40	35	35	mA	14
	CE ≥ V _{CC} - 0.2V; V _{CC} = MAX V _{IN} ≤ V _{SS} + 0.2V or V _{IN} ≥ V _{CC} - 0.2V; f = 0	I _{SB2}	0.4	3	3	3	3	3	5	mA	14

*Preliminary

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T _A = 25°C; f = 1 MHz V _{CC} = 5V	C _I	5	pF	4
Output Capacitance		C _O	7	pF	4



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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; V_{cc} = 5V ±10%)

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DESCRIPTION	SYM	-8*		-10		-12		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle															
READ cycle time	t _{RC}	8		10		12		15		20		25		ns	
Address access time	t _{AA}		8		10		12		15		20		25	ns	
Chip Enable access time	t _{ACE}		7		8		10		12		15		20	ns	
Output hold from address change	t _{OH}	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	t _{LZCE} [†]	2		2		2		2		2		2		ns	7, 15
Chip disable to output in High-Z	t _{HZCE}		4		5		6		7		8		8	ns	6, 7
Chip Enable to power-up time	t _{PU}	0		0		0		0		0		0		ns	
Chip disable to power-down time	t _{PD}		8		10		12		15		20		25	ns	
Output Enable access time	t _{AOE}		4.5		5		6		7		8		8	ns	
Output Enable to output in Low-Z	t _{LZOE}	0		0		0		0		0		0		ns	
Output disable to output in High-Z	t _{HZOE}		4.5		5		5		6		7		8	ns	6
WRITE Cycle															
WRITE cycle time	t _{WC}	8		10		12		15		20		25		ns	
Chip Enable to end of write	t _{CW}	6.5		8		10		12		15		20		ns	
Address valid to end of write	t _{AW}	6.5		8		10		12		15		20		ns	
Address setup time	t _{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t _{AH}	0		0		0		0		0		0		ns	
WRITE pulse width	t _{WP1}	5.5		7		8		10		12		15		ns	
WRITE pulse width	t _{WP2}	8		9		10		14		18		20		ns	
Data setup time	t _{DS}	4.5		6		7		8		9		10		ns	
Data hold time	t _{DH}	0		0		0		0		0		0		ns	
Write disable to output in Low-Z	t _{LZWE}	2		2		2		2		2		2		ns	7
Write Enable to output in High-Z	t _{HZWE}		4		5		5		6		8		8	ns	6, 7

*These specifications are preliminary.

†The difference between the shaded and unshaded parameters is explained in note 15 on the following page.



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AC TEST CONDITIONS

Input pulse levels	V _{ss} to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

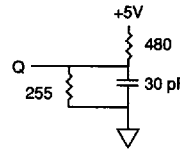


Fig. 1 OUTPUT LOAD EQUIVALENT

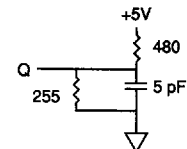


Fig. 2 OUTPUT LOAD EQUIVALENT

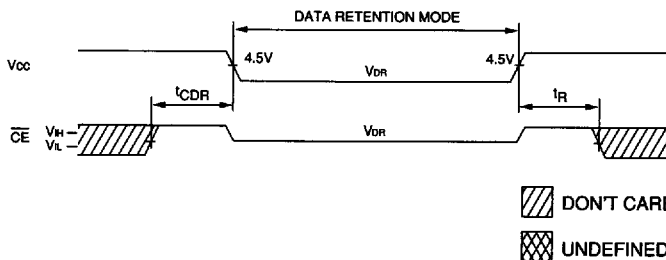
NOTES

1. All voltages referenced to V_{ss} (GND).
2. -3V for pulse width < t_{RC}/2.
3. I_{cc} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. t_{HZCE}, t_{HZWE} and t_{HZOE} are specified with C_L = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} and t_{HZWE} is less than t_{LZWE}.
8. \overline{WE} is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. t_{RC} = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's SRAM Data Book for applicable non-commercial temperature range specifications.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.
15. New designs should use the t_{LZCE} parameters shown unshaded. The shaded t_{LZCE} parameters represent screened parts, which are available upon request until January 1, 1994.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V _{cc} for Retention Data		V _{DR}	2			V	
Data Retention Current	$\overline{CE} \geq (V_{cc} - 0.2V)$ $V_{IN} \geq (V_{cc} - 0.2V)$ or $\leq 0.2V$	V _{cc} = 2V		95	250	μA	
		V _{cc} = 3V		125	400	μA	
Chip Deselect to Data Retention Time		t _{CDR}	0			ns	4
Operation Recovery Time		t _R	t _{RC}			ns	4, 11

LOW V_{cc} DATA RETENTION WAVEFORM



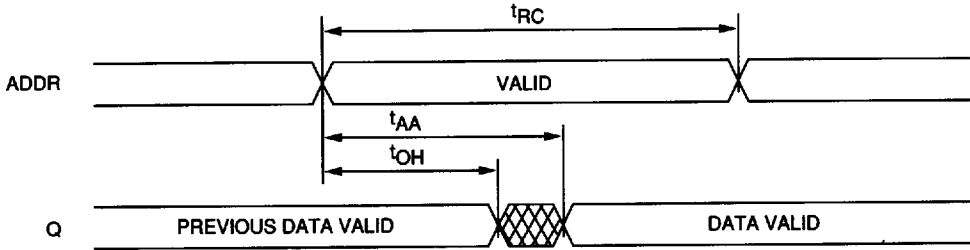
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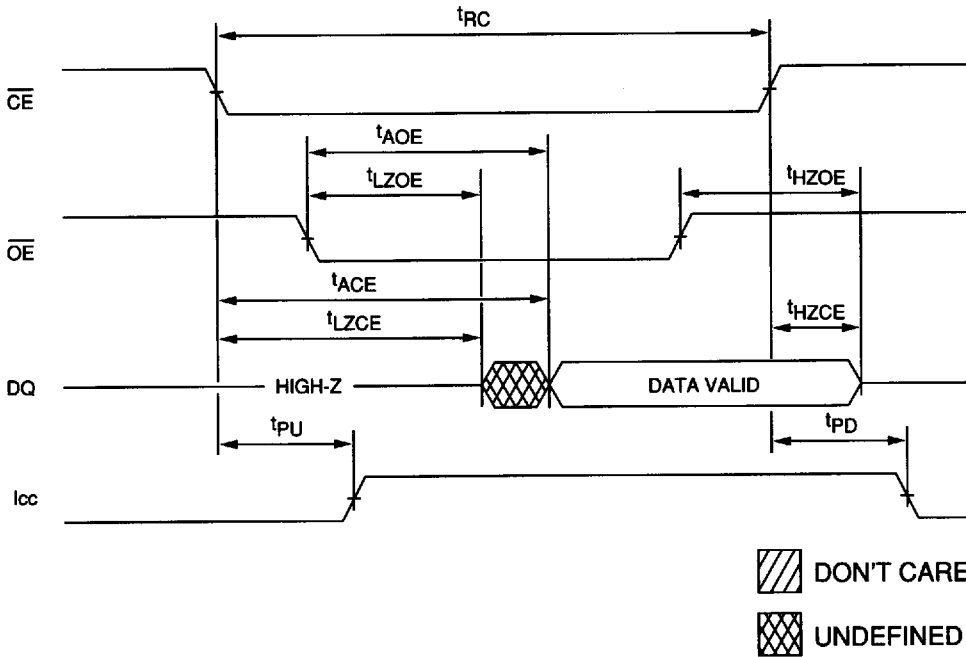
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READ CYCLE NO. 1^{8,9}



READ CYCLE NO. 2^{7,8,10}



 **DON'T CARE**
 **UNDEFINED**

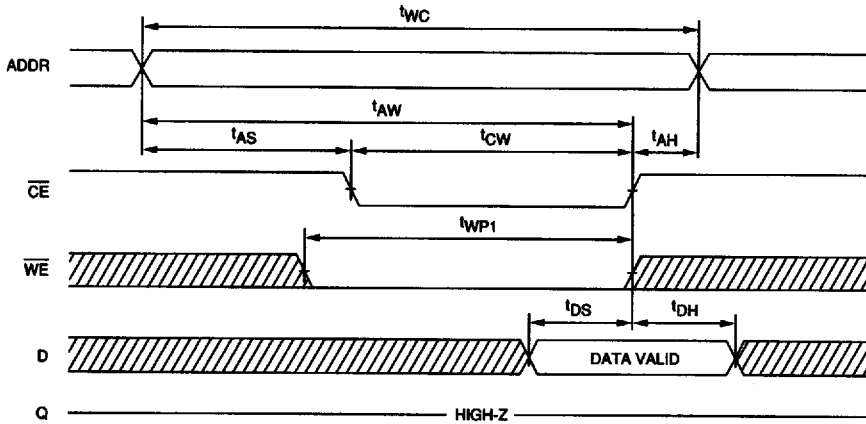
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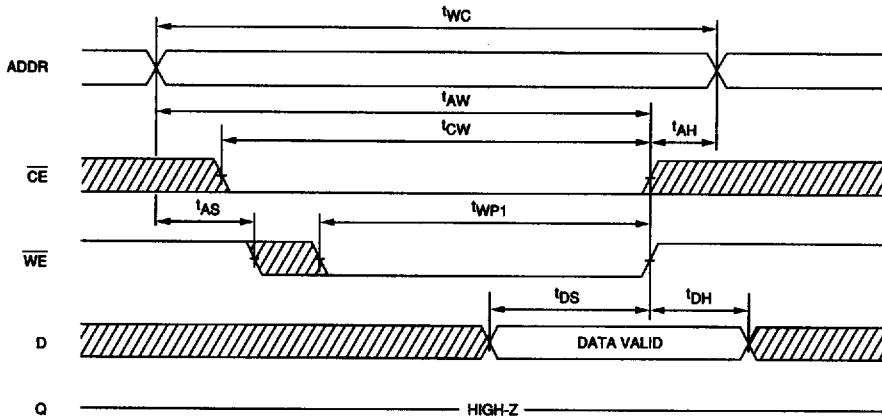
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**WRITE CYCLE NO. 1¹²
(Chip Enable Controlled)**



**WRITE CYCLE NO. 2¹²
(Write Enable Controlled)**



▨ DON'T CARE
▩ UNDEFINED

NOTE: Output enable (\overline{OE}) is inactive (HIGH).

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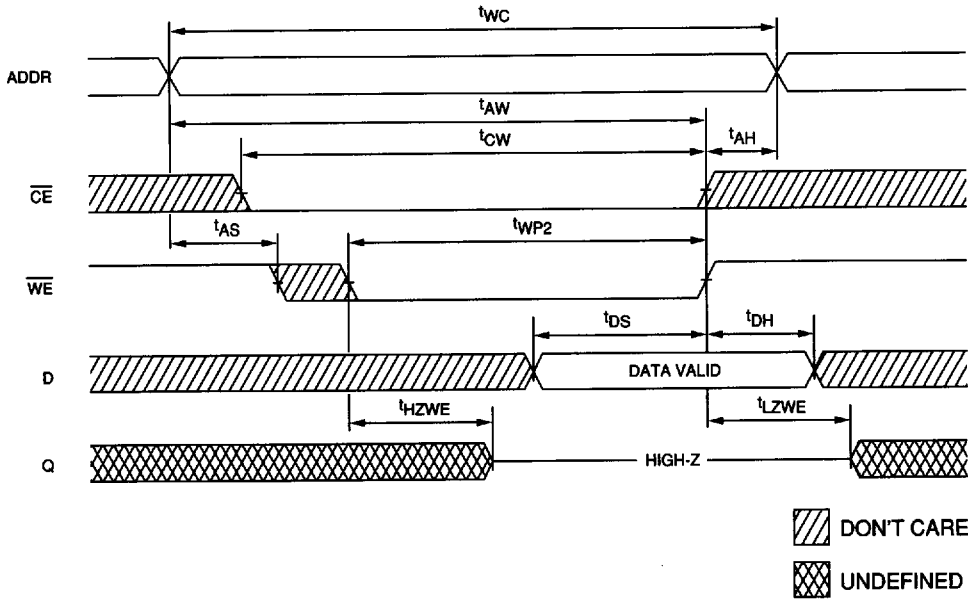
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WRITE CYCLE NO. 3^{7,12}
(Write Enable Controlled)

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NOTE: Output enable (\overline{OE}) is active (LOW).