MC2045-2Y

Postamplifier/Quantizer for Applications to 200 Mbps

The MC2045-2Y is an integrated, high gain limiting amplifier intended for fiber optic communication to 200 Mbps. Normally placed following the photodetector and transimpedance amplifier, the post-amplifier provides the necessary gain to give PECL compatible logic outputs.

The MC2045-2Y includes a programmable signal-level detector, allowing the user to set thresholds at which the logic outputs are enabled. The signal detect function has typically 2 dB (optical) hysteresis which prevents chatter at low input levels.

A JAM function, which turns off the output when no signal is present, is provided by externally connecting the $\overline{ST}$ output to the JAM input.

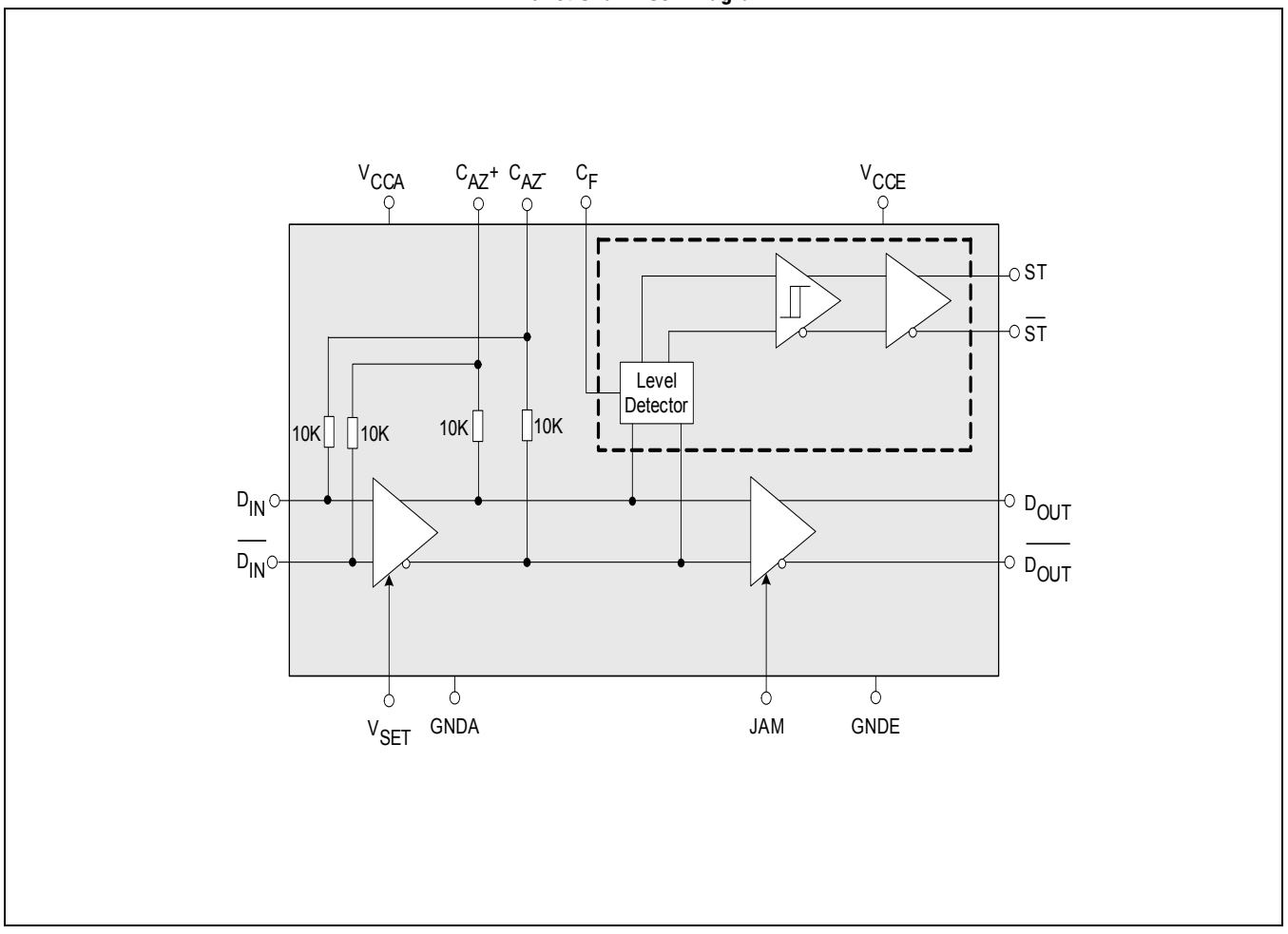
Applications

- SDH/SONET 155 Mbps Transceivers
- Fast Ethernet Receivers
- FDDI 125 Mbps Receivers
- ESCON Receivers
- FTTx and Media Converters

Features

- Operates with a 3.3 V or 5 V supply
- 1.6 mV typical input sensitivity
- Typical Supply Current 12.5 mA at V_{CC} = 3.3 V
- Wide range programmable input-signal level detect
- Complimentary PECL data & signal detect logic outputs
- Output disable function (JAM) when no input signal detected
- Available in TSSOP20, SOIC16, QSOP16 and BCC++16L package as well as die form

Functional Block Diagram



Ordering Information

Part Number	Pin Package	Operating Temperature
MC2045-2YDIEWP	Waffle pack	–40 °C to 85 °C
MC2045-2YWAFER	Expanded wafer on a grip ring	–40 °C to 85 °C
MC2045-2Y04-T	SOIC16	–40 °C to 85 °C
MC2045-2Y03-T	QSOP16	–40 °C to 85 °C
MC2045-2Y01-T	TSSOP20	–40 °C to 85 °C
MC2045-2Y06-T	BCC++16L	–40 °C to 85 °C
M02045-2QEVM	QSOP evaluation board	–40 °C to 85 °C
M02045-P6EVM	QSOP Eval board includes the MC2006 TIA	–40 °C to 85 °C
M02045-P7EVM	QSOP Eval board includes the MC2007 TIA	–40 °C to 85 °C

Revision History

Revision	Level	Date	ASIC Revision	Description
G	Final	April 2004		Update format to new style and add SFF applications circuit.

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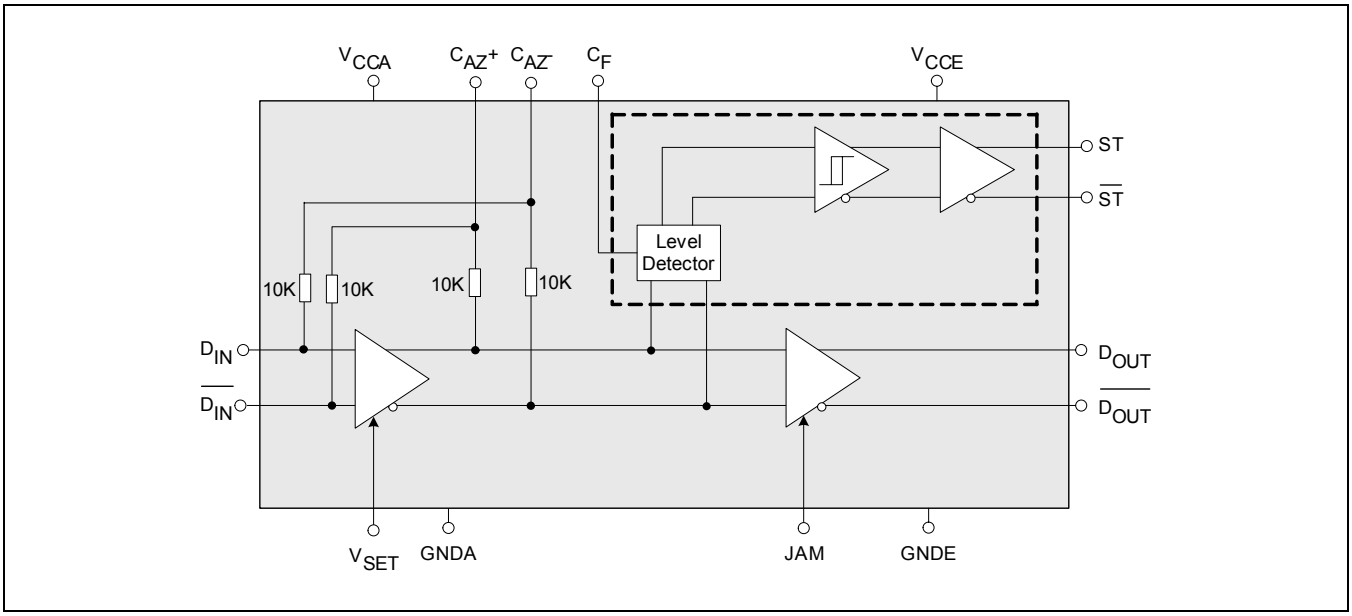
1.0 Functional Description

1.1 Overview

Figure 1-1. Block Diagram Example



1.2 Features

- Operates with a 3.3 V or 5 V supply
- 1.6 mV typical input sensitivity
- Typical Supply Current 12.5 mA at V_{CC} = 3.3 V
- Wide range programmable input-signal level detect
- Complimentary PECL data & signal detect logic outputs
- Output disable function (JAM) when no input signal detected
- Available in TSSOP20, SOIC16, QSOP16 and BCC++16L package as well as die form

1.3 General Description

1.3.1 Data Inputs

The data input pins are internally DC-biased at approximately V_{CC} - 1V so the MC2045-2Y input signals need to be AC-coupled using external capacitors. These capacitors must be large enough to pass the lowest frequencies of interest (consecutive '1's or '0's) considering the input resistance. For example, at 155 Mbps SONET, there can be up to a maximum of 72 consecutive '1' s, which is 465 ns (corresponding to a frequency of 1.08 MHz).

To minimize the data dependent jitter, the AC-coupled input low frequency cutoff needs to be lower than the above by a factor of 10 (<100 kHz). However, it is better to set it an additional factor of 5 - 10 lower (~ 10 to 20 kHz) due to the interaction of the time constants for the input stage and the DC restore circuitry. For example, setting C1 and C2 (Figure 1-2 and Figure 1-3) to 10 nF gives a typical -3 dB point of approximately 1.6 kHz and 4.7 nF gives 3.4 kHz.

1.3.2 DC Offset Compensation

Internal feedback is included to remove the effects of both TIA output DC offset and internal MC2045-2Y DC offset and acts as a DC auto zero circuit. An external capacitor (C_{AZ}) acting with the internal circuit feedback resistors (typically 20 kΩ) ensures that the feedback is effective only at frequencies below the lowest frequency of interest. C_{AZ} is normally set to 300 pF - 10 nF depending upon the application (see Figure 1-2 and Figure 1-3).

1.3.3 Signal Level Detector (ST and $\overline{ST}$)

The gain of the first stage is determined by R_{SET}. This amplification sets the level of input signal at which the status threshold operates. The data from the first stage is rectified and low-pass filtered before being compared with a reference voltage. The low-pass filter is formed by C_F (Figure 1-2) and R_F (on chip resistor).

With C_F equal to 10 nF the time constant is nominally 2 µs, avoiding false triggering due to variation in the edge density of the input data.

1.3.4 Setting the Signal Detect Level

R_{SET} is chosen using the graphs in Figure 2-1 to determine the input signal level at which ST goes high (Assert). The value is dependant on supply voltage and should be chosen for 3.3 V or 5 V operation. If 3.3 V and 5 V operation are to be supported interchangeably set R_{SET} based on the 3.3 V graphs.

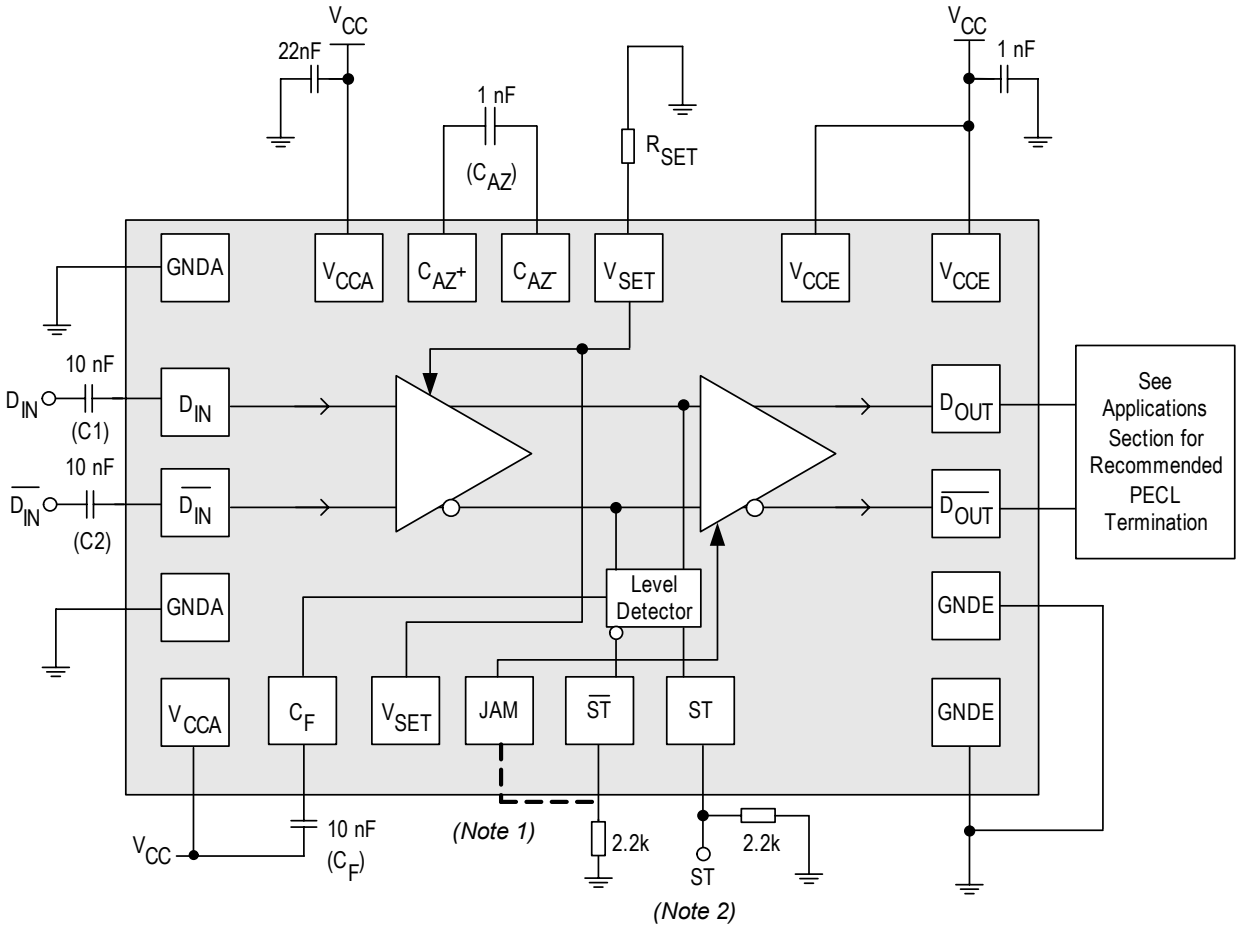
The comparator following the level detector has the equivalent of 2 dB (typical) of optical hysteresis and this determines the deassert level (ST goes LOW).

If the level detect function is not required connect V_{SET} to GndA (maximum signal gain and minimum signal detect level).

1.4 Applications

- SDH/SONET 155 Mbps Transceivers
- Fast Ethernet Receivers
- FDDI 125 Mbps Receivers
- ESCON Receivers
- FTTx and Media Converters

Figure 1-2. Typical 9 Pin Applications Circuit

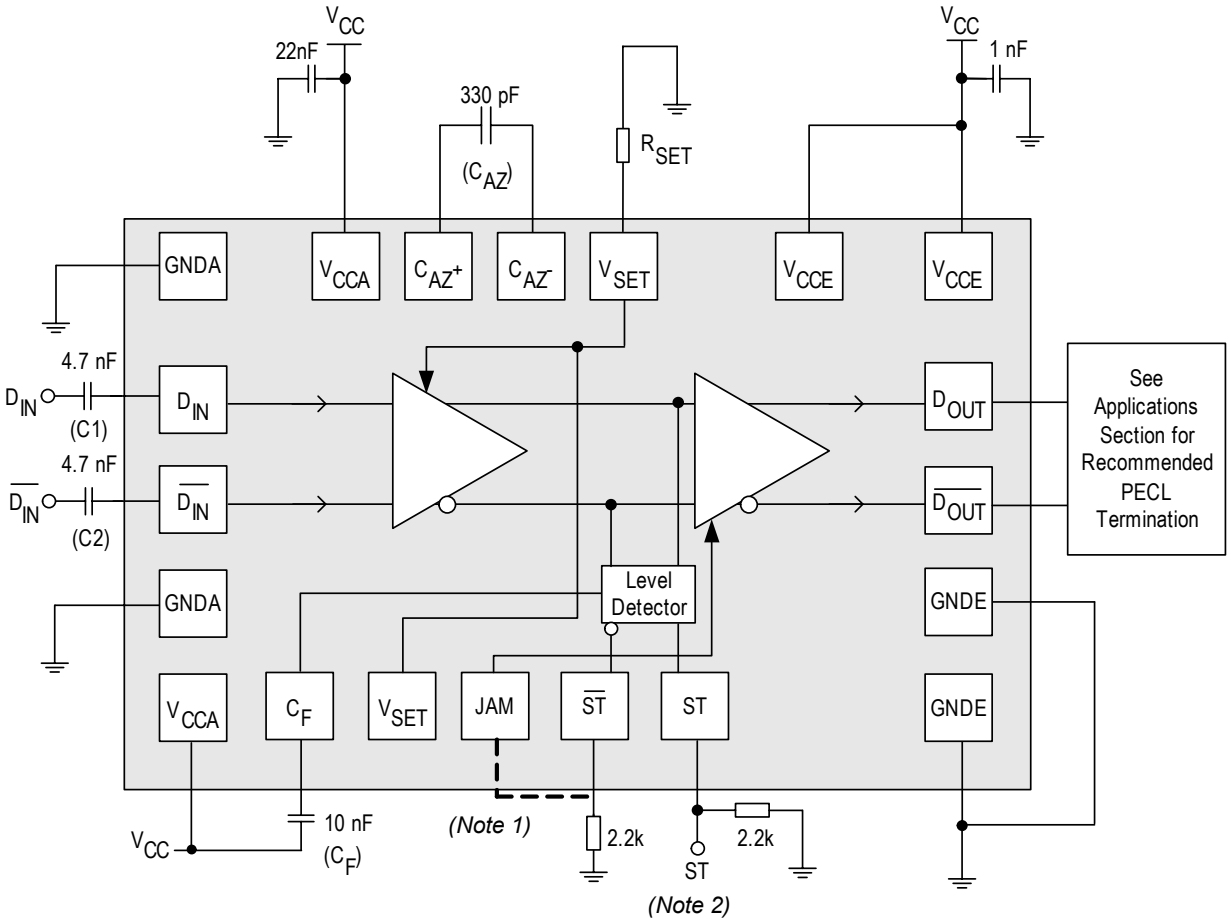


Notes:

1. Optional connection to enable JAM function.

2. Termination value chosen to reduce current consumption and provides PECL type levels. For true PECL levels proper PECL termination must be used.

Figure 1-3. Typical SFF/SFP Applications Circuit



Notes:

1. Optional connection to enable JAM function.
2. Termination value chosen to reduce current consumption and provides PECL type levels. For true PECL levels proper PECL termination must be used.

1.4.1 PECL Termination

The outputs of the MC2045-2Y are 100k/300k PECL compatible and any standard PECL AC or DC-coupling termination technique may be used. Figure 1-4 and Figure 1-5 illustrate typical AC and DC terminations.

AC-coupling is used in applications where the average DC content of the data is zero e.g. SONET. The advantage of this approach is lower power consumption, no susceptibility to DC drift and compatibility with non-PECL interfaces. Pull-down resistors ($R_{PULL-DOWN}$) provide a DC path for the emitter follower outputs to ground, keeping the ECL output transistors in their active region. Figure 1-4 shows the circuit configuration and Table 1-1 lists the resistor values. If using non-50Ω transmission lines, the shunt termination resistance Z_T should equal twice the impedance of the transmission line (Z_0).

DC-coupling can be used when driving PECL interfaces and has the advantage of a reduced component count. A Thevenin termination is used at the receive end to give a 50 Ω load and the correct DC bias. Figure 1-5 shows the circuit configuration and Table 1-1 the resistor values.

Alternatively, if available, terminating to V_{CC} – 2V as shown in Figure 1-6 has the advantage that the resistance value is the same for 3.3 V and 5 V operation and it also has performance advantages at high data rates.

Table 1-1. Termination Resistor Values

Supply	Output Impedance	$R_{Pull-down}$	Z_T	R_{TA}/R_{TB}	R_T/R_B
5 V	50 Ω	270 Ω	100 Ω	2k7 Ω/7k8 Ω	82 Ω/130 Ω
3.3 V	50 Ω	150 Ω	100 Ω	2k7 Ω/4k3 Ω	130 Ω/82 Ω

Figure 1-4. AC-coupled PECL Termination

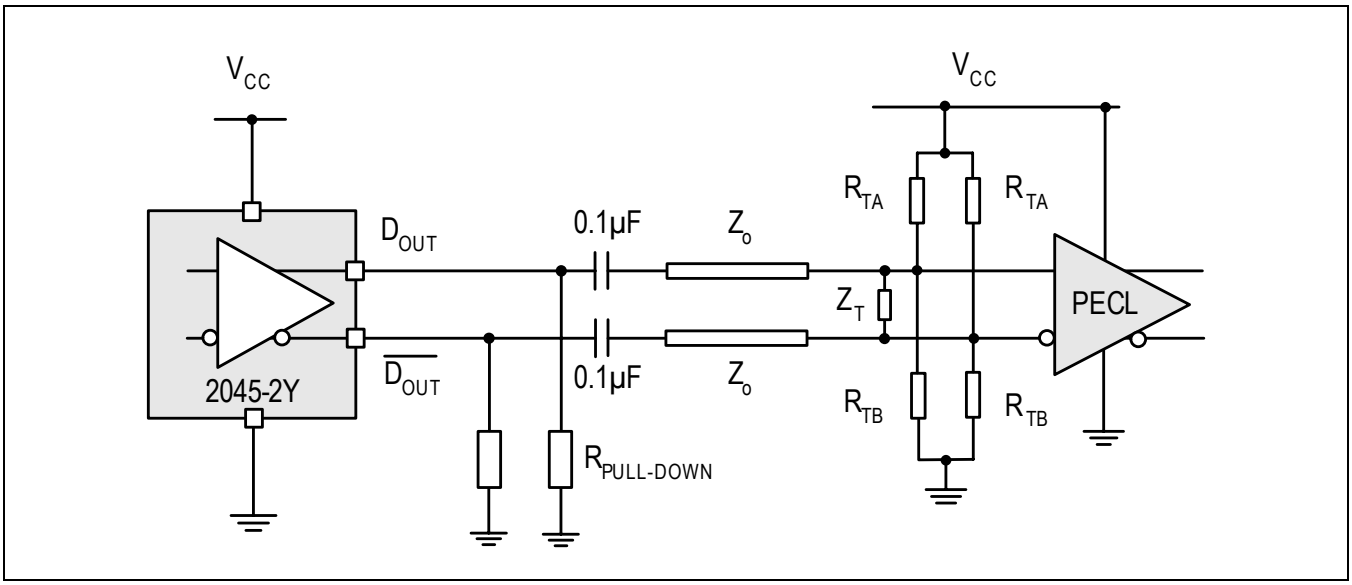


Figure 1-5. DC-coupled PECL Termination

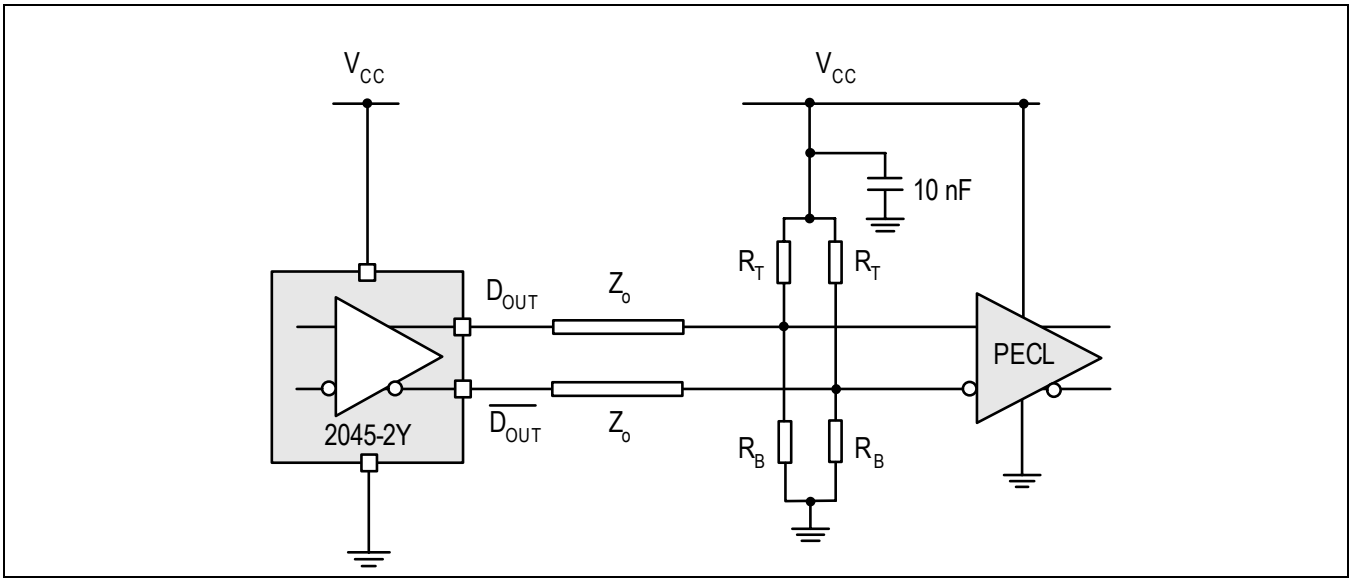
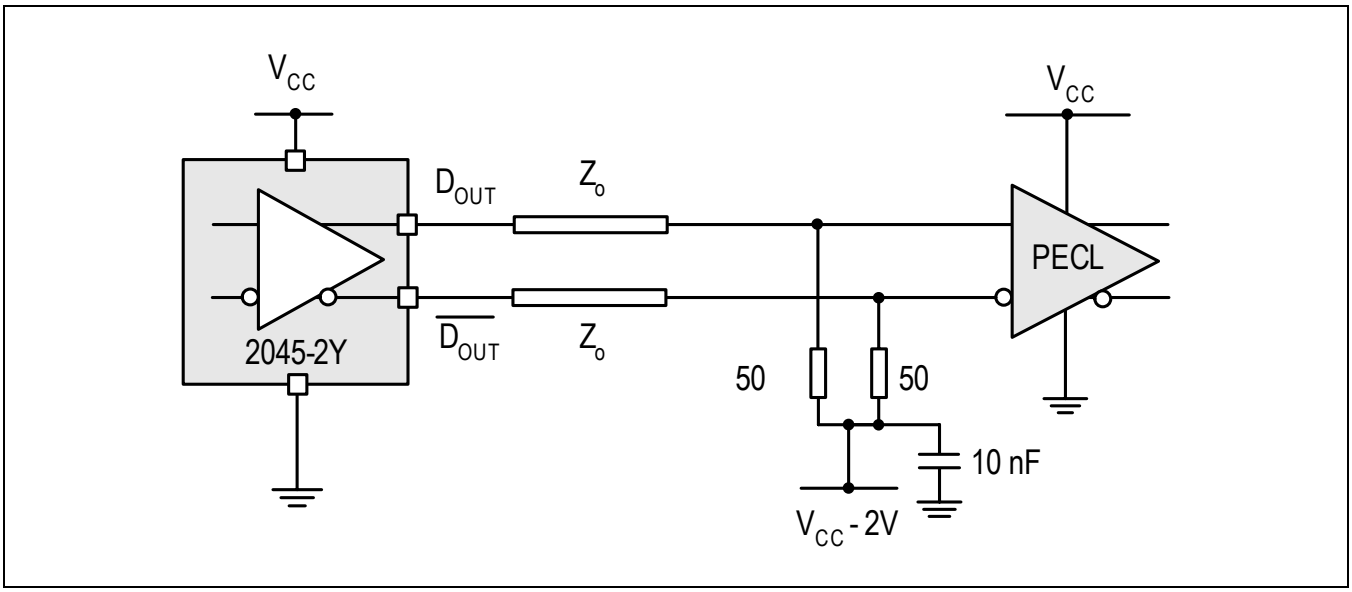


Figure 1-6. True PECL Termination



1.4.2 JAM Function

The JAM function sets the data output to a fixed state when a valid signal level is not present at the inputs (as determined by the user with R_{SET}). This is implemented by externally connecting the $\overline{ST}$ output to the JAM input.

JAM is normally used to allow data to propagate only when the signal is above the users' Bit-Error-Rate (BER) requirement. It stops the data outputs toggling due to noise when a valid signal level is not present at the inputs.

1.4.3 Power supply decoupling & optimizing sensitivity

In most applications the MC2045-2Y gives adequate performance without ferrite beads. In applications where maximum sensitivity is required $V_{CC}A$ and GNDA may be connected to their respective power rails via a ferrite suppressor, such as a Murata BLM31A601SPT.

Capacitors should be chosen with low effective series resistance, low dissipation factor and high Q. NPO or COG temperature characteristics are preferred because they provide more reliable performance over a wide range of environmental conditions.

Small surface mount packages (0603 or smaller) are recommended since they exhibit less parasitic inductance which can lower the overall effectiveness of the bypass capacitor at high frequencies. Filter capacitors should be placed close to power and ground pins to minimize noise coupling.

1.4.4 Differences between the die and packaged parts

The die has two V_{SET} pads. Connect one or the other, but not both.

There are two sets of V_{CCA} and GNDA on the left side of the die. Although two pairs are provided only one pair need be connected. On the TSSOP package, pairs of $V_{CC}E$ and GNDE pins are connected.

2.0 Product Specification

2.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Table 2-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{CC}	Power supply (V_{CC}-GND)	6	V
T_A	Operating ambient	-40 to +85	°C
T_{STG}	Storage temperature	-65 to +150	°C

2.2 Recommended Operating Conditions

Table 2-2. Recommended Operating Conditions

Symbol	Parameter	Rating	Units
V_{CC}	Power supply (V_{CC}-GND)	3.0 to 5.5	V
T_A	Operating ambient	-40 to +85	°C

2.3 DC Characteristics

(V_{CC} = +3.3V ± 10% or +5.0V ±10%, T_A = -40°C to +85°C, unless otherwise noted).

Typical Specifications are for V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

Table 2-3. DC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
I_{CC}	Supply current (outputs un-loaded) (1)	-	12.5	20	mA
V_{OS}	Effective input offset voltage (2)	-	1	-	mV
V_{TH}	Input level detect programmability	2	-	20	mVpp
HYS	Level detect hysteresis (optical)	1.8	2.0	3.0	dB
I_{INJ}	JAM input current HIGH		380		µA
V_{OH}	PECL output HIGH	V_{CC} - 1.025	-	V_{CC} - 0.880	V
V_{OL}	PECL output LOW	V_{CC} - 1.810	-	V_{CC} - 1.620	V
V_{JAM}	Jam Activation Voltage	-	V_{CC} - 1.2	-	V

Dice are designed to operate over an ambient temperature range of -40°C to +85°C (T_A), but are tested and guaranteed only at T_A = 25°C.

Notes:

1. Load is 50 Ω to V_{CC} - 2 V. Typical is 14.5 mA at V_{CC} = 5.0 V.

2. Typical is 0.5 mV at V_{CC} = 5.0 V.

2.4 AC Characteristics

(V_{CC}= +3.3 V ±10% or +5.0V ±10%, T_A = -40°C to +85°C, unless otherwise noted. Guaranteed by design and characterization).

Typical Specifications are for V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

Table 2-4. AC Characteristics

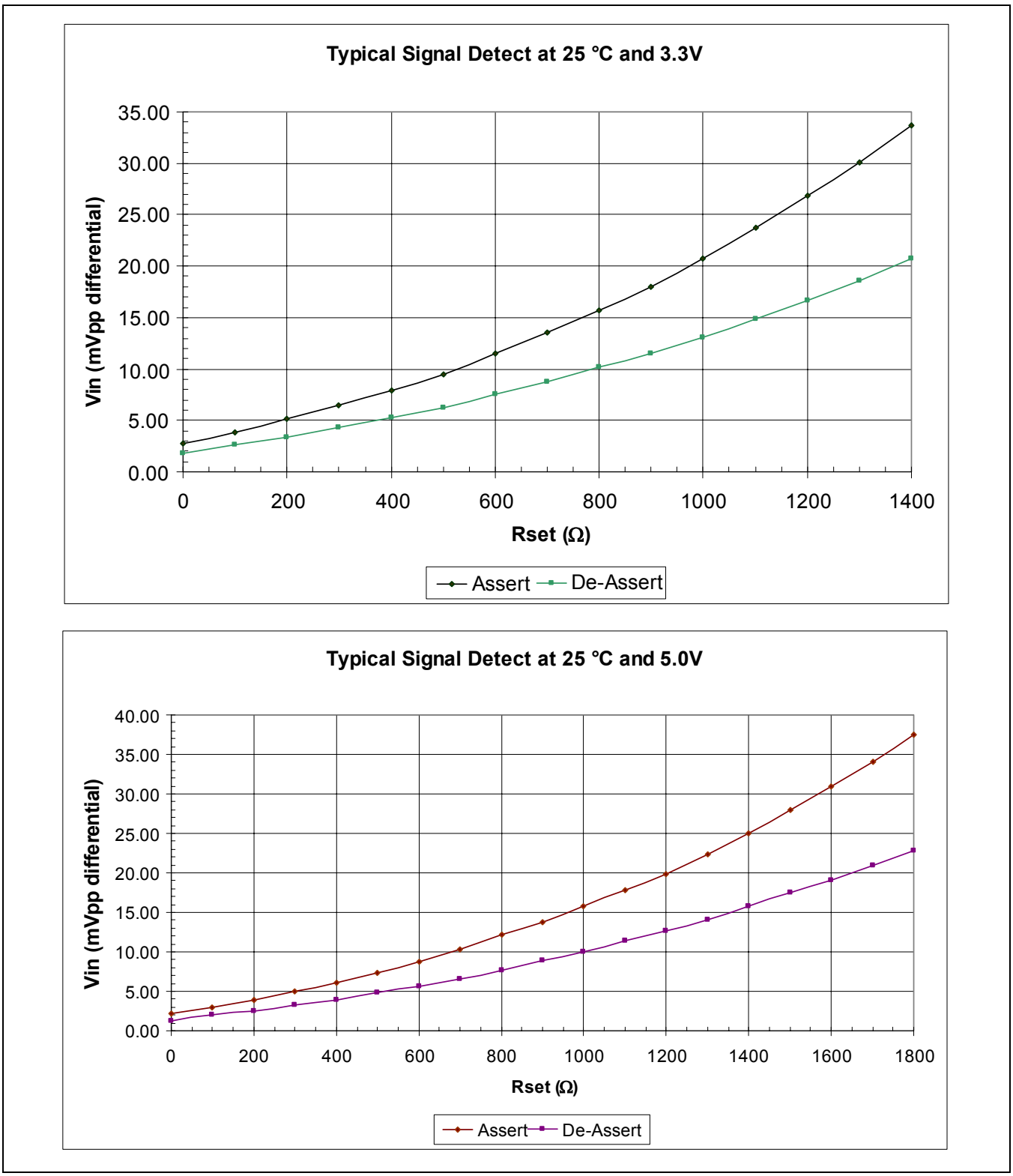
Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IN_MIN}	Differential Input sensitivity	-	1.6	2	mVpp
V_{IN_MAX}	Differential Input Overload	800	-	-	mVpp
BW	Bandwidth (where gain = 60dB)	100	250	-	MHz
R_{IN}	Input resistance	-	10	-	kΩ
C_{IN}	Input capacitance	-	-	2	pF
t_{PWD}	Pulse width distortion	-	-	0.3	ns
t_R, t_F	Data output rise/fall times (20-80%)	-	1.0	2.0	ns
R_F	Signal level detect filter resistance	10	25	41	kΩ
T_{LD}	Signal level detect time constant(1) Assert level Deassert level	0.5	 5 50	 100 100	µs
V_N	Input RMS noise in 100 MHz	-	-	85	µV

Dice are designed to operate over an ambient temperature range of -40°C to +85°C (T_A), but are tested and guaranteed only at T_A = 25°C.

Notes:

1. Using SFF/SFP typical applications circuit, Figure 1-3.

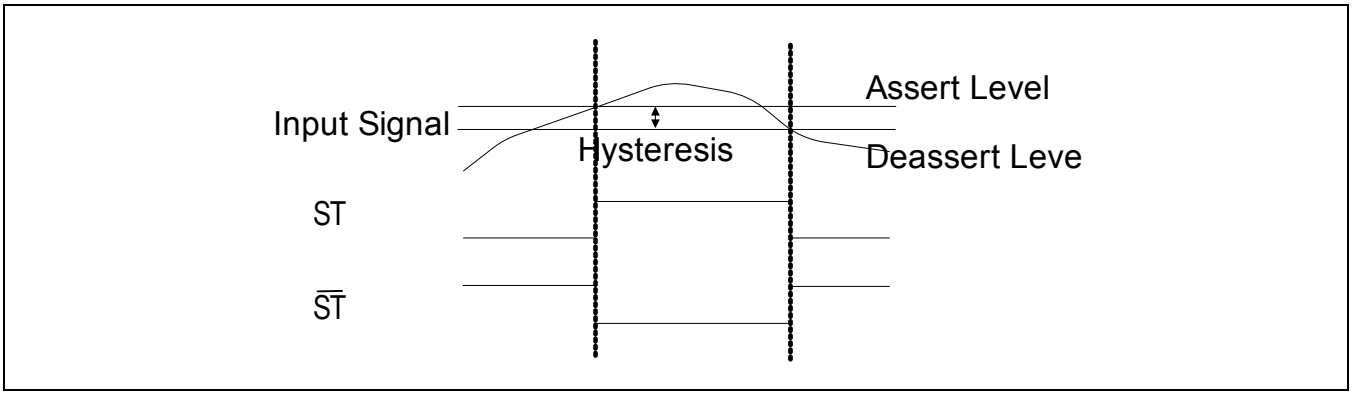
Figure 2-1. Typical Performance Curves



2.4.1 ST Assert and Deassert Level

Figure 2-1 shows the operation of the signal detect function as the signal level varies. The top line indicates the assert level, the bottom the deassert level. The difference between the two levels is the hysteresis. When the signal level goes above the assert level the ST output switches high ($\overline{ST}$ switches low). When the signal level falls below the deassert level, ST output switches low ($\overline{ST}$ switches high).

Figure 2-2. Assert and Deassert Level



2.5 Die and Package Specification

Figure 2-3. Bare Die Information

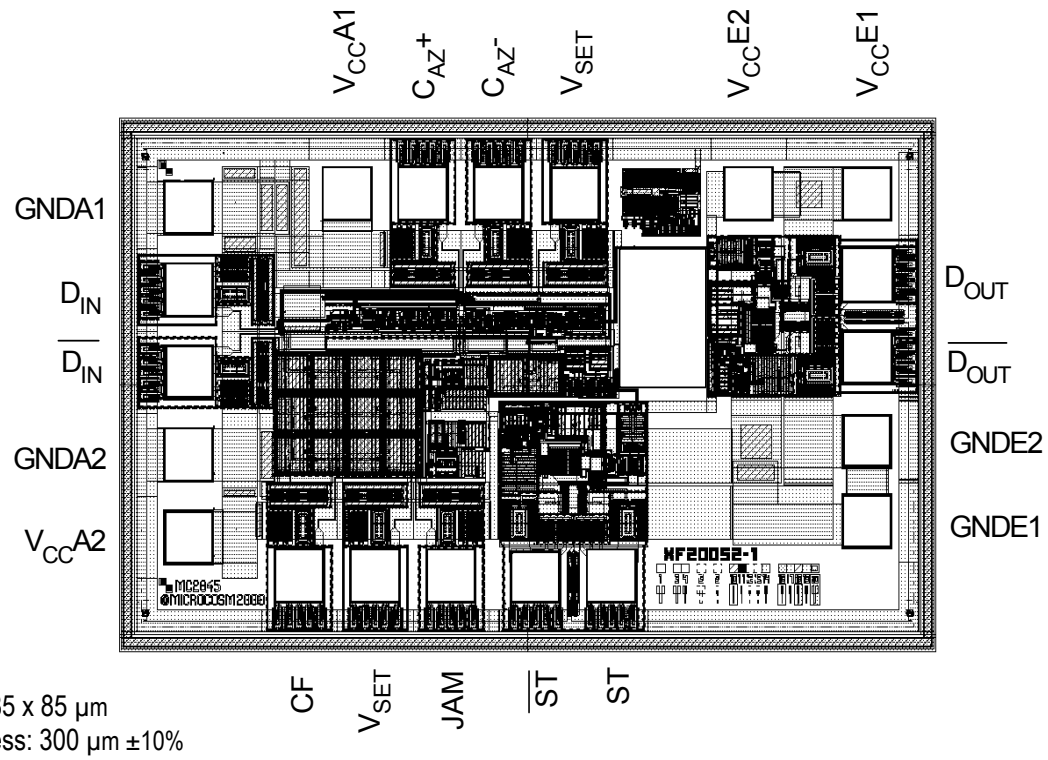


Table 2-5. Pad Centers

Description	X	Y	Description	X	Y
$C_{AZ}-$	-56.8	347.5	JAM	-152.2	-347.5
$C_{AZ}+$	-207	347.5	$\overline{ST}$	15.8	-347.5
$V_{CC}A1$	-356.9	347.5	ST	166	-347.5
GNDA1	-670	322.6	GNDE1	670	-248
D_{IN}	-670	172.6	GNDE2	670	-103
$\overline{D_{IN}}$	-670	22.4	$\overline{D_{OUT}}$	670	50.1
GNDA2	-670	-127.6	D_{OUT}	670	200.3
$V_{CC}A2$	-670	-277.5	$V_{CC}E1$	670	347.5
C_F	-451.4	-347.5	$V_{CC}E2$	436.9	347.5
V_{SET2}	-301.3	-347.5	V_{SET}	93.2	347.5

NOTE:
Pad coordinates are in µm, and are measured from the center of the die to the center of the pad.

Figure 2-4. BCC++16L Package Outline

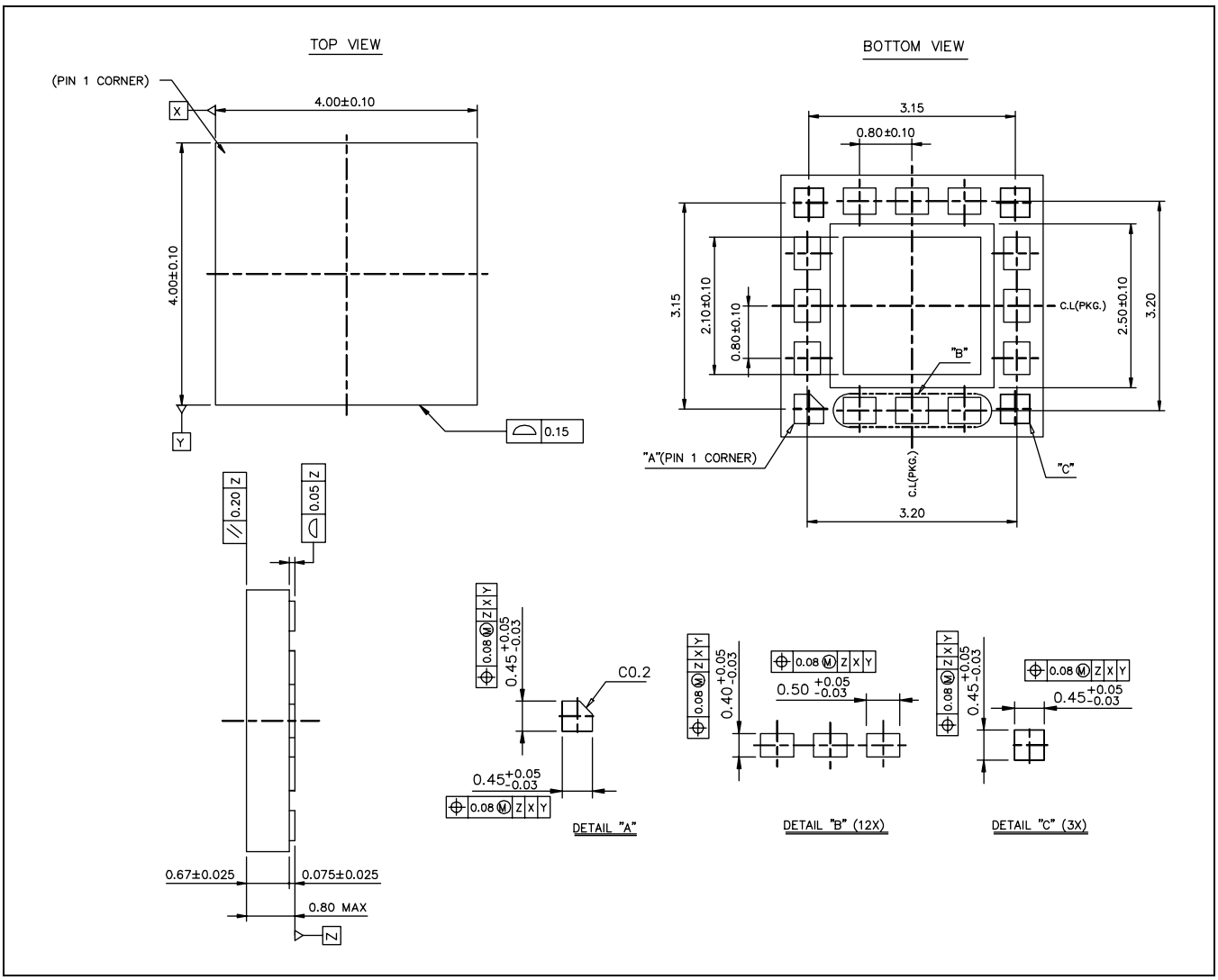
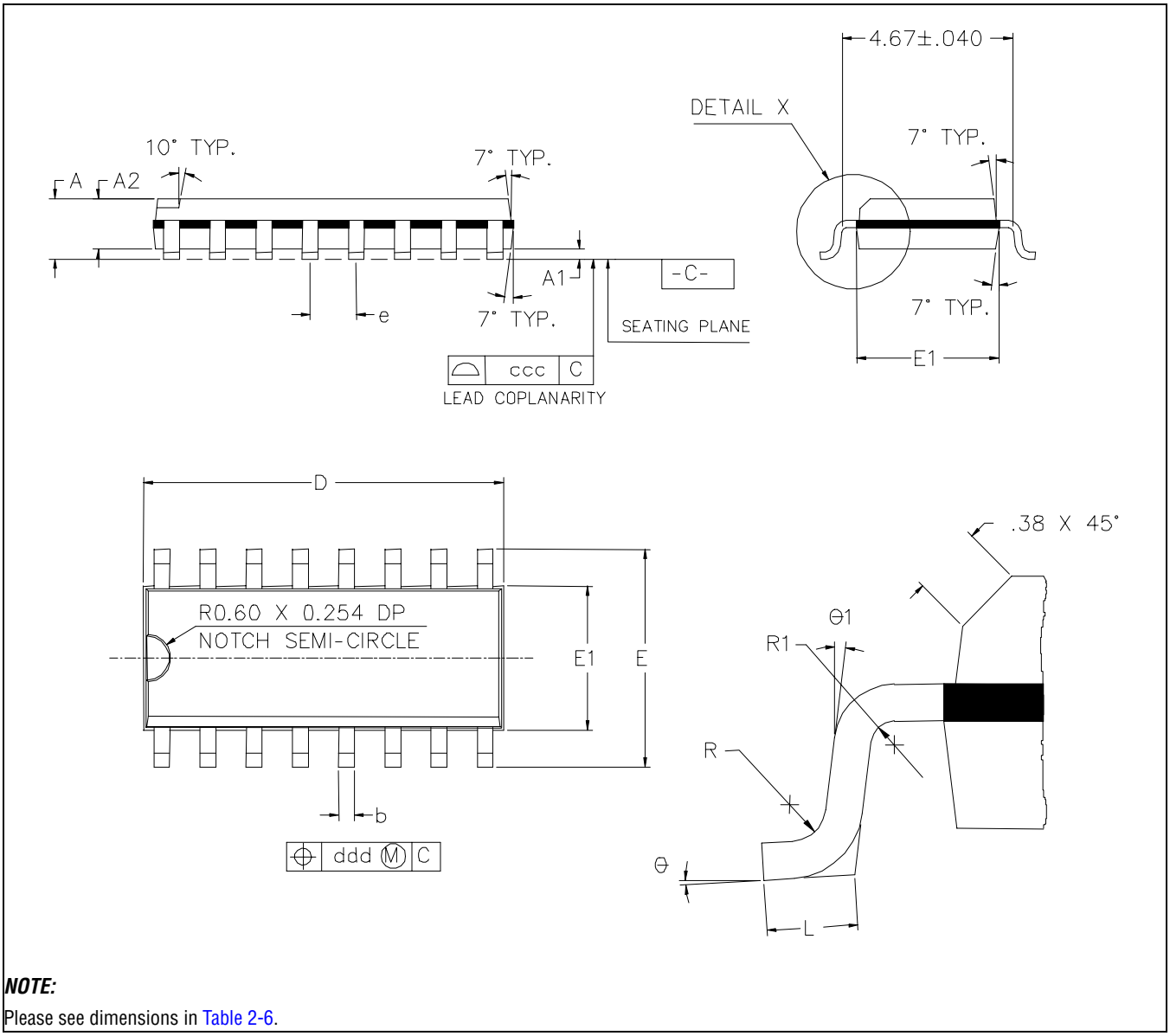


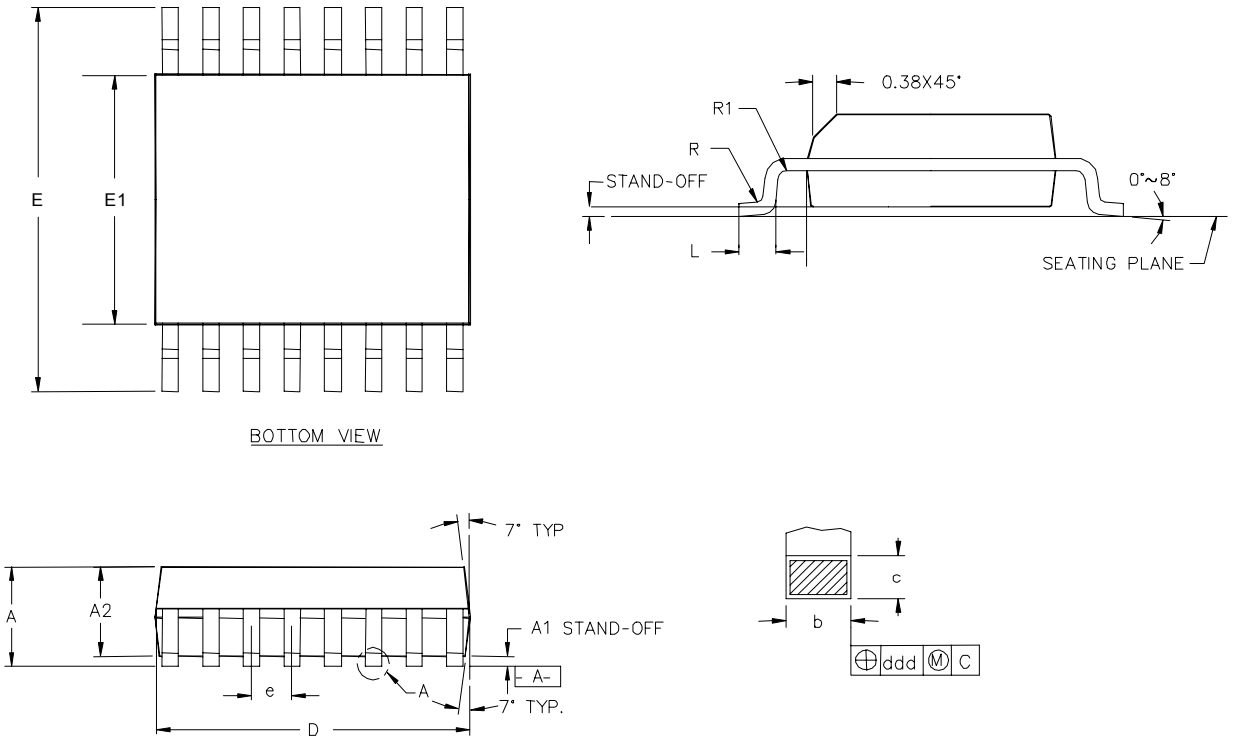
Figure 2-5. SOIC16 Package Information



NOTE:

Please see dimensions in Table 2-6.

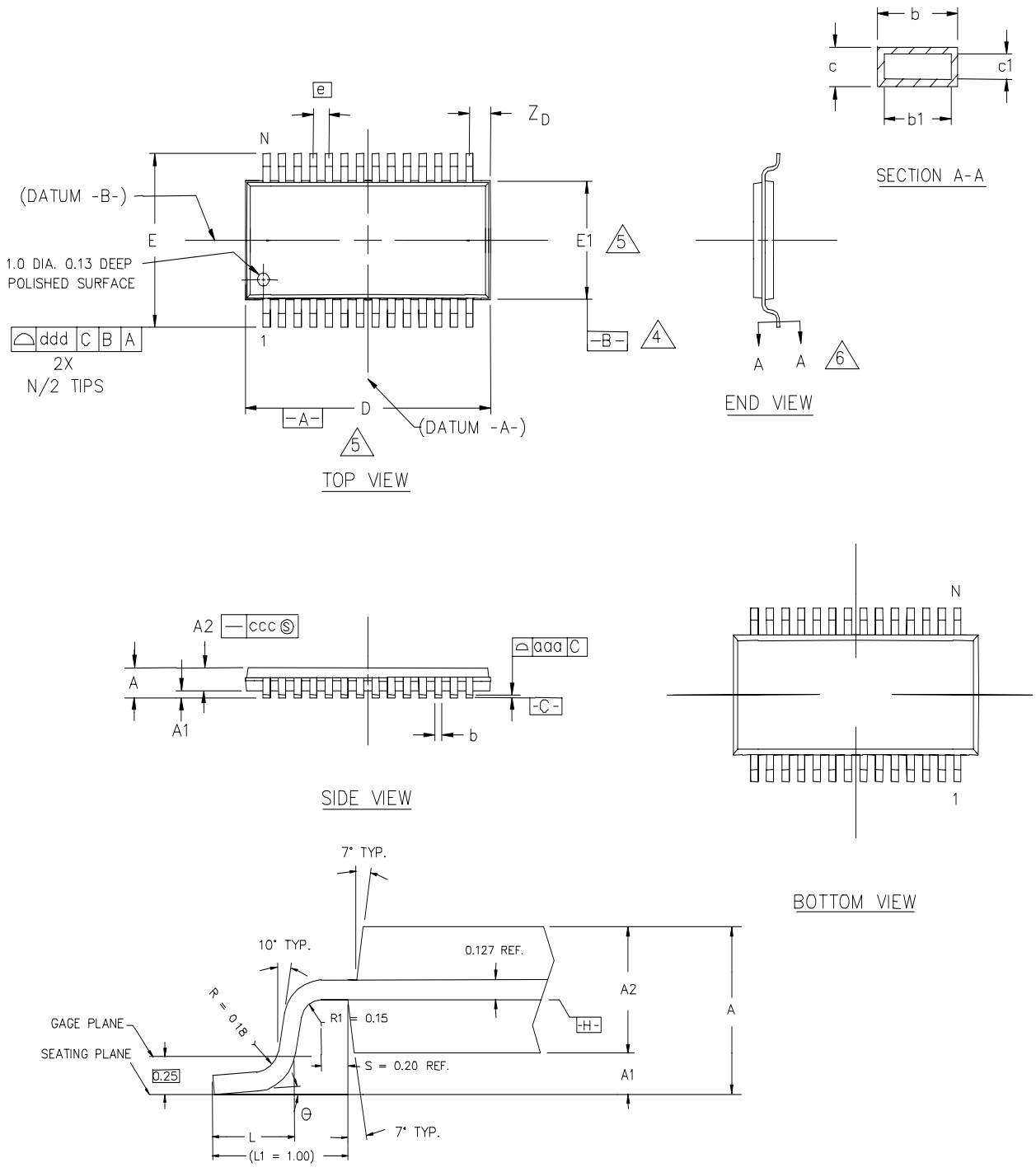
Figure 2-6. QSOP16 Package Information



NOTE:

Please see dimensions in Table 2-7.

Figure 2-7. TSSOP20 Package Information



NOTE:

Please see dimensions in Table 2-8.

Table 2-6. SOIC16 Dimensions

Symbol	Min.	Nom.	Max.
A	1.55	1.63	1.73
A1	0.127	0.15	0.25
A2	1.40	1.47	1.55
B	0.35	0.41	0.49
C	0.19	0.20	0.25
D	9.80	9.93	9.98
E	3.81	3.94	3.99
e	1.27 BSC		
H	5.84	5.99	6.20
h	0.25	0.33	0.41
L	0.41	0.64	0.89
N	16		
a	0°	5°	8°
X	2.16	2.36	2.54

Table 2-7. QSOP16 Dimensions

Symbol	Tols/N	QSOP16
A	MAX.	1.60
A1	±.05	0.1
A2	±.05	1.40
D	±.05	4.95
E	±.10	6.00
E1	±.05	3.90
L	±.15	0.60
ccc	MAX.	0.080
ddd	MAX.	0.10
e	BASIC	0.635
b	±.025	0.224
c	±.02	0.22
R	±.05	0.25
R1	Min.	0.20

Table 2-8. TSSOP20 Dimensions

Symbol	Tols/leads	TSSOP20L
A	MAX	1.20
A1		0.5MIN/.10MAX.
A2	NOM	.90
D	±.05	6.50
E	±.10	6.40
E1	±.10	4.40
L	+.15/-.10	.60
L1	REF.	1.00
Zp	REF.	.325
e	BASIC	.65
b	±.05	.22
c		.13MIN/.20MAX
e	±4°	4°
aaa	MAX.	.10
bbb	MAX.	.10
ccc	MAX	.05
ddd	MAX.	.20

2.6 Package Pinout Description

Figure 2-8. Connections

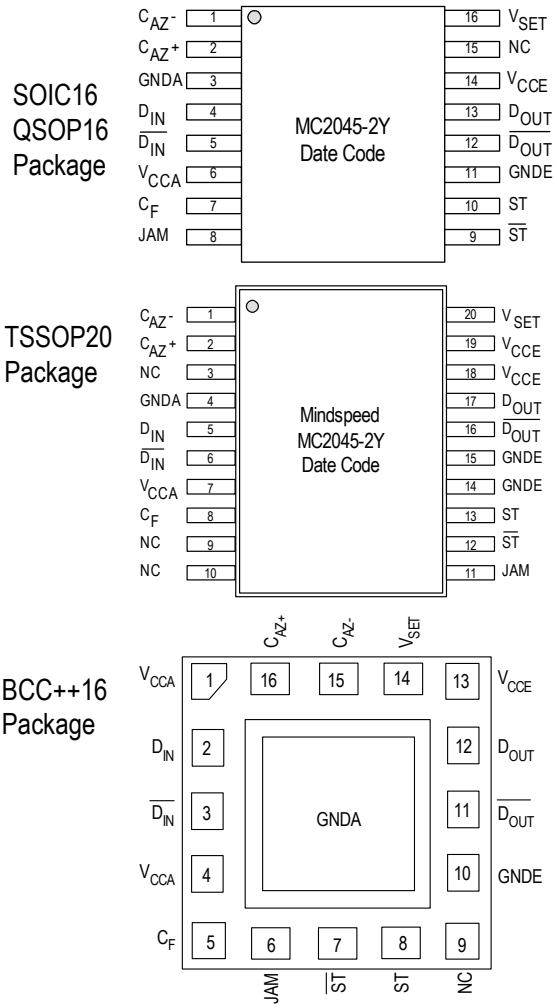


Table 2-9. Pin Description

Pin Name	QSOP16 SOIC16 Pin No.	TSSOP20 Pin No.	BCC++16L Pin No	Function
C_{AZ}-	1	1	15	Auto-zero capacitor pin. Connect C_{AZ} between this pin and C_{AZ}+
C_{AZ}+	2	2	16	Auto-zero capacitor pin. Connect C_{AZ} between this pin and C_{AZ}-
GNDA	3	4	-	Analog section ground pin. Connect to most negative supply.Must be at the same potential as GNDE pin
D_{IN}	4	5	2	Differential data input
$\overline{D_{IN}}$	5	6	3	Inverse differential data input
V_{CCA}	6	7	1, 4	Analog section power pin. Connect to most positive supply.Must be at the same potential as V_{CC}E pin
C_F	7	8	5	Level-detect filter capacitor pin. Connect a capacitor between this pin and V_{CC}A
JAM	8	11	6	PECL compatible input controlling output buffers (D_{OUT} and D_{OUT} pins). On chip 10 kΩ pull down defaults to low. Can be driven from CMOS
$\overline{ST}$	9	12	7	Logical inverse of ST pin. Maybe connected to JAM pin to enable automatic squelch function to operate PECL output
ST	10	13	8	Input signal level status. This PECL output is LOW when the input signal is below the threshold set by the users
GNDE	11	14, 15	10	Digital section ground pin, Connect to the most negative supply. Must be the same potential as GNDA pin
$\overline{D_{OUT}}$	12	16	11	Differential data output. Logical inverse of D_{OUT} pin. JAM high forces $\overline{D_{OUT}}$ High
D_{OUT}	13	17	12	Differential data output. PECL compatible differential data output. JAM high forces D_{OUT} LOW
V_{CCE}	14	18, 19	13	Digital output section power pin. Connect the most positive supply. Must be at same potential as V_{CCA} pin
NC	15	3, 9, 10	9	Not connected
V_{SET}	16	20	14	Input threshold-level setting circuit. Connect to GND via a resistor

NOTE:
Pin 17 (center pin) on the BCC++16 package should be connected to GndA.

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