High Performance Registered Schottky—4-Bit-Wide Generic PROM Family 53/63RAXXX, 53/63RSXXX

Features/Benefits

- Largest generic PROM family available incorporating "D"
- Advanced Schottky processing.
- 4-bit-wide in 18 and 20 pin Skinny DIPs™ for high board density.
- Synchronous enable allow easy busing of outputs for word expansion.
- Lower system package counts.
- Lower system power.
- Faster cycle times.
- 25ns clock to output a 40ns address set-up times guaranteed over commercial specification.
- 24mA output drive capability.

Applications

- Pipelined microprogramming
- State sequencers
- Next address generation
- Mapping PROM

Description

A family of registered PROMs offers new savings for designers of pipelined microprogrammable systems. The wide instruction register, which holds the microinstruction during execution, is now incorporated into the PROM chip.

Edge Triggered Register

The PROM output is loaded into a 4-bit register on the rising edge of the clock. The use of the term "register" is to be distinguished from the term "latch," in that a register contains master slave flipflops and the latch contains gated flip-flops. The advantages of using a register are that system timing is simplified, and faster micro cycle times can be obtained.

The output of the register is buffered by three-state drivers which are compatible with the new low-power Schottky three-state bus standard, i.e., I_{OL} is 24mA at V_{OL} of 0.5V.

The 4-bit-wide family in 18-pin and 20-pin packages feature either synchronous or asynchronous enables the synchronous enables and upwards pin compatibility. The synchronous enable powers up in the high impedance state and is used when more than one registered PROM is bused together to increase word length. All devices are specified over both commercial and military temperature ranges.

5V Supply

High Performance Generic PROM Selection Guide

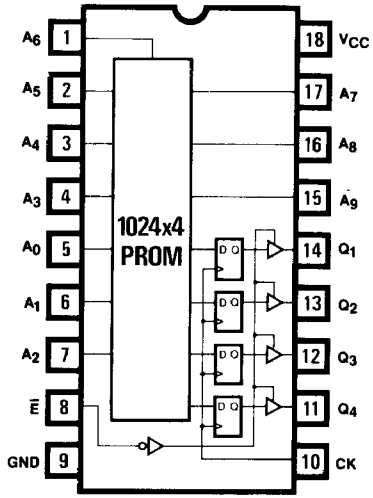
MEMORY			PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION		PINS	TYPE	0°C to 75°C	−55°C to 125°C
4K	1024x4	ASYN	18	J,N,F	~~63RA441~~	~~53RA441~~
		SYN			63RS441	53RS441
8K	2048x4	ASYN	20	J,N	63RA841*	~~53RA841~~*
		SYN			63RS841*	~~53RS841~~*
16K	4096x4	ASYN	20	J,N	40 ~~63RA1641~~*✓	~~53RA1641~~*✓
		SYN			41 63RS1641*✓	~~53RS1641~~*✓

*~~Preliminary~~ Data
Note: This is not a final specification. Some limits of characteristics are subject to change.

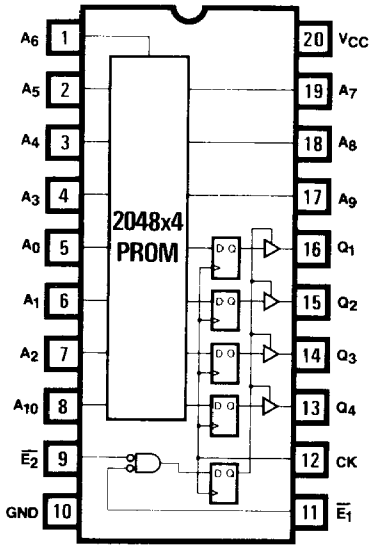
™ Skinny DIP is a trademark of Monolithic Memories

Pin Configurations

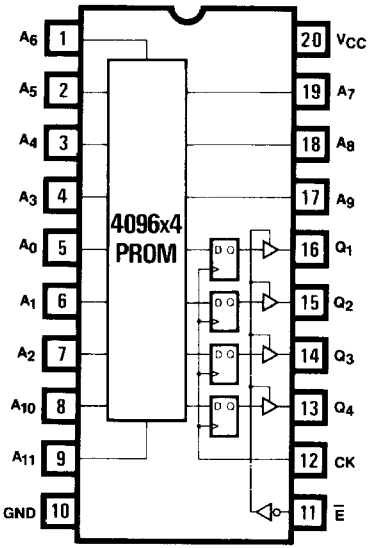
53/63RA441



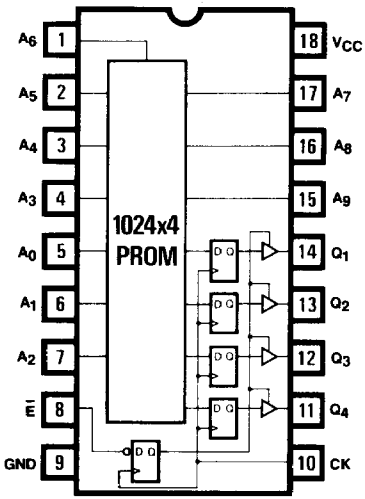
53/63RA841



53/63RA1641



53/63 RS441



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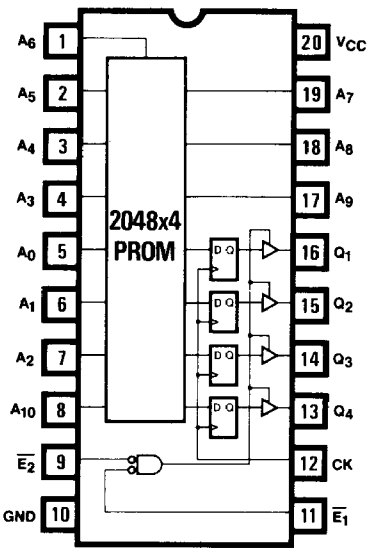

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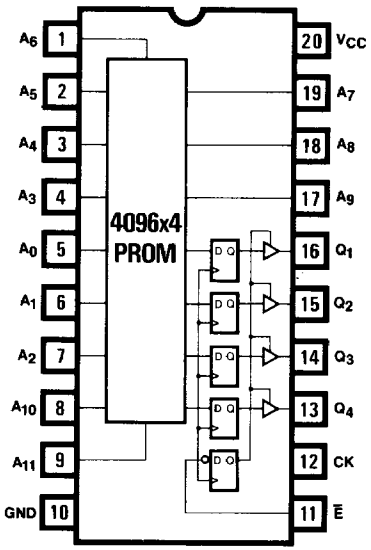

Absolute Maximum Ratings

	Operating	Program
Supply voltage V_{CC}	−.5V to 7V	12V
Input voltage	−1.5V to 5.5V	12V
Off-state output voltage	−1.5V to 5.5V	12V
Storage temperature	−65°C to 150°C	

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			−2.0	2.4		−6.5	mA
I_{OL}	Low-level output current			16			24	mA
T_A	Operating free air temperature	−55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Free Air Tempeature Range

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage			2.0		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.8	V
V_{IC}	Input clamp voltage	V_{CC} = MIN, I_I = −18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = MAX		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = MAX				0.5	V
I_{OZH}	Off-state output current high-level voltage applied	V_{CC} = MAX, V_{IH} = 2V, V_O = 2.4V				100	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC} = MAX, V_{IH} = 2V, V_O = 0.4V				−100	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	High-level input current	V_{CC} = MAX. V_I = 2.4V				25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				−250	μA
I_{OS}	Short-circuit output current	V_{CC} = MAX		−30		−100	mA
C_I	Input capacitance	V_{CC} = 5.0V, f = 1 MHz	V_I = 2.0V		4	10	pF
C_O	Output capacitance	T_A = 25°C	V_O = 2.0V		6	12	pF
I_{CC}	Supply current 441,	V_{CC} = MAX	All inputs GND All outputs open		125	180	mA
	Supply current 841, 1641				130		

Switching Characteristics

Min/Max = Over Recommended Ranges of T_A and V_{CC}
Typ = 5.0V V_{CC}, 25°C T_A

SYMBOL	PARAMETER	DEVICE TYPE	MILITARY (53')			COMMERCIAL (63')		
			MIN	TYP	MAX	MIN	TYP	MAX
t_{pd}	Clock to output	(All)		18	30		18	25
t_{su}	Address set-up	RA441	45	30		40	30	
		RA841		35			35	
		RS1641		45			45	
		RS441	45	30		40	30	
		RS841		35			35	
		RS1641		45			45	
t_h	Address hold	(All)	0	−5		0	−5	
t_{pzx}	$\overline{E}$ to output enable	(All "RA")		15	30		15	25
t_{pxz}	$\overline{E}$ to output disable	(All "RA")		15	30		15	25
t_{pzx}	CK to output enable	(All "RS")		25	40		25	35
t_{pxz}	CK to output disable	(All "RS")		25	40		25	35
t_{su}	Enable set-up	(All "RS")	20	10		15	10	
t_h	Enable hold	(All "RS")	0	−5		0	−5	
t_w	Pulse width	(All)	20	12		20	12	
MAX	Maximum Clock frequency	RS/RA 441	25	24		25	33	
		RS/RA 841		29			33	
		RS/RA1641		25			25	

(See "Definition of Terms and Waveforms")