FEATURES

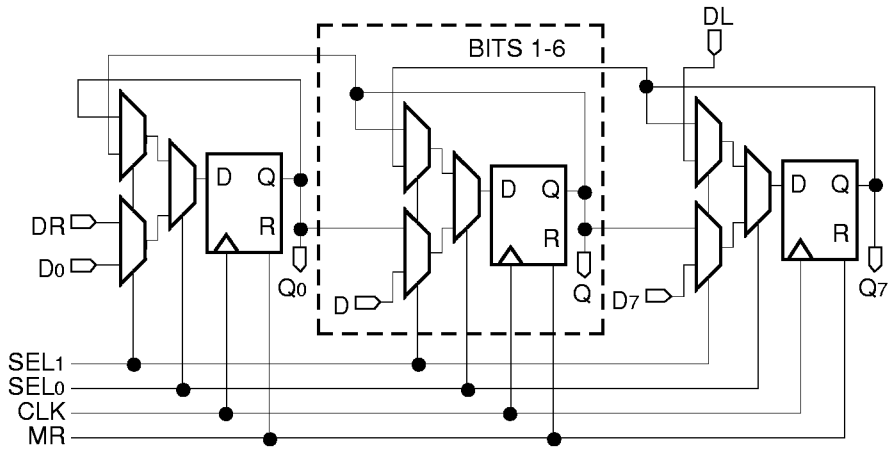
- **700MHz min. shift frequency**
- **Extended 100E V_{EE} range of –4.2V to –5.5V**
- **8 bits wide**
- **Bi-directional**
- **Four selectable modes for full functionality**
- **Asynchronous Master Reset**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Internal 75KΩ input pulldown resistors**
- **ESD protection of 2000V**
- **Fully compatible with Motorola MC10E/100E141**
- **Pin-compatible with E241**
- **Available in 28-pin PLCC package**

DESCRIPTION

The SY10/100E141 are 8-bit, full-function shift registers designed for use in new, high-performance ECL systems. The E141 performs serial/parallel in and serial/parallel out, shifting in either direction. The eight inputs D_0–D_7 accept parallel input data, while DL/DR accept serial input data for left/right shifting.

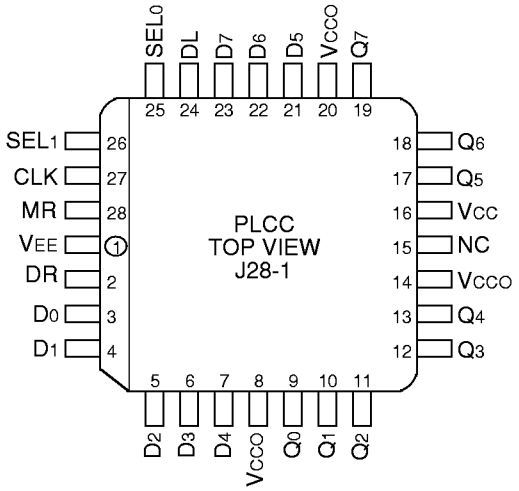
The two select pins, SEL_0 and SEL_1 permit four modes of operation: Load, Hold, Shift Left and Shift Right, as shown in the Truth Table. Input data is clocked into the register on the rising clock edge after meeting the minimum set-up time. A logic HIGH on the Master Reset (MR) pin asynchronously resets all the registers to zero.

BLOCK DIAGRAM



Rev.: C Amendment: /1
Issue Date: February, 1998

PIN CONFIGURATION



PIN NAMES

Pin	Function
D_0-D_7	Parallel Data Inputs
DL, DR	Serial Data Inputs
SEL_0, SEL_1	Mode Select Inputs
CLK	Clock
Q_0-Q_7	Data Outputs
MR	Master Reset
V_{CCO}	V_{CC} to Output

TRUTH TABLE

Function	DL	DR	SEL_0	SEL_1	MR	CLK	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Load	X	X	L	L	L	Z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Shift Right	X	L	L	H	L	Z	L	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6
	X	H	L	H	L	Z	H	L	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5
Shift Left	L	X	H	L	L	Z	L	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	L
	H	X	H	L	L	Z	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	L	H
Hold	X	X	H	H	L	Z	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	L	H
	X	X	H	H	L	Z	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	L	H
Reset	X	X	X	X	H	X	L	L	L	L	L	L	L	L

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current									mA	—	
	10E	—	131	157	—	131	157	—	131	157		
	100E	—	131	157	—	131	157	—	151	181		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{SHIFT}	Max. Shift Frequency	700	900	—	700	900	—	700	900	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay to Output CLK MR	 625 600	 750 725	 975 975	 625 600	 750 725	 975 975	 625 600	 750 725	 975 975	ps	—
t_S	Set-up Time D SEL_0 SEL_1	 175 350 300	 25 200 150	 — — —	 175 350 300	 25 200 150	 — — —	 175 350 300	 25 200 150	 — — —	ps	—
t_H	Hold Time D SEL_0 SEL_1	 200 100 100	 –25 –200 –150	 — — —	 200 100 100	 –25 –200 –150	 — — —	 200 100 100	 –25 –200 –150	 — — —	ps	—
t_{RR}	Reset Recovery Time	900	700	—	900	700	—	900	700	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{skew}	Within-Device Skew	—	60	—	—	60	—	—	60	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	300	525	800	300	525	800	300	525	800	ps	—

NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E141JC	J28-1	Commercial
SY10E141JCTR	J28-1	Commercial
SY100E141JC	J28-1	Commercial
SY100E141JCTR	J28-1	Commercial

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)