

## Signetics

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FAST Products	

## FEATURES

- Synchronous, reversible 4-bit-counting
- Asynchronous parallel load capability
- Asynchronous reset (clear)
- Cascadable without external logic

## DESCRIPTION

The 74F192 and 74F193 are 4-bit synchronous Up/Down Counters. The 74F192 counts in BCD mode and 74F193 counts in the binary mode. Separate up/down clocks,  $CP_U$  and  $CP_D$ , respectively simplify operation. The outputs change state synchronously with the Low-to-High transition of either clock input. If the  $CP_U$  clock is pulsed while  $CP_D$  is held High, the device will count up. If the  $CP_D$  clock is pulsed while  $CP_U$  is held High, the device will count down. The device can be cleared at any time by the asynchronous reset pin. It may also be loaded in parallel by activating the asynchronous parallel load pin. Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, asynchronous preset, load, and synchronous count up and count down functions. Each flip-flop contains JK feedback from slave to master such that a Low-to-High transition on the  $CP_D$  input will decrease the count by one, while a similar transition on the  $CP_U$  input will advance the count by one. One clock should be held High while counting with the other, because the circuit will either count by twos or not at all depending on the state of the first JK flip-flop, which cannot toggle as long as either clock input is Low. Applications requiring reversible operation must make the reversing decision while the activating clock is High to avoid erroneous counts. The terminal count up ( $TC_U$ ) and terminal count down ( $TC_D$ ) outputs are normally High. When the circuit has

# FAST 74F192, 74F193 Counters

'F192 Up/Down Decade Counter With Separate Up/Down Clocks  
'F193 Up/Down Binary Counter With Separate Up/Down Clocks

TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F192	125MHz	32mA
74F193	125MHz	32mA

## ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE
	$V_{CC} = 5V \pm 10\%$ ; $T_A = 0^\circ C$ to $+70^\circ C$
16-Pin Plastic Dip	N74F192N, N74F193N
16-Pin Plastic SO	N74F192D, N74F193D

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$D_0 - D_3$	Data inputs	1.0/1.0	20 $\mu$ A/0.6mA
$CP_U$	Count up clock input (active rising edge)	1.0/3.0	20 $\mu$ A/1.8mA
$CP_D$	Count down clock input (active rising edge)	1.0/3.0	20 $\mu$ A/1.8mA
$\overline{PL}$	Asynchronous parallel load control input (active Low)	1.0/1.0	20 $\mu$ A/0.6mA
MR	Asynchronous Master Reset input	1.0/1.0	20 $\mu$ A/0.6mA
$Q_0 - Q_3$	Flip-flop outputs	50/33	1.0mA/20mA
$TC_U$	Terminal count up (carry) output (active Low)	50/33	1.0mA/20mA
$TC_D$	Terminal count down (borrow) output (active Low)	50/33	1.0mA/20mA

### NOTE:

One (1.0) FAST Unit Load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

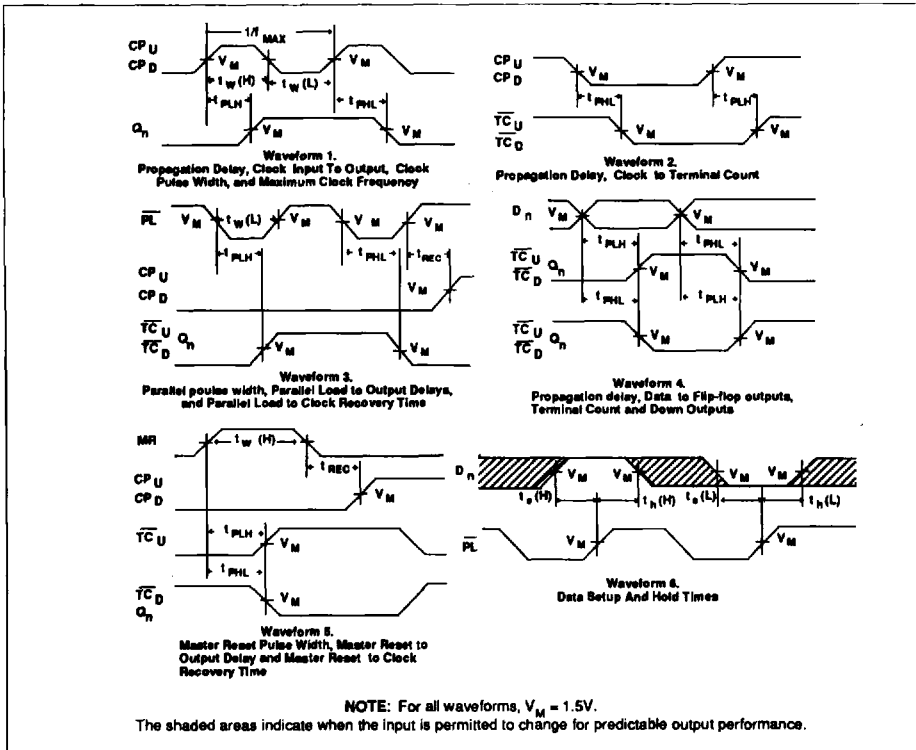
reached the maximum count state (9 for the 'F192 and 15 for the 'F193), the next High-to-Low transition of  $CP_U$  will cause  $TC_U$  to go Low.  $TC_U$  will stay Low until  $CP_U$  goes High again, duplicating the count up clock, although delayed by two gate delays. Likewise, the  $TC_D$  output will go Low when the circuit is in the zero state and  $CP_D$  goes Low. The  $TC$  outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous since there is a two-gate delay time difference added for each stage that is

added. The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs ( $D_0 - D_3$ ) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs when the Parallel Load ( $\overline{PL}$ ) input is Low. A High level on the Master Reset (MR) input will disable the parallel load gates, override both clock inputs, and sets all Q outputs Low. If one of the clock inputs is Low during and after a reset or load operation, the next Low-to-High transition of the clock will be interpreted as legitimate signal and will be counted.

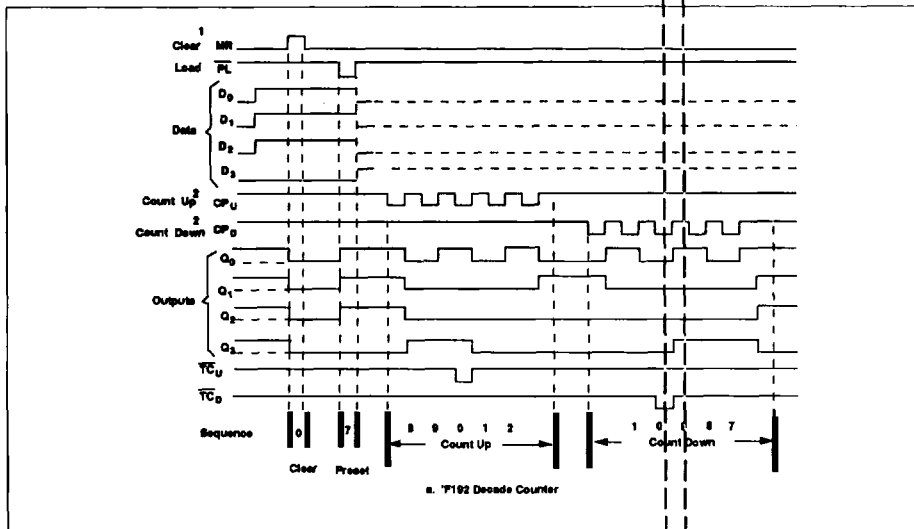
Counters

FAST 74F192, 74F193

AC WAVEFORMS



TIMING DIAGRAM (Typical clear, load, and count sequence ) for 'F192



- NOTES:**
1. Clear overrides load data and count inputs.
  2. When counting up, count down input must be High; when counting down, count up must be High.