
HN62W4416 Series

1048576-word × 16-bit/2097152-word × 8-bit CMOS Mask
Programmable ROM

HITACHI

ADE-203-469(Z)
Preliminary
Rev. 0.0
Nov. 20, 1995

Description

The HN62W4416 is a 16-Mbit CMOS mask-Programmable ROM organized either as 1048576 words by 16 bits or 2097152 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 150 ns (max) is the most suitable to the system using a high speed micro-computer by 16 bits.

Feature

- Low voltage operation Mask ROM
Single 3.3 V supply
- High speed
Access time: 150 ns (max)
- Low power
Active: 216 mW (max)
Standby: 108 μ W (max)
- Byte-wide or word-wide data organization (Switched by BHE terminal)
- Three-state data output for or-tying
- Directly LVTTL compatible
All inputs and outputs

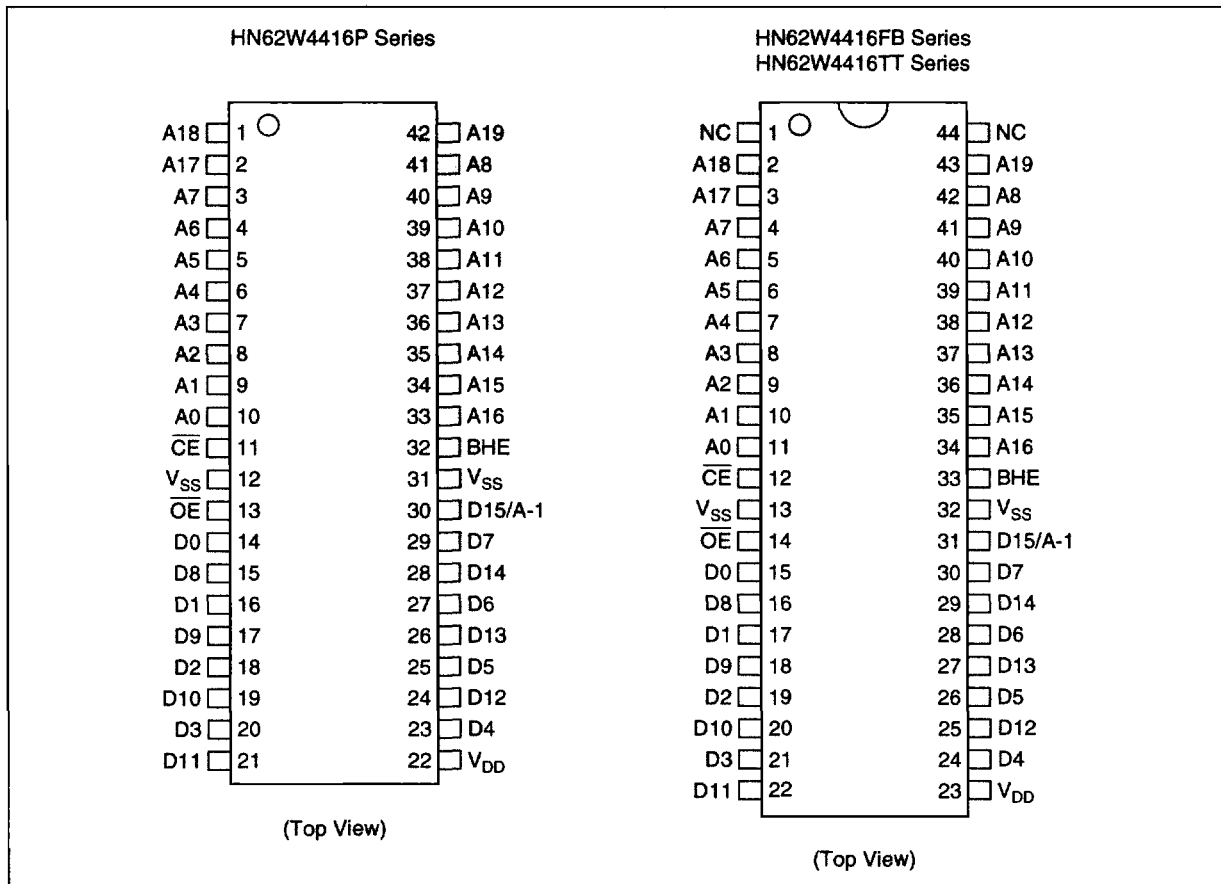
Ordering Information

Type No.	Access time	Package
HN62W4416P-15	150 ns	600 mil 42-pin plastic DIP (DP-42)
HN62W4416FB-15	150 ns	600 mil 44-pin plastic SOP (FP-44D)
HN62W4416TT-15	150 ns	400 mil 44-pin plastic TSOP II (TTP-44D)

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

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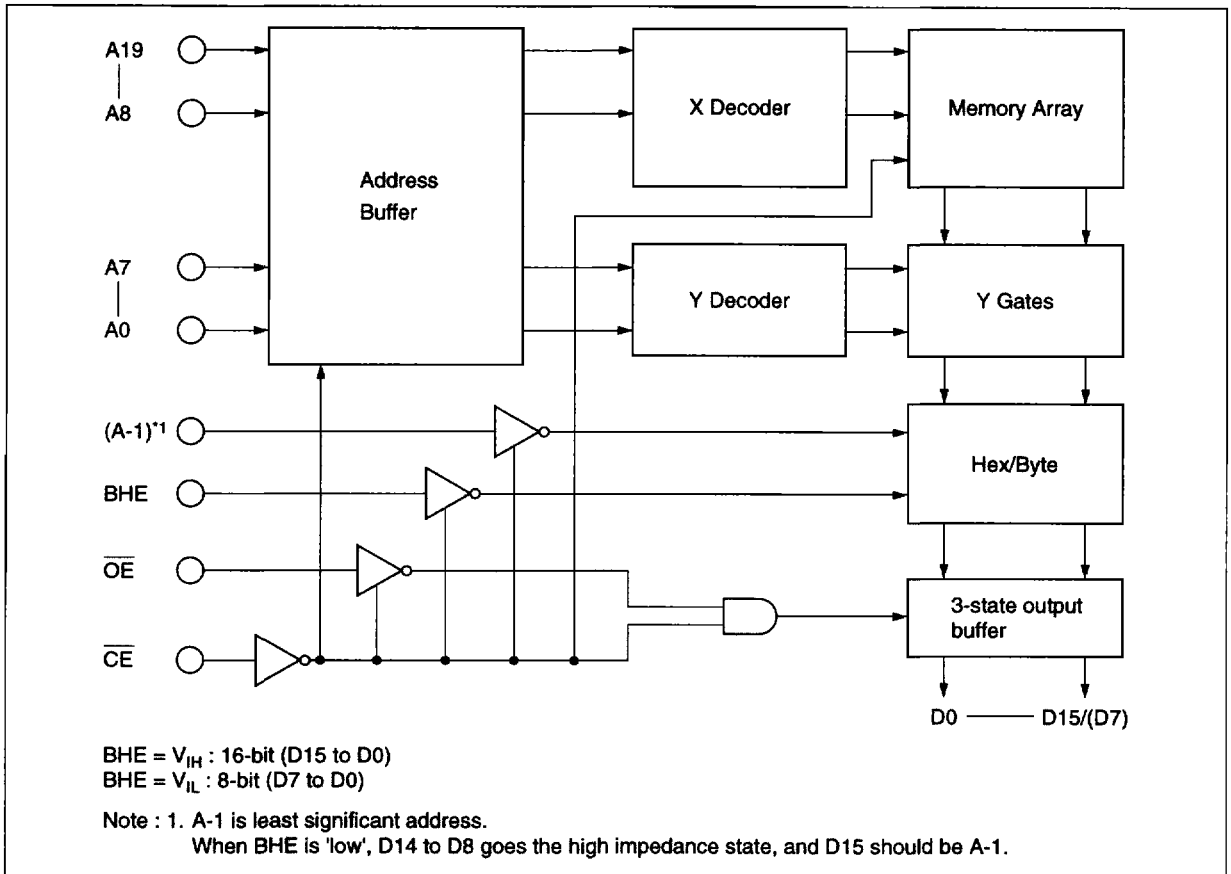
Pin Arrangement



Pin Description

Pin name	Function
A-1, A0 to A19	Address inputs
D0 to D15	Data outputs
BHE	8/16 bit (byte/word) mode switch
\overline{CE}	Chip enable
\overline{OE}	Output enable
NC	No connection
V_{DD}	Power supply
V_{SS}	Ground

Block Diagram



Mode Selection

Mode	Pin				Data output		Address input	
	\overline{CE}	\overline{OE}	BHE	D15/A-1	D0-D7	D8-D15	LSB	MSB
Standby	H	\times^1	\times	\times	High-Z ²	High-Z	—	—
Output disable	L	H	\times	\times	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A19
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A19
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A19

Notes: 1. \times : Don't care.
 2. High-Z: High impedance

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage ¹⁾	V_{DD}	-0.3 to +5.5	V
All input and output voltage ¹⁾	V_{in}, V_{out}	-0.3 to $V_{DD} + 0.3$	V
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	-55 to +125	°C
Temperature under bias	T_{bias}	-20 to +85	°C

Note: 1. With respect to V_{SS} .

Recommended DC Operating Conditions ($T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	$V_{DD} + 0.3$	V
	V_{IL}	-0.3	—	0.8	V

DC Characteristics ($V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	Min	Max	Unit	Test conditions
Supply current	Active I_{DD}	—	60	mA	$V_{DD} = 3.6\text{ V}$, $I_{DOUT} = 0\text{ mA}$, $t_{RC} = 150\text{ ns}$
	Standby I_{SB1}	—	30	μA	$V_{DD} = 3.6\text{ V}$, $\overline{CE} \geq V_{DD} - 0.2\text{ V}$
	Standby I_{SB2}	—	3	mA	$V_{DD} = 3.6\text{ V}$, $\overline{CE} \geq 2.2\text{ V}$
Input leakage current	$ I_{IL} $	—	10	μA	$V_{in} = 0$ to V_{DD}
Output leakage current	$ I_{OL} $	—	10	μA	$\overline{CE} = 2.2\text{ V}$, $V_{out} = 0$ to V_{DD}
Output voltage	V_{OH}	2.4	—	V	$I_{OH} = -2.0\text{ mA}$
	V_{OL}	—	0.4	V	$I_{OL} = 2.0\text{ mA}$

Capacitance ($V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = 25^\circ\text{C}$, $V_{in} = 0\text{ V}$, $f = 1\text{ MHz}$)

Parameter	Symbol	Min	Max	Unit
Input capacitance ¹⁾	C_{in}	—	10	pF
Output capacitance ¹⁾	C_{out}	—	15	pF

Note: 1. This parameter is sampled and not 100% tested. D15/A-1 pin is output.

AC Characteristics ($V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_a = 0 \text{ to } +70^\circ\text{C}$)

- Output load: 1TTL + $C_L = 100 \text{ pF}$ (including jig)
- Input pulse level: 0.4 to 2.4 V
- Input and output timing reference level: 1.4 V
- Input rise and fall time: 5 ns

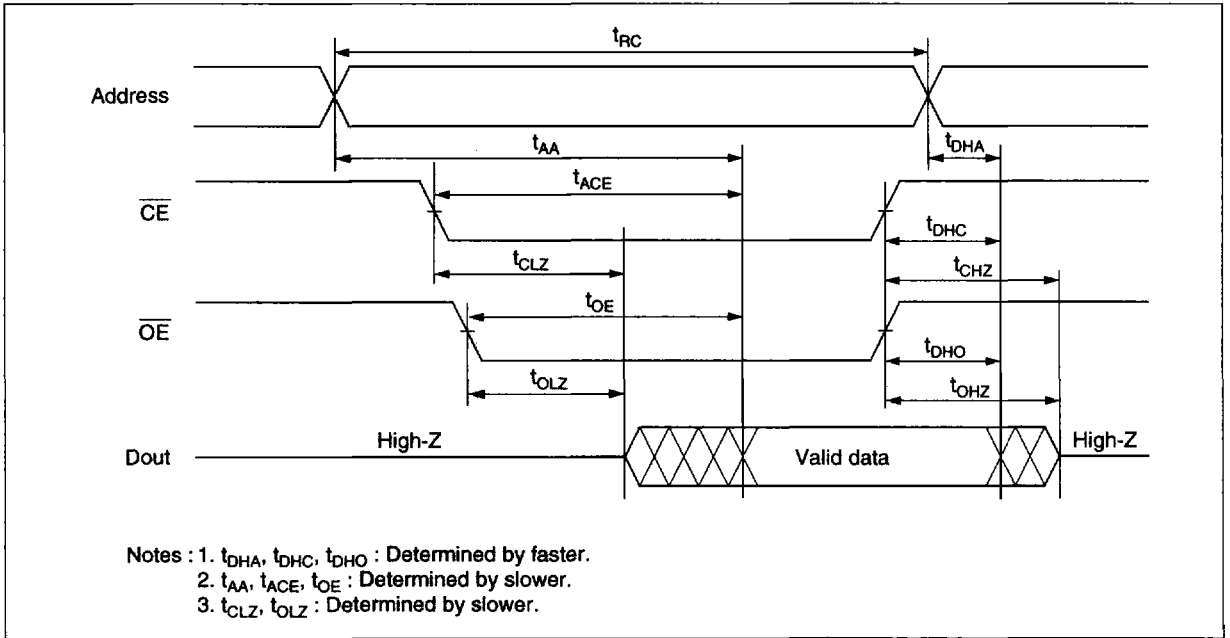
Parameter	Symbol	HN62W4416-15		Unit	Note
		Min	Max		
Read cycle time	t_{RC}	150	—	ns	
Address access time	t_{AA}	—	150	ns	
\overline{CE} access time	t_{ACE}	—	150	ns	
\overline{OE} access time	t_{OE}	—	50	ns	
BHE access time	t_{BHE}	—	150	ns	
Output hold time from address change	t_{DHA}	5	—	ns	
Output hold time from \overline{CE}	t_{DHC}	0	—	ns	
Output hold time from \overline{OE}	t_{DHO}	0	—	ns	
Output hold time from BHE	t_{DHB}	0	—	ns	
\overline{CE} to output in high-Z	t_{CHZ}	—	50	ns	1
\overline{OE} to output in high-Z	t_{OHZ}	—	50	ns	1
BHE to output in high-Z	t_{BHZ}	—	30	ns	1
\overline{CE} to output in low-Z	t_{CLZ}	5	—	ns	
\overline{OE} to output in low-Z	t_{OLZ}	5	—	ns	
BHE to output in low-Z	t_{BLZ}	5	—	ns	

Note: 1. t_{CHZ} , t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

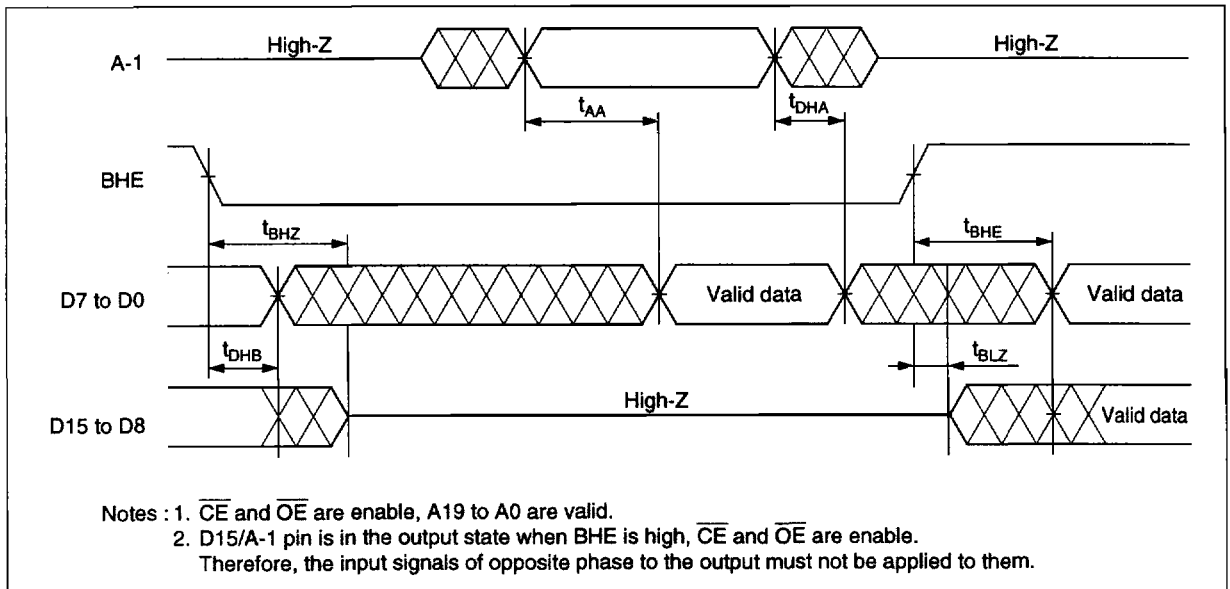
HN62W4416 Series

Timing Waveforms

Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



Word Mode, Byte Mode Switch



Power Up Sequence

