CXG1114EN

Description

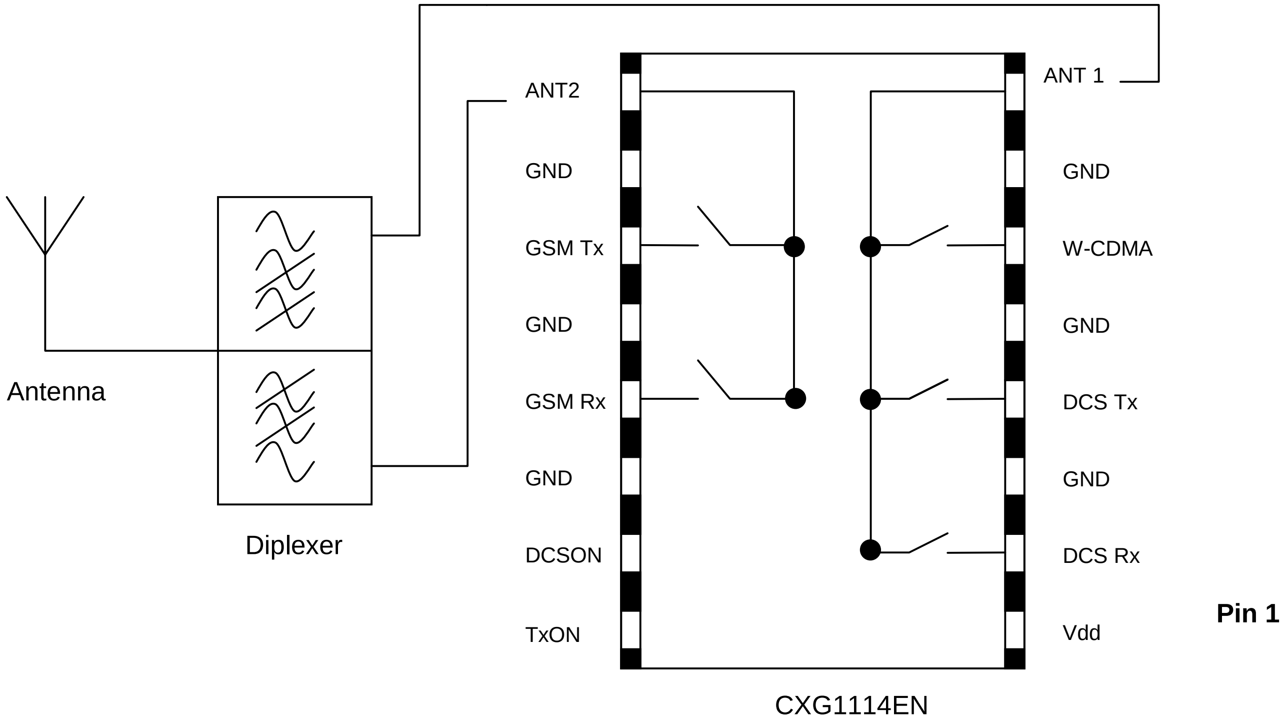
The CXG1114EN is one of a range of **low insertion loss**, high power MMIC antenna switches for Dualmode GSM/UMTS, GSM/GPRS Dualband (CXG1121TN) and Tripleband (CXG1122EN) applications. The low insertion loss on transmit means **increased talk time** as the Tx power amplifier can be operated at a lower output level. **On chip logic** reduces component count and **simplifies PCB layout** by allowing direct connection of the switch to digital baseband control lines with **CMOS logic levels**.

In this switch, one antenna port is routed to a Tx port and an Rx port (SPDT). These are typically used for GSM900. Another antenna port is routed to a Tx port, an Rx port, and a third port that can be used for both Tx and Rx (SP3T). This is typically used for DCS1800 and WCDMA. It requires 2 CMOS control lines (Tx ON/OFF and DCS ON/OFF).

The **Sony GaAs JFET** process is used for low insertion loss.

An evaluation PCB is available.

Pin Out and Block Diagram



Features

- Low transmit insertion loss 0.5dB typical GSM Tx, 0.8dB typical DCS and WCDMA.
- 2 CMOS compatible Control Lines
- Low second harmonic <-36dBm typical at 34dBm (GSM 900)
- Small package Size: VSON-16 pin (2.7mm x 3.5mm x 0.9mm)

Version 2.3 *Date 14/05/01*

Applications

Dualmode Handsets using
GSM900/DCS1800/WCDMA.

Structure

GaAs J-FET MMIC

GaAs MMIC's are ESD sensitive devices. Special handling precautions are required. The IC will be damaged in the range from 100V to 200V @200pF.0.Ω and below 500V @ 100pF 1500Ω The actual ESD test data will be available later.

Truth Table

Mode	Signal Path	DCSON	TxON
WCDMA/GSM Rx	ANT1-WCDMA	L	L
	ANT2-GSM Rx		
GSM TX	ANT1-isolated	L	H
	ANT2-GSM Tx		
DCS Rx	ANT1-DCS Rx	H	L
	ANT2-isolated		
DCS Tx	ANT1-DCS Tx	H	H
	ANT2-isolated		

Electrical Characteristics

(Ta= +25ºC)

	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion Loss	IL	GSM Tx – ANT2	* 1		0.5	0.7	dB
		DCS Tx – ANT1	* 2		0.8	1.0	dB
		WCDMA - ANT1	* 3		0.8	1.0	dB
		ANT2 – GSM Rx	* 4		0.6	0.8	dB
		ANT1 – DCS Rx	* 5		0.9	1.1	dB
		ANT1-WCDMA	* 6		0.9	1.1	dB
VSWR	VSWR				1.2		
Isolation**	Iso	GSM Tx to GSM Rx	* 1	19	22		dB
		GSM Tx to either DCS Rx or WCDMA			50		
		DCS Tx to either DCS Rx or WCDMA	* 2	15	18		dB
		DCS Tx to GSM Rx			35		
		WCDMA to DCS Rx	* 3	15	18		dB
		WCDMA to GSM Rx			31		
P_{1dB} Compression Input Power	P_{1dB}	GSM Tx – ANT2	* 1		36		dBm
		DCS Tx – ANT1	* 2		34		dBm
		WCDMA – ANT1	* 3		32		dBm
Harmonics***	2fo 3fo	GSM Tx – ANT2	* 1		-40 -34	-36 -30	dBm
	2fo 3fo	DCS Tx – ANT1	* 2		-40 -34	-36 -30	dBm
ACPR		WCDMA – ANT1	* 3		TBD		dB
Control Current	I_{ctl}		Vctl=3V		80	120	µA
Supply Current	I_{DD}		Vdd=5V		0.5	TBD	mA
			Vdd=3V		0.35	TBD	mA

Electrical characteristics are measured with all RF ports terminated in 50 Ohms.

** In the application, isolation of the SPDT block from the SP3T block will depend upon the diplexer used when connecting pins ANT1 and ANT2 to a common antenna.

***** Harmonics measured with Tx inputs harmonically matched. We recommend the use of harmonic matching to ensure optimum performance.**

* 1 Power incident on GSM Tx, Pin =34dBm, 880 to 915 MHz,Vdd=5.0V, GSM Tx enabled

* 2 Power incident on DCS Tx, Pin =32dBm, 1710 to 1785 MHz, Vdd=5.0V, DCS Tx enabled

* 3 Power incident on WCDMA, Pin =27dBm, 1920 to 1980 MHz, Vdd=3.0V, WCDMA enabled

* 4 Power incident on ANT2, Pin =10dBm, 925 to 960 MHz, Vdd=3.0V, GSM Rx enabled

* 5 Power incident on ANT1, Pin = 10dBm, 1805 to 1880 MHz, Vdd=3.0V, DCS Rx enabled

* 6 Power incident on ANT1, Pin = 10dBm, 2110 to 2170 MHz, Vdd=3.0V, WCDMA enabled

The worst case values given in this specification are based on those obtained for previous similar products. Sony anticipate that these values will be close to the true worst case values for the CXG1114EN which will be found later through measurement of process variants.

Supply Voltage value (Vdd):

Mode	Minimum	Typical	Maximum
GSM/DCS Tx	4.5V	5V	5.7V
GSM/DCS Rx, WCDMA	TBD	3V	4V

CMOS logic value (Vctl):

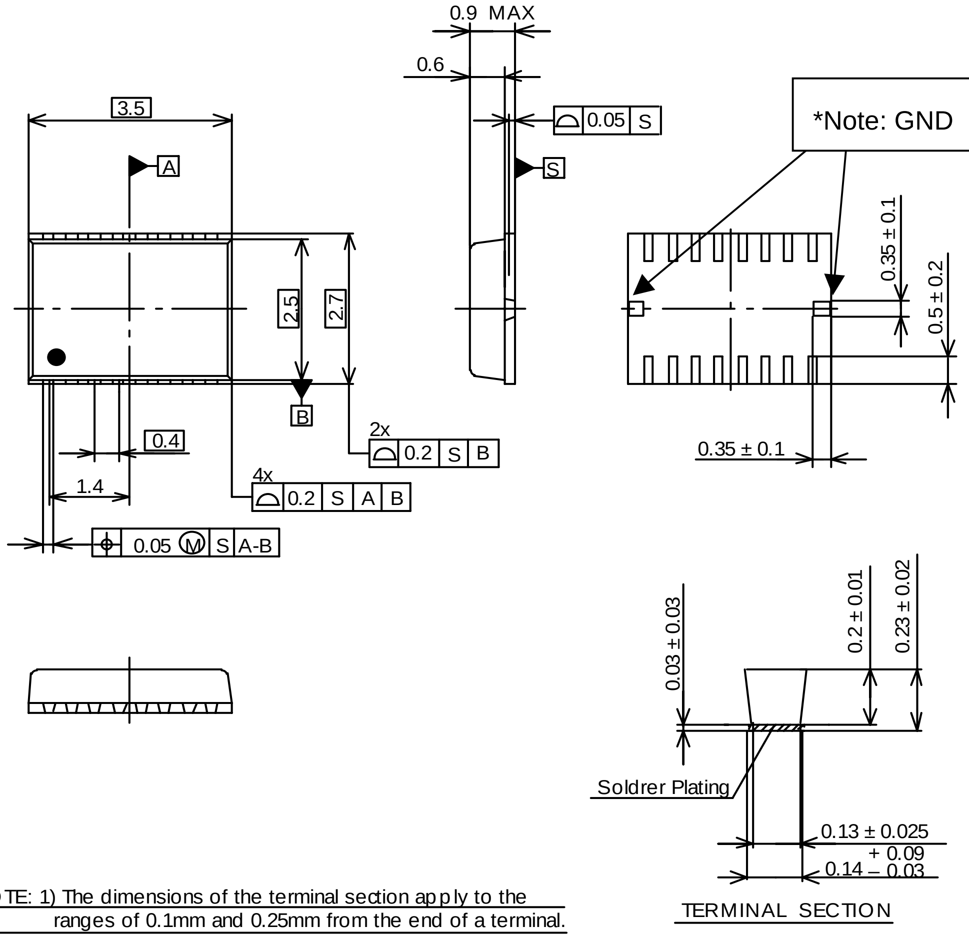
	Minimum	Typical	Maximum
High	2.4V	2.8 V	3.2V
Low	0V		0.4V

Absolute Maximum Ratings (Ta = 25°C)

- Bias Voltage Vdd 7V
- Control Voltage Vctl 5V
- Operating Temperature -20°C to +80°C

Package Outline

16PIN VSON(PLASTIC)



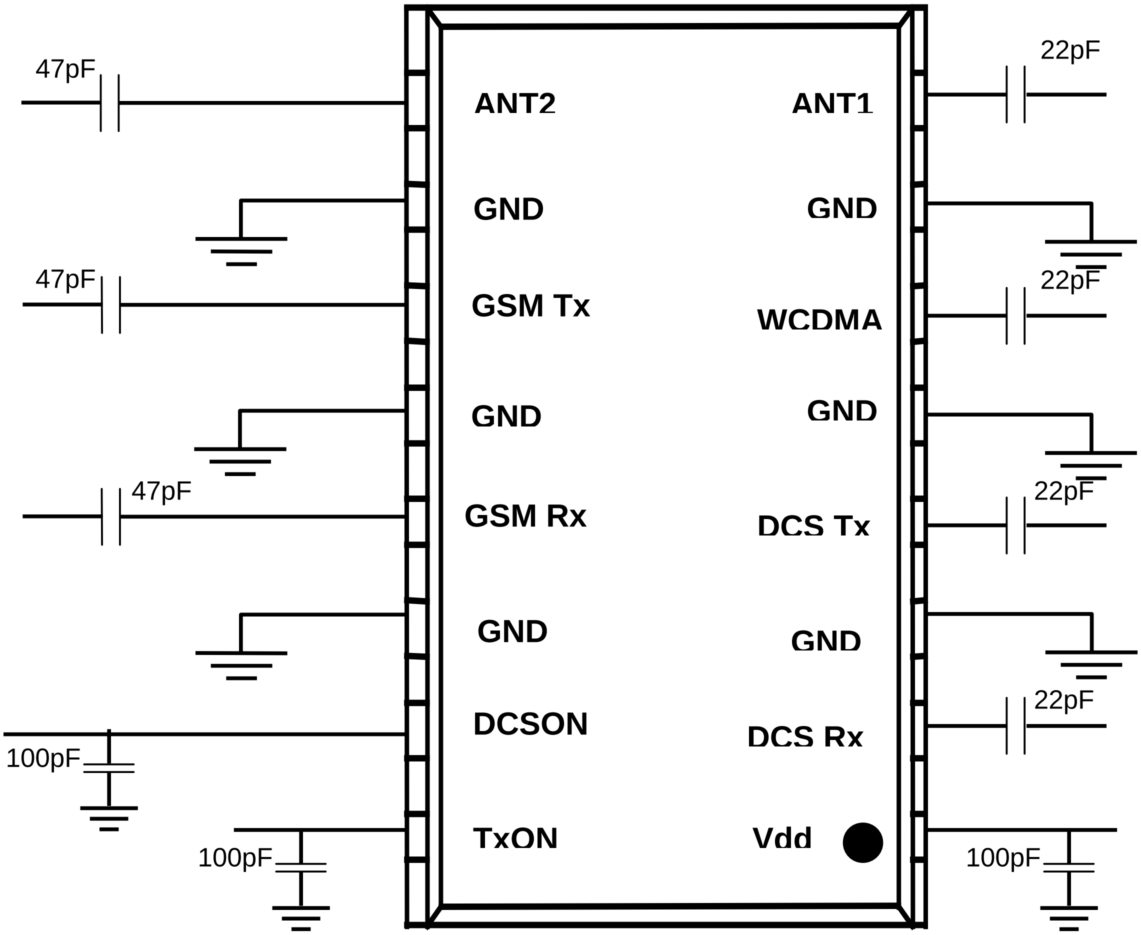
NOTE: 1) The dimensions of the terminal section apply to the ranges of 0.1mm and 0.25mm from the end of a terminal.

SONY CODE	VSON-16P-01
EIAJ CODE	—
JEDEC CODE	—

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEADTREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02 g

DC Blocking Capacitors, Decoupling Capacitors and External Bias Resistors

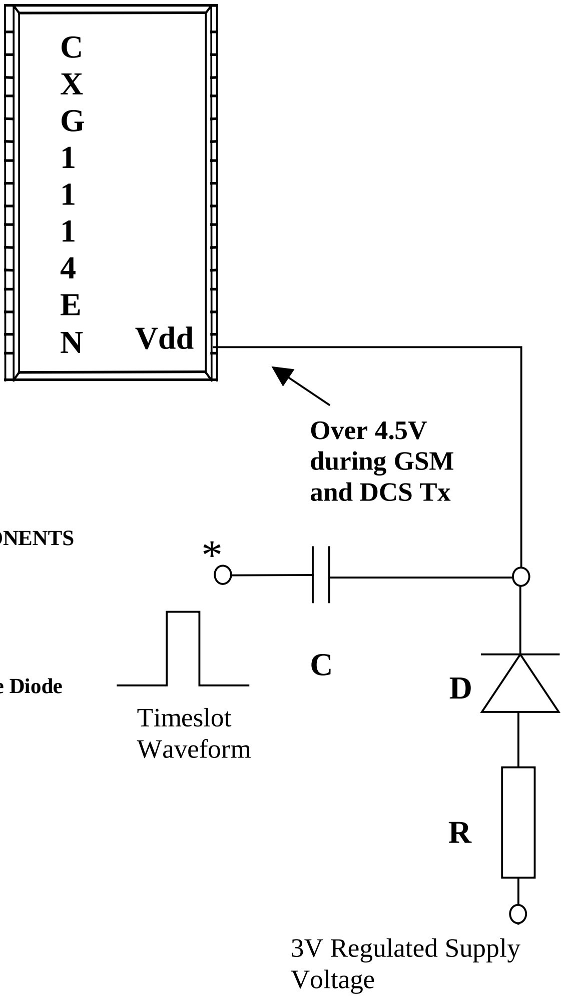


Note: Pin out is tentative.

Note: Capacitors are required on all RF ports as a DC block (22pF – 47pF). Decoupling capacitors are required on Vdd and on control lines (100pF).

Application Note 1

Operating the CXG1114EN from a 3V Regulated Supply



ADDITIONAL COMPONENTS

C: 0603 CAP, uF **

R: 200R

D: Low Turn-On Voltage Diode

Technique

Allows use of CXG1114EN in handsets with 3V regulated supply.

The CXG1114EN is for 5V nominal battery voltage but works well down to a Vdd of 4.5V.

This technique is only necessary for GSM and DCS Tx modes.

Fundamentally, the time slot waveform is added to the 3V supply to give a Vdd of over 4.5V.

This technique is suitable for up to 4 consecutive Tx timeslots (i.e. GPRS Class 12).

***This waveform may be taken from the PA ramping input (or drain supply in case of drain power control) or via the Tx ON/OFF Logic.**

****Minimum and recommended value of capacitance, C, depends on GPRS class and is given by the following table.**

Number of Consecutive Tx Timeslots	Minimum and Recommended Value of Capacitance, C, (uF)
1	1.0
2	2.0
4	2.0

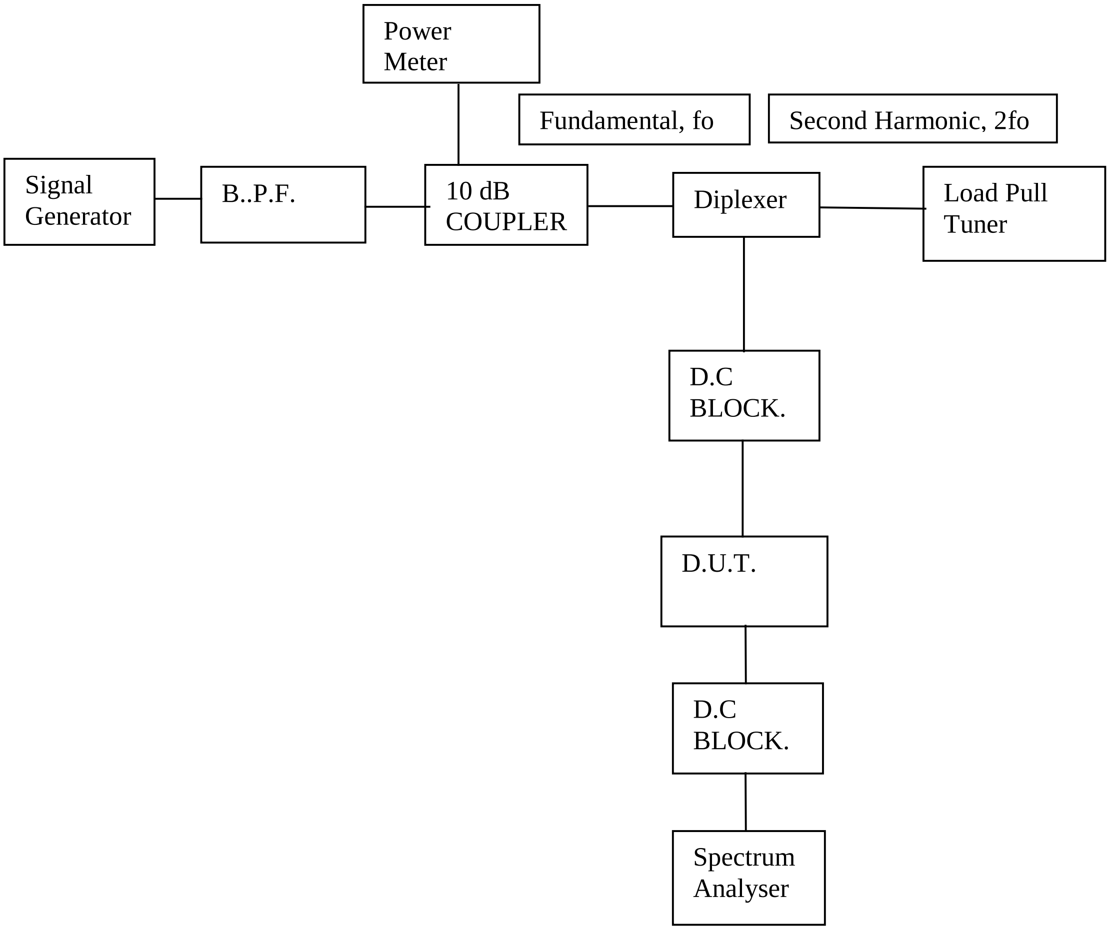
Application Note 2

Impedance Matching for Harmonic Minimisation

This note outlines the method used to find the source impedance to present to a transmit port at the second harmonic frequency (2fo) to reduce the second harmonic level at the antenna.

This should be carried out for a set of devices that represent the process variants. This way a compromise can be found that suits all variants.

The necessary equipment is shown immediately below.



The device should be mounted on a PCB with 50Ω tracks running from all RF pins to SMA connectors on the PCB edge (DUT). All ports should be externally DC blocked and unused ports should be terminated in 50Ω. All measurements should be performed at the incident powers for which the harmonic levels are specified in this document.

The 2nd Harmonic level at the Antenna Port is measured using the Spectrum Analyser and the Vertical and Horizontal position of the Load Pull Stub adjusted such that this level is minimised.

The device should then be removed from the board and an SMA connector mounted such that the source impedance seen by the transmit port at 2fo can be measured using a VNA.

Measurements should be de-embedded to the end of the SMA centre pin.

A network should then be designed to match the impedance of the low pass filter (LPF), which usually comes in front of the device, to the 2fo source impedance that gives sufficiently reduced 2fo levels for all devices measured.

The network should be designed to maintain a good match and insertion loss at the fundamental frequency.

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