Data sheet	
status	Preliminary specification
date of issue	July 1990

TDA4670

Picture signal improvement circuit (PSI) in colour television receivers

GENERAL DESCRIPTION

The TDA4670 contains a luminance signal path which consists of a switchable delay line with peaking and coreing stage as well as two colour difference channels each consisting of a sample and hold circuit for improving the transient time of the chroma signal (see Fig.1).

Y-signal path

The Video Blanking Signal (VBS) input is capacitively coupled to pin 16. In the first stage the signal is clamped to the black level and then reduced to a suitable level for the following delay line. This delay line consists of 13 all-pass cells (t_{cell} = 90 ns) which are built with gyrators. The maximum possible delay time is 1135 ns. This delay time is switchable via the I²C-bus from 25 to 1135 ns in steps of 45 ns. An automatic control circuit ensures a good accuracy for the delay time (t_d = ±30 ns). The control voltage is generated from the line frequency between the 16th and 17th burstkey pulse after start of V-blanking. During the time from the 16th to the 18th burstkey pulse an oscillation voltage is present at the output pin 12.
A peaking circuit is incorporated with two selectable centre frequencies (2.6 and 5 MHz). This circuit consists of two additional delay cells, two 0.5 gain inverting amplifiers and a summation stage. For better noise behaviour the peaking signal is applied via a coreing stage and a switchable amplifier before being added to the main signal.
The suitable centre frequency and the grade of peaking can be controlled by means of I²C-bus commands.
The output buffer stage ensures a low ohmic output signal with zero gain with respect to the input.

Colour difference path

Both colour difference channels consist of a clamping stage at the input, a buffer amplifier, a storage stage and an output amplifier. The storage, which is operated by a differential amplifier, stores the colour difference signal during the transient time of the input signal and then switches rapidly to accept the new signal.
A signal formed by differentiating, full wave rectifying and summing the two colour difference signals is compared with a reference signal. The resultant signal is used to switch the sample-and-hold circuits.

Both CD channels have good uniformity and no signal attenuation. The colour transient improvement function can be switched on or off by means of the I²C-bus commands.

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4670	18	DIL	plastic	SOT102

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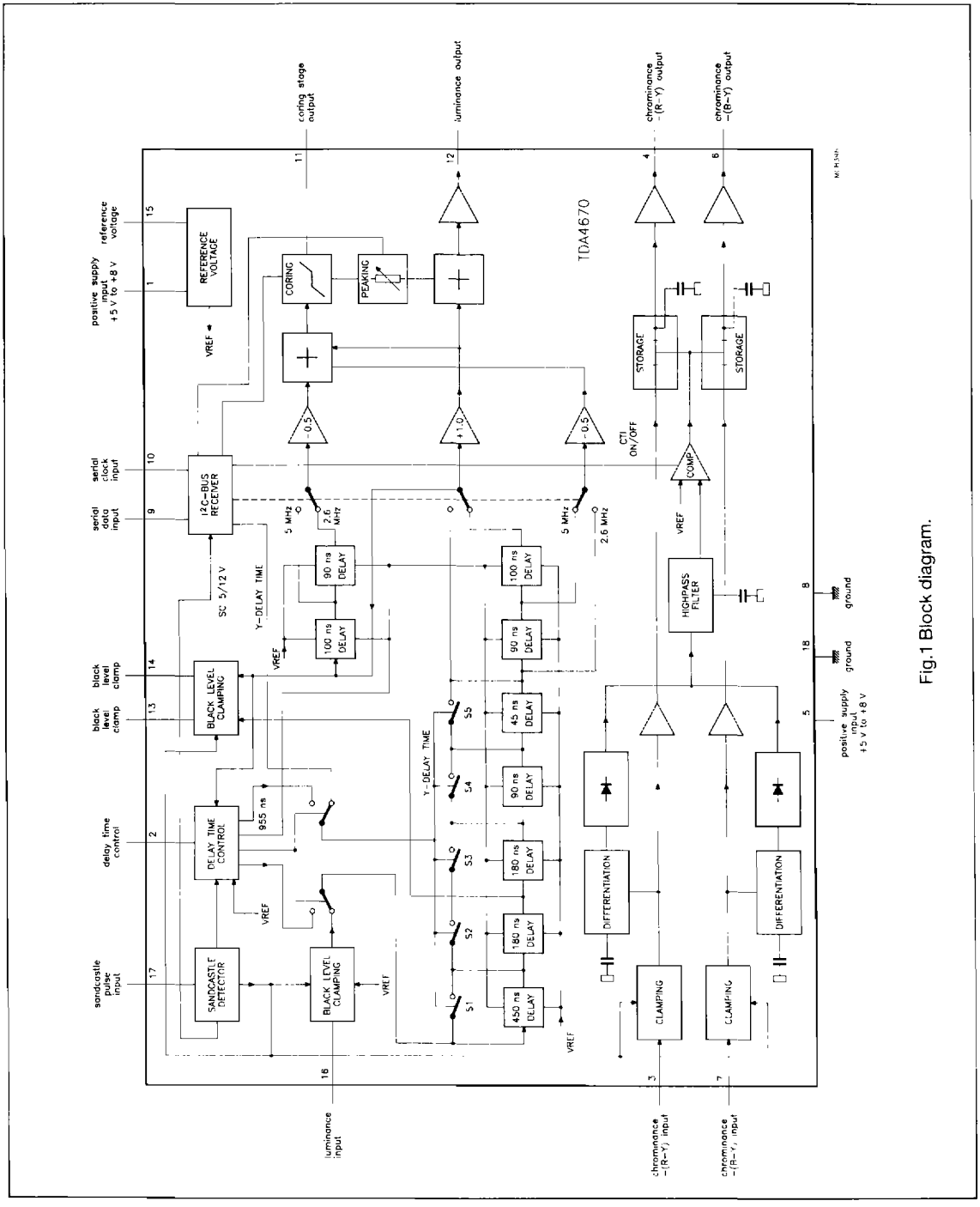

Fig.1 Block diagram.

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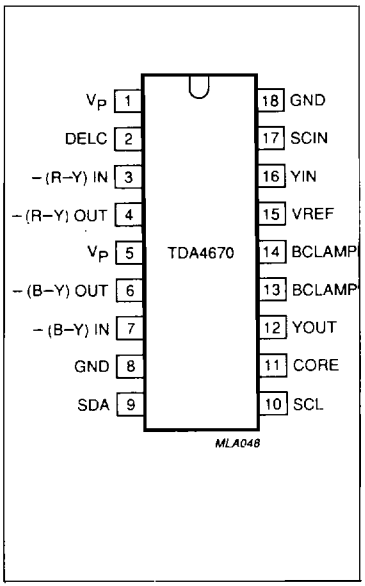

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply input +5 V to +8 V
DELC	2	delay time control
-(R-Y)IN	3	chrominance -(R-Y) input
-(R-Y)OUT	4	chrominance -(R-Y) output
V_P	5	positive supply input +5 V to +8 V
-(B-Y)OUT	6	chrominance -(B-Y) output
-(B-Y)IN	7	chrominance -(B-Y) input
GND	8	ground
SDA	9	serial data input I^2C-bus
SCL	10	serial clock input I^2C-bus
CORE	11	coring stage output
YOUT	12	luminance output
BCLAMP	13	black level clamp
BCLAMP	14	black level clamp
VREF	15	reference voltage
YIN	16	luminance input
SCIN	17	sandcastle pulse input
GND	18	ground

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage	4.5	5.0	8.8	V
I_P	supply current	31	41	52	mA
Y_d	Y-delay time	25	-	1135	µs
Y_{att}	Y-attenuation	-	1.0	-	dB
CD_{att}	(R-Y) and (B-Y) attenuation	-	0	-	dB

LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
t_{stg}	storage temperature range		-25	+150	°C
T_{amb}	operating ambient temperature range		0	+70	°C
P_{tot}	total power dissipation	t_j = 150 °C; t_{amb} = 70 °C	-	0.97	W

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air	-	82	K/W

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CHARACTERISTICS

V_P = 5 V; T_{amb} = 25 °C; measured in application circuit see Fig.3 all voltages measured with respect to pin 18; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	NOM.	MAX.	UNIT
V_P	supply voltage		4.5	-	8.8	V
I_P	supply current		31	41	52	mA
Y-signal path Luminance delay (note 1)						
$V_{16(p-p)}$	Y-input signal composite signal) peak-to-peak value)	capacitive coupling	-	0.45	0.64	V
V_{16}	internal bias voltage	during clamping to black level	-	3.10	-	V
R_{16}	input resistance	outside clamping	5	-	-	MΩ
C_{16}	input capacitance		-	3	10	pF
I_{16}	input current outside clamping		−0.1	-	0.1	µA
$\pm I_{16}$	input current during clamping		95	-	190	µA
t_{Ymax}	maximum Y-signal delay time	note 2	1105	1135	1165	ns
d_{tY}	minimum switchable delay step	delay time adjustable by I²C-bus	40	45	50	ns
t_{Ymin}	minimum Y-signal delay time	without peaking	-	25	-	ns
t_{Ymin}-t_{CDmin}	delay time difference luminance- to chrominance-signal	CTI and peaking off	70	100	130	ns
t_{Ywp}	minimum delay time peaking		185	215	245	ns
G_Y	Y-signal gain at 500 kHz (t_{Ymax}) between pins 12 and 16		−2.0	−1.0	0.0	dB
	Y-signal frequency response from 0.5 to 3 MHz (t_{Ymax})		−2.0	−1.0	0	dB
	Y-signal frequency response from 0.5 to 5 MHz (t_{Ymax})		−4.0	−3.0	−1.0	dB
Y_{tdg}	Y-signal group delay time difference from 0.5 to 5 MHz (t_{Ymax})		−25	0	25	ns
$m=a_{min}/a_{max}$ m	linearity for content	V_{VB} = 315 mV; (V_{VBS} = 0.45 V)	0.85	-	-	
		V_{VB} = 450 mV; (V_{VBS} = 0.64 V)	0.60	-	-	
Luminance peaking						
f_{C1} f_{C2}	peaking frequency	selectable via I²C-bus	4.5 2.3	5.0 2.6	5.5 2.9	MHz MHz
 P_{a1} P_{a2} P_{a3} P_{a4}	peaking amplitude selection (amplitude f_C/amplitude 0.5 MHz)	via I²C-bus	 - - - -	 6 3.5 0 -4.4	 - - - -	 dB dB dB dB
L	limitation of peaking (positive amplitude of correction signal/nominal VB-signal)		-	+20	-	%

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SYMBOL	PARAMETER	CONDITIONS	MIN.	NOM.	MAX.	UNIT
VN	noise voltage (RMS value)	0 to 5 MHz; without peaking	-	-	1	mV
C	coreing of peaking (coreing part/nominal VB-signal)	switchable via I²C-bus	-	20	-	%
	output current	emitter follower with constant current source I_{source}	1.0	-	-	mA
I_{sink}			0.4	-	-	mA
R_O	output resistance		-	-	160	Ω
Colour-difference path (note 3)						
$V_{3(p-p)}$	(R-Y) signal (75% colour bar signal) (peak-to-peak value)		-	1.05	1.48	V
$V_{7(p-p)}$	(B-Y) signal (75% colour bar signal) (peak-to-peak value)		-	1.33	1.88	V
C_3, C_7	input capacitance		-	6	12	pF
I_3, I_7	input current outside clamping		−0.1	0	0.1	μA
$\pm I_3, I_7$	input current during clamping		100	-	190	μA
V_3, V_7	internal bias voltage during clamping		-	2.45	-	V
$V_3, V_7/d_t$	input transient sensitivity		0.15	-	-	V/μS
$V_6/V_3, V_6/V_7$	signal gain		−1	0	1	dB
	uniformity (R-Y/B-Y)		−0.3	0	0.3	dB
$m=a_{min}/a_{max}$	linearity	V_{IN} = 1.33 V_{pp} (nom.)	0.90	-	-	
m		V_{IN} = 1.86 V_{pp} (+3 dB)	0.65	-	-	
V_{Of}/V_{Onom}	signal reduction	higher frequency t_{sig} = 50 ns, $t_r = t_f$ = 1 μs	−1.5	-	-	dB
	switching spikes and offsets in an unused channel with nominal signal in the other channel	R_{source} <= 300 Ω				
V_4, V_6	spikes		−30	-	+30	mV
dV_4, dV_6	offsets		−5	-	+5	mV
dV_4, dV_6	offsets in signal during and after storage time		−18	-	+18	mV
I_{source}	output source current		1.0	-	-	mA
I_{sink}	output sink current		0.4	-	-	mA
$V_{O4,6}$	DC output voltage		-	2.0	-	V
$R_{O4,6}$	output resistance		-	-	100	Ω
sandcastle pulse input						
	12 V sandcastle pulse	SC5 = 0 selectable by I²C-bus				
V_{thHV}	threshold voltage line/field		1.1	1.5	1.9	V
V_{thBG}	threshold voltage burstgate		6.0	7.0	8.0	V
R_{17}	input resistance		30	40	50	kΩ
C_{17}	input capacitance		-	4	8	pF
	5 V sandcastle pulse	SC5 = 1				
V_{thHV}	threshold voltage line/field		1.1	1.5	1.9	V
V_{thBG}	threshold voltage burstgate		3.0	3.5	4.0	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	NOM.	MAX.	UNIT
R_{17}	input resistance		15	20	25	kΩ
C_{17}	input capacitance		-	4	8	pF
t_d	time difference between leading edge of burst gate and internal clamping pulse		-	1	-	µs
t_{BG}	pulse duration of burstgate		3.4	4.0	4.6	µs
SDA, SCL inputs						
f_{SCL}	clock frequency range		0	-	100	kHz
$t_{SU,STA}$	start code set-up		4.7	-	-	µs
$t_{HD,STA}$	start code hold		4	-	-	µs
$t_{SU,STO}$	stop code set-up		4.7	-	-	µs
t_{BUF}	bus free		4.7	-	-	µs
$t_{SU,DAT}$	data set-up		250	-	-	ns
t_{CLKH}	clock pulse HIGH		4	-	-	µs
t_{CLKL}	clock pulse LOW		4.7	-	-	µs
t_r	rise time		-	-	1	µs
t_f	fall time		-	-	0.3	µs

Notes to the characteristics

1. All values specified with V_{VB} = 315 mV (nom), T_{line} = 64.0 µs and $t_{burst\ gate}$ = 4.0 µs unless otherwise stated.
2. The delay time is proportional to $t_{line} + t_{bg/2}$
3. All values specified with $V_{(p-p)}$ = 1.33 V, t_r = 1 µs, t_f = 1 µs, t_{signal} = 1 µs and $t_{burst\ gate}$ = 4 µs

I²C-BUS

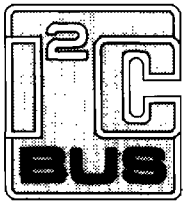
Slave address

A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
1	0	0	0	1	0	0	0

Slave receiver format

S	SLAVE ADDR.	0	A,	SUB ADDR.	A,	DATA BYTE A P

1 or 2 data bytes
auto increment



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

Subaddress byte and data byte format

Function	subaddr.	data	byte						
		D7	D6	D5	D4	D3	D2	D1	D0
00 to 0F (note 1)									
Delay line adjust CTI + sandcastle control	10	0	SC5	CTI	D5	D2B	D2A	D1	D/2
Peaking control	11	COR	PEAK	LCF	0	0	0	PCON1	PCON0
Reserved 12 to 1F		X	X	X	X	X	X	X	X
Test data 0	F0	TB07							TB00
F1 to FE (note 2)									
Test data F	FF	TBF7							TBF0

Notes

1. reserved for colour decoders and RGB processors
2. reserved for testing this device

Bit definition

DXX	bits are activating delay line segments Logic 1: delay line segment active Logic 0: delay line segment inactive		
D/2	control of 45 ns delay line segment		
D1	control of 90 ns delay line segment		
D2A,D2B	control of 180 ns delay line segments		
D5	control of 450 ns delay line segment		
CTI	colour transient improvement control Logic 1: CTI-function operative Logic 0: no CTI-function		
SC5	sand castle detector level control Logic 1: 5 V sandcastle pulse Logic 0: 12 V sandcastle pulse		
LCF	peaking frequency response control Logic 1: low centre frequency 2.6 MHz Logic 0: high centre frequency 5.0 MHz		
PEAK DELAY	peaking delay set up Logic 1: peaking delay operative Logic 0: no peaking delay		
PCON0,1	peaking amplitude control		
	PCON1	PCON0	grade of peaking
	0 0 1 1	0 1 0 1	−4.4 dB 0 dB +3.5 dB +6 dB
COR	coering control Logic 1: coering operative Logic 0: coering		

Slave transmitter format is not acknowledged.

General call address is not acknowledged.

After power-on reset the first 7 control bits of the data byte are set to 0 and the 8th bit (LSB) is set to 1.

Subaddresses 00 to 0F are reserved for colour decoders and for RGB processors and are not acknowledged by this device. Only subaddress 10 and 11, each with 8 bits, are acknowledged by thisdevice.

Data registers with subaddress outside the range 00 to 1F are not tested and are therefore forbidden for the user.

Data registers with subaddress F0 to FF may be used to test the IC in the factory. Thus these subaddresses are forbidden for the user. The bits TBx of these registers may be unique for each device.

The bits presented as don't cares (X) are reserved for functions not yet built-in. Their value should not influence any other function in the device. These bits have to be tested on their don't care function if other devices are available which are using these bits. Thus the microcontroller software can be written in such a way that the whole family of circuits can be used with the same address.

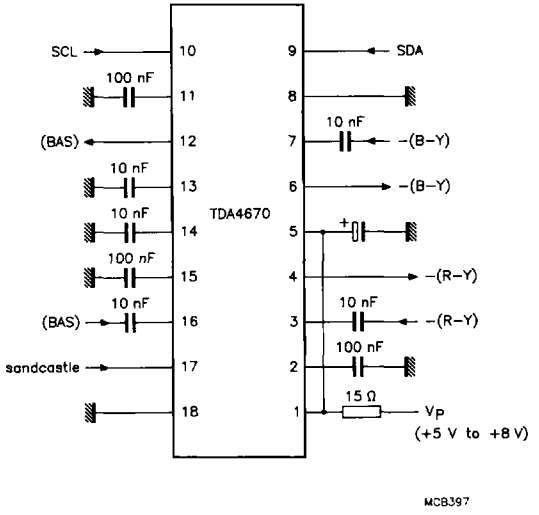


Fig.3 Application circuit.