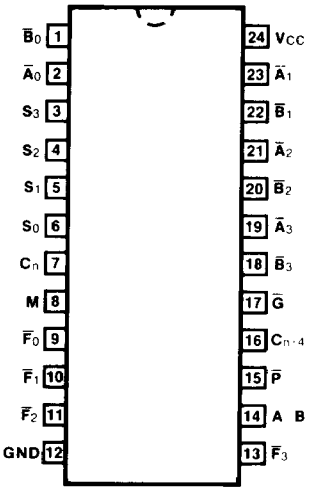
9341
93L41
93S41

4-BIT ARITHMETIC LOGIC UNIT

DESCRIPTION—The '41 4-bit arithmetic logic units can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations; the Add and Subtract modes are the most important. The '41 is a pin replacement for the 54/74181.

- **PROVIDE 16 OPERATIONS**
  ADD, SUBTRACT, COMPARE, DOUBLE
  TWELVE OTHER ARITHMETIC OPERATIONS
- **PROVIDE ALL 16 LOGIC OPERATIONS OF TWO VARIABLES**
  EXCLUSIVE-OR, COMPARE, AND NAND, OR, NOR, PLUS
  TEN OTHER LOGIC OPERATIONS

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9341PC, 93L41PC 93S41PC		9N
Ceramic DIP (D)	A	9341DC, 93L41DC 93S41DC	9341DM, 93L41DM 93S41DM	6N
Flatpak (F)	A	9341FC, 93L41FC 93S41FC	9341FM, 93L41FM 93S41FM	4M

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW	93S (U.L.) HIGH/LOW
$\overline{A}_0 - \overline{A}_3$, $\overline{B}_0 - \overline{B}_3$	Operand Inputs (Active LOW)	3.0/3.0	1.5/0.75	3.75/3.75
$S_0 - S_3$	Function Select Inputs	4.0/4.0	2.0/1.0	5.0/5.0
M	Mode Control Input	1.0/1.0	0.5/0.25	1.25/1.25
C_n	Carry Input	5.0/5.0	2.5/1.25	7.5/7.5
$\overline{F}_0 - \overline{F}_3$	Function Outputs (Active LOW)	20/10	10/5.0 (3.0)	25/12.5
A = B	Comparator Output	OC*/10	OC*/5.0 (3.0)	OC*/12.5
$\overline{G}$	Carry Generator Output (Active LOW)	20/10	10/5.0 (3.0)	25/12.5
$\overline{P}$	Carry Propagate Output (Active LOW)	20/10	10/5.0 (3.0)	25/12.5
C_{n+4}	Carry Output	20/10	10/5.0 (3.0)	25/12.5

*OC—Open Collector

FUNCTIONAL DESCRIPTION — The '41 is a 4-bit high speed parallel arithmetic logic unit (ALU). Controlled by the four Function Select inputs ($S_0 - S_3$) and the Mode Control input (M), it can perform all the 16 possible operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table below lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead betweeen packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, the '41 can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For super high speed operation the Schottky '41 should be used in conjunction with the '42 carry lookahead circuit.

The A = B output from the '41 goes HIGH when all four $\overline{F}_n$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open-collector and can be wired-AND with the other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated the '41 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labled inside the logic symbol.

FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
				LOGIC	ARITHMETIC**	LOGIC	ARITHMETIC**
S_3	S_2	S_1	S_0	(M = H)	(M = L) (C_n = L)	(M = H)	(M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{A}\overline{B}$	AB minus 1	$\overline{A} + \overline{B}$	A + B
L	L	H	L	$\overline{A} + \overline{B}$	$A\overline{B}$ minus 1	$\overline{A}B$	$A + \overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A} + \overline{B}$	A plus $(A + \overline{B})$	$\overline{A\overline{B}}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus $(A + \overline{B})$	$\overline{B}$	$(A + B)$ plus $A\overline{B}$
L	H	H	L	$\overline{A} \oplus \overline{B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$A + \overline{B}$	$A + \overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H	L	L	L	$\overline{A}B$	A plus (A + B)	$\overline{A} + B$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$A \oplus B$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)	B	$(A + \overline{B})$ plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A*	Logic 1	A plus A*
H	H	L	H	$A\overline{B}$	AB plus A	$A + \overline{B}$	$(A + B)$ plus A
H	H	H	L	AB	$A\overline{B}$ minus A	A + B	$(A + \overline{B})$ plus A
H	H	H	H	A	A	A	A minus 1

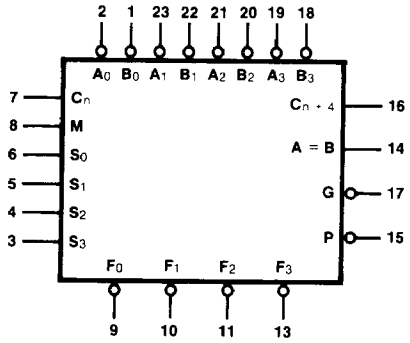
*Each bit is shifted to the next more significant position

**Arithmetic operations expressed in 2s complement notation

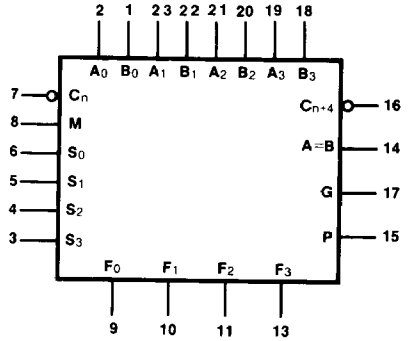
H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC SYMBOLS

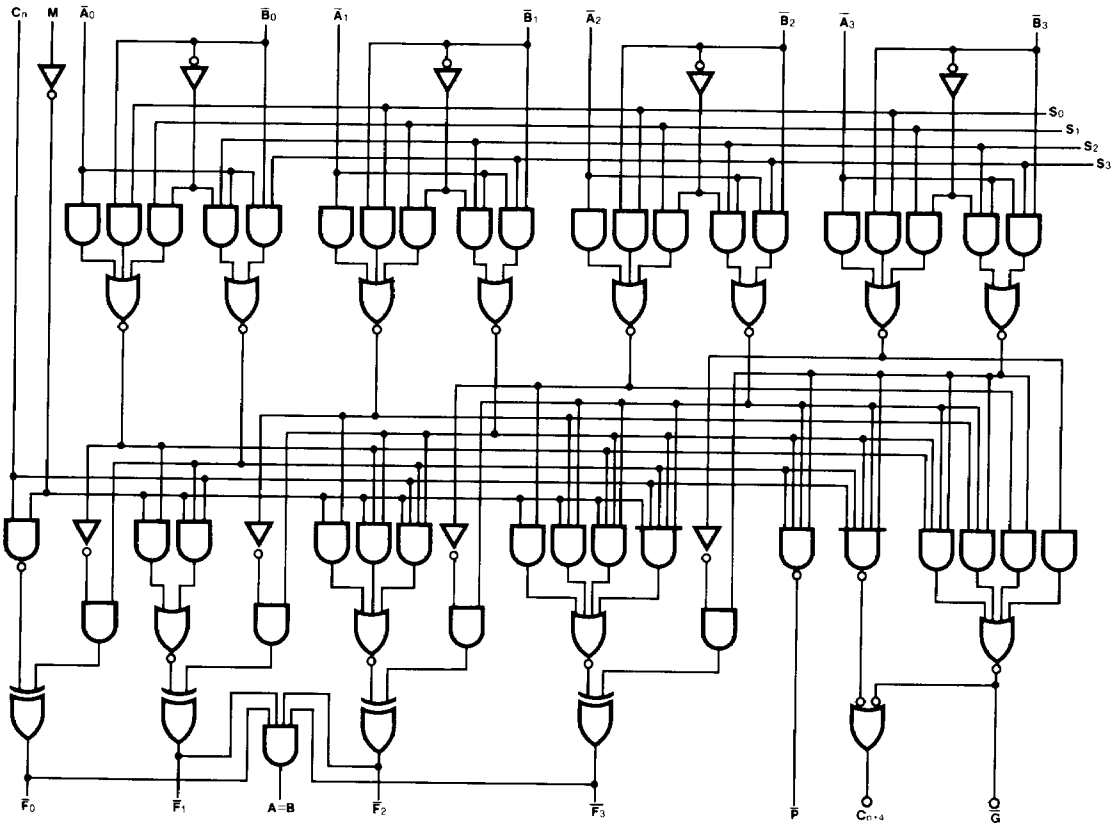
ACTIVE LOW OPERANDS



ACTIVE HIGH OPERANDS



LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		93XX Min	93XX Max	93L Min	93L Max	93S Min	93S Max	UNITS	CONDITIONS
I_{CC}	Power Supply Current	XM		127				125	mA	V_{CC} = Max C_n, $\overline{B}_0$ - $\overline{B}_3$ = Gnd All Other Inputs = 4.5 V
		XC		140				140		
I_{CC}	Power Supply Current	XM		135				135	mA	V_{CC} = Max M, S_0 - S_3 = 4.5 V All Other Inputs = Gnd
		XC		150				150		
I_{CC}	Power Supply Current					36			mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX C_L = 15 pF, R_L = 400 Ω Min	93XX Max	93L C_L = 15 pF Min	93L Max	93S C_L = 15 pF, R_L = 280 Ω Min	93S Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}		16 17		51 22		12 12	ns	M = Gnd Figs. 3-1, 3-4 Tables I & II
t_{PLH} t_{PHL}	Propagation Delay C_n to $\overline{F}$		17 17		37 42		12 12	ns	M = Gnd Figs. 3-1, 3-4 Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$		19 12		51 26		14 14	ns	M, S_1, S_2 = Gnd S_0, S_3 = 4.5 V Figs. 3-1, 3-5 Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$		22 17		50 43		15 15	ns	M, S_0, S_3 = Gnd S_1, S_2 = 4.5 V Figs. 3-1, 3-4, 3-5 Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$		19 15		50 46		14 14	ns	M, S_1, S_2, = Gnd S_0, S_3, = 4.5 V Figs. 3-1, 3-5 Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$		21 21		38 63		15 15	ns	M, S_0, S_3 = Gnd S_1, S_2 = 4.5 V Figs. 3-1, 3-4, 3-5 Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$		26 26		36 65		20 20	ns	M, S_1, S_3 = Gnd S_0, S_3 = 4.5 V Figs. 3-1, 3-5 Table I

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (Cont'd)

SYMBOL	PARAMETER	93XX C_L = 15 pF, R_L = 400 Ω		93L C_L = 15 pF		93S C_L = 15 pF, R_L = 280 Ω		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$		26 32		39 49		21 21	ns	M, S_0, S_3 = Gnd S_1, S_2 = 4.5 V Figs. 3-1, 3-4, 3-5 Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_{i+1}$		29 25		56 62		24 24	ns	M, S_1, S_2 = Gnd S_0, S_3 = 4.5 V Figs. 3-1, 3-5 Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_{i+1}$		29 30		68 71		25 25	ns	M, S_0, S_3 = Gnd S_1, S_2 = 4.5 V Figs. 3-1, 3-4, 3-5 Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}$		24 24		51 49		20 20	ns	M = 4.5 V Figs. 3-1, 3-5 Table III
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+1}		21 30		46 60		18.5 18.5	ns	M, S_1, S_2 = Gnd S_0, S_3 = 4.5 V Figs. 3-1, 3-4 Table I
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+1}		25 30		60 58		23 23	ns	M, S_0, S_3 = Gnd S_1, S_2 = 4.5 V Figs. 3-1, 3-4, 3-5 Table II
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_n$ or $\overline{B}_n$ to A = B		40 42		68 72		23 23	ns	M, S_0, S_3 = Gnd S_1, S_2 = 4.5 V R_L = 400 Ω to 5.0 V; Figs. 3-1, 3-4, 3-5; Table II

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SUM MODE TEST TABLE I **FUNCTION INPUTS:** $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = M = 0$ V

SYMBOL	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II **FUNCTION INPUTS:** $S_1 = S_2 = 4.5$ V, $S_0 = S_3 = M = 0$ V

SYMBOL	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}

LOGIC MODE TEST TABLE III **FUNCTION INPUTS:** $S_1 = S_2 = M = 4.5$ V, $S_0 = S_3 = 0$ V

SYMBOL	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$