

# LMX3161 Single Chip Radio Transceiver

## General Description

The LMX3161 Transceiver is a monolithic, integrated radio transceiver optimized for use in the Digital Enhanced Cordless Telecommunications (DECT) system. It is fabricated using National's ABiC V BiCMOS process ( $f_T = 18$  GHz).

The LMX3161 contains both transmit and receive functions. The transmitter includes a 1.1 GHz phase locked loop (PLL), a 2.0 GHz frequency doubler, and a high frequency buffer. The receiver consists of a 2.0 GHz low noise mixer, an intermediate frequency (IF) amplifier, a high gain limiting amplifier, a frequency discriminator, a received signal strength indicator (RSSI), and an analog DC compensation loop. The PLL, doubler, and buffers can be used to implement open loop modulation. The RSSI output may be used for channel quality monitoring. The circuit features on-board voltage regulation to allow supply voltages from 3.0V to 5.5V. An additional voltage regulator on the LMX3161 provides a stable supply source to external discrete stages in the Rx and Tx chains.

The IF amplifier, high gain limiting amplifier, and discriminator are optimized for 110 MHz operation, with a total IF gain of 85 dB. The single conversion receiver architecture provides a low cost, high performance solution for communications systems.

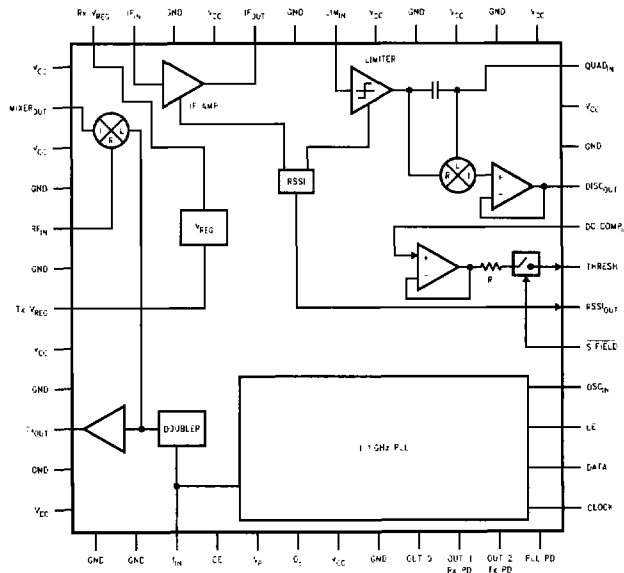
The Single Chip Radio Transceiver is available in a 48-pin 7mm X 7mm X 1.4mm PQFP surface mount plastic package.

## Features

- Single chip solution for DECT RF transceiver
- RF sensitivity to  $-93$  dBm; RSSI sensitivity to  $-100$  dBm
- Two regulated voltage outputs for discrete amplifiers
- High gain (85 dB) intermediate frequency strip
- Allows unregulated 3.0V–5.5V supply voltage range
- Power down mode for increased current savings
- System noise figure 6.5 dB (typ)

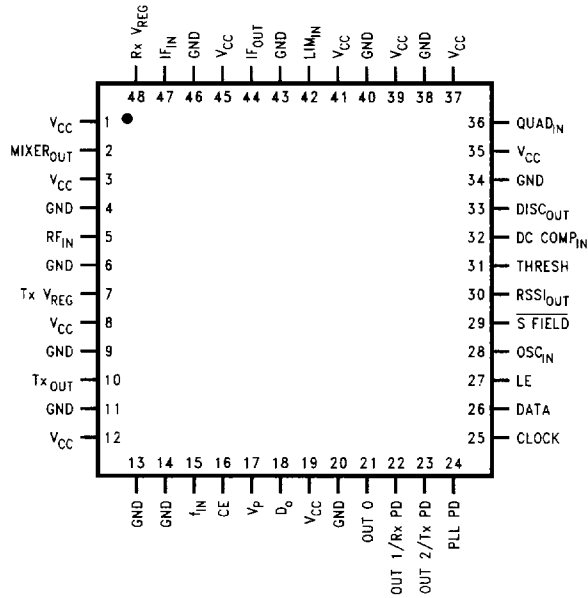
## Applications

- Digital Enhanced Cordless Telecommunications (DECT) Applications:
  - Residential Cordless
  - Wireless PABX
  - Wireless LAN
  - Radio Local Loop
  - Public Access



This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.

### LMX3161 Pin Diagram



TL/W/12815-2

Pin No.	Pin Name	I/O	Description
1	V <sub>CC</sub>	—	Power supply for CMOS section of PLL and ESD bussing. Connect to VBAT (see Note 1).
2	MIXER <sub>OUT</sub>	O	IF output signal of the mixer.
3	V <sub>CC</sub>	—	Power supply voltage input to mixer. Connect to VBAT (see Note 1).
4	GND	—	Ground.
5	RF <sub>IN</sub>	I	RF input to the mixer.
6	GND	—	Ground for the mixer.
7	Tx V <sub>REG</sub>	O	Supply voltage to external gain stage.
8	V <sub>CC</sub>	—	Power supply voltage input to analog sections of doubler/PLL. Connect to VBAT (see Note 1).
9	GND	—	Ground.
10	Tx <sub>OUT</sub>	O	Frequency Doubler output.
11	GND	—	Ground.
12	V <sub>CC</sub>	—	Power supply voltage input to analog sections of doubler/PLL. Connect to VBAT (see Note 1).
13	GND	—	Ground for analog sections of doubler/PLL.
14	GND	—	Ground.
15	f <sub>IN</sub>	I	RF Input to doubler and PLL.
16	CE	I	Chip Enable. LOW powers down entire part. Before taking HIGH all MICROWIRE™ instructions should be loaded for R, N, F latches. Taking CE HIGH will power up the appropriate chip blocks depending on the state of bits F6, F7, F11, and F12. The CE state change will also load the PLL N and R counters to the programmed divide ratios.

## LMX3161 Pin Diagram (Continued)

Pin No.	Pin Name	I/O	Description
17	V <sub>P</sub>	—	Power supply for charge pump.
18	D <sub>o</sub>	O	Internal charge pump output. For connection to a loop filter to provide the tuning voltage of an external VCO.
19	V <sub>CC</sub>	—	Power supply input for CMOS section of PLL and ESD bussing. Connect to VBAT (see Note 1).
20	GND		Ground for CMOS section of PLL and ESD bussing.
21	Out 0	O	Programmable CMOS output (see Programmable Modes).
22	Out 1/Rx PD	I/O	Programmable CMOS output or can be used for hardwire receiver power down (see Programmable Modes).
23	Out 2/Tx PD	I/O	Programmable CMOS output or can be used for hardwire transmitter power down (see Programmable Modes).
24	PLL PD	I	PLL PD = LOW for PLL normal operations. PLL PD = HIGH for PLL power saving.
25	Clock	I	High impedance CMOS input with Schmitt Trigger.
26	Data	I	Binary serial data input. Data entered MSB first. High impedance CMOS input with Schmitt Trigger.
27	LE	I	Load enable input. High impedance CMOS input with Schmitt Trigger.
28	OSC <sub>IN</sub>	I	Oscillator input. CMOS input with self bias 100 kΩ feedback.
29	DC COMP <sub>EN</sub>	I	DC compensation circuit enable. While LOW, the DC compensation circuit is enabled, and the threshold level (stored by an external capacitor) is updated through the DC compensation loop. While HIGH, the switch is opened, and the comparator threshold level is held by the external capacitor.
30	RSSI <sub>OUT</sub>	O	Voltage output of the received signal strength indicator (RSSI).
31	Thresh	O	Threshold level to external comparator. An external parallel capacitor holds the threshold level.
32	DC COMP <sub>IN</sub>	I	Input to DC compensation circuit.
33	DISC <sub>OUT</sub>	O	Demodulated output of discriminator.
34	GND	—	Ground for discriminator circuit.
35	V <sub>CC</sub>	—	Power supply input to discriminator circuit. Connect to VBAT (see Note 1).
36	QUAD <sub>IN</sub>	I	Quadrature input for tank circuit.
37	V <sub>CC</sub>	—	Power supply input to limiter output stage. Connect to VBAT (see Note 1).
38	GND	—	Ground for limiter output stage.
39	V <sub>CC</sub>	—	Power supply input for limiter gain stages. Connect to VBAT (see Note 1).
40	GND	—	Ground for ESD bussing.
41	V <sub>CC</sub>	—	Power supply input for IF amplifier gain stages. Connect to VBAT (see Note 1).
42	LIM <sub>IN</sub>	I	IF input to the limiter.
43	GND	—	Ground for limiter gain stages.
44	IF <sub>OUT</sub>	O	IF output to bandpass filter.
45	V <sub>CC</sub>	—	Power supply input for IF amplifier output. Connect to VBAT (see Note 1).
46	GND	—	Ground for IF amplifier.
47	IF <sub>IN</sub>	I	IF input to IF amplifier.
48	Rx V <sub>REG</sub>	—	Supply voltage to external LNA.

Note 1. VBAT is typically filtered before connecting to the device.

**Absolute Maximum Ratings** (Notes 1, 2)

Power Supply Voltage ( $V_{CC}$ )	-0.3V to +6.5V
$V_P$	-0.3V to +6.5V
Voltage on Any Pin with GND = 0V ( $V_I$ )	-0.3V to $V_{CC} + 0.3V$
Storage Temperature Range ( $T_S$ )	-65°C to +150°C
Lead Temp. (solder, 4 sec)( $T_L$ )	+260°C

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

**Note 2:** This device is a high performance RF integrated circuit with an ESD rating < 2 KeV and is ESD sensitive. Handling and assembly of this device should only be done at ESD workstations.

**Recommended Operating Conditions**

Supply Voltage ( $V_{CC}$ )	3.0V to 5.5V
$(V_P)$	$V_{CC}$ to 5.5V
Operating Temperature ( $T_A$ )	-10°C to +70°C

**Electrical Characteristics**

The following specifications are guaranteed for  $V_{CC} = 3.6V$  and  $T_A = 25^\circ C$  unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$Rx I_{CC}$	Receive Mode Current Consumption	Tx PLL Powered Down		46		mA
$Tx I_{CC}$	Transmit Mode Current Consumption	Rx PLL Powered Down		27		mA
$PLL I_{CC}$	PLL Current	Rx, Tx Powered Down		6		mA
$I_{PD}$	Power Down Current	Tx, Rx, PLL Off		20		$\mu A$
$f_{RF}$	RF Frequency Range		1.7		2.0	GHz
$f_{IF}$	IF Input Frequency (Note 1)			110		MHz
<b>MIXER</b>		$f_{IN} = 1.9 \text{ GHz}, f_{IF} = 110 \text{ MHz}, f_{LO} = 1800 \text{ MHz} (f_{IN} = 900 \text{ MHz})$				
NF	Single Side Band Noise Figure	(Notes 2, 3)		10		dB
$G_C$	Conversion Gain	(Note 2)		15		dB
OIP3	Output Intercept Point	(Note 2)		5		dBm
$Z_{RF IN}$	$RF_{IN}$ Impedance			13-j10		$\Omega$
$Z_{MIXER OUT}$	$MIXER_{OUT}$ Impedance			160-j65		$\Omega$
$f_{IN-RF}$	$f_{IN}$ to RF Isolation	$f_{IN} = 900 \text{ MHz}$		30		dB
		$f_{IN} = 1800 \text{ MHz}$		30		dB
		$f_{IN} = 2700 \text{ MHz}$		30		dB
$f_{IN-IF}$	$f_{IN}$ to IF Isolation	$f_{IN} = 900 \text{ MHz}$		30		dB
		$f_{IN} = 1800 \text{ MHz}$		30		dB
		$f_{IN} = 2700 \text{ MHz}$		30		dB
RF-IF	RF to IF Isolation	$RFP_{IN} = 0$ to -85 dBm		30		dB

## Electrical Characteristics

The following specifications are guaranteed for  $V_{CC} = 3.6V$  and  $T_A = 25^\circ C$  unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>IF AMPLIFIER</b>		$f_{IN} = 110 \text{ MHz}$				
NF	Noise Figure			8		dB
$A_v$	Gain			25		dB
$Z_{IN}$	Input Impedance			150-j400		$\Omega$
$Z_{OUT}$	Output Impedance			190-j20		$\Omega$
<b>IF LIMITER</b>		$f_{IN} = 110 \text{ MHz}$				
Sens	Limiter/Disc. Sensitivity	BER = $10^{-3}$		-65		dBm
$IF_{IN}$	IF Limiter Input Impedance			100-j320		$\Omega$
$V_{max}$	Maximum Input Voltage Level				500	mV <sub>PP</sub>
<b>DISCRIMINATOR</b>		$f_{IN} = 110 \text{ MHz}$				
	Disc Gain (mV/° of Phase Shift from Tank Circuit)	1X Mode		10		mV/°
		3X Mode		33		mV/°
$V_{OUT}$	Discriminator Output Peak to Peak Voltage	3X Mode (Note 4)		400		mV
$V_{OS}$	Disc. Output DC Voltage	Nominal (Note 5)	1.4		1.7	V
$DISC_{OUT}$	Disc. Output Impedance			1000		$\Omega$
<b>RSSI (Note 6)</b>		$f_{IN} = 110 \text{ MHz}$				
RSSI	RSSI Dynamic Range	$P_{IN \text{ MIN}} = -100 \text{ dBm}$	70	80		dB
$RSSI_{OUT}$	RSSI Output Voltage	$P_{in} = -85 \text{ dBm @ IF Amp Input}$	0	0.25	0.4	V
		$P_{in} = 0 \text{ dBm @ IF Amp Input}$	1.15	1.5	1.8	V
	RSSI Slope	$P_{in} = -90 \text{ to } -30 \text{ dBm}$	11	20		mV/dB
<b>DC COMPENSATION SAMPLE AND HOLD CIRCUIT</b>						
$V_{OS}$	Input Offset Voltage			3		mV
$V_{I/O}$	Input/Output Voltage Swing	Centered at 1.5V		1.0		$V_{PP}$
$R_{SH}$	Sample and Hold Resistor		2.2		3.4	k $\Omega$
$D_V$	Threshold Input Voltage Droop	$C_{hold} = 2700 \text{ pF}$		1		mV/ms

## Electrical Characteristics

The following specifications are guaranteed for  $V_{CC} = 3.6V$  and  $T_A = 25^\circ C$  unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>FREQUENCY SYNTHESIZER</b>		$P_{f_{IN}} = -14$ to $-9$ dBm				
$f_{IN}$	Operating Frequency		500		1200	MHz
$f_{OSC}$	Oscillator Frequency		5		20	MHz
$V_{OSC}$	Oscillator Sensitivity		0.5	1.0		$V_{pp}$
$I_{D_{O-source}}$	Charge Pump Output Current	$V_{do} = V_p/2, I_{cpo} = \text{LOW (Note 7)}$		-1.5		mA
$I_{D_{O-sink}}$		$V_{do} = V_p/2, I_{cpo} = \text{LOW (Note 7)}$		1.5		mA
$I_{D_{O-source}}$		$V_{do} = V_p/2, I_{cpo} = \text{HIGH (Note 7)}$		-6.0		mA
$I_{D_{O-sink}}$		$V_{do} = V_p/2, I_{cpo} = \text{HIGH (Note 7)}$			6.0	mA
$I_{D_{O-Tri}}$		$0.5 \leq V_{do} \leq V_p - 0.5$ $T_A = 25^\circ C$		-1.0	0.1	1.0
$V_{OH}$	High-Level Output Voltage	$I_{OH} = -1.0$ mA	$V_{CC} - 0.4$			V
$V_{OL}$	Low-Level Output Voltage	$I_{OL} = 1.0$ mA			0.4	V
$V_{IH}$	High-Level Input Voltage		$V_{CC} - 0.8$			V
$V_{IL}$	Low-Level Input Voltage				0.8	V
$I_{IN}$	Input Current	$GND < V_{IN} < V_{CC}$	-1.0		1.0	mA
$t_{CS}$	Data to Clock Set Up Time	See Data Input Timing	50			ns
$t_{CH}$	Data to Clock Hold Time	See Data Input Timing	10			ns
$t_{CWH}$	Clock Pulse Width High	See Data Input Timing	50			ns
$t_{CWL}$	Clock Pulse Width Low	See Data Input Timing	50			ns
$t_{ES}$	Clock to Load Enable Set Up Time	See Data Input Timing	50			ns
$t_{EW}$	Load Enable Pulse Width	See Data Input Timing	50			ns
<b>FREQUENCY DOUBLER</b>		$f_{IN} = 945$ MHz, $f_{OUT} = 1.89$ GHz				
$f_{IN}$	Input Frequency Range		885		950	MHz
$P_{IN}$	Input Signal Level	$Z_{IN} = 200\Omega$ (Note 8)		-11.5		dBm
$Z_o$	Output Impedance			30		$\Omega$
	Fundamental Output Power	$P_{IN} = -11.5$ dBm, $f_{OUT} = 945$ MHz		-20		dBm
	3rd Harmonic Output Power	$P_{IN} = -11.5$ dBm, $f_{OUT} = 2.835$ GHz		-20		dBm
$P_{OUT}$	Output Power	$P_{IN} = -11.5$ dBm, $f_{OUT} = 1.89$ GHz	-10	-5		dBm
<b>VOLTAGE REGULATOR</b>						
$V_O$	Output Voltage	$I_{LOAD} = 5$ mA	2.65	2.75	2.85	V
$\Delta V_{IN}/\Delta V_O$	Ripple Rejection			TBD		dB

**Note 1:** The IF section of this device is designed for optimum operating performance at 110 MHz to meet the DECT specifications.

**Note 2:** There was no matching network used on  $RF_{IN}$ . The matching circuit used on Mixer Out consisted of a series 150 nH inductance and a shunt 15 pF capacitance into the pin.

**Note 3:** Noise Figure measurements were made with a BPF on the input and matching networks on  $RF_{IN}$  and Mixer Out.

**Note 4:** The discriminator is in 3X mode with the DC level centered at 1.5V. The unloaded Q of the tank is 40.

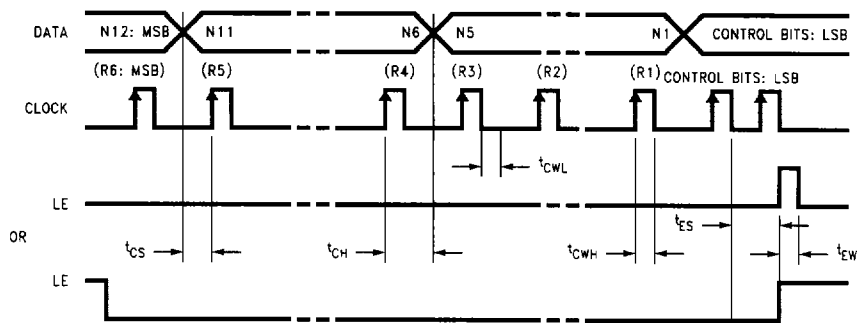
**Note 5:** Nominal refers to zero DC offsets programmed for the discriminator.

**Note 6:** Dependent on loss of inter stage filter. These specifications are for an interstage filter with a loss of 8 dB.

**Note 7:** See programmable modes for  $I_{cpo}$  description.

**Note 8:** Tested in a 50 $\Omega$  environment.

## Serial Data Input Timing



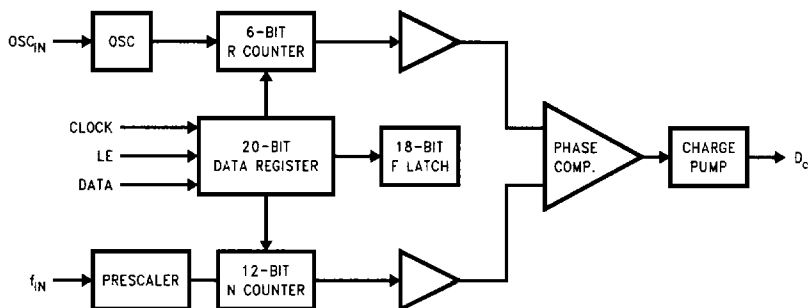
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**Notes:** Parenthesis data indicates programmable reference divider data.  
Data shifted into register on clock rising edge.  
Data is shifted in MSB first.

**Test Conditions:** The Serial Data Input Timing is tested using a symmetrical waveform around  $V_{CC}/2$ . The test waveform has an edge rate of 0.6V/ns.

## PLL Functional Description

The simplified block diagram below shows the 20-bit data register, 18-bit F latch, 12 bit N counter, and 6 bit R counter.



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The data stream is clocked on the rising edge of LE into the DATA input, MSB first. The last two bits are the control bits. DATA is transferred into the counters as follows:

Control Bits		DATA Location
C1	C2	
0	0	N Counter
0	1	R Counter
1	X	F Latch

X = Don't Care

## Programmable Divider (N Counters)

The N counter consists of the 6-bit swallow counter (A counter) and the 6-bit programmable counter (B counter). When the control bits are "00" data is transferred from the 20-bit shift register into two 6-bit latches. One latch sets the A counter while the other sets the B counter, MSB first. Serial data format is shown below.

LSB						MSB													
C1	C2	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	X	X	X	X	X	X
Control Bits		Divide Ratio of Programmable Divider, N										Don't Care							

### 6-Bit Swallow Counter Divide Ratio (A Counter)

Divide Ratio A	N6	N5	N4	N3	N2	N1
0	0	0	0	0	0	0
1	0	0	0	0	0	1
*	*	*	*	*	*	*
63	1	1	1	1	1	1

**Notes:** Divide ratio: 0 to 63

$B \geq A$

### 6-Bit Programmable Counter Divide Ratio (B Counter)

Divide Ratio B	N12	N11	N10	N9	N8	N7
3	0	0	0	0	1	1
4	0	0	0	1	0	0
*	*	*	*	*	*	*
63	1	1	1	1	1	1

**Notes:** Divide ratio: 3 to 63

$B \geq A$



## Programmable Reference Dividers (R Counters)

If the control bits are "01" data is transferred from the 20-bit shift register into a latch which sets the 6-bit R counter. Serial data format is shown below.

LSB		MSB																	
C1	C2	R1	R2	R3	R4	R5	R6	X	X	X	X	X	X	X	X	X	X	X	X
Control Bits		Divide Ratio of Reference Divider						Don't Care											

Divide Ratio R	R6	R5	R4	R3	R2	R1
3	0	0	0	0	1	1
4	0	0	0	1	0	0
*	*	*	*	*	*	*
63	1	1	1	1	1	1

Note: Divide ratio: 3 to 63

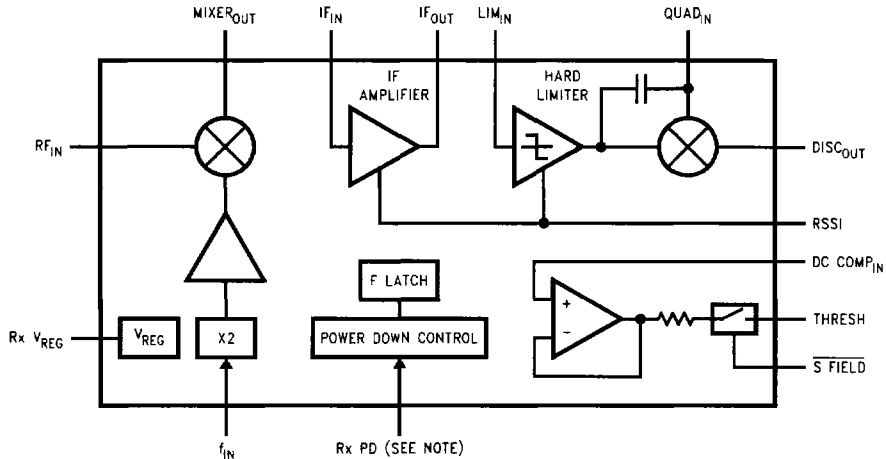
## Pulse Swallow Function

$$f_{vco} = [(P \times B) + A] \times f_{osc} / R$$

- $f_{vco}$ : Output frequency of external voltage controlled oscillator (VCO)
- B: Preset divide ratio of binary 6-bit programmable counter (3 to 63)
- A: Preset divide ratio of binary 6-bit swallow counter ( $0 \leq A \leq P$ ,  $A \leq B$ )
- $f_{osc}$ : Output frequency of the external reference frequency oscillator
- R: Preset divide ratio of binary 6-bit programmable reference counter (3 to 63)
- P: Preset modulus of dual modulus prescaler (32 or 64)

## Receiver Functional Description

The simplified block diagram below shows the mixer, IF amplifier, limiter, and discriminator. In addition, the DC compensation circuit, doubler, and voltage regulator for external LNA are shown. The limiter output is coupled on chip into the QUAD<sub>IN</sub> pin through a 1 pF capacitor. The receiver can be powered down through programmable control (see Programmable Modes).

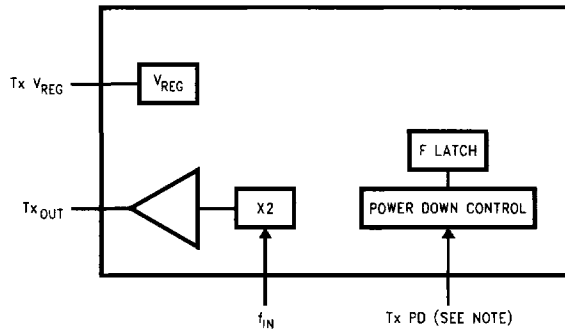


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**Note:** Receiver power down can be controlled by software through the F Latch or hardware through the Rx PD pin. This is determined by the state of F<sub>11</sub> and F<sub>12</sub> (see Programmable Modes). The quadrature tank circuit connected to the QUAD<sub>IN</sub> pin requires a DC bias which is the same as that connected to the discriminator power supply pin (Pin 35).

## Transmitter Functional Description

The simplified block diagram below shows the doubler and voltage regulator for external transmit gain stage. The transmitter can be powered down through programmable control (see Programmable Modes).



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**Note:** Transmitter power down can be controlled by software through the F Latch or hardware through the Tx PD pin. This is determined by the state of F<sub>11</sub> and F<sub>12</sub> (see Programmable Modes).

## Programmable Function Latch (F Latch)

If the control bits are "1X" data is transferred from the 20-bit shift register into the 18-bit F latch. Serial data format is shown below.

LSB																	MSB		
C1	C2	F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16	F17	F18

Control Bits

## Programmable Modes

Several modes of operation can be programmed with the function register bits F1–F18, including the phase detector polarity, charge pump TRI-STATE® and CMOS outputs. In addition, software or hardware power down modes may be selected with bits F11 and F12. The programmable modes are latched in when the control bits are: C1 = 1, C2 = X on the rising edge of LE. Truth tables for the programmable modes are shown in Tables I–III.

**TABLE I. Programmable Modes**

F1	Prescaler Modulus Select (32/64)
F2	Phase Detector Polarity
F3	Charge Pump Current
F4	Charge Pump TRI-STATE
F5	Reserved
F6	Receive Section Power Down
F7	Transmit Section Power Down
F8	Out 0 CMOS Output
F9	Out 1 CMOS Output/Receive Section Power Control Input
F10	Out 2 CMOS Output/Transmit Section Power Control Input
F11	Mode Select. See Mode Select Table
F12	Mode Select. See Mode Select Table
F13	Demodulator Gain 1X/3X
F14	Demodulator DC Level Shift ±
F15	Demodulator DC Level Shift of 1.000V
F16	Demodulator DC Level Shift of 0.500V
F17	Demodulator DC Level Shift of 0.250V
F18	Demodulator DC Level Shift of 0.125V

## Functional Description

F1	Pre-scaler modulus select. LOW selects 32/33 and HIGH selects 64/65.
F2	Phase Detector Polarity. F2 is used to reverse the polarity of the phase detector. Depending upon $V_{CO}$ characteristics, F2 should be set accordingly: When VCO characteristics are positive, F2 should be set HIGH; When VCO characteristics are negative, F2 should be set LOW.
F3	Charge pump current. LOW selects low charge pump current ( $1X I_{CPD}$ ). High selects HIGH charge pump current ( $4X I_{CPD}$ ).
F4	Charge Pump TRI-STATE.
F5	Reserved
F6–F7	Power down. When F11 = 0 and F12 = 0, F6 controls the state of the receive section and F7 controls the state of the transmit section. A LOW powers up the section while a HIGH powers down the section.
F8–F10	CMOS Outputs. When in the MICROWIRE control power down mode (F11 = 0, F12 = 0), F8, F9 and F10 sets the state of Out 0 (pin 20), Out 1 (pin 22) and Out 2 (pin 23) respectively.
F11–F12	Power Down Mode Control. See Table III.
F13	Demodulator Output Gain Control. LOW sets the 1X gain mode and HIGH sets the 3X gain mode.
F14–F18	Demodulator Output DC Level Shifting. F14 selects the level shifting polarity, LOW sets negative polarity and HIGH sets positive polarity. F15–F18 sets the level of DC shift with a HIGH. LOW corresponds to no shift.

TABLE II. Mode Select Truth Table

	F1 Pre-scaler Mod.	F2 Phase Det. polarity	F3 $I_{cpo}$	F4 $D_o$ TRI-STATE	F6-F7 Power Down Modes	F8-F10 CMOS Outputs
0	32/33	Negative	1X Mode (LOW)	Normal Operation	Powered Up	LOW
1	64/65	Positive	4X Mode (HIGH)	TRI-STATE	Powered Down	HIGH

TABLE IIIa. Power Down Modes

Function	F12	F11
Software Control (Note 1)	0	0
Test Mode (See Note 2)	0	1
Test Mode (See Note 2)	1	0
Hardwire Power Down (Note 1)	1	1

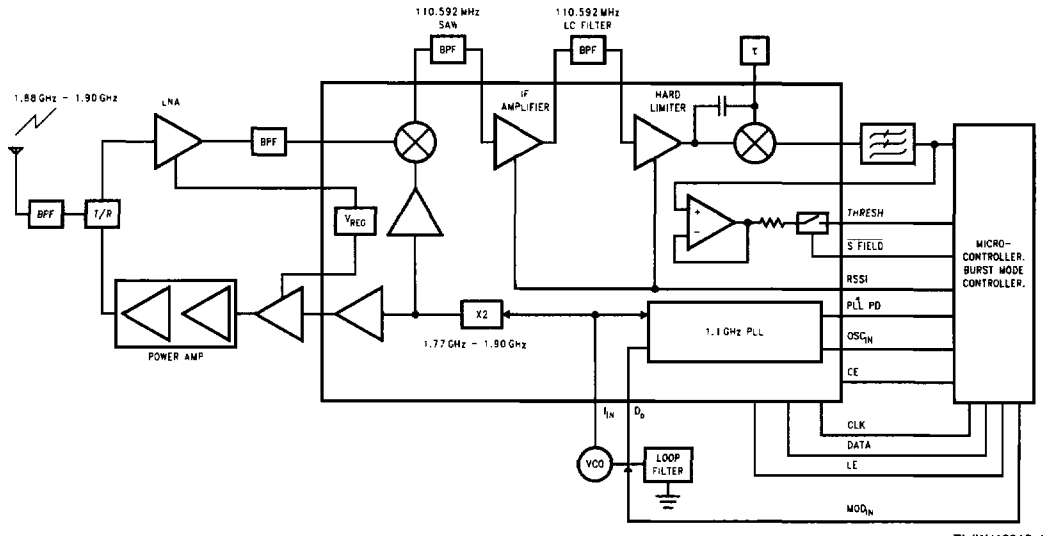
**Note 1:** PLL power control is a hardwire power down regardless of Power Down Modes.

**Note 2:** Not used in application.

TABLE IIIb. Power Control Modes

		High	Low
Software Control	F6	Receiver Off	Receiver On
	F7	Transmitter Off	Transmitter On
Hardwire Control	Rx PD (Pin 22)	Receiver On	Receiver Off
	Tx PD (Pin 23)	Transmitter On	Transmitter Off
PLL Control	PLL PD	PLL Off	PLL On

### Typical Application Block Diagram



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### DECT System Calculation for 3.6V Operation

	Filter and Switch	External LNA	Image Filter	Mixer	SAW	IF Amplifier	Interstage Filter	Cascade Total
NF (dB)	2	2	1.5	10	11	8	8	6.21
Gain (dB)	-2	12	-1.5	15	-11	25	-8	29.50
OIP3 (dBm)	100	7	100	5	100	50	100	10.88
P <sub>OUT</sub> (dBm)	-95.0	-83.0	-84.5	-69.5	-80.5	-55.5	-63.5	
NF+ (dB)		1.09	0.04	1.58	0.05	0.32	0.00	
OIP3+ (dBm)	0.00	0.12	0.00	15.50	0.00	0.00		
Input Power (dBm)	-93.00		Eb/No (dB)	14.77	Input IP3 (dBm)		-18.62	

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**Note:** Assumes 50 dB attenuation of interferer by the SAW filter and 8 dB attenuation by the LC (interstage) filter. Cascaded totals in Input IP3 are calculated at the output of the interstage filter.



## Application Information

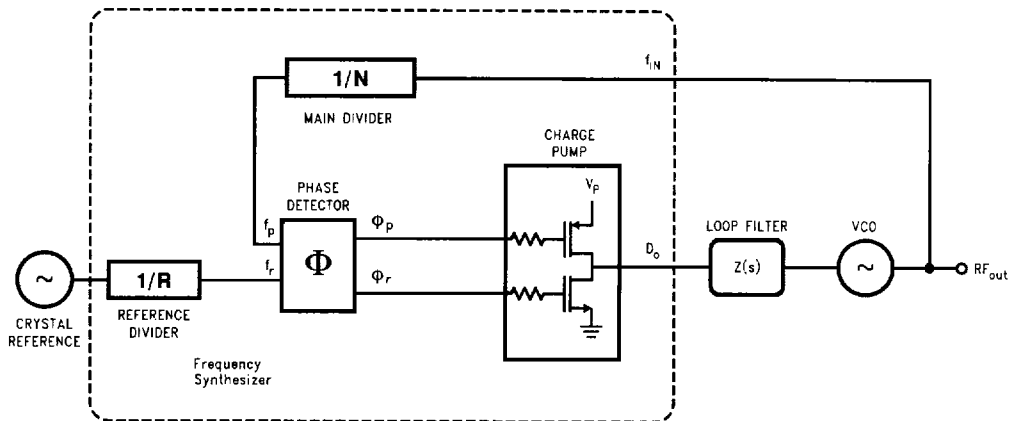
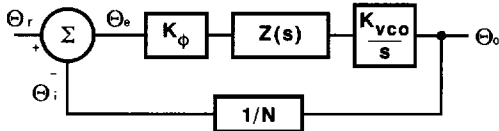


FIGURE 1. Conventional PLL Architecture

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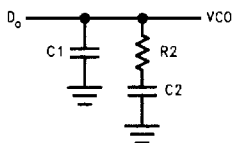
### Loop Gain Equations

A linear control system model of the phase feedback for a PLL in the locked state is shown in Figure 2. The open loop gain is the product of the phase comparator gain ( $K_\phi$ ), the VCO gain ( $K_{VCO}/s$ ), and the loop filter gain  $Z(s)$  divided by the gain of the feedback counter modulus ( $N$ ). The passive loop filter configuration used is displayed in Figure 3, while the complex impedance of the filter is given in Equation 2.



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FIGURE 2. PLL Linear Model



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FIGURE 3. Passive Loop Filter

#### PASSIVE LOOP FILTER

Open loop gain =  $H(s) G(s) = \Theta_i / \Theta_e = K_\phi Z(s) K_{VCO} / Ns$  (1)

$$Z(s) = \frac{s(C2 \cdot R2) + 1}{s^2(C1 \cdot C2 \cdot R2) + sC1 + sC2} \quad (2)$$

The time constants which determine the pole and zero frequencies of the filter transfer function can be defined as

$$T1 = R2 \cdot \frac{C1 \cdot C2}{C1 + C2} \quad (3a)$$

and

$$T2 = R2 \cdot C2 \quad (3b)$$

The 3rd order PLL Open Loop Gain can be calculated in terms of frequency,  $\omega$ , the filter time constants  $T1$  and  $T2$ , and the design constants  $K_\phi$ ,  $K_{VCO}$ , and  $N$ .

$$G(s) \cdot H(s) \Big|_{S=j\omega} = \frac{-K_\phi \cdot K_{VCO}(1 + j\omega \cdot T2)}{\omega^2 C1 \cdot N(1 + j\omega \cdot T1)} \cdot \frac{T1}{T2} \quad (4)$$

From Equation 3 we can see that the phase term will be dependent on the single pole and zero such that the phase margin is determined in Equation 5.

$$\phi(\omega) = \tan^{-1}(\omega \cdot T2) - \tan^{-1}(\omega \cdot T1) + 180^\circ \quad (5)$$