

Description

This device consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable \overline{GAB} and \overline{GBA} are provided to control the transceiver functions. \overline{SAB} and \overline{SBA} control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the HD74AC651.

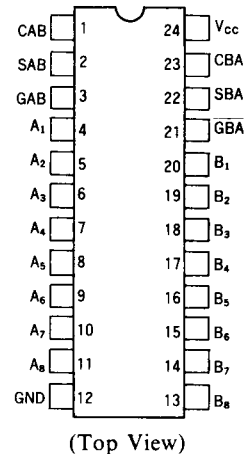
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to high transition at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When \overline{SAB} and \overline{SBA} are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling Enable \overline{GAB} and \overline{GBA} . In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data Transfers
- 3-State Outputs
- 300 mil Slim Dual In-Line Package
- Outputs Source/Sink 24 mA
- HD74ACT6 has TTL-Compatible Inputs

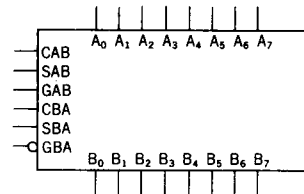
Pin Names

- A_0 - A_7 Data Register A Inputs
- Data Register A Outputs
- B_0 - B_7 Data Register B Inputs
- Data Register B Outputs
- CAB,CBA Clock Pulse Inputs
- $\overline{SAB},\overline{SBA}$ Transmit/Receive Inputs
- $\overline{GAB},\overline{GBA}$ Output Enable Inputs

Pin Assignment

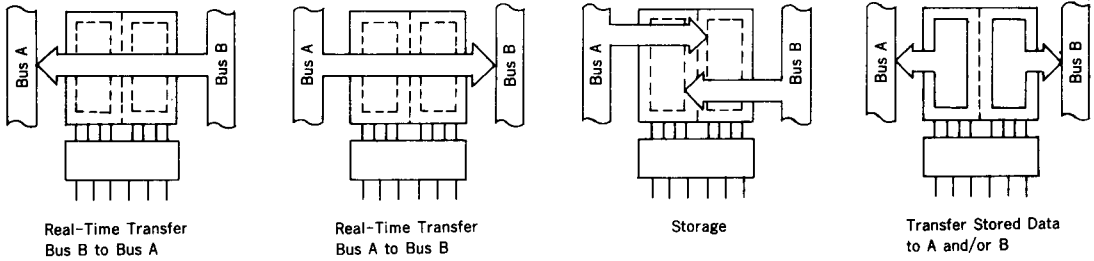


Logic Symbol

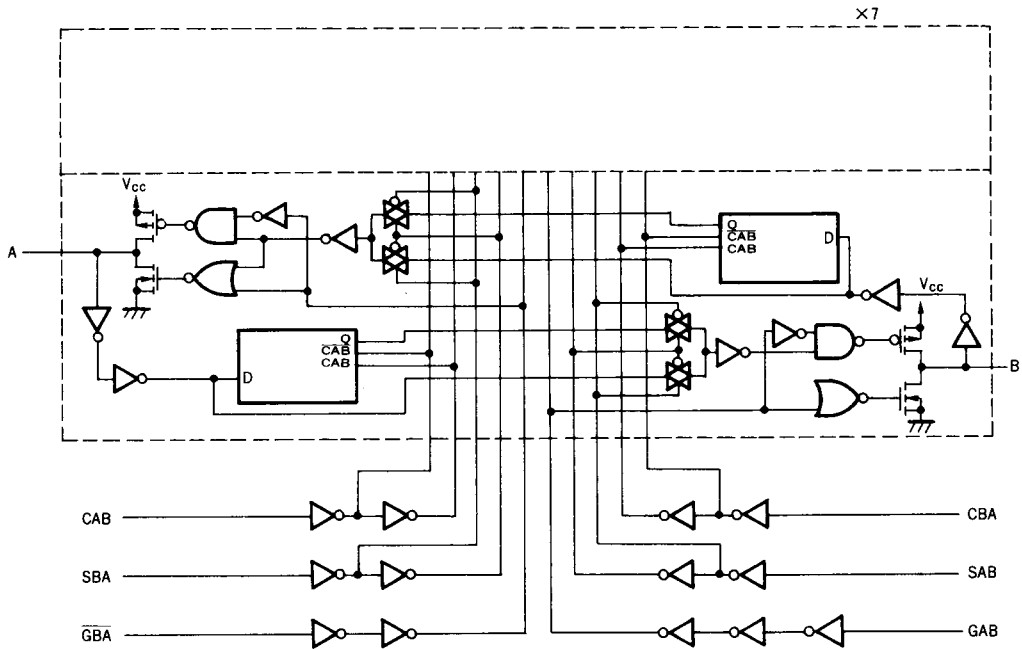


Function Table

	Real-Time Transfer Bus B to Bus A	Real-Time Transfer Bus A to Bus B	Storage	Transfer Stored Data to A and/or B
CAB	X	X		L or H
SAB	X	L	X	H
GAB	L	H	L	H
CBA	X	X		L or H
SBA	L	X	X	H
\overline{GBA}	L	H	H	L



Logic Diagram



DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
I_{cc}	Maximum Quiescent Supply Current	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5V$, $T_a = \text{Worst Case}$
I_{cc}	Maximum Quiescent Supply Current	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5V$, $T_a = 25^\circ C$
I_{ccT}	Maximum Additional I_{cc} /Input(HD74ACT651)	1.5	mA	$V_{IN} = V_{CC} - 2.1V$ $V_{CC} = 5.5V$, $T_a = \text{Worst Case}$

HD74AC651/HD74ACT651

AC Characteristics: HD74AC651

Symbol	Parameter	Vcc* (V)	Ta = +25°C CL = 50pF			Ta = -40°C to +85°C CL = 50pF		Unit
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay Clock to Bus	3.3 5.0	1.0 1.0		18.0 13.0	1.0 1.0	20.5 14.5	ns
t _{PHL}	Propagation Delay Clock to Bus	3.3 5.0	1.0 1.0		18.0 13.0	1.0 1.0	20.5 14.5	ns
t _{PLH}	Propagation Delay Bus to Bus	3.3 5.0	1.0 1.0		13.5 9.5	1.0 1.0	14.5 10.5	ns
t _{PHL}	Propagation Delay Bus to Bus	3.3 5.0	1.0 1.0		13.5 9.5	1.0 1.0	14.5 10.5	ns
t _{PLH}	Propagation Delay SBA or SAB to An or Bn (with An or Bn HIGH or LOW)	3.3 5.0	1.0 1.0		14.0 10.0	1.0 1.0	15.5 11.0	ns
t _{PHL}	Propagation Delay SBA or SAB to An or Bn (with An or Bn HIGH or LOW)	3.3 5.0	1.0 1.0		14.0 10.0	1.0 1.0	15.5 11.0	ns
t _{PZH}	Enable Time GAB or GBA to An or Bn	3.3 5.0	1.0 1.0		14.0 16.0	1.0 1.0	15.5 11.0	ns
t _{PZL}	Enable Time GAB or GBA to An or Bn	3.3 5.0	1.0 1.0		14.5 10.5	1.0 1.0	16.0 11.5	ns
t _{PHZ}	Disable Time GAB or GBA to An or Bn	3.3 5.0	1.0 1.0		17.5 12.5	1.0 1.0	19.5 14.0	ns
t _{PLZ}	Disable Time GAB or GBA to An or Bn	3.3 5.0	1.0 1.0		17.0 12.0	1.0 1.0	19.0 13.5	ns

* Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements: HD74AC651

Symol	Parameter	Vcc* (V)	Ta = +25°C CL = 50pF		Ta = -40°C to +85°C CL = 50pF	Unit
			Typ	Guaranteed Minimum		
t _{SU}	Setup Time, HIGH or LOW Bus to Clock	3.3 5.0		5.5 4.5	5.5 5.0	ns
t _H	Hold Time, HIGH or LOW Bus to Clock	3.3 5.0		1.5 1.5	1.5 1.5	ns
t _w	Clock Pulse Width HIGH or LOW	3.3 5.0		5.0 4.5	5.5 5.0	ns

* Voltage Range 3.3 is 3.3V ± 0.3V
Voltage Range 5.0 is 5.0V ± 0.5V

AC Characteristics: HD74ACT651

Symbol	Parameter	V _{CC} * (V)	T _a = +25°C C _L = 50pF			T _a = -40°C to +85°C C _L = 50pF		Unit
			Min	Typ	Max	Min	Max	
f _{max}	Maximum Clock Frequency	5.0	70			60		MHz
t _{PLH}	Propagation Delay Clock to Bus	5.0	1.0		14.5	1.0	16.0	ns
t _{PHL}	Propagation Delay Clock to Bus	5.0	1.0		14.5	1.0	16.0	ns
t _{PLH}	Propagation Delay Bus to Bus	5.0	1.0		10.5	1.0	11.5	ns
t _{PHL}	Propagation Delay Bus to Bus	5.0	1.0		10.5	1.0	11.5	ns
t _{PLH}	Propagation Delay SBA or SAB to An or Bn (An or Bn LOW)	5.0	1.0		11.5	1.0	12.5	ns
t _{PHL}	Propagation Delay SBA or SAB to An or Bn (An or Bn LOW)	5.0	1.0		11.5	1.0	12.5	ns
t _{PLH}	Propagation Delay SBA or SAB to An or Bn (An or Bn HIGH)	5.0	1.0		11.5	1.0	12.5	ns
t _{PHL}	Propagation Delay SBA or SAB to An or Bn (An or Bn HIGH)	5.0	1.0		11.5	1.0	12.5	ns
t	Enable Time	5.0	1.0		11.0	1.0	12.0	ns
t	Enable Time	5.0	1.0		11.0	1.0	12.0	ns
t	Disable Time	5.0	1.0		13.0	1.0	14.5	ns
t	Disable Time	5.0	1.0		12.5	1.0	14.0	ns

* Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements: HD74AC651

Symbol	Parameter	V _{CC} * (V)	T _a = +25°C C _L = 50pF		T _a = -40°C to +85°C C _L = 50pF		Unit
			Typ	Guaranteed Minimum			
t _{SU}	Setup Time, Bus to Clock HIGH or LOW	5.0		7.0	8.0		ns
t _H	Hold Time, Bus to Clock HIGH or LOW	5.0		1.5	1.5		ns
t _w	Clock Pulse width HIGH or LOW	5.0		7.0	8.0		ns

* Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Unit	Condition
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.5V
C _{PD}	Power Dissipation Capacitance		pF	V _{CC} = 5.5V
C _{I/O}	Input/Output Capacitance	15.0	pF	V _{CC} = 5.0V