TMC2340
Digital Synthesizer
Dual 16-Bit, 25 MOPS

Description

The TMC2340 performs waveform synthesis, modulation, and demodulation. When presented with a TTL clock signal and user-selected 15-bit amplitude and 32-bit phase increment values, the TMC2340 automatically generates quadrature-matched pairs of 16-bit sine and cosine waves in DAC-compatible 16-bit offset binary format. If desired, these waveforms are easily phase or frequency-modulated on-chip, and the amplitude input facilitates gain adjustment or amplitude modulation. Digital output frequencies are restricted only by the Nyquist limit of clock rate/2, with frequency resolution of 0.006 Hz at the guaranteed maximum 25 MHz clock rate.

A new data word pair is available at the output every clock cycle. All input and output data ports are registered, with a user-configurable phase accumulator structure and input clock enables to simplify interfacing. The phase data range over a full 2∏ radians. All signals are TTL compatible.

Fabricated in Raytheon Semiconductor's OMICRON-C™ one-micron CMOS process, the TMC2340 operates at the 25 MHz maximum clock rate over the full commercial temperature (0 to 70°C) and supply (4.75 to 5.25V) voltage ranges, and is available in a low-cost 120 pin plastic pin grid array. The MIL-STD-883 version, the TMC2340L5V, is housed in a ceramic chip carrier and is specified over the full extended (-55°C to 125°C) case temperature range.

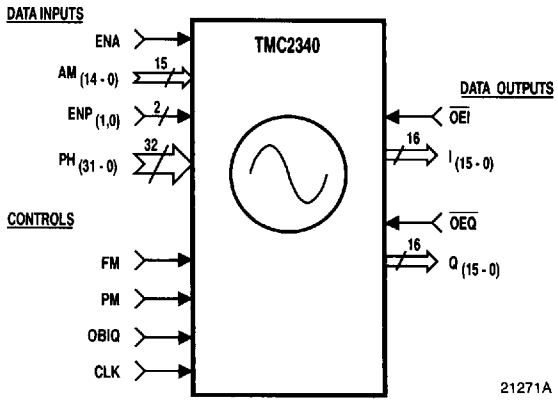
Features

- User-configurable phase accumulator for waveform synthesis, frequency modulation or phase modulation
- Amplitude input for gain adjustment and amplitude modulation
- Guaranteed 25 Msps pipelined data throughput rate
- 15-bit magnitude, 32-bit phase data input precision
- 16-bit offset binary or 15-bit unsigned magnitude output data format
- Input register clock enables simplify interfacing
- Low power consumption CMOS process
- Single +5V power supply
- Available in a 120-pin plastic pin grid array package
- Compliant with MIL-STD-883B in a 132-leaded CERQUAD

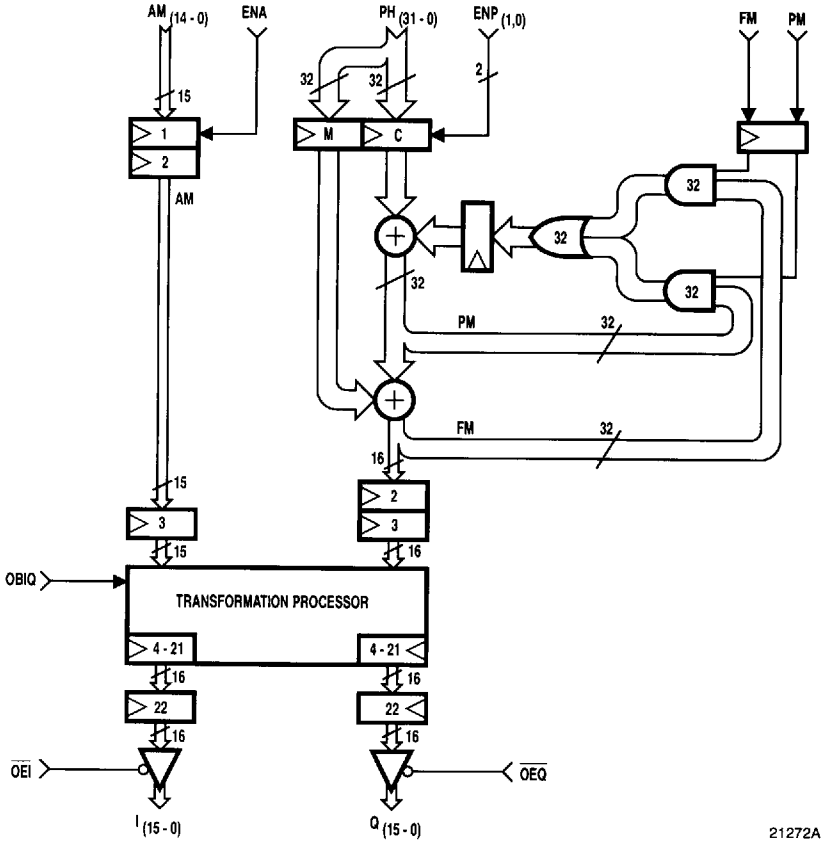
Applications

- Digital waveform synthesis, including quadrature functions
- Digital modulation and demodulation

TMC2340 Logic Symbol



Functional Block Diagram



Functional Description

General Information

The TMC2340 converts Polar (Phase and Magnitude) data into Rectangular (Cartesian) format. The first transformed result is available at the outputs 22 clock cycles after startup, with new output data available every 40ns. All input and output data ports are registered, with input clock enables to simplify system bus connections.

The input ports accept 15-bit amplitude and 32-bit phase data, and the output ports produce 16-bit Rectangular data words in either 16-bit offset binary or 15-bit unsigned magnitude format. The 32-bit phase accumulator handles high-accuracy (0.006Hz at the maximum clock rate) phase increment values with minimal accumulation error. The flexible input phase accumulator structure supports frequency or phase modulation, as determined by the input register clock enable $ENYP_{1,0}$ and accumulator controls FM and PM. The 16 MSBs (Most Significant Bits) of phase data are used in the transformation itself.

Signal Definitions

Power

V_{DD}, GND — The TMC2340 operates from a single +5V supply. All power and ground pins must be connected.

Clock

CLK — The TMC2340 operates from a single clock. All enabled registers are strobed on the rising edge of CLK, which is the reference for all timing specifications.

Inputs/Outputs

AM_{14-0} — AM_{14-0} is the registered peak amplitude 15-bit input data port. AM_{14} is the MSB.

PH_{31-0} — PH_{31-0} is the registered Phase angle increment 32-bit input data port. The input phase accumulators are fed through this port in conjunction with the input enable select $ENP_{1,0}$. PH_{31} is the MSB.

I_{15-0} — I_{15-0} is the registered X-coordinate 16-bit output data port. This output is forced into the high-impedance state when $\overline{OEI}$=HIGH. I_0 is the LSB. I_{15} will be "stuck at" logic HIGH if OBIQ=0.

Q_{15-0} — Q_{15-0} is the registered Cartesian Y-coordinate 16-bit output data port. This output is forced to the high-impedance state when $\overline{OEQ}$=HIGH. Q_0 is the LSB. Q_{15} will remain at logic HIGH if OBIQ=0.

Controls

ENA — Data presented to the input port AM are latched into the input registers on the current clock when ENA is HIGH. When ENA is LOW, the data stored in the register remains unchanged.

$ENP_{1,0}$ — The value presented to the PH input port is latched into the phase accumulator input registers on the current clock, as determined by the control inputs $ENP_{1,0}$, as shown below:

$ENP_{1,0}$	Instruction
00	No registers enabled, current data held
01	M register input enabled, C data held
10	C register input enabled, M data held
11	M register set to 0, C register input enabled

where C is the Carrier register and M is the Modulation register, and 0=LOW, 1=HIGH. See the *Functional Block Diagram*.

FM, PM — The user determines the internal phase Accumulator structure implemented on the next clock by setting the accumulator control word FM, PM, as shown below:

FM, PM	Instruction
00	No accumulation performed
01	PM accumulator path enabled
10	FM accumulator path enabled
11	(Nonsensical) logical OR of PM and FM

where 0=LOW, 1=HIGH. See the *Functional Block Diagram*.

The accumulator will roll over correctly when full-scale is exceeded, allowing the user to perform continuous phase accumulation through 2π radians, or 360 degrees.

OBIQ — The format select control sets the numeric format of the Rectangular data: offset binary format when HIGH, and unsigned when LOW. This is a static input. See the *Timing Diagram*.

$\overline{OEI}$, $\overline{OEQ}$ — Data in the output registers are available at the outputs of the device when the respective asynchronous Output Enables are LOW. When $\overline{OEX}$ or $\overline{OEY}$ is HIGH, the respective output port is in the high-impedance state.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins	L5 Package Pins
Power	V_{DD}	Supply Voltage	C3, E3, H3, L4, L6, L8, L11, F11, E11, C11, C8, C6	1, 9, 21, 37, 45, 53, 67, 87, 91, 99, 112, 120
	GND	Ground	D3, E2, E1, F2, G3, K3, L3, L7, K11, J11, G11, F12, E12, D11, C10, C9, B7, C7, C5, C4	5, 11, 12, 14, 17, 29, 33, 49, 75, 83, 86, 89, 95, 104, 108, 115, 116, 124, 129
Clock	CLK	System Clock	F3	13
Inputs	AM_{14-0}	Radius Data	F13, G13, G12, H13, H12, H11, J13, J12, K13, K12, L13, L12, M13, M12, N13	85, 84, 82, 81, 80, 79, 78, 77, 76, 74, 73, 71, 69, 68, 66
	PH_{31-0}	Phase Data	L10, N12, N11, M10, L9, N10, M9, N9, M8, N8, N7, M7, N6, M6, N5, M5, N4, L5, M4, N3, M3, N2, M2, N1, L2, M1, L1, K2, J3, K1, J2, J1	61, 60, 59, 58, 57, 56, 55, 54, 52, 51, 50, 48, 47, 46, 44, 43, 42, 41, 40, 39, 38, 36, 34, 31, 30, 28, 27, 26, 25, 24, 23, 22
Outputs	I_{15-0}	I Data	D13, D12, C13, B13, C12, A13, B12, A12, B11, A11, B10, A10, B9, A9, B8, A8	90, 92, 93, 94, 96, 97, 100, 102, 105, 106, 107, 109, 110, 111, 113, 114
	Q_{15-0}	Q Data	A7, A6, B6, A5, B5, A4, B4, A3, A2, B3, A1, B2, B1, C2, C1, D2	117, 118, 119, 121, 122, 123, 125, 126, 127, 130, 132, 3, 4, 6, 7, 8
Controls	ENR	Radius In Enable	M11	63
	$ENP_{1,0}$	Phase In Enable	G1, G2	18, 16
	FM, PM	Modulation	H2, H1	20, 19
	OBIQ	Cartesian Data Format	F1	15
	$\overline{OEI}$	I Out Enable	E13	88
	$\overline{OEQ}$	Q Out Enable	D1	10
No Connect	NC	No Connect Pins	–	2, 32, 35, 62, 64, 65, 72, 98, 101, 103, 128, 131
		Index Pin	D4	–

Static Control Input

OBIQ determines the numeric format of the output data: offset binary if HIGH and unsigned magnitude if LOW. This control acts with 2-cycle latency on the chip's 22-cycle data path and is normally hardwired to a system-specific state.

Table 1. Data Input/Output Formats – Integer Format

Port	OBIQ	Bit # 31	30	29	. . .	16	15	14	. . .	0	Format
AM	X							2^{14}	. . .	2^{0}.	U
PH	X	$\pm 2^{0}$	2^{-1}	2^{-2}	. . .	2^{-15}	2^{-16}	2^{-17}	. . .	2^{-31}	($\times\pi$) T/U
I	0							2^{14}	. . .	2^{0}.	U
I	1						2^{15}	2^{14}	. . .	2^{0}.	B
Q	0							2^{14}	. . .	2^{0}.	U
Q	1						2^{15}	2^{14}	. . .	2^{0}.	B

Notes:

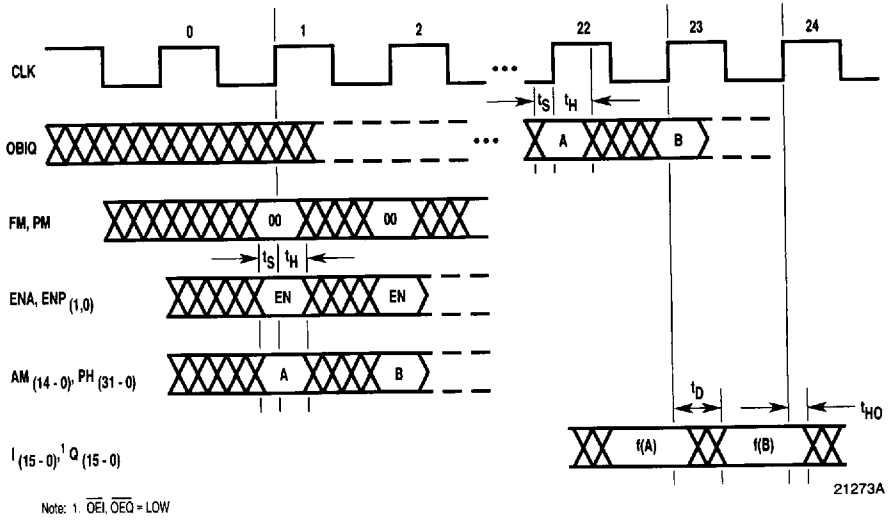
1. $\pm 2^{0}$ denotes two's complement sign or highest magnitude bit - since phase angles are module 2π and phase accumulator is module 2^{32}, this bit may be regarded as $\pm\pi$.
2. All phase angles are in terms of π radians, hence notation "$x\pi$."
3. A sign-and-magnitude "Q" output is obtained by appending the input bit PH_{31} as a sign bit to the corresponding (i.e., delayed 22 cycles) $Q_{14\text{-}0}$.
4. A sign-and-magnitude "I" output is obtained by appending the exclusive OR of PH_{31} and PH_{30} as a sign bit to the corresponding $I_{14\text{-}0}$.
5. When OBIQ=0, outputs I_{15} and Q_{15} become "do not connects" and will stay logic HIGH. (They may be wired to V_{DD}, left open, or connected to any logic input without damage to the part or excessive power consumption.)
6. Formats:

   T/U = Two's Complement/Unsigned Magnitude 32 Bits
   U = Unsigned Magnitude 15 Bits
   B = Offset Binary 16 Bits

AM, I, Q			PH	
HEX	U	B	T	U
FFFF		32767	$-\pi \cdot 2^{-15}$	$\pi(2-2^{-15})$
– –	– –	– –		
8001		1	$-\pi(1-2^{-15})$	$\pi(1+2^{-15})$
8000		0	$-\pi$	π
7FFF	32767	–1	$\pi(1-2^{-15})$	$\pi(1-2^{-15})$
– –	– –	– –		
0001	1	–32767	$\pi \cdot 2^{-15}$	$\pi \cdot 2^{-15}$
0000	0	–32768	0	0

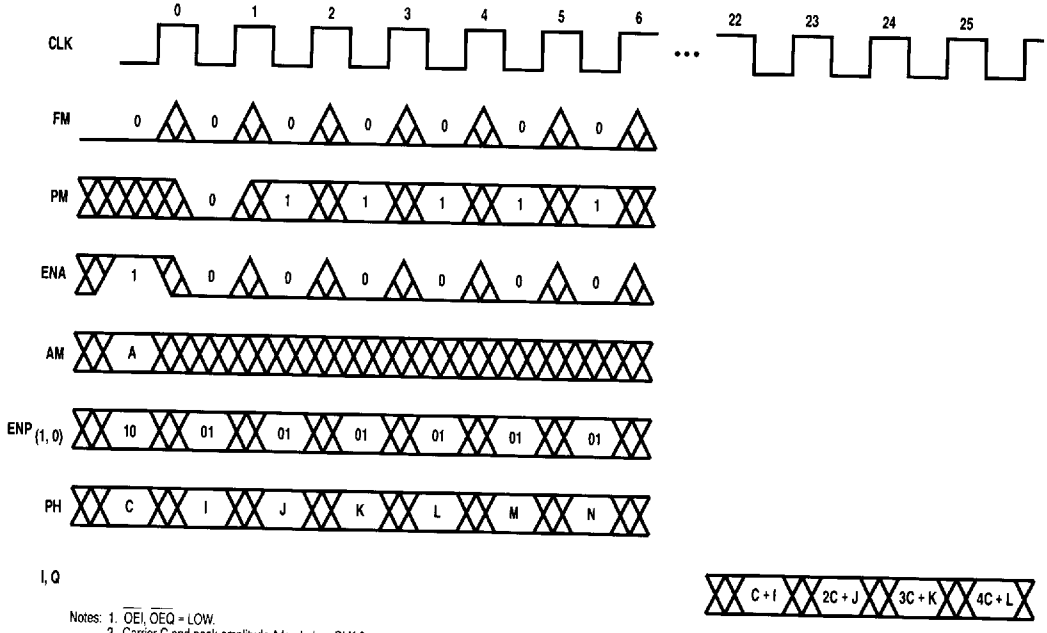
"Hex" column contains the 16 MSBs of the 32-bit phase input (16 LSBs are 0), the 15 bits of the amplitude input or the 16 bits of the offset binary output.

Figure 1. Timing Diagram, Operating Conditions



Note: 1. $\overline{OEI}$, $\overline{OEQ}$ = LOW

Figure 2. Timing Diagram, Phase Modulation



Notes: 1. $\overline{OEI}$, $\overline{OEQ}$ = LOW.
2. Carrier C and peak amplitude A loaded on CLK 0.
3. Modulation values I, J, K, L, . . . loaded on CLK 1, CLK 2, etc.
4. Output corresponding to modulation loaded at CLK i emerged t_{DO} after CLK i + 21.
5. To modulate amplitude, vary AM with ENA = 1.

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Figure 3. Equivalent Input Circuit

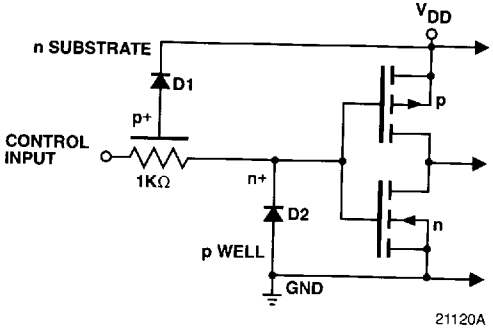

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Figure 4. Equivalent Output Circuit

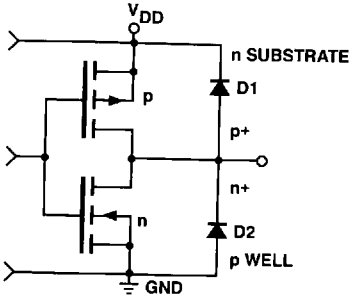

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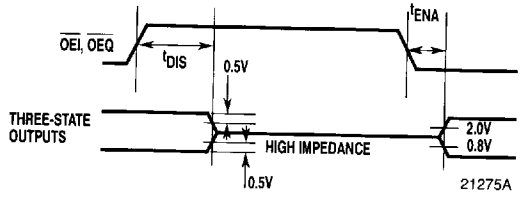
Figure 5. Transition Levels for Three-State Measurements



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Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5 to (V_{DD}+0.5)V

Output Voltage

Applied voltage ..... −0.5 to (V_{DD}+0.5)V [2]

Forced current ..... −6.0 to 6.0mA [3,4]

Short-circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, case ..... −60 to +130°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
V_{DD}	Supply Voltage		4.75	5.25	4.5	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8		0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0		2.0		V
I_{OL}	Output Current, Logic LOW			8.0		8.0	mA
I_{OH}	Output Current, Logic HIGH			-4.0		-4.0	mA
t_{CY}	Cycle Time	V_{DD}=Min		50		55	ns
		TMC2340-1		40		45	ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD}=Min	10		11		ns
		TMC2340-1	8		8		ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD}=Min	8		8		ns
		TMC2340-1	6		6		ns
t_S	Input Setup Time		12		13		ns
		TMC2340-1	10		11		ns
t_H	Input Hold Time		1		2		ns
		TMC2340-1	1		2		ns
T_A	Ambient Temperature, Still Air		0	70			°C
T_C	Case Temperature				-55	125	°C

Electrical characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		10		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 20MHz $\overline{OEI}$ and $\overline{OEQ}$ = V_{DD}		160		160	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V		−10		−10	μA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}		10		10	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V		−40		−40	μA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}		40		40	μA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.	−20	−100	−20	−100	μA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but specified operation is guaranteed.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF		22		25	ns
		TMC2340-1		20		23	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 40pF		4		4	ns
		TMC2340-1		4		4	ns
t_{ENA}	Output Enable Delay	V_{DD} = Min, C_{LOAD} = 40pF		13		17	ns
		TMC2340-1		12		15	ns
t_{DIS}	Output Disable Delay	V_{DD} = Min, C_{LOAD} = 40pF		14		14	ns
		TMC2340-1		13		13	ns

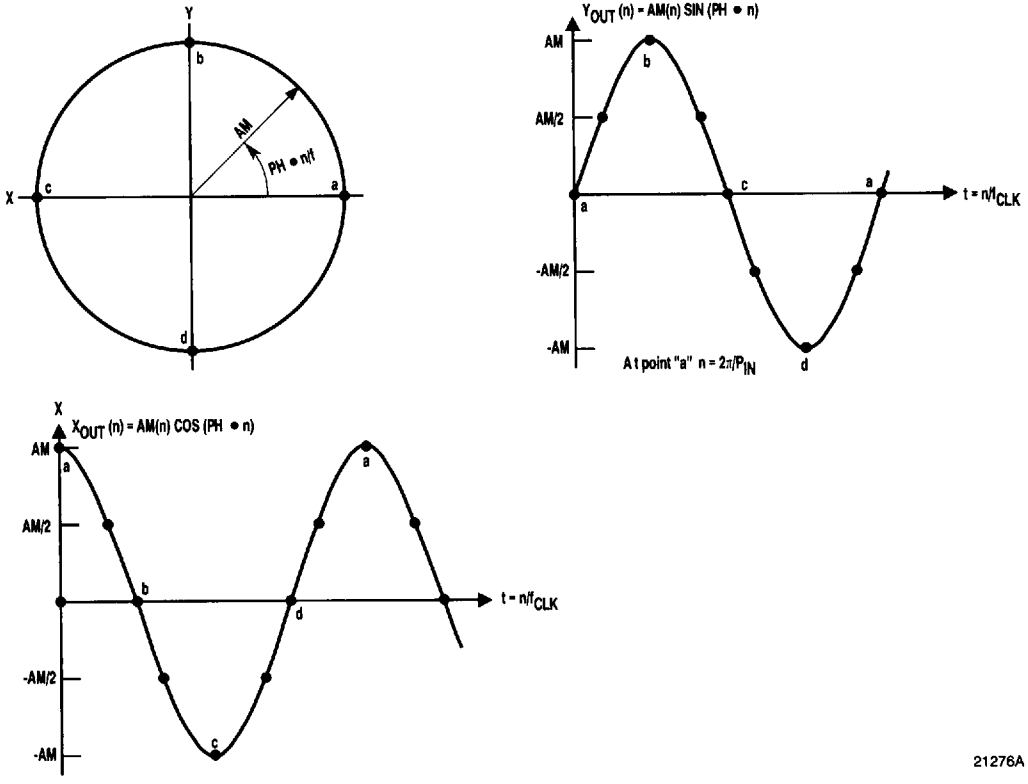
Phase/Amplitude to Sine/Cosine Conversion Geometry

Polar-To-Rectangular Conversion Geometry

The TMC2340 performs a coordinate-space transformation according to the familiar trigonometric relationships shown in *Figure 6*.

With constant amplitude and phase increment values and either FM or PM HIGH, the TMC2340 will output a series of complex number pairs representing the horizontal and vertical projections of a vector rotating about the origin, i.e., a cosine wave and a sine wave.

Figure 6. Input to Output Relationship for Sinusoid Generation



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Digital Waveform Synthesis

Waveform Generation and Modulation

Utilizing the internal phase accumlators in a TMC2340, users can easily generate high-accuracy digital quadrature *sinusoidal* waveforms with minimal support. The 32-bit data path ensures negligible cumulative error in most applications, and the accuracy of the transform is limited only by the truncation of the result to 16 bits prior to the Transform Processor and the ±1 LSB maximum error of the transform algorithm. Amplitude Modulation is of course performed simply by varying the amplitude input. Either Frequency (phase angle shifted by the cumulative sum of the modulation input) or Phase (phase angle shifted by the instantaneous modulation input) Modulation can be realized by configuring the TMC2340 as shown in *Figures 7 and 8*.

In *Figure 7*, the output valid during clock rising edge m+22 is:

$$I_{m+22} = AM_m \cos(PH_m + mPC)$$
$$Q_{m+22} = AM_m \sin(PH_m + mPC)$$

where PH_m and AM_m are the chip inputs at rising edge m, PC is the (constant) carrier phase increment, $PM_1 = 0$, $PM_{2,...m} = 1$, and $FM_{1\text{-}m} = 0$.

Expressed in terms of time instead of clock cycles,

$$I_{(m+22)/f_{clk}} = AM_{m/f_{clk}} \cos(PH_{m/f_{clk}})$$

where f_{clk} is the frequency of the square wave applied to CLK.

Figure 7. Performing Phase Modulation

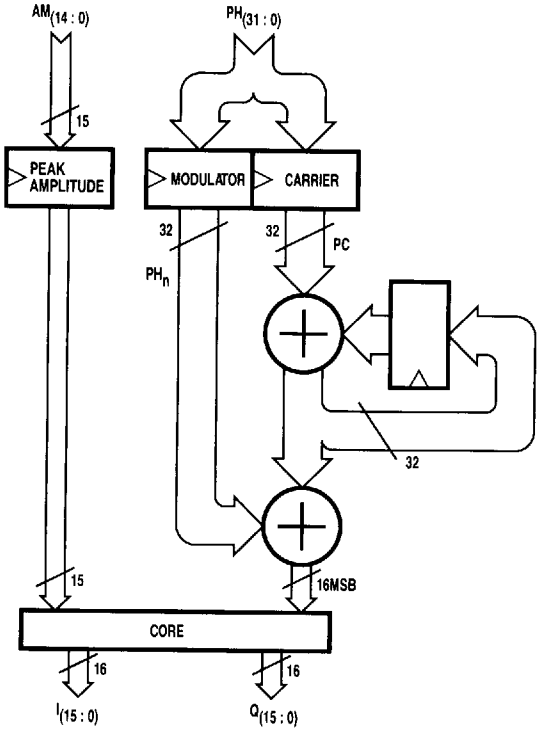

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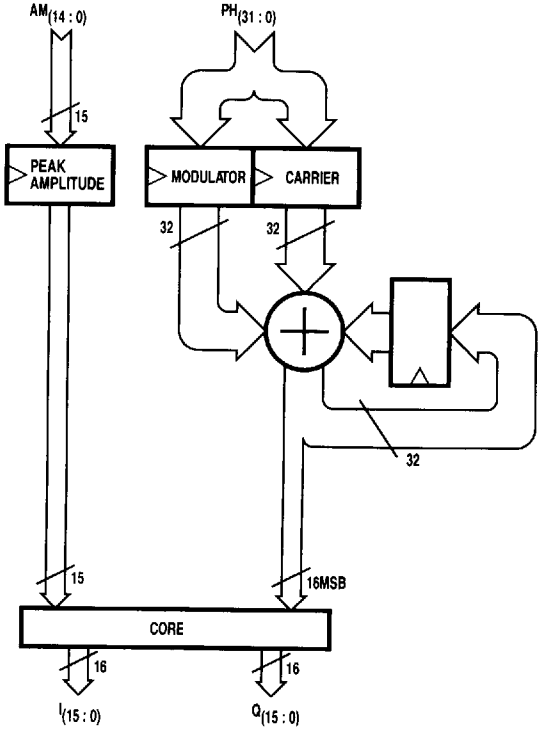
Figure 8. Performing Frequency Modulation



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In *Figure 8*, the output valid during clock rising edge n+22 is:

$$I_{m+22} = AM_m \cos\left(\sum_{m=1}^{n} PH_m + nPC\right)$$

$$Q_{n+22} = AM_m \sin\left(\sum_{m=1}^{n} PH_m + nPC\right)$$

where PH_m and AM_m are the chip inputs at rising edge AM, PC is the (constant) carrier phase increment, $FM_1 = 0$, $FM_{2...n} = 1$, and PM = 0.

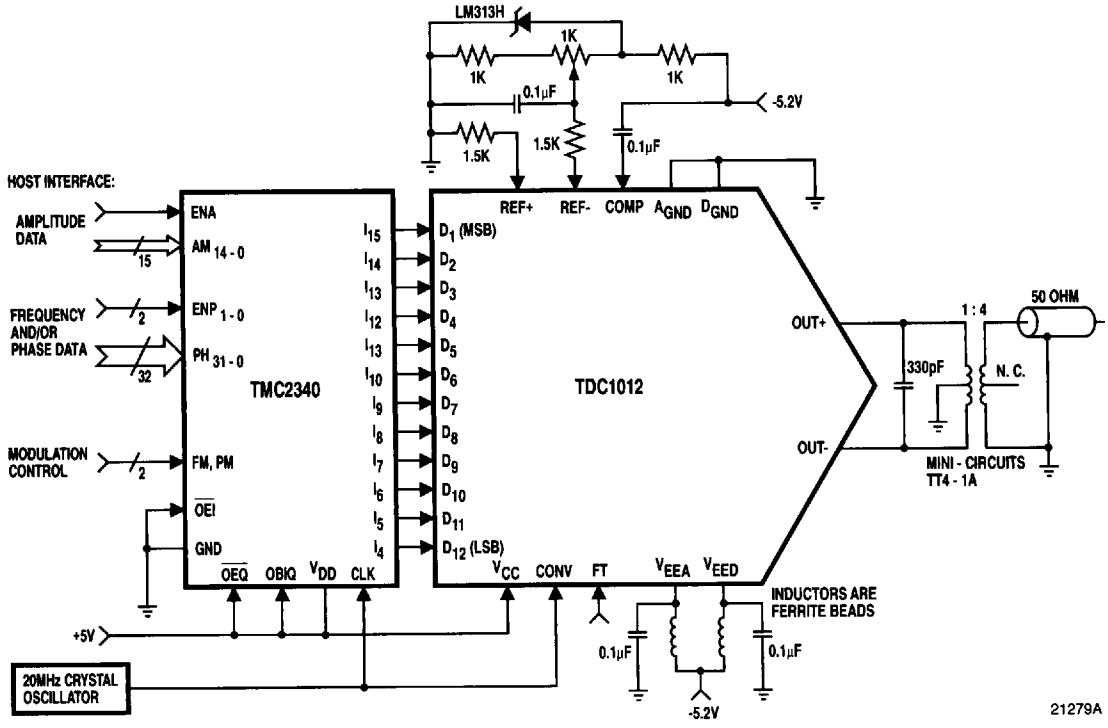
Expressed in terms of time instead of clock cycles,

$$I_{(n+22)/fclk} = AM_{m/fclk} \cos\left(\sum_{m-1}^{n} PH_{m/fclk} + PC \bullet m/fclk\right)$$

Digital Synthesizer with TDC1012 D/A Converter

Connection of the TMC2340 to the TDC1012 D/A converter is straightforward. As shown in *Figure 9*, the TDC1012 data lines are connected to either the I or Q outputs. Both outputs may be used, with two TDC1012's for quadrature synthesis.

Figure 9. Frequency Synthesizer



Note: To use two TDC1012's in quadrature, connect second TDC1012 to Q_{15} (MSB) to Q_4 and ground $\overline{OEQ}$.

Control of the TMC2340

The TMC2340 needs to be initialized to tell it what frequency and amplitude sinusoid to generate. To initialize amplitude, apply the desired full-scale amplitude to the AM input port of the TMC2340 (AM_{14} through AM_0) and pull ENA HIGH for one clock cycle. This will load the amplitude. If ENA is held HIGH, then the amplitude will follow the inputs on the AM port. If the user assumes an implied binary point before the MSB of the AM port, the input range will be 0 to just under 1, and the outputs will fall between 0 and 2, with binary points after I_{15} and Q_{15}.

To set the frequency, the C register must be loaded with a value which is the phase increment per clock cycle. If the binary point is considered to be just left of the MSB (input range is 0 to almost 1) then the output frequency is the TMC2340 clock frequency multiplied by the number loaded into C. Since C is 32 bits wide, with a 20MHz clock, one LSB represents a frequency increment of 0.005Hz.

To load the C register, set $ENYP_1 = 1$ and $ENYP_0 = 0$; the data presented at the PH port will be loaded on the next clock rising edge.

At this point the TMC2340 has been initialized and can be put into one of three modes depending upon the states of FM and PM:

Mode 0 — FM = 0, PM = 0
In this mode the chip is in standby. The unchanging output corresponds to AM cos(PM) on the I outputs with PM being the phase increment.

Mode 1 — FM = 1, PM = 0
Frequency Modulation Mode. The chip generates an output signal of peak amplitude AM and frequency determined by accumulating the sum of the phase increment values in the C and M registers (more about the M register in a later section).

Mode 2 — FM = 0, PM = 1
Phase Modulation Mode. The TMC2340 generates a sinusoid of the frequency represented in the C register and the peak amplitude in the AM register. On each clock cycle, the phase of the signal is offset by the value in the M register.

Modulation

The output of the TMC2340 can be phase (Mode 2) or frequency (Mode 1) modulated. An unmodulated sinusoid results if the contents of registers C and M are held constant. Its frequency is set by C (Mode 2) or C+M (Mode 1). Since the state of the M register is not defined at power up, the M register should be loaded or cleared to begin operation.

If the signal is to be frequency modulated then the modulation signal is loaded into the M register. The format for the frequency is the same as that for the C register. If $ENYP_{1,0} = 0, 1$ then the data that is presented at the PH port is automatically loaded on each clock rising edge.

For phase modulation, the phase deviation is loaded into the M register (same manner as for frequency modulation). The units of the phase offset are cycles and full-scale is just under one output cycle per TMC2340 clock cycle. The MSB represents a phase of 180°, and the LSB a phase of about 8×10^{-8} degrees (eight one-hundred-millionths of a degree), or $\pi/2^{31}$ radians.

To synchronize two TMC2340s, first load them with their respective data in mode 0, then switch them simultaneously to either Mode 1 or Mode 2.

Calculating Frequency, Amplitude, and Phase Input Values for the TMC2340

This Application Brief discusses equations which simplify the calculation of register values which control the TMC2340. These values allow the generation of output carrier frequency, frequency or phase modulation, and output amplitude.

The results of the equations are converted to binary register values and should be rounded to the resolution of the applicable register (32 or 15-bits). For negative values of phase or frequency modulation, use these equations for positive values and see Table 1 of the TMC2340 data sheet to convert them to negative values.

The TMC2340 operates by continuously incrementing a register (phase accumulator) that rolls over when it becomes full. For example, if the next increment to the phase accumulator causes it to overflow by 47 LSBs, the phase accumulator retains the value 47. The value present in the carrier register (C) is the amount by which the phase accumulator is incremented each system clock cycle. As the value of the carrier register is increased, the value with which the the phase accumulator is incremented each clock cycle is increased, resulting in an increased carrier frequency.

The magnitude of the carrier is determined or modulated by the value loaded in the AM register. Phase modulation is accomplished by adding the value of the phase accumulator to the value of the modulation (M) register. This adds an offset to the phase of the carrier. This does not affect the increment value of the phase accumulator and therefore only effects the phase of the carrier, leaving the frequency constant.

Adding the value of the modulation register to the phase accumulator along with the value of the carrier register on each clock cycle results in a shift in frequency. This is because the phase accumulator is incremented by a different amount each clock cycle.

Frequency or phase modulation is selected with the FM and PM input pins which configure the TMC2340. The equations presented herein are useful for setting carrier frequency and phase, output amplitude, and frequency and phase modulation. To modulate the carrier with an external signal, the signal must be digitized and those values loaded into the modulation inputs of the TMC2340.

The carrier and modulation registers are loaded through the PH_{31-0} inputs. The $ENP_{1,0}$ inputs select the desired register. The amplitude register is loaded through the AM_{14-0} inputs.

CARRIER FREQUENCY:

$$\text{Carrier Register (C) Value} = \frac{\text{Desired Carrier Frequency}}{\text{Clock Frequency}} \times 2^{32}$$

AMPLITUDE AND AMPLITUDE MODULATION:

$$\text{AM Register Value} = \frac{\text{Desired Output Amplitude}}{\text{Full-Scale Output Amplitude}} \times (2^{15} - 1)$$

FREQUENCY MODULATION:

$$\text{Modulation Register (M) Value} = \frac{\text{Desired Change in Carrier Frequency}}{\text{Clock Frequency}} \times 2^{32}$$

PHASE MODULATION:

$$\text{Modulation Register (M) Value} = \frac{\text{Desired Change in Phase in radians (degrees)}}{2\pi\ (360°)} \times 2^{32}$$

EXAMPLE 1: Set carrier frequency to 3.579545 MHz with a system clock of 20MHz.

$$\text{Carrier Register (C) Value} = \frac{\text{Desired Carrier Frequency}}{\text{Clock Frequency}} \times 2^{32} = \frac{3.579545 \times 10^6}{20 \times 10^6} \times 2^{32}$$

C = 0.17897725 X 4,294,967,296 = 768,701,436 = 2DD1 73FBh
= 0010 1101 1101 0001 0111 0011 1111 1011 = PH_{31-0}

EXAMPLE 2: Set output amplitude to be 12.2% of full-scale.

$$\text{AM Register Value} = \frac{\text{Desired Output Amplitude}}{\text{Full-Scale Output Amplitude}} \times (2^{15}-1) = \frac{0.122}{1.000} \times 32767$$

AM = 3,998 = 0F9Eh = 0001 1111 0011 1100 = AM_{14-0}

EXAMPLE 3: Change carrier frequency by 10kHz with a system clock of 3 MHz.

$$\text{Modulation Register (M) Value} = \frac{\text{Desired Change in Carrier Frequency}}{\text{Clock Frequency}} \times 2^{32}$$

$$M = \frac{10 \times 10^3}{3 \times 10^6} \times 2^{32} = 14,316,558 = 00DA\ 740Eh$$

M = 0000 0000 1101 1010 0111 0100 0000 1110 = PH_{31-0}

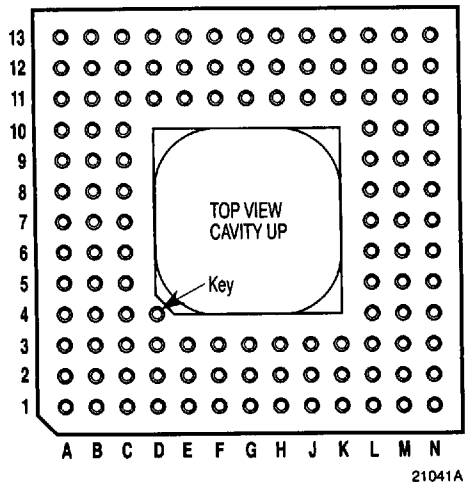
EXAMPLE 4: Shift the phase of any carrier frequency by 12°.

$$\text{Modulation Register (M) Value} = \frac{\text{Desired Change in Phase}}{360°} \times 2^{32} = \frac{12}{360} \times 2^{32}$$

M = 0.033333 X 2^{32} = 143,165,577 = 0888 8889h
= 0000 1000 1000 1000 1000 1000 1000 1001 = PH_{31-0}

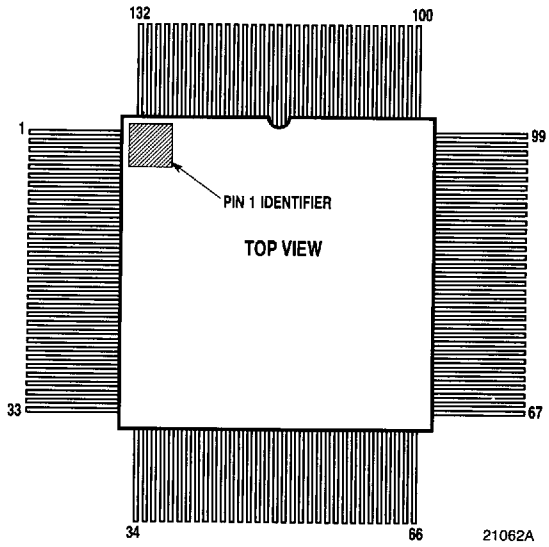
Pin Assignments — 121-Pin Plastic Pin Grid Array, H5 Package; 120-Pin Ceramic PGA, G1 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	Q_5	B3	Q_6	C5	GND	E1	GND	G11	GND	K1	PH_2	L10	PH_{31}	M12	AM_1
A2	Q_7	B4	Q_9	C6	V_{DD}	E2	GND	G12	AM_{12}	K2	PH_4	L11	V_{DD}	M13	AM_2
A3	Q_8	B5	Q_{11}	C7	GND	E3	V_{DD}	G13	AM_{13}	K3	GND	L12	AM_3	N1	PH_8
A4	Q_{10}	B6	Q_{13}	C8	V_{DD}	E11	V_{DD}	H1	PM	K11	GND	L13	AM_4	N2	PH_{10}
A5	Q_{12}	B7	GND	C9	GND	E12	GND	H2	FM	K12	AM_5	M1	PH_6	N3	PH_{12}
A6	Q_{14}	B8	I_1	C10	GND	E13	$\overline{OEI}$	H3	V_{DD}	K13	AM_6	M2	PH_9	N4	PH_{15}
A7	Q_{15}	B9	I_3	C11	V_{DD}	F1	OBIQ	H11	AM_9	L1	PH_5	M3	PH_{11}	N5	PH_{17}
A8	I_0	B10	I_5	C12	I_{11}	F2	GND	H12	AM_{10}	L2	PH_7	M4	PH_{13}	N6	PH_{19}
A9	I_2	B11	I_7	C13	I_{13}	F3	CLK	H13	AM_{11}	L3	GND	M5	PH_{16}	N7	PH_{21}
A10	I_4	B12	I_9	D1	$\overline{OEQ}$	F11	V_{DD}	J1	PH_0	L4	V_{DD}	M6	PH_{18}	N8	PH_{22}
A11	I_6	B13	I_{12}	D2	Q_0	F12	GND	J2	PH_1	L5	PH_{14}	M7	PH_{20}	N9	PH_{24}
A12	I_8	C1	Q_1	D3	GND	F13	AM_{14}	J3	PH_3	L6	V_{DD}	M8	PH_{23}	N10	PH_{26}
A13	I_{10}	C2	Q_2	D11	GND	G1	ENP_1	J11	GND	L7	GND	M9	PH_{25}	N11	PH_{29}
B1	Q_3	C3	V_{DD}	D12	I_{14}	G2	ENP_0	J12	AM_7	L8	V_{DD}	M10	PH_{28}	N12	PH_{30}
B2	Q_4	C4	GND	D13	I_{15}	G3	GND	J13	AM_8	L9	PH_{27}	M11	ENA	N13	AM_0



Pin Assignments — 132 Leaded CERQUAD, L5 Package

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{DD}	23	PH_1	45	V_{DD}	67	V_{DD}	89	GND	111	I_2
2	NC	24	PH_2	46	PH_{18}	68	AM1	90	I_{15}	112	VDD
3	Q_4	25	PH_3	47	PH_{19}	69	AM2	91	V_{DD}	113	I_1
4	Q_3	26	PH_4	48	PH_{20}	70	GND	92	I_{14}	114	I_0
5	GND	27	PH_5	49	GND	71	AM_3	93	I_{13}	115	GND
6	Q_2	28	PH_6	50	PH_{21}	72	NC	94	I_{12}	116	GND
7	Q_1	29	GND	51	PH_{22}	73	AM_4	95	GND	117	Q_{15}
8	Q_0	30	PH_7	52	PH_{23}	74	AM_5	96	I_{11}	118	Q_{14}
9	V_{DD}	31	PH_8	53	V_{DD}	75	GND	97	I_{10}	119	Q_{13}
10	$\overline{OEQ}$	32	NC	54	PH_{24}	76	AM_6	98	NC	120	V_{DD}
11	GND	33	GND	55	PH_{25}	77	AM_7	99	V_{DD}	121	Q_{12}
12	GND	34	PH_9	56	PH_{26}	78	AM_8	100	I_9	122	Q_{11}
13	CLK	35	NC	57	PH_{27}	79	AM_9	101	NC	123	Q_{10}
14	GND	36	PH_{10}	58	PH_{28}	80	AM_{10}	102	I_8	124	GND
15	OBIQ	37	V_{DD}	59	PH_{29}	81	AM_{11}	103	NC	125	Q_9
16	ENP_0	38	PH_{11}	60	PH_{30}	82	AM_{12}	104	GND	126	Q_8
17	GND	39	PH_{12}	61	PH_{31}	83	GND	105	I_7	127	Q_7
18	ENP_1	40	PH_{13}	62	NC	84	AM_{13}	106	I_6	128	NC
19	PM	41	PH_{14}	63	ENA	85	AM_{14}	107	I_5	129	GND
20	FM	42	PH_{15}	64	NC	86	GND	108	GND	130	Q_6
21	V_{DD}	43	PH_{16}	65	NC	87	V_{DD}	109	I_4	131	NC
22	PH_0	44	PH_{17}	66	AM_0	88	$\overline{OEI}$	110	I_3	132	Q_5



Ordering Information

Product Number	Temperature Range	Screening	Package	Pakcage Marking
TMC2340H5C1	STD: T_A = 0 to 70°C	Commercial	121-Pin Plastic Pin Grid Array	2340H5C1
TMC2340H5C	STD: T_A = 0 to 70°C	Commercial	121-Pin Plastic Pin Grid Array	2340H5C
TMC2340L5V1	EXT: T_C = -55°C to 125°C	MIL-STD-883B	132-Leaded CERQUAD	2340L5V1
TMC2340L5V	EXT: T_C = -55°C to 125°C	MIL-STD-883B	132-Leaded CERQUAD	2340L5V
TMC2340G1V1	EXT: T_C = -55°C to 125°C	MIL-STD-883B	120-Pin Ceramic PGA	2340G1V1
TMC2340G1V	EXT: T_C = -55°C to 125°C	MIL-STD-883B	120-Pin Ceramic PGA	2340G1V

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