S4802CBI12

Missouri Datasheet

Revision 2.3

February 12, 2002

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PRODUCT BRIEF

SONET/SDH STS-48/STM-16 Framer/Pointer Processor

Features

Features

- SONET/SDH Mux/Demux, Transport Overhead Terminating Transceiver, and Pointer Processors for a single STS-48/STM-16, 4 x STS-12/STM-4s, and 16 x STS-3/STM-1s.
- Parallel STS-48/STM-16, Serial STS-12/STM-4, and Serial STS-3/STM-1 interfaces.
- Provisionable as SONET or SDH on a per line basis.
- Built-in 192x48 cross-connect for STS-1 level cross-connection or add/drop in both Mux and Demux directions.
- Compliant with Bellcore GR-253, ITU G.707, and ANSI T1.105 -1995 standards.
- Packaged in a 624-pin CBGA.

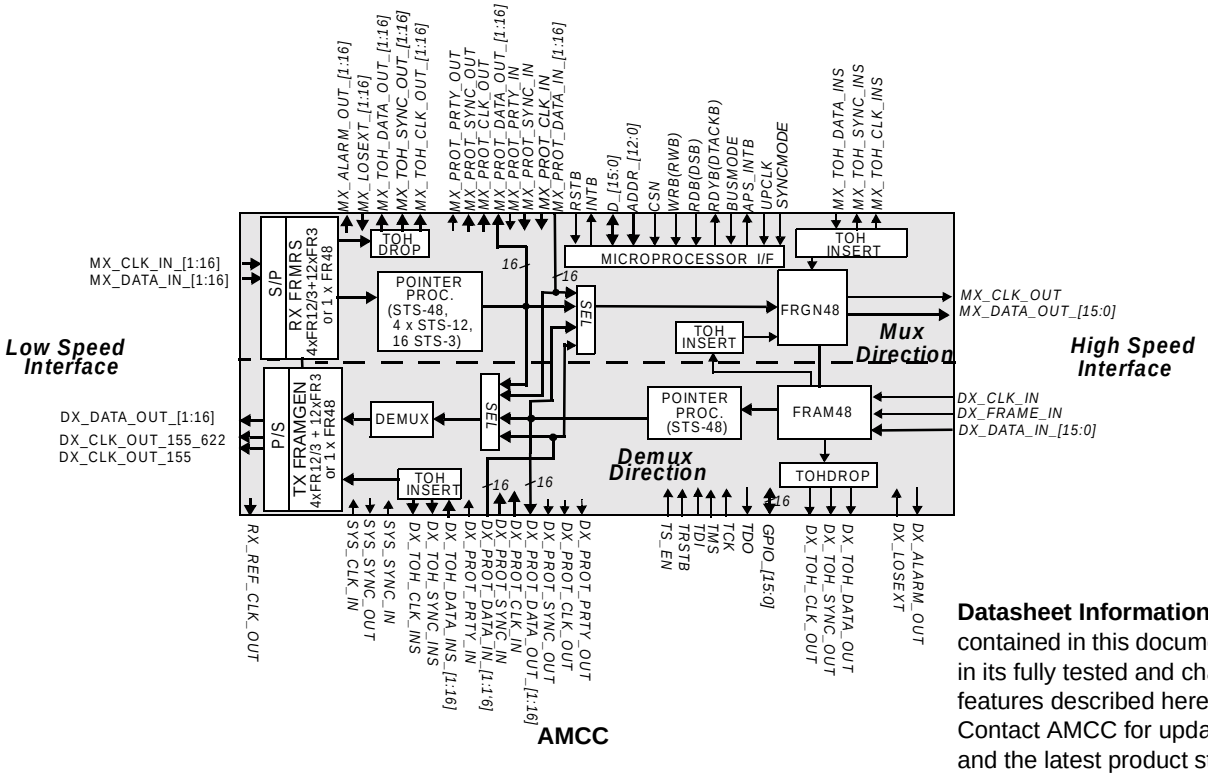
Multiplex Direction:

- Multiplexes all valid combination of STS-12/STM-4 and STS-3/STM-1 tributaries into a STS-48/STM-16 or bypass for STS-48/STM-16 -to- STS-48/STM-16 connection.
- Pointer Processors for all valid input combinations of STS-48c/AU-4-16c, STS-12c/AU-4-4c, STS-3c/AU4, or STS-1/AU-3 signals.
- Configurable selector for choosing tributaries from mux pointer processor, demux pointer processor, and Protection inputs.
- 1 x STS-48/STM-16, or 4 x STS-12/STM-4, or 16 x STS-3/STM-1 framers.
- TOH (Regenerator/Multiplex Sections) Monitors with provisionable B2 signal Fail and Degrade detection algorithms.
- Provisionable TOH Generator for STS-48/STM-16 output.
- STS-48/STM-16 frame synchronous scrambler.

Demultiplex Direction:

- Demultiplexes all valid combination of STS-12/STM-4 and STS-3/STM-1 tributaries from a STS-48/STM-16 or bypass for STS-48/STM-16 -to- STS-48/STM-16 connection.
- Pointer Processor for all valid input combinations of STS-48c/AU-4-16c, STS-12c/AU-4-4c, STS-3c/AU4, or STS-1/AU-3 signals.
- Configurable selector for choosing tributaries from mux pointer processor, demux pointer processor, and Protection inputs.
- STS-48/STM-16 framer.
- STS-48/STM-16 TOH (Regenerator and Multiplex sections) monitor.
- Provisionable TOH (Regenerator/Multiplex Sections) Generators for STS48/STM-16, STS-12/STM-4, and STS-3/STM-1 outputs.
- STS-48/STM-16, STS-12/STM-4, and STS-3/STM-1 frame synchronous scramblers.

S4802 Block Diagram



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Datasheet Information - The information contained in this document is about a product in its fully tested and characterized stage. All features described herein are supported. Contact AMCC for updates to this document and the latest product status.

Applications:

- ATM and POS (Packet Over SONET) switches and routers.
- SONET/SDH add/drop multiplexers, terminal multiplexers, and digital cross connects.
- WDM/DWDM Mux/Demux.

Overview and Applications

SONET Processing

The S4802 can be used in SONET and SDH applications. On the low-speed side, the S4802 can interface to (1) a single STS-48/STM-16 or (2) four STS-12/STM-4 or (3) sixteen STS-3/STM-1 or (4) any valid combination of STS-12/STM-4s and STS-3/STM-1s in each direction.

In the demultiplex direction, the S4802 accepts a 16-bit wide STS-48/STM-16 signal. This input may have originated from a deserialized STS-48/STM-16 signal. The S4802 locates the frame, optionally performs descrambling, processes the TOH bytes, and performs pointer processing. If an STS-48c/AU-4-16c payload is not present, the S4802 demultiplexes the signal into four STS-12/STM-4 or sixteen STS-3/STM-1 tributaries or any valid combination of STS-12/STM-4s and STS-3/STM-1s. The 192x48 STS-1 level cross-connect can select any tributaries from (1) the demux tributaries (after pointer-processing), (2) the mux tributaries (after pointer-processing), and (3) the protection port inputs for processing. The S4802 then generates and inserts the TOH/SOH bytes, optionally performs frame synchronous scrambling, and then transmits the data through a single 16-bit parallel interface or up to sixteen serial interfaces.

In the multiplex direction, the S4802 accepts (1) a single parallel STS-48/STM-16 (2.5 Gb/s), or (2) four serial STS-12/STM-4 (622 Mb/s) signals, or (3) four groups of four (16 total) serial (155 Mb/s) STS-3/STM-1 signals, or (4) any valid combination of STS-12/STM-4s and STS-3/STM-1s. The S4802 locates the frame(s), optionally descrambles the data, and processes the TOH/SOH bytes. The S4802 uses the 192x48 STS-1 level cross-connect to select any combination of signals from (1) the mux tributaries (after pointer-processing), (2) demux tributaries (after pointer-processing), and (3) the protection port inputs and sends them to FRGEN48. The S4802 then generates the TOH/SOH bytes, optionally performs frame synchronous scrambling, and outputs the data on the MX_DATA_OUT[15:0] bus.

Low-Speed Interface

On the low-speed side, in both the mux and demux directions, the S4802 supports (1) a single STS-48/STM-16 signal operating at 155 MHz, or (2) four serial STS-12/STM-4 signals operating at 622 MHz, or (3) 4 groups of 4 serial (16 total) STS-3/STM-1 signals operating at 155 MHz, or (4) any valid combination of STS-12/STM-4 and STS-3/STM-1 signals operating at 155 MHz. The S4802 is designed to bolt directly to fiber optic transceivers (XCVR) and clock recovery units (CRU) (see figure below).

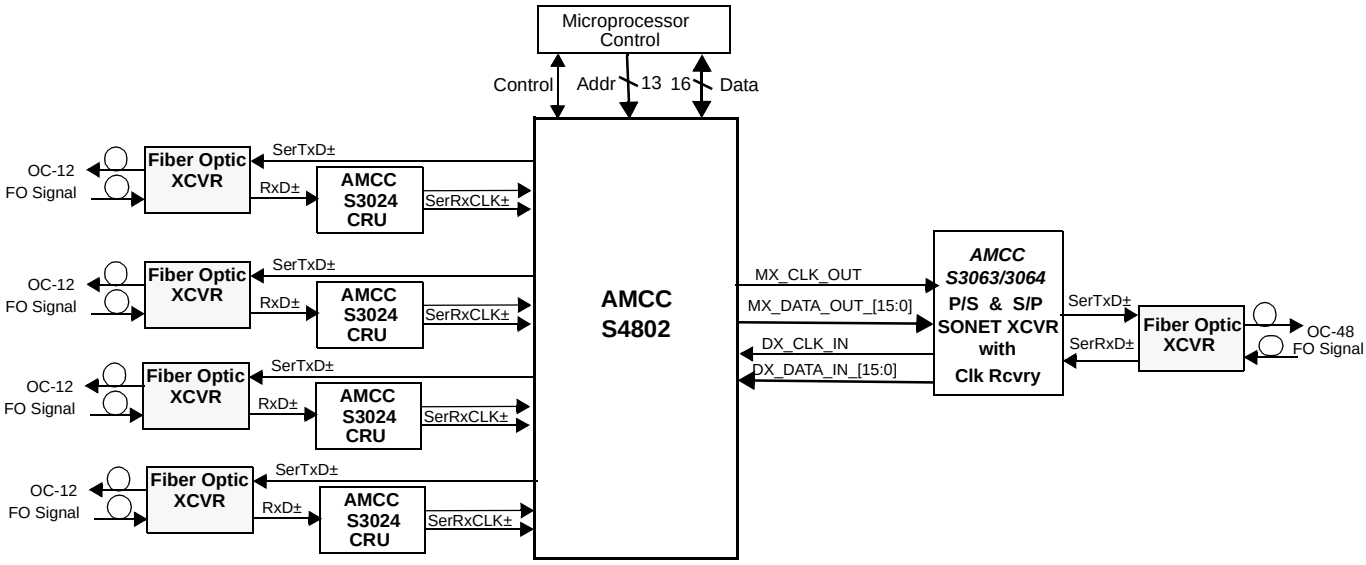
High-Speed Interface

On the high-speed side, in both the mux and demux directions, the S4802 supports 16-bit parallel interfaces operating at 155 MHz.

Controller Interface

A high-speed microprocessor interface is provided for configuration and monitoring. The S4802 provides numerous automatic monitoring functions. It can be configured to provide an interrupt to the control system, or it can be operated in polled mode.

Typical Application: S4802 in 2.488 Gb/s SONET/SDH Add/Drop Multiplexer Application



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Specification Revision History

Rev.	Date	Description of Change
1.0	4/16/99	Incorporated Engineering Requirements document and I/O document into Customer Specification.
1.1	5/7/99	Incorporated new I/O document into Customer Specification.
1.2	5/14/99	Incorporated Drafts 12 and 13 of I/O document into Customer Specification.
1.3	5/14/99	APS Functional Timing Diagrams added.
1.4	6/7/99	Incorporated Engineering Requirements (2.01), and Drafts 14 and 15 of I/O document into Customer Specification
1.5	6/11/99	Updated ACElectrical Characteristics.
1.6	6/21/99	Updated company name.
1.7	6/21/99	Made correction to header title.
1.8	7/19/99	Updated AC Timing Diagrams and LVPECL DC Specifications
1.9	7/21/99	Updated DC Specifications and added Pull_Up/Pull_Down information to Pinout. Modifed description of WRB/RWB signal.
1.10	7/23/99	Updated DC Specifications. Modifed VIH and VIL LVDS and LVPECL parameters. Changed 3.3V Supply tolerance to 5%.
1.11	8/26/99	Added Register Index. Updated TOH Insert and Drop Functional Timing Diagrams. Rrenamed pins DX_CLK_OUT_155 and DX_CLK_OUT_155_622 to DX_CLK_OUT_[2], and DX_CLK_OUT_[1], respectively. Updated sections 5.4.4.1 and 5.4.7.1, associated with replacing MX_SF_PAIS_INH_[i] MX_B2_ERR_SF_[i] in the last sentence of each section. Edited the description of DX_CLK_OUT_[2:1] in section 6.9. Edited section 5.6.1 for typos.
1.12	8/30/99	Updated Register Index. Updated Mechanical Specifications and included mention of 624 CBGA package type in this section. Removed maximum Pulse width requirements for *SYS_SYNC_IN* input signal. Removed mention of CE0_TEST, TEST_EN and TEST_CLK from top level block diagram, since these are non-functional test signals.
1.13	9/30/99	Removed MX_CLK_8Kz from block diagram. Revised setup and hold time parameters on the Low Speed Interface Mux timing diagrams and the Protection Interface timing diagrams. Fixed databus widths and specied when DTACK tri-states on the Microprocessor interface timing diagrams. Added thermal information to package section.
1.14	10/7/99	Performed some minor editing and clean up of document.
1.15	11/12/99	Added Appendix for updated MX/DX Pointer Interpreter Memory Maps, removed mention of DX_CLK_OUT_[3:4] and related invert and inhibit control signals within spec and memory map, specified that SYS_CLK_IN needs to be a 155 MHz clock when Low Speed Side of Missouri is configured for STS-48/STM-16, and performed some minor editing and clean up of document. Also updated V_{IH} on LVECL and LVDS DC characteristic tables.
1.16	11/19/99	Added updated memory maps of MX and DX configuration maps to Appendix A. Added signal type to DX_CLK_OUT_[2:1]. Updated Mechanical drawing.
1.17	12/6/99	Corrected header (specifically the part number) on Summary Datasheet; added headings from product spec to those instances above Memory Map tables in Appendix A for easier locating; added secondary index entries from Memory Map tables. Added an Absolute Maximum Ratings table. Also updated Vindiff and Vinsingle on LVDS/LVPECL DC Characteristics.
1.18	1/14/00	Corrected Mechanical Packing drawing; embellished index of registers. Modified timing information in sections 13.3, 13.7 and 13.9.

Rev.	Date	Description of Change
1.19	1/28/00	Corrected reset values for MUXSEL and DEMUXSEL in Register Map tables.
2.0	2/29/00	Changed publication's stage from Advanced to Preliminary. Changed the VIH, VIL and VICM levels on the LVDS and LVPECL I/O Specifications. Modified Mechanical Package Information.
2.1	5/3/00	Specified the MSB on all data busses within the Pinout section. Added some additional text in both the MX and DX TOH insert sections. Switched around the current numbers in the Absolute Maximum Ratings Table. Added TRSTB minimum pulse width. Added PLL_REF_CLK_N and moved PLL_VDDA to ground (in Table 9: Power, Ground, No Connect, and Extract Pull Down).
2.2	7/30/01	• In, 2.0 Pin Assignments and Descriptions: removed all references to active edges (covered in 12.0 Input and Output Descriptions). • Formatting changes to Tables 1, 3, 4, and 5. • DX_CLK_OUT_1 renamed to DX_CLK_OUT_155_622. DX_CLK_OUT_2 renamed to DX_CLK_OUT_155. • Corrected descriptions of SYS_SYNC_IN and SYS_SYNC_OUT in Table 1. • Minor editorial and formatting changes to other tables. • Corrected array indicies and MSB on data busses. • Corrected description of MUXSEL_x to control the mux frame selection. • Corrected Signal Fail and the Signal Degrade Provisioning Values for STS-12/STM-4 GROUP_CLR for 10E-7 to 5 in Table 17. • Added LVPECL and LVDS interfacing notes to end of section. • Rest of document: • Corrected bus indices to be consistent with Pin Descriptions. • Minor formatting and editorial changes (i.e., remove run-on sentences). • Corrected SYNC_OUT timing reference to TOH_CLK_OUT/INS in 5.5 Serial • TOH/SOH Drop Channels, 5.9.3.1 Serial TOH/SOH Insert Channel, 6.5.1 Serial • TOH/SOH Drop Channel, and 6.9.3.4 Serial TOH/SOH Insert Channel. • Updated 13.11 Mux TOH Drop Timing, 13.12 Mux TOH Insert Timing, 13.13 Demux TOH Drop Timing, 13.14 Demux TOH Insert Timing diagrams to reflect the correction. • Aggregated the register map into one continguous section. • Removed obsolete register map tables and Appendix A. • Register Map: Corrected DX_SF_PAIDS_INH to be a single bit.
2.3		• Incorporated User Notes into spec as an appendix. • Added references to User Notes to applicable sections. • Changed profile mechanical drawing to a BGA. • Added nominal currents to nominal power supply. • Minor editorial changes.

Table of Contents

Table of Contents (continued)

Table of Contents (continued)

Table of Contents (continued)

Table of Contents (continued)

Missouri Datasheet

Revision 2.3

1.0 Applicable Documents

1. Bellcore Specification “SONET Transport Systems: Common Generic Criteria,” GR-253-CORE, Issue 2, Rev. 1, December 1997.
2. Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks, G.783, (01/94).

2.0 Functional Descriptions

2.1 Common Conventions, Controls, and Configuration

Note: Bytes within the SONET or SDH signal are transmitted MSB first. By convention, the MSBs of SONET/SDH bytes are referred to as bit 1 and the LSBs as bit 8. However, the register words that provision and monitor SONET/SDH bytes are defined with bit 7 or 15 as the MSB and bit 0 as the LSB.

2.2 Multiplexing and Tributary Indexing Convention

The Missouri interfaces to SONET/SDH signals on both the high-speed and low-speed interfaces. On the high-speed side, in both directions, the Missouri has a 16-bit wide 155.52 MHz interface to a STS-48/STM-16 signal. On the low-speed side, the Missouri interfaces with a single STS-38/STM-16 signal or four tributary quadrants, each of which can consist of a single STS-12/STM-4 signal or four STS-3/STM-1 signals, in each direction. If the interface consists of a single STS-48/STM-16, then the interface is parallel and operates at 155.52 MHz. If a quadrant consists of a single STS-12/STM-4 signal, the quadrant interface is serial and operates at 622.08 MHz. If the quadrant consists of four STS-3/STM-1 signals, the quadrant interface is serial and operates at 155.52 MHz.

The indexing scheme used by the Missouri for defining the provisioning and monitoring is based on the byte-interleaving sequence defined in GR-253-CORE and G.707 for multiplexing SONET and SDH signals. An example of the SONET interleaving scheme is illustrated in Figure 1, which is derived from Figure 5-2 of GR-253. In Figure 1, the bytes are transmitted from right to left.

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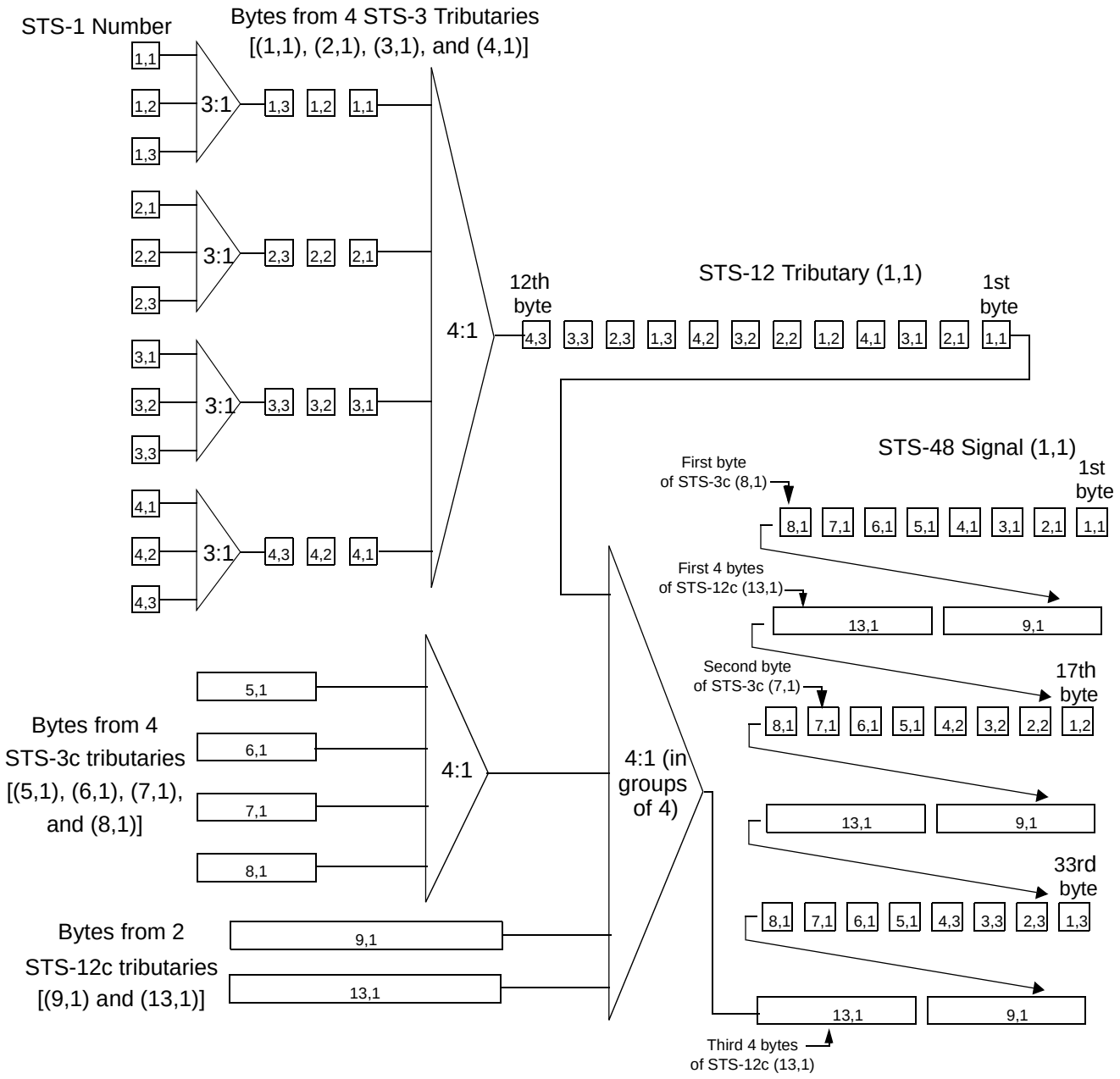


Figure 1: Example of Byte Interleaving to form an STS-12

The tributaries in Figure 1 are labeled using the 2-level “STS-3 #/STS-1 #” convention that is specified in requirement R6-3 of GR-253 for use on “OS/NE, WS/NE (including any GUI display), and NE/NE interfaces.”

Interleaving to form SDH signals is similar, except that the first level of the SDH hierarchy is STM-1. For the purpose of interleaving in Figure 1, an STM-1/AU-4 is equivalent to an STS-3c and an AU-3 is equivalent to an STS-1.

The Missouri has many configuration and monitoring registers that are accessible through the microprocessor interface. Because the SONET interface signals can be multiplexed from as many as 48 different STS-1 tributaries, there are some parameters that require 48 separate provisioning and monitoring registers. An **[x]** is used to indi-

cate 1 of these tributaries, where **x** ranges from [1]_[1] through [16]_[3]. There are other parameters that are only applicable to the STS-3/STM-1 tributary level. Only the first index, **[i]**, of the 2-indexes nomenclature **[x]** is used to indicate 1 of these tributaries, where **[i]** ranges from 1 to 16. In the following descriptions, a **[q]** is used in the names of certain registers that are required on a quadrant basis, rather than a per-tributary basis; **[q]** ranges from 1 to 4.

Unless Missouri is configured to interface to STS-48/STM-16 signals containing 48 STS-1/AU-3 tributaries, not all of the registers for some parameters are used. The unused provisioning registers are “don’t care,” and the unused monitoring registers should be ignored. The registers that are used depend on the configuration (see Table 1 and Table 2).

Table 1. SONET/SDH Register Index Values, Indexed to STS-1/AU-3 Level, x

Tributary Type	q=1	q=2	q=3	q=4
STS-48c or AU-4-16c	[1,1]	n/a	n/a	n/a
STS-12c or AU-4-4c	[1,1]	[5,1]	[9,1]	[13,1]
STS-3c or AU-4	[1,1], [2,1], [3,1], [4,1]	[5,1], [6,1], [7,1], [8,1]	[9,1], [10,1], [11,1], [12,1]	[13,1], [14,1], [15,1], [16,1]
STS-1/AU-3	[1,1], [1,2], [1,3] [2,1], [2,2], [2,3] [3,1], [3,2], [3,3] [4,1], [4,2], [4,3]	[5,1], [5,2], [5,3] [6,1], [6,2], [6,3] [7,1], [7,2], [7,3] [8,1], [8,2], [8,3]	[9,1], [9,2], [9,3] [10,1], [10,2], [10,3] [11,1], [11,2], [11,3] [12,1], [12,2], [12,3]	[13,1], [13,2], [13,3] [14,1], [14,2], [14,3] [15,1], [15,2], [15,3] [16,1], [16,2], [16,3]

Table 2. SONET/SDH Register Index Values, Indexed to STS-3/STM-1 Level, i

Tributary Type	q=1	q=2	q=3	q=4
STS-12c or AU-4-4c	[1]	[5]	[9]	[13]
STS-3c or AU-4	[1], [2], [3], [4]	[5], [6], [7], [8]	[9], [10], [11], [12]	[13], [14], [15], [16]

2.3 Monitors and Control Interface

For performance-monitoring purposes, Missouri contains a number of “delta” bits, “event” bits, “second event” bits, and error counters.

Delta bits are set (logic 1) by when a monitored parameter changes state. The delta bit then stays high until the controller clears (logic 0) the bit by writing a 1 to the bit. If a write-to-1 occurs simultaneously with a parameter state change, the delta bit is set.

Event bits are similar to delta bits, but they do not have a corresponding status bit. Event bits are set (logic 1) by the Missouri when the associated event occurs (such as a FIFO overflow). The event bit then stays high, regardless of whether or not the event reoccurs, until the controller clears (logic 0) the bit by writing a 1 to the bit. If a write-to-1 occurs simultaneously with the event occurrence, the event bit is set. Event bits are identified by a **_E** suffix.

There are several “events” that are monitored for occurrence each second. This allows the controller to accumulate the number of seconds that contain a particular event. For example, the number of seconds that at least 1 error

was detected in a received signal by monitoring the B1 bytes. For this purpose, Missouri creates a signal, SEC_EVENT, that oscillates at a 1 Hz. rate. Alternatively, the timing for “second events” can be controlled by the **LATCH_CNT** registers.

When Missouri detects a rising edge of SEC_EVENT (**CNT_SEC_EN** = 1) or when **LATCH_CNT** in the receive control interface is written from a 0 to a 1 (**CNT_SEC_EN** = 0), it produces a pulse on an internal signal, LATCH_EVENT. When a pulse occurs on LATCH_EVENT, the ***_SECE** register bits are set if their corresponding internal current second event monitoring bits are active. Like delta and event bits, the ***_SECE** bits are not cleared until they are written to 1 by the controller. The microprocessor is notified via **LATCH_E** when a pulse occurs on LATCH_EVENT.

All the internal, performance-monitoring counter blocks comprise a running error counter and a holding register that presents stable results to the controller. The counts in all of the running counters are latched to the hold registers and the running counters are cleared when a pulse occurs on LATCH_EVENT. To prevent missing a count that occurs when latching occurs, a counter is set to 1 rather than 0, if the clear signal is simultaneous with an increment.

After being latched, the results are held to be read by the controller. All the internal counters have the ability to store more than the maximum possible count in a 1-second interval for a bit error rate of 10^{-3}. As long as the count values are latched (and the results read) every second, no counts will be lost. In case this doesn’t happen, all the running counters will hold their maximum value rather than roll over to 0.

For testing purposes, the running counters can be preloaded with a value close to its maximum, that is a function of the size of the counter. The preload occurs when **CNT_LOAD** transitions from 0 to 1.

Summary delta/event/second event bits provide a consolidated view of the various individual delta/event/second event bits, grouped either by function or tributary. Summary delta/event/second events are therefore a function of the other delta/event/second events bits in the register maps. These summary bits don’t behave as their individual counterparts do, in that the summary bits are NOT cleared when written to a 1 by the microprocessor. The summary bits are read only and strictly combinatorialy derived; they clear only when all delta/event/second event bits that contribute to them are cleared.

Two of these summary bits, **MX_SUM_INT** and **DX_SUM_INT**, are “ORed” to form the Missouri *INTB* output. The contribution of any of these bits to the summary interrupt can be deleted by setting the corresponding “mask” bit (see section 13.0).

2.4 Configuration

The **MX_LINE_CONFIG_[4:0]** and **DX_LINE_CONFIG_[4:0]** registers determine the SONET/SDH rate configuration of the low-speed inputs and outputs, respectively, that is, whether the entire data stream is an STS-48/STM-16, or whether, for each of the 4 quadrants, that quadrant is an STS-12/STM-4 or STS-3/STM-1. This is illustrated in Table 3. The **MX_LINE_CONFIG_[4:0]** and **DX_LINE_CONFIG_[4:0]** registers should normally be provisioned identically; if they are not, Missouri will transmit and receive data correctly, but RDI/REI information imbedded in the SONET/SDH frames will be unpredictable.

Table 3. MX_/DX_LINE_CONFIG_[4:0] Definition

MX_/DX_LINE_CONFIG_[4:0]	Data Format at MX_DATA_IN/DX_DATA_OUT
1 xxxx	Single STS-48 signal (using *MX48_PDATA_IN*, *MX48_PCLK_IN* / *DX48_PDATA_OUT*, *DX48_PCLK_OUT*)
0 **1**xxx	Quadrant #1 contains an STS-12 signal

Table 3. MX_/DX_LINE_CONFIG_[4:0] Definition

MX_/DX_LINE_CONFIG_[4:0]	Data Format at MX_DATA_IN/DX_DATA_OUT
0 x**1**xx	Quadrant #2 contains an STS-12 signal
0 xx**1**x	Quadrant #3 contains an STS-12 signal
0 xxx**1**	Quadrant #4 contains an STS-12 signal
0 **0**xxx	Quadrant #1 contains 4 STS-3 signals
0 x**0**xx	Quadrant #2 contains 4 STS-3 signals
0 xx**0**x	Quadrant #3 contains 4 STS-3 signals
0 xxx**0**	Quadrant #4 contains 4 STS-3 signals

See User Note 14.1.1.1 for important information.

3.0 Processing of Data in the Mux Direction

On the low-speed side, Missouri accepts any of the following:

1. A 16-bit parallel data stream on *MX48_PDATA_IN_[15:0]* and its associated single 155.52 MHz clock input *MX48_PCLK_IN*. **See User Notes 14.1.1.1 and 14.1.6.1 for important information.**
2. Serial data streams from *Line Interfaces MX_DATA_IN_[i], i=1,5,9,13,* and their associated 622.08 MHz clock inputs, *MX_CLK_IN_[i],* associated with STS-12/STM-4 signals.
3. Sixteen serial data stream signals, *MX_DATA_IN_[i]*, and sixteen 155.52 MHz clocks *MX_CLK_IN_[i],* associated with up to sixteen STS-3/STM-1 signals.

Combinations of STS-12/STM-4 and STS-3/STM-1 signals are supported also; provisioning of these combinations is via the **MX_LINE_CONFIG_[4:0]** register, as described in section 2.4.

3.1 Low-Speed Loopbacks

3.1.1 DX_TO_MX

The Missouri low-speed interface **[i]** can be configured to loopback the receive demuxed tributaries into the MX low-speed inputs (*MX_DATA_IN_[i]*) if **DX_TO_MX_LS_LOOP_[i]** = 1. While in loopback, the *DX_CLK_OUT_155* and *DX_CLK_OUT_155_622* signals are used to clock the MX low-speed inputs (*MX_DATA_IN_[i]*). Loopbacks of individual tributaries can also be accomplished via the **MUXSEL_x_[7:0]** functionality.

If both low-speed mux and demux sides are both configured as STS-48 signals (**DX_LINE_CONFIG_[4]** = **MX_LINE_CONFIG_[4]** = 1) then setting **DX_TO_MX_LS_LOOP_[1]** = 1 loops the entire STS-48 signal. The other loopback bits are ignored.

3.2 Input Monitor

3.2.1 LOC

The active *MX_CLK_IN_[i]* inputs are monitored for loss of clock using the *UPCLK* input. If no transitions are detected on the receive line side clocks for 16 periods of *UPCLK*, the **MX_LOC_[i]** bit is set. It is cleared when transitions are detected.

The **MX_LOC_[i]_D** delta bit is set if **MX_LOC_[i]** transitions from either a 0 to a 1, or from a 1 to a 0.

See User Note 14.1.3.1 for important information.

3.2.2 LOS

The Missouri provides an internal LOS monitor, as well as the ability to accept a signal from an external LOS monitor.

Input signals, *MX_LOSEXT_[i]*, are provided for external Loss-of-Signal indicators for the Missouri. The state of these inputs are reported to the management interface via the **MX_LOSEXT_[i]** registers. *MX_LOSEXT_[i]* can be active high (**MX_LOSEXT_LEVEL_[i]** = 0, the default) or active low (**MX_LOSEXT_LEVEL_[i]** = 1). **See User Note 14.1.3.3 for important information.**

MX_LOSEXT_[i] can contribute directly to the declaration of an LOS condition for tributary [i] (which results in **MX_LOS_[i]** being set), or may first enter a delay block, where it must be set for a minimum of 3.29 µs for OC-12/OC-48 or 13.16 µs for OC-3 before **MX_LOS_[i]** is set. Inhibits, **MX_LOSEXT_INH_[i]** and

MX_LOSEXT_DELAY_INH_[i], are provided to control both the immediate and delayed contributions of **MX_LOSEXT_[i]** to **MX_LOS_[i]**, respectively. **See User Note 14.1.3.1 for important information.**

In addition, the Missouri can detect an LOS condition on tributary [i] by monitoring the receive data, the appropriate *MX_DATA_IN_[i]* signals, for a continual stream of all-zeros. If the appropriate *MX_DATA_IN_[i]* == 0 for 3.29 µs for OC-12/OC-48 or 13.16 µs for OC-3 (see Table 1 and Table 2 for assignments of input signals to tributaries), the Missouri declares Loss of Signal (**MX_LOS_[i]** = 1). A separate, inhibit-bit controls this all-zeros detection feature, **MX_LOS_ALL_ZERO_INH_[i]**.

MX_LOS_[i] is cleared when all non-inhibited contributors are cleared: **MX_LOSEXT_[i]** = 0, the incoming signal had two consecutively valid frame alignment patterns, and no all-zeros pattern qualified as an LOS defect (*MX_DATA_IN_[i]* = 0 for 3.29 µs for OC-12/OC-48 or 13.16 µs for OC-3) was present during the intervening time (1 frame).

MX_LOS_[i] contributes to downstream AIS-P generation and line RDI insertion in the demux direction (see section 4.9.3.7).

3.3 STS-3/STM-1, STS-12/STM-4 or STS-48/STM-16 Framers

The SONET/SDH framers locate the framing bytes. After finding the frame, the framers shift the data so that their output data are byte aligned. They also descramble the data and provide frame counter outputs to the TOHMON, TOHDROP, and pointer-processor blocks.

3.3.1 Framing

When a multiplexer side framer is out-of-frame (**MX_OOF_[i]** = 1), the framer searches for the 32-bit A1-A1-A2-A2 framing byte sequence (0xF6F6_2828). When the framer finds 2 successive sequences separated in time by 125 µs that exactly match the framing pattern, it goes into frame (**MX_OOF_[i]** = 0) and byte aligns its output data bus.

The framer remains in-frame, until it receives 5 successive frames with at least 1 bit error in the A1-A1-A2-A2 framing pattern. When this occurs, **MX_OOF_[i]** is set to 1, and a new frame search is started.

The framers also provide loss-of-frame indications. If **MX_OOF_[i]** is set (1) continuously for 24 consecutive frames (3 ms), the **MX_LOF_[i]** bit is set to 1. Once **MX_LOF_[i]** is set, it remains high until **MX_OOF_[i]** is inactive (0) continuously for either 24 (if **MX_LOF_ALG_[i]** = 1) or 8 (if **MX_LOF_ALG_[i]** = 0) consecutive frames.

The **MX_LOF_[i]** bits contribute to the generation of PAIS in the Pointer Generator (see section 3.6.4.4). They also contribute to the generation of the LRDI signals used in the Demultiplex Direction (see section 4.9.3.7). The **MX_OOF_[i]_D** and **MX_LOF_[i]_D** delta bits contribute to the summary interrupt. The **MX_OOF_[i]_SECE** and **MX_LOF_[i]_SECE** second event bits are set at the end of each second where the **MX_OOF_[i]** and **MX_LOF_[i]** bits were in the active state at any time during the second.

3.3.2 Descrambling

Data may be descrambled with frame synchronous descrambling sequences generated from the polynomial **$g(x) = x^7 + x^6 + 1$** before it is output from the Framer blocks (see section 4.3.3). For testing purposes or when the *MX_DATA_IN_[i]* (or *MX48_PDATA_IN*) data originates from a signal that has already been descrambled, one or more of the descramblers can be disabled by setting the appropriate **MX_DSCRINH_[i]** bits to 1.

3.4 Transport Overhead Monitors

The TOH/SOH monitoring blocks consists of B1, J0, B2, K1K2, S1, and M1 monitoring.

3.4.1 B1 Monitor

Missouri checks the B1 bytes for correct bit interleaved parity 8 (BIP-8) values. Even parity BIP-8 is calculated over all bytes of each frame before descrambling. This value is then compared to the received B1 value in the following

frame after descrambling. The comparison can result in 0 to 8 mismatches (B1 bit errors).

Missouri contains sixteen 16-bit B1 error counters that either counts every B1 bit error (if **MX_BIT_BLKCNT_[i]** = 0) or every frame with at least 1 B1 bit error (if **MX_BIT_BLKCNT_[i]** = 1). When the performance-monitoring counters are latched, the B1 error counts are latched into the **MX_B1_ERRCNT_[i]_[15:0]** registers and then the B1 error counters are cleared (see section 2.3).

If there has been at least 1 B1 error in the previous second (since the last pulse on LATCH_EVENT), then the B1 error event bit, **MX_B1ERR_[i]_SECE**, is set.

3.4.2 J0 Monitoring

If **MX_SDH_J0_[i]** = 0, J0 monitoring consists of examining the received J0 bytes for values that match consistently for 3 consecutive frames. When a consistent J0 value is received for input **i**, it is written to **MX_J0_[i]_[15]_[7:0]**. This mode is normally used for SONET applications.

If **MX_SDH_J0_[i]** = 1, the J0 byte is expected to contain a repeating 16-byte section trace frame that includes the Section Access Point Identifier. J0 monitoring consists of locking on to the start of the 16-byte section trace frame and examining the received section trace frames for values that match consistently for 3 consecutive section trace frames. When a consistent frame value is received, it is written to **MX_J0_[i]_[15:0]_[7:0]**. The first byte of the section trace frame, containing the frame start marker, is written to **MX_J0_[i]_[15]_[7:0]**. This mode is normally used for SDH applications.

3.4.2.1 Framing

In the SDH mode (**MX_SDH_J0_[i]** = 1), the MSBs of all section-trace frame bytes are “0” except for the MSB of the frame start marker byte. The J0 monitor framers search for a single J0 byte with a “1” in its MSB, followed by 15 consecutive J0 bytes that have “0” for their MSB. When this pattern is found, a framer goes into frame (**MX_J0_OOF_[i]** = 0). Once a J0 monitor framer is in-frame, it remains in frame until three consecutive section trace frames are received with at least one MSB bit error.

The **MX_J0_OOF_[i]_D** delta bit is set when **MX_J0_OOF_[i]** changes state.

In the SONET mode (**MX_SDH_J0_[i]** = 0), the J0 frame indication is held in the in-frame state (**MX_J0_OOF_[i]**=0).

3.4.2.2 Pattern Acceptance and Comparison

Once in frame, the J0 monitor blocks look for 3 consecutive 16 byte (**MX_SDH_J0_[i]** = 1) or 1 byte (**MX_SDH_J0_[i]** = 0) section trace frames. When 3 consecutive identical frames are received, the accepted frame is stored in **MX_J0_[i]_[15:0]_[7:0]** (if **MX_SDH_J0_[i]** = 1) or **MX_J0_[i]_[15]_[7:0]** (if **MX_SDH_J0_[i]** = 0).

Accepted frames are compared to the previous contents of these registers. When a new value is stored, the **MX_J0_[i]_D** delta bit is set.

3.4.3 BIP-96 or BIP-24 (B2) Checking

The Missouri checks the received B2 bytes for correct BIP-8 values. Even parity BIP-384 is calculated over all groups of 3, 12, or 48 bytes of each frame (for STS-3, STS-12 or STS-48 signals, respectively), except the first three rows of TOH (SOH in SONET and RSOH in SDH). The calculation is done on the received data after descrambling. This value is then compared to the B2 values in the following frame after descrambling. The comparison can result in from 0 to 24, 96, or 384 mismatches (B2 bit errors) for STS-3, STS-12, or STS-48 signals respectively.

The number of B2 bit errors detected each frame is transferred to the Demux side Frame Generator, which may insert the result into the transmitted M1 byte of the corresponding interface (see section 4.9.3.9).

3.4.3.1 B2 Error Counting

Missouri contains sixteen 22-bit B2 error counters that either count every B2 bit error (if **MX_BIT_BLKCNT_[i]** = 0)

or every frame with at least one B2 bit error (if **MX_BIT_BLKCNT_[i]** = 1). When the performance-monitoring counters are latched, the values of these counters are latched to the **MX_B2_ERRCNT_[i]_[21:0]** registers, and the B2 error counters are cleared (see section 2.3).

If there had been at least one B2 error in the previous second (since the last pulse on LATCH_EVENT) on input **i,** then the B2 error event bit is set (**MX_B2ERR_[i]_SECE** = 1).

3.4.3.2 B2 Error Rate Threshold Blocks

For the purpose of determining whether the bit error rates of the received multiplexer side signals are above or below two different provisionable thresholds (the Signal Fail and the Signal Degrade conditions), Missouri provides two B2 error rate threshold blocks for each input. If the SF block or the SD block determines that the error rate is above the threshold, it sets **MX_B2_ERR_SF_[i]** or **MX_B2_ERR_SD_[i]**. The delta bits **MX_B2_ERR_SF_[i]_D** and **MX_B2_ERR_SD_[i]_D** are set if the corresponding error rate bits change value.

Based on the desired Signal Fail and Signal Degrade error rate thresholds, the user may provision BLOCK_SF and BLOCK_SD registers and two pairs of THRESH_SF, THRESH_SD, GROUP_SF and GROUP_SD registers. In order to allow hysteresis in setting and clearing the state bits, one of the pair of THRESH_SF, THRESH_SD, GROUP_SF and GROUP_SD registers is used for setting the state and the other of the pair of these registers for clearing the state. Thus, the registers used in the error rate threshold blocks are:

- **MX_B2_ERR_SF_[i]** = 0, determine if it should be set using: **MX_B2_BLOCK_SF_[i]_[7:0]**, **MX_B2_THRESH_SET_SF_[i]_[7:0]**, and **MX_B2_GROUP_SET_SF_[i]_[5:0]**
- **MX_B2_ERR_SF_[i]** = 1, determine if it should be cleared using: **MX_B2_BLOCK_SF_[i]_[7:0]**, **MX_B2_THRESH_CLR_SF_[i]_[7:0]**, and **MX_B2_GROUP_CLR_SF_[i]_[5:0]**
- **MX_B2_ERR_SD_[i]** = 0, determine if it should be set using: **MX_B2_BLOCK_SD_[i]_[15:0]**, **MX_B2_THRESH_SET_SD_[i]_[5:0]**, and **MX_B2_GROUP_SET_SD_[i]_[5:0]**
- **MX_B2_ERR_SD_[i]** = 1, determine if it should be cleared using: **MX_B2_BLOCK_SD_[i]_[15:0]**, **MX_B2_THRESH_CLR_SD_[i]_[5:0]**, and **MX_B2_GROUP_CLR_SD_[i]_[5:0]**

The values that should be provisioned in these registers as a function of the desired BER at which Signal Fail and Signal Degrade should be declared is shown in Table 4, Table 5, and Table 6. Note that the Signal Fail B2 BER-threshold is limited to 10^{-3} to 10^{-6} for STS-48/STM-16, 10^{-3} to 10^{-5} for STS-12/STM-4, and 10^{-3} to 10^{-5} for STS-3/STM-1.

Table 4. Signal Fail and the Signal Degrade Provisioning Values for STS-48/STM-16

BER	BLOCK	THRESH_SET	THRESH_CLR	GROUP_SET	GROUP_CLR
10^{-3}	**1**	**154**	**30**	**4**	**5**
10^{-4}	**2**	**55**	**7**	**4**	**4**
10^{-5}	**10**	**24**	**4**	**4**	**4**
10^{-6}	**100**	**28**	**4**	**2**	**4**
10^{-7}	1000	28	4	2	4
10^{-8}	5000	15	2	2	4
10^{-9}	65000	18	3	2	4

Table 5. Signal Fail and the Signal Degrade Provisioning Values for STS-12/STM-4.

BER	BLOCK	THRESH_SET	THRESH_CLR	GROUP_SET	GROUP_CLR
10^{-3}	**1**	**39**	**8**	**4**	**5**
10^{-4}	**6**	**37**	**7**	**4**	**5**
10^{-5}	**40**	**28**	**4**	**2**	**5**
10^{-6}	400	28	4	2	5
10^{-7}	4000	28	4	2	5
10^{-8}	20,000	15	2	2	4
10^{-9}	60,000	5	1	3	6

.

Table 6. Signal Fail and the Signal Degrade Provisioning Values for STS-3/STM-1.

BER	BLOCK	THRESH_SET	THRESH_CLR	GROUP_SET	GROUP_CLR
10^{-3}	**3**	**28**	**7**	**4**	**5**
10^{-4}	**16**	**23**	**4**	**4**	**5**
10^{-5}	**160**	**28**	**4**	**2**	**5**
10^{-6}	1600	28	4	2	5
10^{-7}	16,000	28	4	2	5
10^{-8}	40,000	7	1	3	5
10^{-9}	65,000	2	1	4	28

3.4.4 K1K2 Monitoring

The K1 and K2 bytes, which are used for sending Line/MS AIS or RDI and for APS signalling, are monitored for change in status.

3.4.4.1 Line/MS AIS Monitoring and DX_LRDI_GEN and PAIS Generation

The 3 LSBs of K2 can be used as an AIS or Remote Defect Indication (RDI) at the line/MS level.

For input **i**, if K2[2:0] are received as “111” for **MX_K2_CONSEC_[i]_[3:0]** consecutive frames, then **MX_LAIS_[i]** is set. If K2[2:0] is not received as “111” for **MX_K2_CONSEC_[i]_[3:0]** consecutive frames, then **MX_LAIS_[i]** is cleared. The **MX_LAIS_[i]_D** delta bit is set when **MX_LAIS_[i]** changes state. Note that **MX_K2_CONSEC_[i]** is only defined for values between 2-15.

If **MX_LOF_[i]**, **MX_LAIS_[i]**, **MX_LOS_[i]**, or **MX_B2_ERR_SF_[i]** are active, then PAIS is generated for the affected tributaries on the multiplex side (see section 3.6.4.4). The contribution of **MX_LOS_[i]** to LRDI and PAIS

can be inhibited by setting **MX_LOS_INH_[i]** = 1. The contribution of **MX_B2_ERR_SF_[i]** to PAIS can be inhibited by setting **MX_SF_PAIS_INH_[i]** = 1. Note that **MX_LOS_INH_[i]** and **MX_SF_PAIS_INH_[i]** have no impact on the contribution of **MX_LOS_[i]** or **MX_B2_ERR_SF_[i]** to summary interrupt and delta bits.

3.4.4.2 Line/MS RDI Monitoring

K2[2:0] is also monitored for **MX_K2_CONSEC_[i]_[3:0]** consecutive receptions of “110.” **MX_LRDI_[i]** is set when this occurs. If K2[2:0] is not received as “110” for **MX_K2_CONSEC_[i]_[3:0]** consecutive receptions, then **MX_LRDI_[i]** is cleared. **MX_LRDI_[i]_D** is set when **MX_LRDI_[i]** changes state. Note that **MX_K2_CONSEC_[i]** is only defined for values between 2-15.

3.4.4.3 APS Monitoring

If the K1 byte and the 4 MSBs of the K2 byte, which are used for sending APS requests and channel numbers, are received identically for 3 consecutive frames, their values are written to **MX_K1_[i]_[7:0]** and **MX_K2_[i]_[7:4]**. Accepted values are compared to the previous contents of these registers, and when a new 12-bit value is stored, the **MX_K1_[i]_D** delta bit is set.

The K1 byte is checked for instability. If for 12 successive frames no 3 consecutive frames are received with identical K1 bytes, the **MX_K1_UNSTAB_[i]** bit is set. It is cleared when 3 consecutive identical K1 bytes are received. When **MX_K1_UNSTAB_[i]** changes state, the **MX_K1_UNSTAB_[i]_D** delta bit is set.

Bits 3 down to 0 of K2 may contain APS mode information. These bits are monitored for **MX_K2_CONSEC_[i]_[3:0]** consecutive identical values. **MX_K2_[i]_[3:0]** is written when this occurs, unless the value of bits 2 and 1 of K2 is “11” (indicating Line/MS AIS or RDI). The **MX_K2_[i]_D** delta bit is set when a new value is written to **MX_K2_[i]_[3:0]**. Note that **MX_K2_CONSEC_[i]** is only defined for values between 2-15.

The delta bits associated with the APS monitor, **MX_K1_[i]_D, DX_K2_D,** and **DX_K1_UNSTAB_D** all contribute to an APS interrupt signal, *APS_INTB.* In addition, these deltas also contribute to the standard summary interrupt signal, *INTB* (see section 7.1).

3.4.5 S1 Monitoring

The 4 LSBs of the received S1 bytes are monitored for consistent values in either 8 consecutive frames in the SONET mode, **MX_SDH_S1_[i]** = 0, or 3 consecutive frames in the SDH mode, **MX_SDH_S1_[i]** = 1. When these bits contain a consistent synchronization status message, the accepted value is written to **MX_S1_[i]_[3:0]**. Accepted values are compared to the previous contents of this register, and when a new value is stored, the **MX_S1_[i]_D** delta bit is set.

The S1 byte is also checked for message failure. If no message has met the above validation criterion (whether it is the same or different from the last accepted value) during the last second (since the last pulse on LATCH_EVENT), then the S1 fail event bit, **MX_S1FAIL_[i]_SECE**, is set.

3.4.6 M1 Monitoring

The M1 byte indicates the number of B2 errors that were detected by the remote terminal in its received signal. Missouri contains sixteen 22-bit M1 error counters that either counts every error indicated by M1 (if **MX_BIT_BLKCNT_[i]** = 0) or every frame received with M1 not equal to 0 (if **MX_BIT_BLKCNT_[i]** = 1). When the performance-monitoring counters are latched, the number of M1 errors are latched into the **MX_M1_ERRCNT_[i]_[21:0]** registers and then the M1 error counters are cleared (see section 2.3). M1 values greater than 255 for STS-48/STM-16, greater than 96 for an STS-12/STM-4 interface, or greater than 24 for an STS-3/STM-1 interface are counted as 0 errors.

For input **i**, if there has been at least one received M1 error indication in the previous second (since the last pulse on LATCH_EVENT), then the M1 error event bit, **MX_M1ERR_[i]_SECE**, is set.

3.4.7 Maintenance Action on Incoming Failures

3.4.7.1 PAIS Generation

If **MX_LOF_[i]**, **MX_LAIS_[i], MX_LOS_[i]**, or **MX_B2_ERR_SF_[i]** are active, then PAIS is generated for the affected tributaries (see section 3.6.4.4). The contribution of **MX_LOS_[i]** to LRDI and PAIS can be inhibited by setting **MX_LOS_INH_[i]** = 1. The contribution of **MX_B2_ERR_SF_[i]** to PAIS can be inhibited by setting **MX_SF_PAIS_INH_[i]** = 1. Note that **MX_LOS_INH_[i]** and **MX_SF_PAIS_INH_[i]** have no impact on the contribution of **MX_LOS_[i]** or **MX_B2_ERR_SF_[i]** to summary interrupt and delta bits.

3.4.7.2 DX_LRDI Generation

The failures listed in section 3.4.7.1 also cause maskable RDI-L to be generated on the demux transmit side (see section 4.9.3.7).

3.5 Auxiliary Data Channels

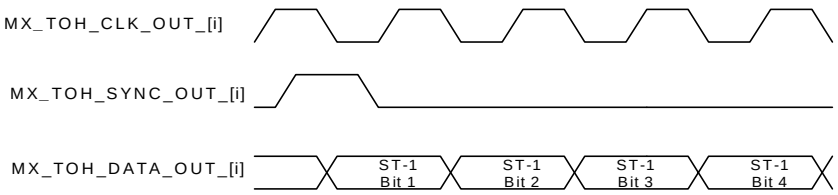
3.5.1 Serial TOH/SOH Drop Channels

The Missouri provides a serial channel for each of the sixteen possible line signals, through which the user can drop certain received TOH/SOH bytes. The bytes that are accessible via these serial channels are (in order of transmission over the serial channel): E1, F1, D1-D3, K1, K2, D4-D12, E2. The E1 and E2 orderwire bytes are defined for the purpose of carrying two 64kb/s-digitized voice signals. The F1 byte is available for use by the network provider. There are 2 DCCs defined in the TOH/SOH. The Section/Regenerator Section DCC uses the D1, D2, and D3 bytes to create a 192 kb/s channel. The Line/Multiplex Section DCC uses bytes D4 through D12 to create a 576 kb/s channel. The K1 and K2 bytes carry APS messages.

The multiplex block for each line-interface outputs a single-serial channel, *MX_TOH_DATA_OUT_[i]*. If a quadrant contains four STS-3 interfaces, then all four serial channels for that quadrant are active. If a quadrant contains a STS-12 interface, then only the first serial channel for that quadrant (*MX_TOH_DATA_OUT_[i]* for *i = 1, 5, 9,* and *13*) is active. If the MX interface is configured for a single STS-48, then only the first channel (*MX_TOH_DATA_OUT_[1]*) is active.

Each serial channel carries 27 bytes per frame, consisting of the 17 TOH bytes identified in the previous paragraph, plus 10 stuff bytes. Sixteen independent 1728 kHz clocks (*MX_TOH_CLK_OUT_[i]*) are output from the Missouri in order to provide a timing reference for all active *MX_TOH_DATA_OUT_[i]* outputs. The Missouri also provides 16 *MX_TOH_SYNC_OUT_[i]* signals that provide byte-delineation indications for each of the 16 serial channels. The Missouri will provide the TOH/SOH bytes on the 16 serial channels in the following order (ST*n* indicates a stuff byte) ST1, E1, F1, D1-D3, ST2, ST3, ST4, ST5, K1, K2, D4-D12, ST6, ST7, E2, ST8, ST9, ST10. All bytes are provided in MSB to LSB order. The Missouri will provide the first bit (the MSB) of the ST1 byte on *MX_TOH_DATA_OUT_[i]* concurrent with the falling edge of *MX_TOH_CLK_OUT_[i]* when *MX_TOH_SYNC_OUT_[i]* is asserted. The value of ST1-ST10 are undefined.

Note that the timing for *MX_TOH_CLK_OUT_[i]*, *MX_TOH_SYNC_OUT_[i]*, and *MX_TOH_DATA_OUT_[i]* is derived from an internal 77.76 MHz clock which is derived from the associated MX line clock (*MX_CLK_IN_[i]*). The falling-edge of *MX_TOH_CLK_OUT_[i]* should be used for latching *MX_TOH_SYNC_OUT_[i]*. The rising-edge of *MX_TOH_CLK_OUT_[i]* should be used for latching *MX_TOH_DATA_OUT_[i]*.



In addition to this method of reporting the received K1 and K2 bytes for each tributary, the Missouri also provides register map access to these same bytes (see section 3.4.4.1).

3.5.2 External Alarm Signal

The Missouri provides 16 output signals, *MX_ALARM_OUT_[i]*, that report SONET/SDH Receive alarms, on a per tributary basis. *MX_ALARM_OUT_[i]* is set (= 1) when any of the unmasked alarm conditions exist for tributary [i], and is cleared (= 0) when all unmasked alarm conditions are cleared for tributary [i]. The alarm set that contributes to *MX_ALARM_OUT_[i]* is provisionable, via individual mask registers.

MX_ALARM_OUT_[i] = (**MX_OOF_[i]** && !**MX_OOF_ALARM_INH_[i]**) ||

(**MX_LOF_[i]** && !**MX_LOF_ALARM_INH_[i]**) ||

(**MX_LOC_[i]** && !**MX_LOC_ALARM_INH_[i]**) ||

(**MX_LAIS_[i]** && !**MX_LAIS_ALARM_INH_[i]**) ||

(**MX_LOS_[i]** && !**MX_LOS_ALARM_INH_[i]**)

3.6 Pointer Processors

3.6.1 Concatenation Provisioning

The operation of the Pointer Processors is influenced by the concatenation state of the received signals, and whether they are SONET or SDH signals. The expected concatenation state of the received signals is provisioned through the **MX_CONFIG_[20:0]** registers. The interpretation of these registers, given in Table 7, is a function of the **MX_SDH_PI_[i]** (to the extent that it determines whether the payloads are SONET or SDH payloads) and the **MX_LINE_CONFIG_[4:0]** registers. Note that configurations with STS-48c/AU-4-16c payloads are only valid if **MX_LINE_CONFIG_[4]**=1, and configurations with STS-12c/AU-4-4c payloads are only valid if **MX_LINE_CONFIG_[4]**=0, and **MX_LINE_CONFIG_[q]**=1 for the corresponding quadrant.

The received H1 and H2 bytes contain concatenation information. The Missouri can be provisioned to use the **MX_CONFIG_[20:0]** register for determining the line MX port configuration by setting **MX_CONFIG_AUTO** = 0. The Missouri will ignore the concatenation information in the H1-H2 bytes in this state. Alternatively, the **MX_CONFIG_[20:0]** register is ignored and the H1-H2 bytes concatenation information is used to configure the MX port if **MX_CONFIG_AUTO** = 1 (see section 3.6.2.2).

Table 7. SONET/SDH Payload Configuration with STS-3/12/48 (STM-1/4/16) Signals

MX_CONFIG_[20:0][a]	Interpretation
1_xxxx_xxxx_xxxx_xxxx_xxxx	STS-48c/AU-4-16c payload (Tributary Index = 1,1)
0_**1**xxx_xxxx_xxxx_xxxx_xxxx	STS-12c/AU-4-4c payload in first quadrant (Tributary index = 1,1)
0_x**1**xx_xxxx_xxxx_xxxx_xxxx	STS-12c/AU-4-4c payload in second quadrant (Tributary index = 5,1)
0_xx**1**x_xxxx_xxxx_xxxx_xxxx	STS-12c/AU-4-4c payload in third quadrant (Tributary index = 9,1)
0_xxx**1**_xxxx_xxxx_xxxx_xxxx	STS-12c/AU-4-4c payload in fourth quadrant (Tributary index = 13,1)
0_0xxx_**1**xxx_xxxx_xxxx_xxxx	STS-3c/AU-4 payload in first STS-3 tributary group of first quadrant (Tributary index = 1,1)
0_0xxx_**0**xxx_xxxx_xxxx_xxxx	STS-3/3xAU-3 payloads in first STS-3 tributary group of first quadrant (Tributary indexes = (1,1), (1,2), (1,3))
0_0xxx_x**1**xx_xxxx_xxxx_xxxx	STS-3c/AU-4 payload in second STS-3 tributary group of first quadrant (Tributary index = 2,1)
0_0xxx_x**0**xx_xxxx_xxxx_xxxx	STS-3/3xAU-3 payloads in second STS-3 tributary group of first quadrant (Tributary indexes = (2,1), (2,2), (2,3))
. . .	
0_xxx0_xxxx_xxxx_xxxx_xxx**1**	STS-3c/AU-4 payload in fourth STS-3 tributary group of fourth quadrant (Tributary index = 16,1)
0_xxx0_xxxx_xxxx_xxxx_xxx**0**	STS-3/3xAU-3 payloads in fourth STS-3 tributary group of fourth quadrant (Tributary indexes = (16,1), (16,2), (16,3))

a. **MX_CONCAT_[20:0]** has a similar interpretation.

3.6.2 Pointer State Determination

Pointer state determination involves examining the 12 pairs of H1-H2 bytes in each quadrant to establish the state of each pair and from these states, determining which of the SPE/VCs are indicated as being concatenated by the received pointers. For tributaries in the Normal state (or transitioning to Normal), the path overhead offset indicated by the pointer value (PTR) carried within the appropriate H1-H2 byte pair is determined.

3.6.2.1 State Transition Rules

Each of the 12 pairs of H1-H2 bytes in each quadrant are monitored and are considered to be in 1 of 4 states:

- Normal (NORM = 00)
- Alarm Indication Signal (AIS = 01)
- Loss of Pointer (LOP = 10)
- Concatenated (CONC = 11)

The individual states are stored in **MX_PTR_STATE_[x]_[1:0]**. The states of individual pairs of H1-H2 bytes are then combined to determine which received SPE/VCs are concatenated and to determine the state of the concatenated pointers. **See User Note 14.1.5.2 for important information.**

3.6.2.2 Concatenated Pointer Determination

The **MX_CONCAT_[20:0]** register contains the received signal concatenation configuration as indicated by the H1-H2 bytes. The bits in this register are interpreted in a manner similar to those in the **MX_CONFIG_[20:0]** register as shown in Table 7. Transitions of bits in this register are driven directly from the individual H1-H2 states, **MX_PTR_STATE_x_[1:0]**. When a transition occurs, the corresponding **MX_CONCAT_[20:0]_D** delta bit is set.

The operation of the remainder of the pointer processor is influenced either by the **MX_CONCAT** register (if **MX_CONFIG_AUTO** = 1), or by the provisioned configuration values, **MX_CONFIG** (if **MX_CONFIG_AUTO** = 0). Based on one of these registers, the pointer processor establishes which of the SPE/VCs are concatenated and thus determines which pointer states to set **MX_PAIS_x** and **MX_LOP_x** register bits to, which pointer bytes to interpret, and the kind of pointers that are generated (see section 3.6.4).

See User Note 14.1.5.2 for important information.

3.6.2.3 State of Concatenated Pointers

The device sets **MX_PAIS_x** and **MX_LOP_x** register bits that indicate the pointer state for the configured or automatically determined tributaries (see section 3.6.2.2).

Changes in **MX_PAIS_x** and **MX_LOP_x** state values are indicated by the **MX_PAIS_x_D** and **MX_LOP_x_D** delta bits.

3.6.3 Pointer Interpretation

3.6.3.1 Interpretation Rules

The H1-H2 byte pairs (or the first H1-H2 byte pair of concatenated tributaries) is interpreted to locate the start of the SPE/VC for that tributary. The pointer is interpreted using SDH rules if **MX_SDH_PI_[i]**=1 or SONET rules if **MX_SDH_PI_[i]**=0. In addition, the SS bits are considered only in SDH mode (**MX_SDH_PI_[i]**=1) when **MX_SS_EN_[i]**=1.

In SDH mode (**MX_SDH_PI_[i]**=1), the pointer interpreter looks for “10” in the received SS bits when the SS bits are being used (**MX_SS_EN_[i]**=1). If the SS bits are not received as “10” when **MX_SS_EN_[i]**=1, a LOP is generated which in turn generates an AIS-P. When the SS bits are not being considered (**MX_SS_EN_[i]**=0) the SS bits are ignored and an AIS-P is not generated when the SS bits are not received as “10.”

3.6.3.2 Justification Counters

Using these pointer interpretation rules, the pointer processor blocks determine which bytes belong to the SPE/VC, and locate the start of the POH for each of the possible 12 tributaries.

The Pointer Processors contain 5-bit pointer interpreter justification counters that count every positive and negative justification. When the performance-monitoring counters are latched, the positive and negative justification counts are latched into the **MX_PI_POSCNT_x_[4:0]** and **MX_PI_NEGCNT_x_[4:0]** registers, respectively, and then the justification counters are cleared (see section 2.3).

If for tributary **x**, there has been at least one positive or negative justification in the previous second, the **MX_PI_POSCNT_SECE_x** or **MX_PI_NEGCNT_SECE_x** bit, respectively, is set.

3.6.4 Pointer Generation

Based on the interpreted received pointers, the Pointer Processors writes all SPE/VC bytes into FIFOs using the Multiplexer input clocks, *MX_CLK_IN_[i]*. The received TOH/SOH bytes are eliminated upon being written to the FIFOs. The SPE/VC are read from the FIFOs using the system reference input clock, *SYS_CLK_IN*, as they are needed to fill the SPE/VC bytes of SONET/SDH frames created by the Pointer Processors. The TOH/SOH bytes in these frames are “dummy” bytes, except for H1H2H3, as they are later overwritten by the multiplexer frame generator block. If a FIFO is near its empty or full level, a positive or negative justification, respectively, is created in the generated pointer.

3.6.4.1 Frame Boundary Alignment

If the quadrants contains STS-3 signals, all four of the Pointer Processors within the quadrant are active and four separate SONET/SDH frames are created. The frame boundaries of these frames are created in alignment so that these may be multiplexed together with outputs from the other quadrants into a single STS-48/STM-16 stream.

There is the potential for timing ambiguities associated with the exact position of the *SYS_SYNC_IN* input as it is retimed to the Missouri's internal clock. Therefore, the period of the rising edge of the *SYS_SYNC_IN* input may not be precisely 125 µs each and every period. The Missouri will not rely on the position of the *SYS_SYNC_IN* input on a frame by frame basis, but will instead 'resync' its frame generation circuitry to a single rising edge of *SYS_SYNC_IN* when instructed to by the user. This resynchronization to the *SYS_SYNC_IN* is armed when **SYS_SYNC_IN_RESYNC** is set to 1. Missouri will then resynchronize its internal frame position generator to the next rising edge of *SYS_SYNC_IN*. Missouri's frame generator will flywheel on this frame position, regardless of the *SYS_SYNC_IN* signal, until instructed to resync again.

See User Note 14.1.7.1 for important information.

3.6.4.2 Pointer Generation Rules

Pointers are generated on the output based upon incoming pointer values and justifications, frequency variations between input and reference clocks, and the fill level of internal FIFOs.

When an AIS is not generated, the SS bits in H1 are generated as "00" in the default SONET mode (**MX_SDH_PG_[1]**=0) or "10" in the alternate SDH mode (**MX_SDH_PG_[1]**=1). Note that setting (**MX_SDH_PG_[1]**=1, the first bit in the 16-bit register, will insert "10" into the SS-bits of all tributaries in the output STS-48/STM-16 frame. The other 15 bits, **MX_SDH_PG_[2:16]**, are unused.

3.6.4.3 FIFO Overflow or Underflow

If a FIFO overflows or underflows, the **MX_PG_FIFO_x_E** event bit is set.

See User Note 14.1.5.1 for important information.

3.6.4.4 PAIS Generation

PAIS for tributary **x** is generated by setting the H-bytes and the entire SPE/VC for tributary **x** to all-ones.

If **MX_LOF_[i]** = 1, **MX_LAIS_[i]** = 1, (**MX_LOS_[i]** = 1 and **MX_LOS_INH_[i]** = 0), or (**MX_B2_ERR_SF_[i]**=1 and **MX_SF_PAIS_INH_[i]** = 0) then PAIS is generated for the affected tributaries. For example, if **MX_LOF_[i]**=1, then PAIS is generated for all tributaries input through the associated low-speed mux signal (*MX_DATA_IN_[i]* for a STS-3 or STS-12 signal, or *MX48_PDATA_IN* for a STS-48 signal).

If **MX_PAIS_x** or **MX_LOP_x** is active, then Missouri inserts PAIS for tributary **x**. If **MX_FAST_AIS_x** = 1 and the last frame received for tributary **x** contains all ones in its H-bytes, then Missouri inserts PAIS for tributary **x.**

The user may force PAIS generation for tributary **x** by setting **MX_PAIS_GEN_x** = 1.

See User Note 14.1.5.2 for important information.

3.6.4.5 Unequipped Generation

The Pointer Generators can also insert Unequipped signal. If **MX_PAIS_GEN_x** = 0, and **MX_UNEQ_GEN_x** = 1, the entire SPE/VC, for tributary **x**, is generated with all-zeros. The pointer value used for unequipped insertion must be a valid pointer value; the specific value is not specified. An NDF does not need to be generated when the unequipped signal insertion is removed (**MX_UNEQ_GEN_x** is cleared).

3.6.4.6 Justification Counters

The Pointer Processors contain 5-bit pointer generator justification counters that count every positive or negative justification on a per STS-1 basis. When the performance-monitoring counters are latched, the positive and negative justification counts are latched into the **MX_PG_POSCNT_x_[4:0]** and **MX_PG_NEGCNT_x_[4:0]** registers,

respectively, and then the justification counters are cleared (see section 2.3).

If for tributary **x**, there has been at least one positive or negative justification in the previous second, the **MX_PG_POSCNT_SECE_x** or **MX_PG_NEGCNT_SECE_x** bit, respectively, is set.

3.7 MX Prot Interface

3.7.1 MX PROT Interface Description

The Missouri's MX Protection interface consists of a standard STS-48/STM-16 multiplexed data stream (regardless of the original signal combination on the low-speed interface) as a 16-bit wide parallel bus with an accompanying clock at 155.52 MHz.

The Missouri outputs *MX_PROT_SYNC_OUT* and *MX_PROT_CLK_OUT* signals with the Protection *MX_PROT_DATA_OUT[16:1]* data stream. The 0 to 1 transition of *MX_PROT_SYNC_OUT* indicates that the first A1 byte is on bits 16:9 of the *MX_PROT_DATA_OUT_[16:1]* data bus. **See User Note 14.1.2.1 for important information.**

An external framer must supply the Missouri with a start of frame indication, *MX_PROT_SYNC_IN* and a clock signal *MX_PROT_CLK_IN* along with the Protection *MX_PROT_DATA_IN[16:1]* data stream. A 0 to 1 transition on the *MX_PROT_SYNC_IN* signal should indicate that the first A1 byte is on bits 16:9 of the *MX_PROT_DATA_IN_[16:1]* data bus.

The MX Protection interface also provides an odd parity check bit, which is received and transmitted on signals *MX_PROT_PRTY_IN* and *MX_PROT_PRTY_OUT*. Parity is performed across all 16 bits of the data, as well as the frame sync indication, in each direction. If a parity error occurs, the **MX_APS_PROT_PRTY_E** register bit is set. For testing purposes, the outgoing parity is even if **MX_APS_PROT_PRTY_OUT** is set to 1.

3.8 Mux Selector/Cross-Connect

The STS-48 data from the MX Pointer Processor is output to a mux selector/Cross-Connect function, which also receives STS-48 data from three other sources: *MX_PROT_DATA_IN_[16:1]*, *DX_DATA_IN* (after Pointer Processing by the demux side Pointer Processor), and *DX_PROT_DATA_IN_[16:1]*. Any of the 4 input streams can be selected as the input to the SONET/SDH frame generation block on the multiplexer side via the **MUXSEL_x_[7:0]** registers. Furthermore, the selector is based on a per-STS-1 basis, and includes a time-slot-interchanger, so that on a per output STS-1 time slot basis, any of the input STS-1s from any of the four sources may be selected. A multicast function is provided since it is permitted to select the same input for multiple output time-slots. Table 8 illustrates how the selections are made. **MUXSEL_x_[7:0]** selects the source for output STS-1 **x**.

Table 8. Mux Selector/Cross-Connect Table

MUXSEL_x_[7:0]	Data Selected
00_0000_00	**MX_DATA_IN** (or *MX48_PDATA_IN*) data: Tributary 1_1
00_0000_01	**MX_DATA_IN** (or *MX48_PDATA_IN*) data: Tributary 1_2
00_0000_1x	**MX_DATA_IN** (or *MX48_PDATA_IN*) data: Tributary 1_3
00_0001_[00:1x]	**MX_DATA_IN** (or *MX48_PDATA_IN*) data: Tributary 2_[1:3]
:	:
00_1111_[00:1x]	**MX_DATA_IN** (or *MX48_PDATA_IN*) data: Tributary 16_[1:3]
01_[0000:1111]_[00:1x]	**MX_PROT_DATA_IN** data: Tributary 1:16_[1:3]

Table 8. Mux Selector/Cross-Connect Table

MUXSEL_x_[7:0]	Data Selected
10_[0000:1111]_[00:1x]	**DX_DATA_IN** data: Tributary 1:16_[1:3]
11_[0000:1111]_[00:1x]	**DX_PROT_DATA_IN** data: Tributary 1:16_[1:3]

See User Note 14.1.8.3 for important information.

3.9 SONET/SDH Frame Generation

The SONET/SDH frame generation block on the Multiplexer side creates an STS-48/STM-16 output by generating the TOH/SOH bytes and scrambling (if enabled) all bytes of the SONET/SDH signal except for the first row of TOH/SOH bytes.

3.9.1 Frame Alignment

The position of the generated frame(s) is fixed but unspecified with respect to the input *SYS_SYNC_IN* signal (after the **SYS_SYNC_IN_RESYNC** bit was set).

If **MX_FRAME_IN_INH** = 1, the Missouri does not use the *SYS_SYNC_IN* input to synchronize its frame generator. The frame generator instead flywheels and produces its own internal 8-kHz frame sync signal.

3.9.2 TOH/SOH Generation

3.9.2.1 Frame Bytes (A1 and A2)

For testing purposes, A1 and A2 can be generated with errors by setting **MX_A1A2_ERR**. If **MX_A1A2_ERR** = 1, then **MX_A1A2_ERR_NUM_[2:0]** consecutive frames in each group of 8 frames is generated with A1 and A2 exclusive-ORed with the contents of **MX_A1A2_ERR_PAT_[15:0]**. The MSB of A1 is XORed with **MX_A1A2_ERR_PAT_[15]**, and the LSB of A2 is XORed with **MX_A1A2_ERR_PAT_[0]**.

3.9.2.2 Section Trace/Regenerator Section Trace (J0) and Section Growth/Spare (Z0)

Section Trace. Over periods of 16 consecutive frames, the Frame Generator continuously transmits the 16-byte pattern contained in **MX_J0_[15:0]_[7:0]**. The bytes are transmitted in descending order starting with **MX_J0_[15]_[7:0]**.

Section Growth/Spare. The Z0 bytes are transmitted in order as the binary equivalent of 2 to 48.

3.9.2.3 Section BIP-8 (B1)

The B1 Bit Interleaved Parity 8 (BIP-8) is transmitted as even parity (normal) if **MX_B1_INV** = 0. Otherwise, odd parity (incorrect) is generated. The BIP-8 is calculated over all bits of the previous frame after scrambling and placed into the B1 byte of the current frame before scrambling.

By definition of BIP-8, the first bit of B1 provides parity over the first bit of all bytes of the previous frame, the second bit of B1 provides parity over the second bit of all bytes of the previous frame, etc.

3.9.3 AIS Generation

Normal frame generation is suspended during transmission of a Line (Multiplex Section) Alarm Indication Signal, AIS-L, or Path AIS, AIS-P.

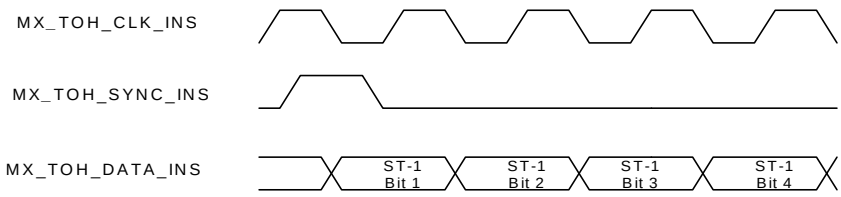
LAIS generation is controlled by the **MX_LAIS_GEN** register. If **MX_LAIS_GEN** = 1, the first 3 rows of the TOH/SOH are generated normally, but the remainder of the TOH/SOH bytes and the SPE/VC bytes are transmitted as all-ones.

3.9.3.1 Serial TOH/SOH Insert Channel

The Missouri provides a serial channel, through which the user can insert certain TOH/SOH bytes. The bytes that are accessible via this serial channel are (in order of transmission over the serial channel): E1, F1, D1-D3, K1, K2, D4-D12, E2. The E1 and E2 orderwire bytes are defined for the purpose of carrying two 64kb/s digitized voice signals. The F1 byte is available for use by the network provider. There are 2 DCCs defined in the TOH/SOH. The Section/Regenerator Section DCC uses the D1, D2, and D3 bytes to create a 192 kb/s channel. The Line/Multiplex Section DCC uses bytes D4 through D12 to create a 576 kb/s channel. The K1 and K2 bytes carry APS messages.

The transmit block accepts a single serial input, *MX_TOH_DATA_INS.* The serial channel carries 27 bytes per frame, consisting of the 17 TOH bytes identified in the previous paragraph, plus 10 stuff bytes. A single 1728 kHz *MX_TOH_CLK_INS* clock is output from the Missouri in order to provide a timing reference for the *MX_TOH_DATA_INS* input. The Missouri also provides a single *MX_TOH_SYNC_INS* signal as a byte delineation indication for the serial channel. The Missouri will interpret the bytes received on the serial channel in the following order (ST# indicates a stuff byte, which will be ignored by the Missouri) ST1, E1, F1, D1-D3, ST2, ST3, ST4, ST5, K1, K2, D4-D12, ST6, ST7, E2, ST8, ST9, ST10. All bytes are expected to be received in MSB to LSB order. The Missouri will interpret the bit received on *MX_TOH_DATA_INS* concurrent with the output of a falling-edge of *MX_TOH_SYNC_INS* as the first bit (the MSB) of the ST1 byte.

MX_TOH_SYNC_INS should be sampled on the falling edge of *MX_TOH_CLK_INS*. The falling-edge of *MX_TOH_CLK_INS* should be used to clock-out *MX_TOH_DATA_INS* to the Missouri. The Missouri latches *MX_TOH_DATA_INS* on the rising-edge of *MX_TOH_CLK_INS*.



Note that *MX_TOH_CLK_INS* and *MX_TOH_SYNC_INS* are generated synchronously from an internal 77.76 MHz clock that is derived from *SYS_CLK_IN*.

In addition to this method of inserting the K1 and K2 bytes, the Missouri also provides register map access to these same bytes as described in section 3.9.3.4.

3.9.3.2 Pointer Bytes (H1, H2) and Pointer Action Byte (H3)

Except in the case of AIS generation, the H1, H2, and H3 bytes are always passed unchanged through the Multiplexer Frame Generator.

3.9.3.3 Line/MS BIP-384 (B2)

There are 48 B2 bytes in the TOH/SOH, and together they provide a BIP-384 error detection capability. Each B2 byte provides BIP-8 parity over bytes in 1 of 48 groups of bytes in the previous frame. The B2 byte in column j, provides BIP-8 parity over bytes in the previous frame (except those in the first 3 rows of TOH/SOH) that appear in columns j + 48k, where k = 0 through 89. The BIP-8 is transmitted as even parity (normal) if **MX_B2_INV** = 0.

Otherwise, odd parity (incorrect) is generated. The BIP-8 values are calculated over bytes in the previous STS-48/STM-16 frame before scrambling and placed into the B2 bytes of the current frame before scrambling.

3.9.3.4 APS Channel and Line/MS AIS/RDI (K1 and K2)

The user can select the method of access for the K1K2 bytes via the **MX_K1K2_APS** and **MX_K2_3LSB** registers.

K1 and the 5 MSBs of K2 are used for automatic protection switching (APS) signaling. In the default **MX_K1K2_APS** = 0 state, the **MX_K1GEN_[7:0]** and **MX_K2GEN_[7:3]** bits are the source for the K1[7:0] and K2[7:3] bits in the outgoing TOH/SOH. If **MX_K1K2_APS** = 1, *MX_TOH_DATA_INS* is the source for the outgoing K1[7:0] and K2[7:3] bits.

The 3 LSBs of K2 are used as an AIS or Remote Defect Indication (RDI) at the line/MS level, and in SONET, they are also used for APS signalling. In the default **MX_K2_3LSB** = 0 state, the 3 LSBs of K2 are controlled from 3 sources. In order of priority, these are:

- If **MX_LAIS_GEN** = 1, they are transmitted as all-ones (as are all line/MS overhead bytes)
- else if **MX_LRDI_INH** = 0 and if ((**DX_LOS**=1 and not **DX_LOS_INH**=1) or **DX_LOF**=1 or **DX_LOC**=1 or **DX_LAIS** = 1), they are transmitted as “110” for a minimum of 20 frames
- else **MX_K2GEN_[2:0]** is transmitted

If **MX_K2_3LSB** = 1, *MX_TOH_DATA_INS* is the source of the 3 LSBs of K2.

See User Note 14.1.4.1 for important information.

3.9.3.5 Synchronization Status (S1)

The transmitted S1 byte is set to **MX_S1GEN_[7:0]**.

3.9.3.6 Line/MS REI (M1)

The Demux Side monitors B2 bit errors in the received signal. The number of B2 errors detected each frame is transmitted from the Demux Side to the Mux side (see section 4.4.3). This error value can range from 0 to 255 and values greater than 255 are truncated to 255.

The user can force the transmission of REI error indications by setting **MX_M1GEN_ERR** = 1. This causes all-ones to be transmitted in the M1 byte. Else if **MX_LREI_INH** = 0, the M1 byte is set equal to the most recent B2 error count. Otherwise, when **MX_LREI_INH** = 1, the M1 byte is set to all zeros.

3.9.3.7 Growth/Undefined (Z1 and Z2)

The Missouri fills these bytes with all-zeros.

3.9.4 Scrambling

The SONET/SDH signals are scrambled by the Frame Generators using the frame synchronous scrambling sequence generated from the polynomial **$g(x) = x^7 + x^6 + 1$**. For testing purposes, the scrambler can be disabled by setting **MX_SCRINH** = 1.

3.10 High-Speed Loopbacks

3.10.1 DX_TO_MX

No high-speed loopback is provided in this direction. It may be emulated by using the **MUXSEL_x_[7:0]** register (see section 3.8).

3.11 Clock Reference Output

Missouri outputs a reference clock signal through output signal *RX_REF_CLK_OUT.* The user can select any of the input clocks its receives to serve as the clock source for this reference output. The register **RX_REF_CLK_SEL_[4:0]** selects between the possible reference clocks for *RX_REF_CLK_OUT* and **RX_REF_CLK_FREQ_[1:0]** selects the frequency of this output clock.

Table 9. RX_REF_CLK_SEL_[4:0] Register Values

RX_REF_CLK_SEL_[4:0]	Reference Clock
0 0000	MX_CLK_IN_[1]
0 0001	MX_CLK_IN_[2]
0 0010	MX_CLK_IN_[3]
:	:
0 1111	MX_CLK_IN_[16]
1 0000	DX_CLK_IN
1 1111	SYS_CLK_IN
(other values)	Undefined

Table 10. RX_REF_CLK_FREQ_[1:0] Register Value

RX_REF_CLK_FREQ_[1:0]	Reference Clock Frequency
00	8 kHz (note that this is not a frame sync in that it has no fixed relationship to the framing of the input signal)
01	19.44 MHz
10	38.88 MHz
11	77.76 MHz

3.12 Mux I/O Disable and Clock Inversion

Primarily for power savings, but also to reduce external EMI and internal noise, all primary data I/O (including their associated clocks) have disable capability. The method of disable varies depending on the type of I/O:

1. Differential LVPECL: Outputs tristated and also disabled internally. Inputs are disabled at the front end of the receiver.
2. Differential LVDS: Same as for Differential LVPECL.
3. LVCMOS outputs: Outputs are gated (prior to retiming) to keep at a static level. LVCMOS inputs will have internal pulldowns; for maximum power savings, the accompanying clock inputs should also be disabled.

MX_IN_INH_[i] disables *MX_DATA_IN_[i]* and *MX_CLK_IN_[i]* (LVPECL). **MX_OUT_INH** inhibits *MX_DATA_OUT* and *MX_CLK_OUT_[i]* (LVPECL). **MX_IN_INH_[15:0]** should be all-ones to disable *MX48_PDATA_IN_[15:0].*

MX_PROT_OUT_INH inhibits *MX_PROT_DATA_OUT_[16:1], MX_PROT_SYNC_OUT, MX_PROT_PRTY_OUT* (LVCMOS) and *MX_PROT_CLK_OUT* (LVDS).

MX_PROT_IN_INH inhibits *MX_PROT_DATA_IN_[16:1], MX_PROT_SYNC_IN, MX_PROT_PRTY_IN* (LVCMOS) and *MX_PROT_CLK_IN* (LVDS).

All inhibits are active high and default to 0 (all inputs and outputs enabled).

The MX side protection output clock defaults to the non-inverted sense (**MX_PROT_CLK_OUT_INV** = 0). The MX side protection output clock can be inverted by changing the **MX_PROT_CLK_OUT_INV** bit. **See User Note 14.1.2.1 for important information.**

The MX side primary output clock defaults to the inverted sense (**MX_CLK_OUT_INV** = 1). The MX side primary output clock can be restored to non-inverted by changing the **MX_CLK_OUT_INV** bit.

4.0 Processing of Data in the Demux Direction

On the high-speed side, Missouri accepts a 16-bit wide datapath, *DX_DATA_IN_[15:0]*, a frame start indication, *DX_FRAME_IN*, and a 155.52 MHz clock, *DX_CLK_IN,* associated with a STS-48/STM-16 signal. The data may have originated from a high-speed device that performs serial-to-parallel conversion of an STS-48/STM-16 signal or from a high-speed device that locates frame, does byte disinterleaving, and performs serial-to-parallel conversion of a STS-192/STM-64 signal.

4.1 High-Speed Loopbacks

4.1.1 MX_TO_DX

The Missouri DX high-speed receive section can be configured to loopback the generated MX high-speed transmit signal if **MX_TO_DX_HS_LOOP** = 1. Otherwise, the DX received signal from the *DX_DATA_IN_[15:0]* interface is selected. While in loopback, the *MX_CLK_OUT* signal is used to clock the receiver framer. If loopback is not selected, the *DX_CLK_IN* input is used to clock this circuitry.

4.2 Demux Input Monitor

4.2.1 LOC

The *DX_CLK_IN* input is monitored for loss of clock using the *UPCLK* input. If no transitions are detected on the receive line side clock for 16 periods of *UPCLK*, the **DX_LOC** bit is set. It is cleared when transitions are detected.

The **DX_LOC_D** delta bit is set if **DX_LOC** transitions from either a 0 to a 1, or from a 1 to a 0.

See User Note 14.1.3.1 for important information.

4.2.2 LOS

Missouri provides an internal LOS monitor, as well as the ability to accept a signal from an external LOS monitor.

Input signal, *DX_LOSEXT*, is provided for an external Loss of Signal indication for the Missouri. The state of this input is reported to the management interface via register **DX_LOSEXT**. *DX_LOSEXT* can be active high (**DX_LOSEXT_LEVEL** = 0, the default) or active low (**DX_LOSEXT_LEVEL** = 1). **See User Note 14.1.3.3 for important information.**

DX_LOSEXT can contribute directly to the declaration of an LOS condition which results in **DX_LOS** being set, or may first enter a delay block, where it must be set for a minimum of 3.29 µs before **DX_LOS** is set. Inhibits, **DX_LOSEXT_INH** and **DX_LOSEXT_DELAY_INH,** are provided to control both the immediate and delayed contributions of **DX_LOSEXT** to **DX_LOS**, respectively. **See User Note 14.1.3.1 for important information.**

In addition, the Missouri can itself detect an LOS condition, by monitoring the receive data (*DX_DATA_IN_[15:0]*) for a continual stream of all-zeros. If *DX_DATA_IN* == 0 for 3.29 µs, the Missouri declares Loss of Signal (**DX_LOS** = 1). A separate inhibit bit, **DX_LOS_ALL_ZERO_INH**, controls this all-zeros detection feature.

DX_LOS is cleared when all non-inhibited contributors are cleared: **DX_LOSEXT** = 0, and the incoming signal has 2 consecutive valid framing alignment patterns and, during the intervening time (one frame), no all-zeros pattern qualifying as an LOS defect (*DX_DATA_IN* == 0 for 3.29 µs) was present.

DX_LOS also contributes to Line RDI insertion in the Mux direction (see section 3.9.3.4).

4.3 STS-48/STM-16 Frame Location and Descrambler

The Missouri Receive Framer operates in 2 modes. If **DX_FRMR_INH** = 0 (the default), the Missouri device framer

is enabled. In this mode, the parallel input signal is not assumed to be byte aligned. The SONET/SDH framer locates the framing bytes in the selected data signal, and by doing so is able to find byte alignment and determine the position of all TOH/SOH bytes. After finding frame, the framer shifts the data so that its output data is byte aligned. It also descrambles the data, performs B1 monitoring, and provides frame counter outputs to the TOHMON block.

Note that DX_FRAME_IN must be tied low in the "framer enabled" mode, that is, if **DX_FRMR_INH** = 0.

If **DX_FRMR_INH** = 1, the framer circuitry in the Missouri is bypassed. In this mode, the Missouri requires a frame start indication, *DX_FRAME_IN*, as well as data and clock

4.3.1 Framer Enabled Operation

If the framer is enabled (**DX_FRMR_INH** = 0), the Missouri devices performs the following framer processing:

When the framer state machine is out-of-frame (**DX_OOF** = 1), it searches for the 32-bit A1-A1-A2-A2 framing byte sequence of 0xF6F6_2828. This pattern may start on any of the 16 input data lines and span up to 3 input words. When the framer finds 2 successive sequences separated in time by 125 µs that exactly match the framing pattern, it goes into frame (**DX_OOF** = 0) and byte aligns its output data bus.

The framer remains in-frame, until it receives 5 successive frames with at least 1 bit error in the A1-A1-A2-A2 framing pattern. When this occurs, **DX_OOF** is set to 1, and a new frame search is begun.

The framer also provides a loss-of-frame indication. If **DX_OOF** is active (1) continuously for 24 consecutive frames (3 ms), the **DX_LOF** bit is set to 1. Once **DX_LOF** is set, it remains high until **DX_OOF** is inactive (0) continuously for either 24 (if **DX_LOF_ALG** = 1) or 8 (if **DX_LOF_ALG** = 0) consecutive frames.

The out-of-frame and loss-of-frame indications are also available via the *DX_ALARM_OUT* Missouri output. The **DX_OOF_D** and **DX_LOF_D** delta bits contribute to the summary interrupt, and the **DX_OOF_SECE** and **DX_LOF_SECE** second event bits are set at the end of each second that the **DX_OOF** and **DX_LOF** bits are in the active state at any time during the second.

4.3.2 Framer Bypass Operation

If the framer is bypassed (**DX_FRMR_INH** = 1), the Missouri devices performs the following:

An external framer must supply the Missouri with a start of frame indication, *DX_FRAME_IN.* The Missouri sets its internal frame counter when the *DX_FRAME_IN* input transitions from 0 to 1. The Missouri continues to monitor *DX_FRAME_IN* as long as it is present. If the *DX_FRAME_IN* signal is lost, or no longer detected, the Missouri will flywheel. The relationship of the start of frame to the 0 to 1 transition of *DX_FRAME_IN* is provisioned through the **DX_FIN_BYTE_TYPE_[1:0]** register. This provisioning register allows the Missouri to interface directly to external framers that may supply a start of frame indication in different positions relative to the first row of section/multiplex section overhead.The values that should be provisioned in the **DX_FIN_BYTE_TYPE_[1:0]** register is given in Table 11.

Table 11. STS-48/STM-16 Provisioning for DX_FIN_BYTE_TYPE_[1:0]

Data on *DX_DATA_IN_[15:8]* when *DX_FRAME_IN* transitions to 1	Data on *DX_DATA_IN_[7:0]* when *DX_FRAME_IN* transitions to 1	DX_FIN_BYTE_TYPE_[1:0]
next to last payload byte of frame	last payload byte of frame	00 (the default)
first A1 byte	second A1 byte	01
next to last Z0 byte	last Z0 byte	10

Table 11. STS-48/STM-16 Provisioning for DX_FIN_BYTE_TYPE_[1:0]

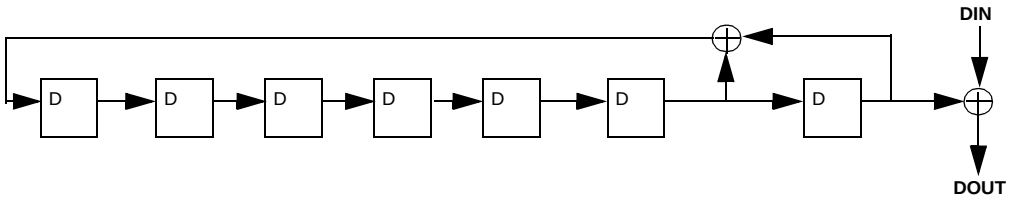
Data on *DX_DATA_IN_[15:8]* when *DX_FRAME_IN* transitions to 1	Data on *DX_DATA_IN_[7:0]* when *DX_FRAME_IN* transitions to 1	DX_FIN_BYTE_TYPE_[1:0]
first byte after last Z0 byte (first payload byte in frame)	second payload byte	11

Based on the *DX_FRAME_IN* input and the value of **DX_FIN_BYTE_TYPE_[1:0]**, the Missouri monitors the A1 and A2 bytes for errors. While out-of-frame in the framer bypass mode, the Missouri does not search for frame. It continues to keep its internal frame counter aligned with the *DX_FRAME_IN* input.

4.3.3 Descrambling

Data may be descrambled with a frame synchronous descrambling sequence generated from the polynomial **g(x) = $x^7 + x^6 + 1$** before it is output from Frame monitoring. The descrambling is done in parallel, but the result is equivalent to the serial descrambler shown in Figure 2. The descrambler is initialized to “1111111” at the beginning of the byte in column 144 of row 1 (the first SPE/VC byte), and it descrambles the entire SONET/SDH signal except for the first row of TOH/SOH. For testing purposes and when the *DX_DATA_IN_[15:0]* data originates from an STS-192/STM-64 signal that has already been descrambled, the descrambler can be disabled by setting the **DX_DSCRINH** bit to 1.

Figure 2: SONET/SDH Descrambler



4.4 Transport Overhead Monitoring

The TOH/SOH monitoring block consists of B1, J0, B2, K1K2, S1 and M1 monitoring. These TOH/SOH bytes are monitored for errors or changes in states.

4.4.1 B1 Monitor

The Missouri checks the B1 bytes for correct Bit Interleaved Parity 8 (BIP-8) values. Even parity BIP-8 is calculated over all bytes of each frame before descrambling. This value is then compared to the received B1 value in the following frame after descrambling. The comparison can result in from 0 to 8 mismatches (B1 bit errors).

The Missouri contains a single 16-bit B1 error counter that either counts every B1 bit error (if **DX_BIT_BLKCNT** = 0) or every frame with at least one B1 bit error (if **DX_BIT_BLKCNT** = 1). When the performance-monitoring counters are latched, the B1 error count is latched into the **DX_B1_ERRCNT_[15:0]** register and then the B1 error counter is cleared (see section 2.3).

If there has been at least one B1 error in the previous second (since the last pulse on LATCH_EVENT), then the B1 error event bit, **DX_B1ERR_SECE**, is set.

4.4.2 J0 Monitoring

In the SONET mode, **DX_SDH_J0** = 0, J0 monitoring consists of examining the received J0 bytes for values that match consistently for 3 consecutive frames. When a consistent J0 value is received, it is written to **DX_J0_[15]_[7:0]**.

In the SDH mode, **DX_SDH_J0** = 1, the J0 byte is expected to contain a repeating 16-byte section trace frame that includes the Section Access Point Identifier. J0 monitoring consists of locking on to the start of the 16-byte section trace frame and examining the received section trace frames for values that match consistently for 3 consecutive section trace frames. When a consistent frame value is received, it is written to **DX_J0_[15:0]_[7:0]**, with the first byte of the section trace frame, containing the frame start marker, being written to **DX_J0_[15]_[7:0]**.

4.4.2.1 Framing

In the SDH mode (**DX_SDH_J0** = 1), the MSBs of all section trace frame bytes are “0”, except for the MSB of the frame start marker byte. The J0 monitor framer searches for a single J0 byte with a “1” for its MSB, followed by 15 consecutive J0 bytes that have “0” for their MSB. When this pattern is found, the framer goes in-frame (**DX_J0_OOF** = 0). Once the J0 monitor framer is in-frame, it remains in-frame until three consecutive section trace frames are received with at least one MSB bit error.

The **DX_J0_OOF_D** delta bit is set when **DX_J0_OOF** changes state.

In the SONET mode (**DX_SDH_J0** = 0), the J0 frame indication is held in the in-frame state (**DX_J0_OOF** = 0).

4.4.2.2 Pattern Acceptance and Comparison

Once in frame, the J0 monitor block looks for 3 consecutive 16 byte (in the SDH mode) or 1 byte (in the SONET mode) section trace frames. When 3 consecutive identical frames are received, the accepted frame is stored in **DX_J0_[15:0]_[7:0]** (or **DX_J0_[15]_[7:0]** in the SONET mode).

Accepted frames are compared to the previous contents of these registers. When a new value is stored, the **DX_J0_D** delta bit is set.

4.4.3 BIP-384 (B2) Checking

The Missouri checks the received B2 bytes for correct BIP-384 values. The 48 B2 bytes together form a BIP-384. Even parity BIP-384 is calculated over all groups of 48 bytes of each frame, except the first 3 rows of TOH (SOH in SONET and RSOH in SDH). The calculation is done on the received data after descrambling. This value is then compared to the B2 values in the following frame after descrambling. The comparison can result in from 0 to 384 mismatches (B2 bit errors).

The number of B2 bit errors detected each frame is transferred to the Mux side Frame Generator, which may insert the result into the transmitted M1 byte (see section 3.9.3.6).

4.4.3.1 B2 Error Counting

The Missouri contains a single 22-bit B2 error counter that either counts every B2 bit error (if **DX_BIT_BLKCNT** = 0) or every frame with at least one B2 bit error (if **DX_BIT_BLKCNT** = 1). When the performance-monitoring counters are latched, the B2 error count is latched into the **DX_B2_ERRCNT_[21:0]** register and then the B2 error count is cleared (see section 2.3).

If there had been at least one B2 error in the previous second (since the last rising edge of LATCH_EVENT), then the B2 error event bit is set (**DX_B2ERR_SECE** = 1).

4.4.3.2 B2 Error Rate Threshold Blocks

For the purpose of determining whether or not the bit error rate of the received signal is above or below two different provisionable thresholds (the Signal Fail and the Signal Degrade conditions), the Missouri provides two B2 error rate threshold blocks. If the SF block or the SD block determines that the error rate is above the threshold, it sets **DX_B2_ERR_SF** or **DX_B2_ERR_SD**. The delta bits **DX_B2_ERR_SF_D** or **DX_B2_ERR_SD_D** are set if

the corresponding error rate bit changes value.

For each error rate threshold block, the user may provision a BLOCK register and two pairs of THRESH and GROUP registers. In order to allow hysteresis in setting and clearing the state bits, each error rate threshold block has one pair of THRESH and GROUP registers for setting the state and one pair of THRESH and GROUP registers for clearing the state. Thus, the registers used in the error rate threshold blocks are:

- **DX_B2_ERR_SF** = 0, determine if it should be set using: **DX_B2_BLOCK_SF_[7:0]**, **DX_B2_THRESH_SET_SF_[7:0]**, and **DX_B2_GROUP_SET_SF_[5:0]**
- **DX_B2_ERR_SF** = 1, determine if it should be cleared using: **DX_B2_BLOCK_SF_[7:0]**, **DX_B2_THRESH_CLR_SF_[7:0]**, and **DX_B2_GROUP_CLR_SF_[5:0]**
- **DX_B2_ERR_SD** = 0, determine if it should be set using: **DX_B2_BLOCK_SD_[15:0]**, **DX_B2_THRESH_SET_SD_[5:0]**, and **DX_B2_GROUP_SET_SD_[5:0]**
- **DX_B2_ERR_SD** = 1, determine if it should be cleared using: **DX_B2_BLOCK_SD_[15:0]**, **DX_B2_THRESH_CLR_SD_[5:0]**, and **DX_B2_GROUP_CLR_SD_[5:0]**

The values that should be provisioned in these registers as a function of the desired BER at which Signal Fail and Signal Degrade should be declared is shown in Table 12. Note that the Signal Fail B2 BER threshold is limited to 10^{-3} to 10^{-6}.

Table 12. STS-48/STM-16 Signal Fail and the Signal Degrade Provisioning Values

BER	BLOCK	THRESH_SET	THRESH_CLR	GROUP_SET	GROUP_CLR
10^{-3}	**1**	**154**	**30**	**4**	**5**
10^{-4}	**2**	**55**	**7**	**4**	**4**
10^{-5}	**10**	**24**	**4**	**4**	**4**
10^{-6}	**100**	**28**	**4**	**2**	**4**
10^{-7}	1000	28	4	2	4
10^{-8}	5000	15	2	2	4
10^{-9}	65000	18	3	2	4

4.4.4 K1K2 Monitoring

The K1 and K2 bytes, which are used for sending Line/MS AIS or RDI and for APS signalling, are monitored for change in status.

4.4.4.1 Line/MS AIS Monitoring and DX_LRDI Generation

The 3 LSBs of K2 can be used as an AIS or Remote Defect Indication (RDI) at the line/MS level.

If K2[2:0] is received as “111” for **DX_K2_CONSEC_[3:0]** consecutive frames, then **DX_LAIS** is set and the *DX_ALARM_OUT* output is asserted high (if **DX_LAIS_ALARM_INH** = 0). If K2[2:0] are not received as “111” for **DX_K2_CONSEC_[3:0]** consecutive frames, then **DX_LAIS** and *DX_ALARM_OUT* are both cleared. The **DX_LAIS_D** delta bit is set when **DX_LAIS** changes state. Note that **DX_K2_CONSEC** is only defined for values between 2-15.

4.4.4.2 Line/MS RDI Monitoring

K2[2:0] is also monitored for **DX_K2_CONSEC_[3:0]** consecutive receptions or non-receptions of “110.” **DX_LRDI** is set when this occurs. If K2[2:0] is not received as “110” for **DX_K2_CONSEC_[3:0]** consecutive receptions then

DX_LRDI is cleared. **DX_LRDI_D** is set when **DX_LRDI** changes state. Note that **DX_K2_CONSEC** is only defined for values between 2-15.

4.4.4.3 APS Monitoring

If the K1 byte and the 4 MSBs of the K2 byte, which are used for sending APS requests and channel numbers, are received identically for 3 consecutive frames, their values are written to **DX_K1_[7:0]** and **DX_K2_[7:4]**. Accepted values are compared to the previous contents of these registers, and when a new 12-bit value is stored, the **DX_K1_D** delta bit is set.

The K1 byte is checked for instability. If for 12 successive frames no 3 consecutive frames are received with identical K1 bytes, the **DX_K1_UNSTAB** bit is set. It is cleared when 3 consecutive identical K1 bytes are received. When **DX_K1_UNSTAB** changes state, the **DX_K1_UNSTAB_D** delta bit is set.

Bits 3 down to 0 of K2 may contain APS mode information. These bits are monitored for **DX_K2_CONSEC_[3:0]** consecutive identical values. **DX_K2_[3:0]** is written when this occurs, unless the value of bits 2 and 1 of K2 is “11” (indicating Line/MS AIS or RDI). The **DX_K2_D** delta bit is set when a new value is written to **DX_K2_[3:0]**. Note that **DX_K2_CONSEC** is only defined for values between 2-15.

The delta bits associated with the APS monitor, **DX_K1_D, DX_K2_D,** and **DX_K1_UNSTAB_D** all contribute to an APS interrupt signal, *APS_INTB.* In addition, these deltas also contribute to the standard summary interrupt signal, *INTB* (see section 7.1).

4.4.5 S1 Monitoring

The 4 LSBs of received S1 bytes are monitored for consistent values in either 8 consecutive frames in the SONET mode (**DX_SDH_S1** = 0) or 3 consecutive frames in the SDH mode (**DX_SDH_S1** = 1). When these bits contain a consistent synchronization status message, the accepted value is written to **DX_S1_[3:0]**. Accepted values are compared to the previous contents of this register, and when a new value is stored, the **DX_S1_D** delta bit is set.

The S1 byte is also checked for message failure. If no message has met the above validation criterion -- whether it was the same or different from the last accepted value -- at any time during the last second (since the last rising edge of LATCH_EVENT*),* then the S1 fail event bit, **DX_S1FAIL_SECE**, is set.

4.4.6 M1 Monitoring

The M1 byte indicates the number of B2 errors that were detected by the remote terminal in its received signal. The Missouri contains a single 22-bit M1 error counter that either counts every error indicated by M1 (if **DX_BIT_BLKCNT** = 0) or every frame received with M1 not equal to 0 (if **DX_BIT_BLKCNT** = 1). When the performance-monitoring counters are latched, the number of M1 errors are latched into the **DX_M1_ERRCNT_[21:0]** register and then the M1 error counter is cleared (see section 2.3). M1 values greater than 255 are counted as 0 errors.

If there has been at least one received M1 error indication in the previous second (since the last rising edge of LATCH_EVENT*),* then the M1 error event bit, **DX_M1ERR_SECE**, is set.

4.4.7 Maintenance Action on Incoming Failures

4.4.7.1 PAIS Generation

If **DX_LOF**, **DX_LAIS**, **DX_B2_ERR_SF** or **DX_LOS**, is active, then PAIS is generated for the affected tributaries on the Demux side (see section 4.6.4.4). The contribution of **DX_LOS** to LRDI and PAIS can be inhibited by setting **DX_LOS_INH** = 1. The contribution of **DX_B2_ERR_SF** to PAIS can be inhibited by setting **DX_SF_PAIS_INH** = 1.Note that **DX_LOS_INH** and **DX_SF_PAIS_INH** have no impact on the contribution of **DX_LOS** or **DX_B2_ERR_SF** to summary interrupt and delta bits.

4.4.7.2 DX_LRDI Generation

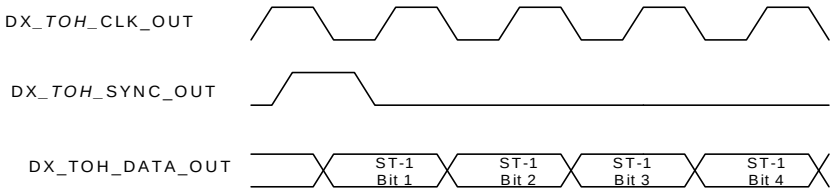
These failures also cause maskable RDI-L to be generated on the Mux transmit side (see section 3.9.3.4).

4.5 Auxiliary Data Channels

4.5.1 Serial TOH/SOH Drop Channel

The Missouri provides a serial channel for the OC-48 signal, through which the user can drop certain received TOH/SOH bytes. The bytes that are accessible via this serial channel are (in order of transmission over the serial channel): E1,F1, D1-D3, K1, K2, D4-D12, E2. The E1 and E2 orderwire bytes are defined for the purpose of carrying two 64 kb/s digitized voice signals. The F1 byte is available for use by the network provider. There are 2 DCCs defined in the TOH/SOH. The Section/Regenerator Section DCC uses the D1, D2, and D3 bytes to create a 192 kb/s channel. The Line/Multiplex Section DCC uses bytes D4 through D12 to create a 576 kb/s channel. The K1 and K2 bytes carry APS messages.

The receive block outputs a single serial channel, *DX_TOH_DATA_OUT.* The serial channel carries 27 bytes per frame, consisting of the 17 TOH bytes identified in the previous paragraph, plus 10 stuff bytes. An independent 1728 kHz clock (*DX_TOH_CLK_OUT*) is output from the Missouri in order to provide a timing reference for the *DX_TOH_DATA_OUT* output. The Missouri also provides a *DX_TOH_SYNC_OUT* signal that provides a byte delineation indication for the serial channel. The Missouri will provide the TOH/SOH bytes on the serial channel in the following order (ST# indicates a stuff byte) ST1, E1, F1, D1-D3, ST2, ST3, ST4, ST5, K1, K2, D4-D12, ST6, ST7, E2, ST8, ST9, ST10. All bytes are provided in MSB to LSB order. The Missouri will provide the first bit (the MSB) of the ST1 byte on *DX_TOH_DATA_OUT* concurrent with the falling edge of *DX_TOH_CLK_OUT* when *DX_TOH_SYNC_OUT* is asserted. The value of ST1-ST10 are undefined.



In addition to this method of reporting the received K1 and K2 bytes for each tributary, the Missouri also provides register map access to these same bytes (see section 4.4.4.1).

Note that the timing for *DX_TOH_CLK_OUT, DX_TOH_SYNC_OUT*, and *DX_TOH_DATA_OUT* is derived from an internal 77.76 MHz clock that is derived from the DX line interface clock (*DX_CLK_IN*). The falling-edge of *DX_TOH_CLK_OUT* should be used for latching *DX_TOH_SYNC_OUT*. The rising-edge of *DX_TOH_CLK_OUT* should be used for latching *DX_TOH_DATA_OUT*.

4.5.2 External Alarm Signal

The Missouri provides the output signal, *DX_ALARM_OUT*, that reports SONET/SDH Demux alarms. *DX_ALARM_OUT* is set (1) when any of the unmasked alarm conditions exist, and is cleared (0) when all unmasked alarm conditions are cleared. The alarm set that contributes to *DX_ALARM_OUT* is provisionable, via individual mask registers.

DX_ALARM_OUT = (**DX_OOF** && !**DX_OOF_ALARM_INH**) ||
(**DX_LOF** && !**DX_LOF_ALARM_INH**) ||
(**DX_LOC** && !**DX_LOC_ALARM_INH**) ||
(**DX_LAIS** && !**DX_LAIS_ALARM_INH**) ||
(**DX_LOS** && !**DX_LOS_ALARM_INH**)

4.6 Pointer Processor

4.6.1 Concatenation Provisioning

The operation of the Pointer Processor is influenced by the concatenation state of the received signals, and whether they are SONET or SDH signals. The expected concatenation state of the received signals is provisioned through the **DX_CONFIG_[20:0]** registers. The interpretation of this register, given in Table 13, is a function of the **DX_SDH_PI_[i]** register. If **DX_SDH_PI_[i]** = 0, the concatenation state of the received signals is interpreted to be SONET signals, else they are interpreted to be SDH signals.

The received H1 and H2 bytes contain concatenation information. The Missouri can be provisioned use the **DX_CONFIG_[20:0]** register for determining the line DX port configuration by setting **DX_CONFIG_AUTO** = 0. The Missouri will ignore the concatenation information in the H1-H2 bytes in this state. Alternatively, the **DX_CONFIG_[20:0]** register is ignored and the H1-H2 bytes concatenation information is used to configure the DX port if **DX_CONFIG_AUTO** = 1 (see section 4.6.2.2).

Table 13. SONET/SDH Configuration

DX_CONFIG_[20:0][a]	Interpretation
1_xxxx_xxxx_xxxx_xxxx_xxxx	STS-48c/AU-4-16c (Tributary index = 1,1)
0_**1**xxx_xxxx_xxxx_xxxx_xxxx	Within the STS-48/STM-16, the first group of 4 bytes is part of a single STS-12c/AU-4-4c (Tributary index = 1,1)
0_x**1**xx_xxxx_xxxx_xxxx_xxxx	Within the STS-48/STM-16, the second group of 4 bytes is part of a single STS-12c/AU-4-4c (Tributary index = 5,1)
0_xx**1**x_xxxx_xxxx_xxxx_xxxx	Within the STS-48/STM-16, the third group of 4 bytes is part of a single STS-12c/AU-4-4c (Tributary index = 9,1)
0_xxx**1**_xxxx_xxxx_xxxx_xxxx	Within the STS-48/STM-16, the fourth group of 4 bytes is part of a single STS-12c/AU-4-4c (Tributary index = 13,1)
0_0xxx_**1**xxx_xxxx_xxxx_xxxx	Within the STS-48/STM-16, the first byte of the first group of 4 bytes is part of a single STS-3c/AU-4 (Tributary index = 1,1)
0_0xxx_**0**xxx_xxxx_xxxx_xxxx	Within the STS-48/STM-16, the first byte of the first group of 4 bytes is part of an STS-1/AU-3 (Tributary index = 1,1)
0_0xxx_x**1**xx_xxxx_xxxx_xxxx	Within the STS-48/STM-16, the second byte of the first group of 4 bytes is part of a single STS-3c/AU-4 (Tributary index = 2,1)

Table 13. SONET/SDH Configuration

DX_CONFIG_[20:0][a]	Interpretation
0_0xxx_x**0**xx_xxxx_xxxx_xxxx	Within the STS-48/STM-16, the second byte of the first group of 4 bytes is part of an STS-1/AU-3 (Tributary index = 2,1)
. . .	
0_xxx0_xxxx_xxxx_xxxx_xxx**1**	Within the STS-48/STM-16, the fourth byte of the fourth group of 4 bytes is part of a single STS-3c/AU-4 (Tributary index = 16,1)
0_xxx0_xxxx_xxxx_xxxx_xxx**0**	Within the STS-48/STM-16, the fourth byte of the fourth group of 4 bytes is part of an STS-1/AU-3 (Tributary index = 16,1)

a. **DX_CONCAT_[20:0]** has a similar interpretation

4.6.2 Pointer State Determination

Pointer state determination involves examining the 48 pairs of H1-H2 bytes to establish the state of each pair and from these states, determine if the SPE/VCs are indicated as being concatenated by the received pointers. For tributaries in the Normal state (or transitioning to Normal), the path overhead offset indicated by the pointer value (PTR) carried within the appropriate H1-H2 byte pair is determined.

4.6.2.1 State Transition Rules

Each of the 48 pairs of H1-H2 bytes are monitored and are considered to be in 1 of 4 states. These are

- Normal (NORM = 00)
- Alarm Indication Signal (AIS = 01)
- Loss of Pointer (LOP = 10)
- Concatenated (CONC = 11)

The individual states are stored in **DX_PTR_STATE_x_[1:0]**. The states of individual pairs of H1-H2 bytes are then combined to determine which received SPE/VCs are concatenated and to determine the state of the concatenated pointers.

4.6.2.2 Concatenated Pointer Determination

The **DX_CONCAT_[20:0]** register contains the received signal concatenation configuration as indicated by the H1-H2 bytes. The bits in this register are interpreted in a manner similar to those in the **DX_CONFIG_[20:0]** register as shown in Table 13. Transitions of bits in this register are driven directly from the individual H1-H2 states, **DX_PTR_STATE_x_[1:0]**. When a transition occurs, the corresponding **DX_CONCAT_[20:0]_D** delta bit is set.

The operation of the remainder of the Pointer Processor is influenced either by the **DX_CONCAT** register (if **DX_CONFIG_AUTO** = 1), or by the provisioned configuration values, **DX_CONFIG** (if **DX_CONFIG_AUTO** = 0). Based on one of these registers, the Pointer Processor establishes which of the SPE/VCs are concatenated and thus determines which pointer states to set **DX_PAIS_x** and **DX_LOP_x** registers to, which pointer bytes to interpret, and the kind of pointers that are generated (see section 4.6.4).

4.6.2.3 State of Concatenated Pointers

The device supplies the **DX_PAIS_x** and **DX_LOP_x** register bits, to indicated the pointer state for the configured or automatically determined tributaries via the control interface. Changes in these state values are indicated by the **DX_PAIS_x_D** and **DX_LOP_x_D** delta bits.

4.6.3 Pointer Interpretation

4.6.3.1 Interpretation Rules

The H1-H2 byte pairs (or the first H1-H2 byte pair of concatenated tributaries) is interpreted to locate the start of the SPE/VC for that tributary. The pointer is interpreted using SDH rules if **DX_SDH_PI_[i]**=1 or SONET rules if **DX_SDH_PI_[i]**=0. In addition, the SS bits are considered only in SDH mode (**DX_SDH_PI_[i]**=1) when **DX_SS_EN_[i]**=1.

In SDH mode (**DX_SDH_PI_[i]**=1), the pointer interpreter looks for “10” in the received SS bits when the SS bits are being used (**DX_SS_EN_[i]**=1). If the SS bits are not received as “10” when **DX_SS_EN_[i]**=1, a LOP is generated which in turn generates an AIS-P. When the SS bits are not being considered (**DX_SS_EN_[i]**=0) the SS bits are ignored and an AIS-P is not generated when the SS bits are not received as “10.”

4.6.3.2 Justification Counters

Using these pointer interpretation rules, the Pointer Processor determines which bytes belong to the SPE/VC, and locates the start of the POH for each of the possible 12 tributaries.

The Pointer Processors contain 5-bit pointer interpreter justification counters that count every positive or negative justification. When the performance-monitoring counters are latched, the positive and negative justification counts are latched to the **DX_PI_POSCNT_x_[4:0]** and **DX_PI_NEGCNT_x_[4:0]** registers, respectively, and then the justification counters are cleared (see section 2.3).

If for tributary **x**, there has been at least one positive or negative justification in the previous second, the **DX_PI_POSCNT_SECE_x** or **DX_PI_NEGCNT_SECE_x** bit, respectively, is set.

4.6.4 Pointer Generation

Based on the interpreted received pointers, the Pointer Processors writes all SPE/VC bytes into FIFOs using the Demultiplexer input clock, *DX_CLK_IN*. The received TOH/SOH bytes are eliminated upon being written to the FIFOs. The SPE/VC are read from the FIFOs using the system reference input clock, *SYS_CLK_IN*, as they are needed to fill the SPE/VC bytes of SONET/SDH frames created by the Pointer Processors. The TOH/SOH bytes in these frames are “dummy” bytes, except for H1H2H3, as they are later overwritten by the demultiplexer frame generator block. If a FIFO is near its empty or full level, a positive or negative justification, respectively, is created in the generated pointer.

4.6.4.1 Frame Boundary Alignment

The start of the SONET/SDH frame that is created by the pointer processor is a function of the *SYS_SYNC_IN* signal. The exact internal relationship is not specified, but it must be such that the output of the Frame Generator blocks have the right relationship to the *SYS_SYNC_IN* signal, as per section 4.9.

4.6.4.2 Pointer Generation Rules

Pointers are generated on the output based upon incoming pointer values and justifications, frequency variations between input and reference clocks, and the fill level of internal FIFOs.

When an AIS is not generated, the SS bits in H1 are generated as “00” in the default SONET mode (**DX_SDH_PG_[i]**=0) or “10” in the alternate SDH mode (**DX_SDH_PG_[i]**=1).

4.6.4.3 FIFO Overflow or Underflow

If a FIFO overflows or underflows, the **DX_PG_FIFO_x_E** event bit is set.

See User Note 14.1.5.1 for important information.

4.6.4.4 PAIS Generation

PAIS for tributary **x** is generated by setting the H-bytes and the entire SPE/VC for tributary **x** to all-ones.

If **DX_LOF** = 1, **DX_LAIS** = 1, (**DX_LOS** = 1 and **DX_LOS_INH** = 0), or (**DX_B2_ERR_SF** = 1 and **DX_SF_PAIS_INH** = 0), then PAIS is generated for all tributaries.

If **DX_PAIS_x** or **DX_LOP_x** is active, the Missouri inserts PAIS for tributary **x**. If **DX_FAST_AIS_x** = 1 and the last frame received for tributary **x** contained all ones in its H-bytes. The Missouri immediately inserts all-ones into the outgoing H-bytes (the rest of the SPE/VC is not changed) and does not wait for **DX_PAIS_x** to become active.

The user may force PAIS generation for tributary **x** by setting **DX_PAIS_GEN_x** = 1.

4.6.4.5 Unequipped Generation

The Pointer Generators can also insert Unequipped. If **DX_PAIS_GEN_x** = 0, and **DX_UNEQ_GEN_x** = 1, the entire SPE/VC is generated with all-zeros. The pointer value used for unequipped insertion must be a valid pointer value; the specific value is not specified. An NDF does not need to be generated when the unequipped signal insertion is removed (**DX_UNEQ_GEN_x** is cleared).

4.6.4.6 Justification Counters

The Pointer Processors contain 5-bit pointer generator justification counters that count every positive or negative justification. When the performance-monitoring counters are latched, the positive and negative justification counts are latched into the **DX_PG_POSCNT_x_[4:0]** and **DX_PG_NEGCNT_x_[4:0]** registers, respectively, and then the justification counters are cleared (see section 2.3).

If for tributary **x**, there has been at least one positive or negative justification in the previous second, the **DX_PG_POSCNT_SECE_x** or **DX_PG_NEGCNT_SECE_x** bit, respectively, is set.

4.7 DX Prot Interface

4.7.1 DX PROT Interface Description

The Missouri's DX Protection interface consists of a standard STS-48/STM-16 multiplexed data stream (regardless of the original signal combination on the low-speed interface) as a 16-bit wide parallel bus with an accompanying clock at 155.52 MHz.

The Missouri outputs *DX_PROT_SYNC_OUT* and *DX_PROT_CLK_OUT* signals with the Protection *DX_PROT_DATA_OUT_[16:1]* data stream. The 0 to 1 transition of *DX_PROT_SYNC_OUT* indicates that the first A1 byte is on bits 16:9 of the *DX_PROT_DATA_OUT_[16:1]* data bus. **See User Note 14.1.2.1 for important information.**

An external framer must supply the Missouri with a start of frame indication, *DX_PROT_SYNC_IN* and a clock signal *DX_PROT_CLK_IN* along with the Protection D*X_PROT_DATA_IN_[16:1]* data stream. A 0 to 1 transition on the *DX_PROT_SYNC_IN* signal should indicate that the first A1 byte is on bits 16:9 of the *DX_PROT_DATA_IN_[16:9]* data bus.

The DX Protection interface also provides an odd parity check bit, which is received and transmitted on signals *DX_PROT_PRTY_IN* and *DX_PROT_PRTY_OUT*. Parity is performed across all 16 bits of the data, as well as the frame sync indication, in each direction. If a parity error occurs, the **DX_APS_PROT_PRTY_E** register bit is set. For testing purposes, the outgoing parity is even if **DX_APS_PROT_PRTY_OUT** is set to 1.

4.8 Demux Selector/Cross-Connect Function

The STS-48 data from the DX Pointer Processor is output to a Demux selector/Cross-Connect function, which also receives STS-48 data from three other sources: *DX_PROT_DATA_IN_[16:1]*, *MX_DATA_IN/MX48_PDATA_IN* (after Pointer Processing by the Mux side Pointer Processor) and *MX_PROT_DATA_IN_[16:1]*. Any of these 4 input streams can be selected as the input to the SONET/SDH frame generation block on the Demultiplexer side via the **DMUXSEL_x_[7:0]** registers. Furthermore, the selector is based on a per-STS-1 basis, and includes a time-slot-interchanger, so that on a per output STS-1 time slot basis, any of the input STS-1s from any of the four

data streams may be selected. A multicast function is provided since it is permitted to select the same input for multiple output time-slots. Table 14 illustrates how this selection is made. **DMUXSEL_x_[7:0]** selects the source for output STS-1 **x**.

Table 14. Demux Selector/Cross-Connect Table

DMUXSEL_x_[7:0]	Data Selected
00_0000_00	**DX_DATA_IN** data: Tributary 1_1
00_0000_01	**DX_DATA_IN** data: Tributary 1_2
00_0000_1x	**DX_DATA_IN** data: Tributary 1_3
00_0001_[00:1x]	**DX_DATA_IN** data: Tributary 2_[1:3]
:	:
00_1111_[00:1x]	**DX_DATA_IN** data: Tributary 16_[1:3]
01_[0000:1111]_[00:1x]	**DX_PROT_DATA_IN** data: Tributary 1:16_[1:3]
10_[0000:1111]_[00:1x]	**MX_DATA_IN** (or *MX48_PDATA_IN*) data: Tributary 1:16_[1:3]
11_[0000:1111]_[00:1x]	**MX_PROT_DATA_IN** data: Tributary 1:16_[1:3]

4.8.1 DX Demux

The DX demux block demultiplexes the selected data streams, as appropriate, to provide the configured output signal format as determined by the **DX_LINE_CONFIG_[4:0]** register.

4.9 SONET/SDH Frame Generation (FRGEN3/12/48)

The SONET/SDH frame generation blocks on the Demultiplexer side create any valid combination of STS-48/STM-16, STS-12/STM-4, and STS-3/STM-1 outputs by generating the TOH/SOH bytes and scrambling (if enabled) all bytes of the SONET/SDH signal except for the first row of TOH/SOH bytes. If a quadrant contains a STS-12/STM-4 signal, only the first Frame Generation block of the quadrant is active and a single 622.08 MHz serial STS-12/STM-4 data stream is output on the corresponding *DX_DATA_OUT_[i]* channel. If a quadrant consists of four STS-3/STM-1 signals, all four Frame Generation blocks in that quadrant are active and four 155.52 MHz serial STS-3/STM-1 data streams are output on the appropriate *DX_DATA_OUT_[i]* channels.

The *DX_CLK_OUT_155* and *DX_CLK_OUT_155_622* signals are defined as follows:

DX_CLK_OUT_155_622 is either a 622.08 MHz or 155.52 MHz clock, depending upon SYS_CLK_IN. It should be used as the reference clock for all *DX_DATA_OUT_[i]* signals at 622.08 Mb/s.

DX_CLK_OUT_155 is always a 155.52 MHz clock, either via a divided down version of SYS_CLK_IN operating at 622.08 MHz (**CLK_155_MODE**=0) or via a 155.52 MHz *SYS_CLK_IN* (**CLK_155_MODE**=1). It should be used as the reference clock for all *DX_DATA_OUT_[i]* signals at 155.52 Mb/s.

If the interface comprises of a STS-48 signal, then *DX48_PDATA_OUT_[15:0]* contains a 16-bit parallel signal at 155.52 Mb/s with an accompanying clock *DX48_PCLK_OUT* at 155.52 MHz.

4.9.1 Frame Alignment

If **DX_FRAME_IN_INH** = 0, the Missouri's frame generators contain a frame counter that is synchronized to the sampled *SYS_SYNC_IN* signal (after the **SYS_SYNC_IN_RESYNC** bit was set).

If **DX_FRAME_IN_INH** = 1, the Missouri does not use the *SYS_SYNC_IN* input to synchronize its frame genera-

tors.

See User Note 14.1.7.1 for important information.

4.9.2 AIS Generation

Normal frame generation is suspended during transmission of a Line (Multiplex Section) Alarm Indication Signal (AIS-L) or Path AIS (AIS-P).

LAIS generation is controlled by the **DX_LAIS_GEN_[i]** registers. If **DX_LAIS_GEN_[i]** = 1, the first 3 rows of the TOH/SOH are generated normally, but the remainder of the TOH/SOH bytes and the SPE/VC bytes are transmitted as all-ones for output **i**.

4.9.3 TOH/SOH Generation

The following sections define the values generated for all TOH/SOH bytes when they are not overwritten with all-ones during AIS insertion. Where the byte names differ between SONET and SDH, the SONET name will be listed first. Table 15 shows the TOH/SOH bytes for a STS-12/STM-4. Table 16 shows the TOH/SOH bytes for a STS-3/STM-1. The TOH/SOH of a STS-3/STM-1 has all of the same types of bytes as the TOH/SOH of a STS-12/STM-4, however there are only 9 columns of TOH/SOH. Entries that are blank in Table 15 and Table 16 are SONET undefined or SDH non-standardized reserved bytes. The Missouri fills these bytes with all-zeros if they are not overwritten with all-ones during AIS.

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Table 15. STS-12/STM-4 TOH/SOH

	Column					
Row	1	2-12	13	14-24	25	26-36
1	A1[1]	A1[2:12]	A2[1]	A2[2:12]	J0[1]	Z0[2:12]
2	B1		E1		F1	
3	D1		D2		D3	
4	H1[1]	H1[2:12]	H2[1]	H2[2:12]	H3[1]	H3[2:12]
5	B2[1]	B2[2:12]	K1		K2	
6	D4		D5		D6	
7	D7		D8		D9	
8	D10		D11		D12	
9	S1	Z1[2:12][a]	Z2[1][a]	Z2[2][a], M1, Z2[4:12][a]	E2	

[a]The Z1 and Z2 bytes are non-standardized reserved bytes for STM-4.

.

Table 16. STS-3/STM-1 TOH/SOH

	Column					
Row	1	2-3	4	5-6	7	8-9
1	A1[1]	A1[2:3]	A2[1]	A2[2:3]	J0[1]	Z0[2:3]
2	B1		E1		F1	
3	D1		D2		D3	

Table 16. STS-3/STM-1 TOH/SOH

Row	Column 1	2-3	4	5-6	7	8-9
4	H1[1]	H1[2:3]	H2[1]	H2[2:3]	H3[1]	H3[2:3]
5	B2[1]	B2[2:3]	K1		K2	
6	D4		D5		D6	
7	D7		D8		D9	
8	D10		D11		D12	
9	S1	Z1[2:3][a]	Z2[1][a]	Z2[2][a], M1	E2	

[a]The Z1 and Z2 bytes are non-standardized reserved bytes for STM-1.

4.9.3.1 Frame Bytes (A1 and A2)

The frame bytes are normally generated with the fixed patterns:

- A1: 1111_0110 = F6
- A2: 0010_1000 = 28

For testing purposes, A1 and A2 can be generated with errors by setting 1 or more bits of **DX_A1A2_ERR_[i]**. If **DX_A1A2_ERR_[i]** = 0, no A1A2 errors are generated for output **i**. If **DX_A1A2_ERR_[i]** = 1, then **DX_A1A2_ERR_NUM_[i]_[2:0]** consecutive frames in each group of 8 frames is generated with A1 and A2 XORed with the contents of **DX_A1A2_ERR_PAT_[i]_[15:0]**. The MSB of A1 is XORed with **DX_A1A2_ERR_PAT_[i]_[15]**, and the LSB of A2 is XORed with **DX_A1A2_ERR_PAT_[i]_[0]**.

4.9.3.2 Section Trace/Regenerator Section Trace (J0) and Section Growth/Spare (Z0)

Section Trace. The generation of J0 bytes by the 16 Frame Generators on the Demultiplexer side are controlled by **DX_J0_[i]_[15:0]_[7:0]**. Over periods of 16 consecutive frames, Frame Generator **i** continuously transmits the 16-byte pattern contained in **DX_J0_[i]_[15:0]_[7:0]**. The bytes are transmitted in descending order starting with **DX_J0_[i]_[15]_[7:0]**.

The SDH G.707 standard states that a 16-byte section trace frame containing the Section Access Point Identifier (SAPI) defined in clause3/G.831 should be transmitted continuously in consecutive J0 bytes. Note that only the frame start marker byte should contain a 1 in its MSB, however the user is free to provision any value.

The Section Trace function is not currently defined for SONET. Unless a similar section trace is defined for SONET, all of the **DX_J0_[i]** bytes should be filled with “0000_0001” so that a decimal 1 is transmitted continuously in J0.

Section Growth/Spare. The Z0 bytes are transmitted in order as the binary equivalent of 2 to 48 for STS-48/STM-16 tributaries, 2 to 12 for STS-12/STM-4 tributaries, or 2 to 3 for STS-3/STM-1 tributaries, as determined by the setting of **DX_LINE_CONFIG_[4:0]**.

4.9.3.3 Section BIP-8 (B1)

For output **i**, the B1 Bit Interleaved Parity 8 (BIP-8) is transmitted as even parity (normal) if **DX_B1_INV_[i]** = 0. Otherwise, odd parity (incorrect) is generated. The BIP-8 is calculated over all bits of the previous frame after scrambling and placed into the B1 byte of the current frame before scrambling.

By definition of BIP-8, the first bit of B1 provides parity over the first bit of all bytes of the previous frame, the second bit of B1 provides parity over the second bit of all bytes of the previous frame, etc.

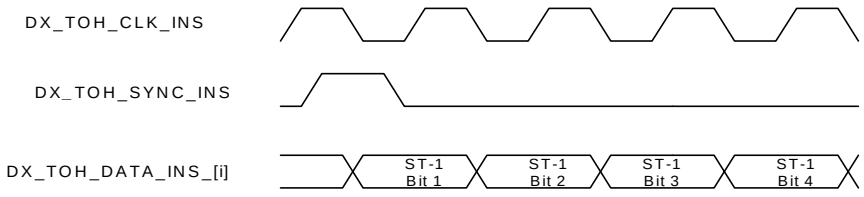
4.9.3.4 Serial TOH/SOH Insert Channel

The Missouri provides a serial channel for each of the sixteen possible line signals, through which the user can insert certain TOH/SOH bytes. The bytes that are accessible via this serial channel are (in order of transmission over the serial channel): E1, F1, D1-D3, K1, K2, D4-D12, E2. The E1 and E2 orderwire bytes are defined for the purpose of carrying two 64kb/s digitized voice signals. The F1 byte is available for use by the network provider. There are 2 DCCs defined in the TOH/SOH. The Section/Regenerator Section DCC uses the D1, D2, and D3 bytes to create a 192 kb/s channel. The Line/Multiplex Section DCC uses bytes D4 through D12 to create a 576 kb/s channel. The K1 and K2 bytes carry APS messages.

The transmit block for each demultiplexer line interface accepts a single serial input, *DX_TOH_DATA_INS_[i].* If a quadrant contains four STS-3 interfaces, then all four serial channels for that quadrant are active. If a quadrant contains a STS-12 interface, then only the first serial channel for that quadrant (*DX_TOH_DATA_INS_[i]* for *i = 1, 5, 9,* and *13*) is active. If the DX interface is configured for a single STS-48, then only the first channel (*DX_TOH_DATA_INS_[1]*) is active.

Each serial channel carries 27 bytes per frame, consisting of the 17 TOH bytes identified in the previous paragraph, plus 10 stuff bytes. A single 1728 kHz *DX_TOH_CLK_INS* clock is output from the Missouri in order to provide a timing reference for all active *DX_TOH_DATA_INS_[i]* inputs. The Missouri also provides a single *DX_TOH_SYNC_INS* signal as a byte delineation indication for the serial channels. The Missouri will interpret the bytes received on the sixteen serial channels in the following order (ST# indicates a stuff byte, which will be ignored by the Missouri) ST1, E1, F1, D1-D3, ST2, ST3, ST4, ST5, K1, K2, D4-D12, ST6, ST7, E2, ST8, ST9, ST10. All bytes are expected to be received in MSB to LSB order. The Missouri will interpret the bit received on *DX_TOH_DATA_INS_[i]* concurrent with the output of a falling-edge of *DX_TOH_SYNC_INS* as the first bit (the MSB) of the ST1 byte. The falling-edge of *DX_TOH_CLK_INS* should be used to clock-out *DX_TOH_DATA_INS_[i]* to the Missouri. The Missouri samples *DX_TOH_DATA_INS_[i]* on the rising-edge of *DX_TOH_CLK_INS.*

Note that *DX_TOH_CLK_INS* and *DX_TOH_SYNC_INS* are generated synchronously from an internal 77.76 MHz clock that is derived from *SYS_CLK_IN*.



In addition to this method of inserting the K1 and K2 bytes, the Missouri also can generate these same bytes internally as described in section 4.9.3.7.

4.9.3.5 Pointer Bytes (H1, H2) and Pointer Action Byte (H3)

Except in the case of AIS-L generation, the H1, H2, and H3 bytes are always passed unchanged through the Demultiplexer Frame Generator blocks.

4.9.3.6 Line/MS BIP-96 or BIP-24 (B2)

The B2 bytes for output **i** are transmitted as even parity (normal) if **DX_B2_INV_[i]** = 0. Otherwise, odd parity (incorrect) is generated. The B2 values are calculated over bytes in the previous frame before scrambling and

placed into the B2 bytes of the current frame before scrambling.

4.9.3.7 APS Channel and Line/MS AIS/RDI (K1 and K2)

The user can select the method of access for the K1K2 bytes via the **DX_K1K2_APS_[i]** and **DX_K2_3LSB_[i]** registers.

K1 and the 5 MSBs of K2 are used for automatic protection switching (APS) signaling. In the default **DX_K1K2_APS_[i]** = 0 state, the Frame Generator inserts **DX_K1GEN_[i]_[7:0]** in the transmitted K1 bytes and **DX_K2GEN_[i]_[7:3]** in the transmitted 5 MSBs of K2 bytes, for output **i**. If **DX_K1K2_APS_[i]** = 1, *DX_TOH_DATA_INS_[i]* is the source of K1 and the 5 MSBs of K2.

The 3 LSBs of K2 are used as an AIS or Remote Defect Indication (RDI) at the line/MS level, and in SONET, they are also used for APS signalling. In the default **DX_K2_3LSB_[i]** = 0 state, the 3 LSBs of K2 are inserted according to the following logic, in order of priority:

- If **DX_LAIS_GEN_[i]** = 1, they are transmitted as all-ones (as are all line/MS overhead bytes)
- else if **DX_LRDI_INH_[i]** = 0 and if ((**MX_LOS_[i]**=1 and not **MX_LOS_INH_[i]**=1) or **MX_LOF_[i]**=1**,** **MX_LOC_[i]** or **MX_LAIS_[i]**=1), they are transmitted as “110” for a minimum of 20 frames
- else **DX_K2GEN_[i]_[2:0]** is transmitted

If **DX_K2_3LSB_[i]** = 1, *DX_TOH_DATA_INS_[i]* is the source of the 3 LSBs of K2.

See User Note 14.1.4.1 for important information.

Requirements R6-180 through R6-182 of GR-253 specify that RDI should be inserted and removed within 125 µs of detection and removal of received LOS, LOF, or LAIS, provided the 20 frame minimum criterion has been met. If **DX_K2_3LSB_[i]** = 1, the user is responsible for meeting the detection/removal timing and the 20 frame minimum via his/her external generation of this data. The Missouri provides a transparent pass-through of this data in this mode of operation.

4.9.3.8 Synchronization Status (S1)

The 4 LSBs of this byte convey synchronization status messages. The transmitted S1 byte for output **i** is set to **DX_S1GEN_[i]_[7:0]**.

4.9.3.9 Line/MS REI (M1)

The Multiplex Side monitors B2 bit errors in its received signals. The numbers of B2 errors detected each frame are placed in the Demultiplexer’s transmitted M1 bytes (see section 3.4.3).

The user can force the transmission of REI error indications for output **i** by setting **DX_M1GEN_ERR_[i]** = 1. This causes the binary equivalent of 96 for STS-12/STM-4 tributaries or 24 for STS-3/STM-1 tributaries to be transmitted in the M1 byte. Else if **DX_LREI_INH_[i]** = 0, the M1 byte is set equal to the most recent B2 error count. Otherwise, the M1 byte is set to all zeros.

4.9.3.10 Growth/Undefined (Z1 and Z2)

The use of the Z1 and Z2 bytes is not standardized. The Missouri fills these bytes with all-zeros.

4.9.4 Scrambling

The SONET/SDH signals are scrambled by the Frame Generators using the frame synchronous scrambling sequence generated from the polynomial $\mathbf{g(x) = x^7 + x^6 + 1}$. For testing purposes, one or more of the scramblers can be disabled by setting the appropriate **DX_SCRINH_[i]** to 1.

4.10 Demux I/O Disable and Clock Inversion

Demux side I/O may be disabled similarly to Mux side I/O (see section 3.12).

DX_IN_INH disables *DX_DATA_IN_[15:0]*, *DX_CLK_IN*, and *DX_FRAME_IN* (LVPECL). **DX_OUT_INH_[i]** inhibits *DX_DATA_OUT_[i]* (LVPECL) and **DX_CLK_OUT_INH_[1]** disables *DX_CLK_OUT_155_622* (LVPECL) and **DX_CLK_OUT_INH_[2]** disables *DX_CLK_OUT_155* (LVPECL). DX_OUT_INH_[16:1] should be all-ones to disable *DX48_PDATA_OUT* and its clock.

DX_PROT_OUT_INH inhibits *DX_PROT_DATA_OUT_[16:1], DX_PROT_SYNC_OUT, DX_PROT_PRTY_OUT* (LVCMOS), and *DX_PROT_CLK_OUT* (LVDS).

DX_PROT_IN_INH inhibits *DX_PROT_DATA_IN_[16:1], DX_PROT_SYNC_IN, DX_PROT_PRTY_IN* (LVCMOS), and *DX_PROT_CLK_IN* (LVDS).

All inhibits are active high, and default to 0 (all inputs and outputs enabled).

The DX side protection output clock defaults to the non-inverted sense (**DX_PROT_CLK_OUT_INV**=0). The DX side protection output clock can be inverted by changing the **DX_PROT_CLK_OUT_INV** bit. **See User Note 14.1.2.1 for important information.**

The DX side primary output clocks default to the inverted sense (**DX_CLK_OUT_INV_[1:2]** = ”11”). The DX side primary output clocks can be restored to non-inverted by changing the **DX_CLK_OUT_INV_[1:2]** bits (**DX_CLK_OUT_INV_[1:2]** = ”00”).

5.0 System Clock Generation and References

5.1 System Clock and Sync Inputs and Outputs

The *SYS_CLK_IN* input signal can be a 622.08 MHz clock used to time all of the Framer and Pointer Processor blocks within the Missouri, for STS-3/STM-1 or STS-12/STM-4 signals. If the Low Speed inputs are all STS-3/STM-1 signals (**MX_LINE_CONFIG_[4:0]**= 00000) the *SYS_CLK_IN* input signal can accept a 155.52 MHz clock. If the Low Speed input is a parallel STS-48/STM-16 signal (**MX_LINE_CONFIG_[4:0]**=1xxxx) the *SYS_CLK_IN* input signal requires a 155.52 MHz clock.

The Missouri also generates an *SYS_SYNC_OUT* signal. The timing of the *SYS_SYNC_OUT* signal is such that this output from a “master” Missouri device can be connected to the *SYS_SYNC_IN* inputs for other “slave” Missouri devices and will result in all MX (and DX) side outputs from all Missouri devices being frame-aligned.

There is the potential for timing ambiguities associated with the exact position of the *SYS_SYNC_IN* input as it is retimed to the Missouri’s internal clock. Therefore, the period of the rising edge of the *SYS_SYNC_IN* input may not be precisely 125 µs each and every period. The Missouri will not rely on the position of the *SYS_SYNC_IN* input on a frame by frame basis, but will instead ‘resync’ its frame generation circuitry to a single rising edge of *SYS_SYNC_IN* when instructed to by the user. This resynchronization to the *SYS_SYNC_IN* is armed when **SYS_SYNC_IN_RESYNC** is set to 1. Missouri will then resynchronize its internal frame position generator to the next rising edge of *SYS_SYNC_IN*. Missouri’s frame generator will flywheel on this frame position, regardless of the *SYS_SYNC_IN* signal, until instructed to resync again.

6.0 Microprocessor Interfaces

This section describes the Microprocessor interfaces to the Missouri. The Microprocessor interface enables the System to access all registers within Missouri. The Missouri supports 4 types of microprocessor interfaces. These interfaces are controlled by the *BUSMODE* and *SYNCMODE* signals. If *SYNCMODE* = 0, the microprocessor interface operates as the management interface defined in the ATM Utopia Level 2 specification, [2]. This interface is an asynchronous, 8-bit wide interface. If *SYNCMODE* = 1, the microprocessor interface operates as a synchronous, 16-bit interface. In synchronous or asynchronous mode, the microprocessor can be programmed to support either Motorola or Intel protocols, via *BUSMODE.* Note that a reference clock must be provided on signal *UPCLK* for both synchronous and asynchronous operation.

The Microprocessor interface is capable of operating in either an interrupt driven or a polled mode. In the interrupt mode, the Missouri is capable of supporting multiple Interrupt Sources. The Missouri is capable of masking out any of the interrupts in either mode.

6.1 Microprocessor Interface Signal Definition - Asynchronous Operation

SIGNAL	I/O	DESCRIPTION
RDB(DSB)	I	Read or data strobe. If *BUSMODE*=1, the active-low RDB input is LOW to enable read data from the addressed location on the data bus. If *BUSMODE*=0, the active-low DSB input is LOW to enable read data from the Missouri, or strobe write data into the Missouri.
D_[7:0]	I/O	Byte-wide bidirectional data bus. MSB is D_[7].
ADDR_[12:0]	I	Device address bus. MSB is ADDR_[12].
UPCLK	I	Microprocessor system clock.
CSN	I	Chip Select. Active-low enable signal used to validate the address bus for read and write transfers.
WRB(RWB)	I	Write, or read/write. If *BUSMODE*=1, the active-low WRB input is LOW to read data from the address location. The active-low WRB input is HIGH to write data from the data bus into the address location. If *BUSMODE*=0, the active-low WRB input is HIGH to read data from the address location. The active-low WRB input is LOW to write data from the data bus into the address location.
RDYB(DTACKB)	O	Ready or data acknowledge. Tri-state acknowledge signal low to end data transfers over the data bus. For either *BUSMODE* RDYB (DTACKB) is LOW to complete a transfer.
BUSMODE	I	Selects the mode of operation of the Microprocessor interface. *BUSMODE*=1 is for the Intel mode (RDB, WRB, RDYB) and *BUSMODE*=0 is for the Motorola mode (DSB, RWB, DTACKB).
SYNCMODE	I	Selects the mode of operation of the Microprocessor interface. *SYNCMODE*=1 is 16-bit, synchronous operation; *SYNCMODE*=0 is for the 8-bit asynchronous operation.
INTB	O	Interrupt. Level sensitive interrupt signal LOW by the Missouri. For either *BUSMODE*, INTB is an open-drain active-low output.
APS_INTB	O	APS Interrupt. Level sensitive interrupt signal LOW by the Missouri. For either *BUSMODE*, APS_INTB is an open-drain active-low output.
RSTB	I	Reset. Active low (level sensitive) input to reset the Missouri.

6.2 Microprocessor Interface Signal Definition - Synchronous Operation

SIGNAL	I/O	DESCRIPTION
D_[15:0]	I/O	Byte wide bidirectional data bus. MSB is D_[15].

SIGNAL	I/O	DESCRIPTION
ADDR_[12:1]	I	Device address bus; MSB is ADDR_[12].
UPCLK	I	Microprocessor system clock.
CSN	I	Chip Select. Active low enable signal used to validate the address bus for read and write transfers.
WRB(RWB)	I	Write, or read/write. If *BUSMODE*=1, the active-low WRB input is LOW to read data from the address location. The active-low WRB input is HIGH to write data from the data bus into the address location. If *BUSMODE*=0, the active-low WRB input is HIGH to read data from the address location. The active-low WRB input is LOW to write data from the data bus into the address location.
RDYB(DTACKB)	O	Ready or data acknowledge. Tri-state acknowledge signal LOW to end data transfers over the data bus. For either busmode RDYB (DTACKB) is LOW to complete a transfer.
BUSMODE	I	Selects the mode of operation of the Microprocessor interface. *BUSMODE*=1 is for the Intel mode (WRB, RDYB) and *BUSMODE*=0 is for the Motorola mode (RWB, DTACKB).
INTB	O	Interrupt. Level sensitive interrupt signal LOW by the Missouri. For either *BUSMODE*, INTB is an open-drain active low output.
APS_INTB	O	APS interrupt. Level sensitive interrupt signal LOW by the Missouri. For either Busmode, INTB is an open-drain active low output.
RSTB	I	Reset. Active-low (level sensitive) input to reset the Missouri.

7.0 Management Interface

This section describes the Management interface to the Missouri and defines the address of all registers that are available for reading or writing by an external microprocessor.

The MSB of the microprocessor bus address, *ADDR_[12]*, designates whether the map is associated with the Multiplexer (*ADDR_[12]* = 0) or Demultiplexer (*ADDR_[12]* = 1) direction. *ADDR_[11:0]* indicates the address of the specific 8-bit register to be accessed.

For 8-bit operations, all twelve address bits, *ADDR_[11:0],* must be used.

For 16-bit operations, only eleven address bits, *ADDR_[11:1]*, are used. The single 16-bit word that corresponds to *ADDR_[11:1]* is accessed in a single cycle. The 16-bit data transfer is two 8-bit transfers to/from **ADDR_[XXXXXXXXXXX1]** and **ADDR_[XXXXXXXXXXX0]**, the high-byte and low-byte, respectively. Bit 7 of the high-byte is the MSB and bit 0 of the low-byte is the LSB of this 16-bit data transfer.

To facilitate accessing specific tributaries within these maps, the following addressing convention is utilized whenever possible: within a particular map, Tributary [1] registers begin in address 0xXY00, Tributary [2] registers begin in address 0xXY10, etc. When referencing register addresses in the following text, the convention “0xXXXX **-** 0xYYYY” or “0xXXXX through 0xYYYY” enumerates all consecutive registers within the specified range.

7.1 Interrupt or Polled Operation

The Management interface can be operated in either an interrupt driven or a polled mode. In both modes, the Missouri register bits **MX_SUM_INT** in address 0x0004 and **DX_SUM_INT** in address 0x1002 can be used to determine whether or not changes have occurred in the state of monitoring registers in the Missouri.

7.1.1 Interrupt Sources

7.1.1.1 Multiplexer Side

The Multiplexer Side register map includes summary status bits for the multiplexer side in registers 0x0003 to 0x0009, and GPIO monitors. If any of these indications are active, the **MX_SUM_INT** bit in register 0x0002 will be high (logic 1). If **MX_SUM_INT_MASK** = 0, the interrupt output for the microprocessor interface, *INTB,* 0x0004, becomes active (logic 0).

7.1.1.2 Demultiplexer Side

The summary status bits for the Demultiplexer Side are in registers 0x1004-9. These bits contribute to the **DX_SUM_INT** bit in register 0x1002 If any of the summary status bits is “1” and the corresponding mask bit is “0”, then the **DX_SUM_INT** bit will be set to “1.”

The summary status bits in registers 0x1003-9 are “1” if 1 or more of the corresponding group of bits is “1”. Individual TOH/SOH delta and second event bits can be masked (Table 42, addresses 0x1204-0x1206).

7.1.2 Interrupt Driven

In an interrupt driven mode, the **MX_SUM_INT_MASK** bit in register 0x000D and the **DX_SUM_INT_MASK** bit in register 0x100C should be cleared (to logic 0). This allows the *INTB* output to become active (logic 0). This output is

INTB = !((!**MX_SUM_INT_MASK** && **MX_SUM_INT) OR** (!**DX_SUM_INT_MASK** && **DX_SUM_INT**))

In addition, the **DX_APS_INT_MASK** and **MX_APS_INT_MASK_[i]** bits of the should be cleared (to logic 0). This allows the *APS_INTB* output to become active (logic 0). This output is

APS_INTB = !((!**DX_APS_INT_MASK** && **DX_APS_INT**) OR (!**MX_APS_INT_MASK_[1]** && **MX_APS_INT_[1]**))

See User Note 14.1.2.2 for important information.

If an interrupt occurs, the microprocessor can first read the summary status registers to determine the class(es) of interrupt source(s) that is active, and then read the specific registers in that class(es) to determine the exact cause of the interrupt.

7.1.3 Polled mode

The **MX_SUM_INT_MASK, DX_SUM_INT_MASK, MX_APS_INT_MASK_[i]** and **DX_APS_INT_MASK** bits should be set (to logic 1), to suppress all hardware interrupts and operate in a polled mode. In this mode, the Missouri outputs *INTB* and *APS_INTB* are held in the inactive (logic 1) state.

Note that the **MX_SUM_INT_MASK, DX_SUM_INT_MASK, MX_APS_INT_MASK_[i], DX_APS_INT_MASK** bits do not affect the state of the register bits **MX_SUM_INT, DX_SUM_INT, MX_APS_INT** and **DX_APS_INT**. These bits can be polled to determine if further register interrogation is needed.

8.0 Pin Assignments and Descriptions

Figure 3. Missouri Pin Assignments

(S4802)

624 CBGA
(VIEWED FROM TOP)

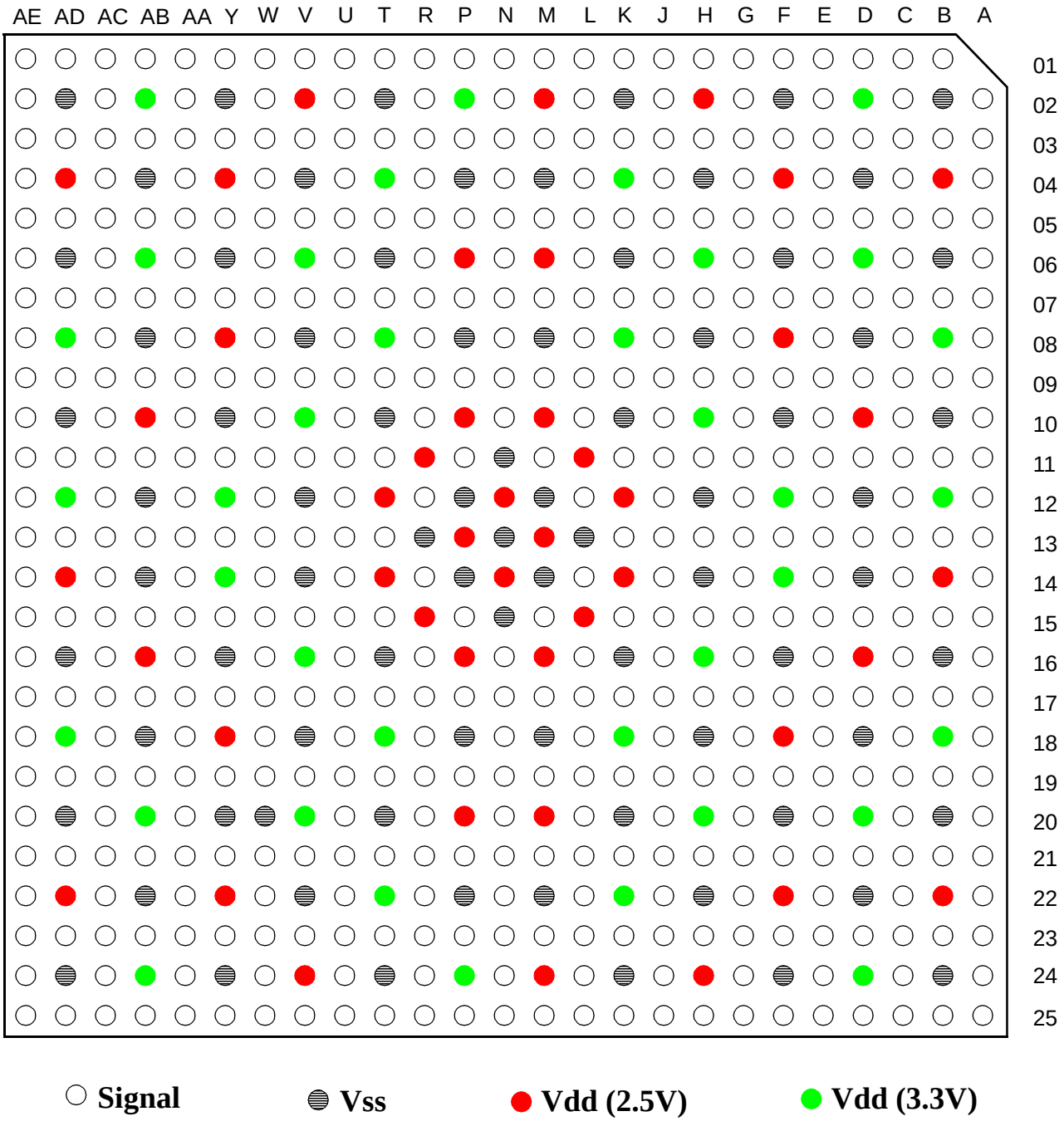


Table 17. Low-Speed SONET Interface

Signal Name STS-48/STM-16 Mode	Signal Name STS-12/STM-4 Mode	Signal Name STS-3/STM-1 Mode	Pin	Signal Type	Signal Description
DX48_PDATA_OUT[15]-	DX_DATA_OUT[1]-	DX_DATA_OUT[1]-	W22	LVPECL Output	**STS-3/STM-1 Mode:** Serial Demultiplexer output data when Missouri's Demultiplexer side is configured for STS-3/STM-1 signals.
DX48_PDATA_OUT[15]+	DX_DATA_OUT[1]+	DX_DATA_OUT[1]+	V21		
DX48_PDATA_OUT[11]-		DX_DATA_OUT[2]-	L24		
DX48_PDATA_OUT[11]+		DX_DATA_OUT[2]+	L23		
DX48_PDATA_OUT[10]-		DX_DATA_OUT[3]-	K23		
DX48_PDATA_OUT[10]-		DX_DATA_OUT[3]+	L21		
DX48_PDATA_OUT[9]-		DX_DATA_OUT[4]-	H25		
DX48_PDATA_OUT[9]+		DX_DATA_OUT[4]+	J23		
DX48_PDATA_OUT[14]-	DX_DATA_OUT[5]-	DX_DATA_OUT[5]-	T21	LVPECL Output	**Mixed STS-3/STM-1 and STS-12/STM-4 Mode:** Serial Demultiplexer output data when Missouri's Demultiplexer side is configured for STS-12/STM-4 and STS-3/STM-1 signals.
DX48_PDATA_OUT[14]-	DX_DATA_OUT[5]+	DX_DATA_OUT[5]+	U22		
DX48_PDATA_OUT[8]-		DX_DATA_OUT[6]-	D25		
DX48_PDATA_OUT[8]+		DX_DATA_OUT[6]+	E22		
DX48_PDATA_OUT[7]-		DX_DATA_OUT[7]-	B21		
DX48_PDATA_OUT[7]+		DX_DATA_OUT[7]+	A22		
DX48_PDATA_OUT[6]-		DX_DATA_OUT[8]-	D19		
DX48_PDATA_OUT[6+]		DX_DATA_OUT[8]+	E18		
DX48_PDATA_OUT[13]-	DX_DATA_OUT[9]-	DX_DATA_OUT[9]-	T23	LVPECL Output	**STS-12/STM-4 Mode:** Serial Demultiplexer output data on channels 1, 5, 9, & 13 when Missouri's Demultiplexer side is configured for STS-12/STM-4 signals.
DX48_PDATA_OUT[13]+	DX_DATA_OUT[9]+	DX_DATA_OUT[9]+	R25		
DX48_PDATA_OUT[5]-		DX_DATA_OUT[10]-	E16		
DX48_PDATA_OUT[5]+		DX_DATA_OUT[10]+	D17		
DX48_PDATA_OUT[4]-		DX_DATA_OUT[11]-	A14		
DX48_PDATA_OUT[4]+		DX_DATA_OUT[11]+	C14		
DX48_PDATA_OUT[3]-		DX_DATA_OUT[12]-	E13		
DX48_PDATA_OUT[3]+		DX_DATA_OUT[12]+	D13		

Table 17. Low-Speed SONET Interface

Signal Name STS-48/STM-16 Mode	Signal Name STS-12/STM-4 Mode	Signal Name STS-3/STM-1 Mode	Pin	Signal Type	Signal Description
DX48_PDATA_OUT[12]-	DX_DATA_OUT[13]-	DX_DATA_OUT[13]-	N24	LVPECL Output	**STS-48/STM-16 Mode:** Parallel Demultiplexer output data when Missouri's Demultiplexer side is configured for STS-48/STM-16 signals. DX48_PDATA_OUT[15] is the MSB.
DX48_PDATA_OUT[12]+	DX_DATA_OUT[13]+	DX_DATA_OUT[13]+	N22		
DX48_PDATA_OUT[2]-		DX_DATA_OUT[14]-	A11		
DX48_PDATA_OUT[2]+		DX_DATA_OUT[14]+	A10		
DX48_PDATA_OUT[1]-		DX_DATA_OUT[15]-	B9		
DX48_PDATA_OUT[1]+		DX_DATA_OUT[15]+	A9		
DX48_PDATA_OUT[0]-		DX_DATA_OUT[16]-	D5		
DX48_PDATA_OUT[0]+		DX_DATA_OUT[16]+	E7		
	MX_DATA_IN[1]-	MX_DATA_IN[1]-	U18	LVPECL Input	**STS-3/STM-1 Mode:** Serial Multiplexer input data when Missouri's Multiplexer side is configured for STS-3/STM-1 signals.
	MX_DATA_IN[1]+	MX_DATA_IN[1]+	W21		
		MX_DATA_IN[2]-	N23		
		MX_DATA_IN[2]+	N25		
MX48_PDATA_IN[14]-		MX_DATA_IN[3]-	L25		
MX48_PDATA_IN[14]+		MX_DATA_IN[3]+	K25		
MX48_PDATA_IN[12]-		MX_DATA_IN[4]-	G24		
MX48_PDATA_IN[12]+		MX_DATA_IN[4]+	F25		
	MX_DATA_IN[5]-	MX_DATA_IN[5]-	R17	LVPECL Input	**Mixed STS-3/STM-1 & STS-12/STM-4 Mode:** Serial Multiplexer input data when Missouri's Multiplexer side is configured for STS-12/STM-4 and STS-3/STM-1 signals.
	MX_DATA_IN[5]+	MX_DATA_IN[5]+	T19		
MX48_PDATA_IN[10]-		MX_DATA_IN[6]-	A24		
MX48_PDATA_IN[10]+		MX_DATA_IN[6]+	B23		
MX48_PDATA_IN[8]-		MX_DATA_IN[7]-	G21		
MX48_PDATA_IN[8]+		MX_DATA_IN[7]+	G20		
MX48_PDATA_IN[6]-		MX_DATA_IN[8]-	A18		
MX48_PDATA_IN[6]+		MX_DATA_IN[8]+	C18		

Table 17. Low-Speed SONET Interface

Signal Name STS-48/STM-16 Mode	Signal Name STS-12/STM-4 Mode	Signal Name STS-3/STM-1 Mode	Pin	Signal Type	Signal Description
	MX_DATA_IN[9]-	MX_DATA_IN[9]-	R21	LVPECL Input	**STS-12/STM-4 Mode:** Serial Multiplexer input data on channels 1,5, 9, & 13 when Missouri's Multiplexer side is configured for STS-12/STM-4 signals.
	MX_DATA_IN[9]+	MX_DATA_IN[9]+	P25		
MX48_PDATA_IN[4]-		MX_DATA_IN[10]-	H17		
MX48_PDATA_IN[4]+		MX_DATA_IN[10]+	E19		
MX48_PDATA_IN[2]-		MX_DATA_IN[11]-	D15		
MX48_PDATA_IN[2]+		MX_DATA_IN[11]+	C15		
MX48_PDATA_IN[0]-		MX_DATA_IN[12]-	A13		
MX48_PDATA_IN[0]+		MX_DATA_IN[12]+	B13		
	MX_DATA_IN[13]-	MX_DATA_IN[13]-	N21	LVPECL Input	**STS-48/STM-16 Mode:** Parallel Multiplexer input data when Missouri's Multiplexer side is configured for STS-48/STM-16 signals. MX48_PDATA_IN[15] is the MSB.
	MX_DATA_IN[13]+	MX_DATA_IN[13]+	N20		
		MX_DATA_IN[14]-	B11		
		MX_DATA_IN[14]+	C11		
		MX_DATA_IN[15]-	A8		
		MX_DATA_IN[15]+	C9		
		MX_DATA_IN[16]-	B7		
		MX_DATA_IN[16]+	A6		
	MX_CLK_IN[1]-	MX_CLK_IN[1]-	U21	LVPECL Input	**STS-3/STM-1 Mode:** 155.52 MHz clocks for the associated STS-3/STM-1 MX_DATA_IN serial data.
	MX_CLK_IN[1]+	MX_CLK_IN[1]+	U20		
MX48_PCLK_IN-		MX_CLK_IN[2]-	L19		
MX48_PCLK_IN+		MX_CLK_IN[2]+	L18		
MX48_PDATA_IN[15]-		MX_CLK_IN[3]-	J24		
MX48_PDATA_IN[15]+		MX_CLK_IN[3]+	J25		
MX48_PDATA_IN[13]-		MX_CLK_IN[4]-	F23		
MX48_PDATA_IN[13]+		MX_CLK_IN[4]+	E24		

Table 17. Low-Speed SONET Interface

Signal Name STS-48/STM-16 Mode	Signal Name STS-12/STM-4 Mode	Signal Name STS-3/STM-1 Mode	Pin	Signal Type	Signal Description
	MX_CLK_IN[5]-	MX_CLK_IN[5]-	R22	LVPECL Input	**Mixed STS-3/STM-1 & STS-12/STM-4 Mode:** 622.08 MHz clocks for the associated STS-12/STM-4 and STS-3/STM-1 MX_DATA_IN serial data.
	MX_CLK_IN[5]+	MX_CLK_IN[5]+	R23		
MX48_PDATA_IN[11]-		MX_CLK_IN[6]-	F21		
MX48_PDATA_IN[11]+		MX_CLK_IN[6]+	C24		
MX48_PDATA_IN[9]-		MX_CLK_IN[7]-	J20		
MX48_PDATA_IN[9]+		MX_CLK_IN[7]+	J19		
MX48_PDATA_IN[7]-		MX_CLK_IN[8]-	C20		
MX48_PDATA_IN[7]+		MX_CLK_IN[8]+	A20		
	MX_CLK_IN[9]-	MX_CLK_IN[9]-	P19	LVPECL Input	**STS-12/STM-4 Mode:** 622.08 MHz clocks for the associated STS-12/STM-4 MX_DATA_IN serial data.
	MX_CLK_IN[9]+	MX_CLK_IN[9]+	P21		
MX48_PDATA_IN[5]-		MX_CLK_IN[10]-	E17		
MX48_PDATA_IN[5]+		MX_CLK_IN[10]+	F17		
MX48_PDATA_IN[3]-		MX_CLK_IN[11]-	C16		
MX48_PDATA_IN[3]+		MX_CLK_IN[11]+	A15		
MX48_PDATA_IN[1]-		MX_CLK_IN[12]-	H13		
MX48_PDATA_IN[1]+		MX_CLK_IN[12]+	G13		
	MX_CLK_IN[13]-	MX_CLK_IN[13]-	N18	LVPECL Input	**STS-48/STM-16 Mode:** MX48_PCLK_IN is a single 155.52 MHz clock for the associated STS-48/STM-16 MX48_PDATA_IN parallel data.
	MX_CLK_IN[13]+	MX_CLK_IN[13]+	N19		
		MX_CLK_IN[14]-	C12		
		MX_CLK_IN[14]+	A12		
		MX_CLK_IN[15]-	E8		
		MX_CLK_IN[15]+	F9		
		MX_CLK_IN[16]-	C6		
		MX_CLK_IN[16]+	B5		
DX_CLK_OUT_155_622-	DX_CLK_OUT_155_622-	DX_CLK_OUT_155_622-	W19	LVPECL Output	DX_CLK_OUT_155_622 is either a 155.52 or 622.08 MHz clock. **CLK_155_MODE=0:** DX_CLK_OUT_155_622 is a 622.08 MHz clock. **CLK_155_MODE=1:** DX_CLK_OUT_155_622 is a 155.52 MHz clock.
DX_CLK_OUT_155_622+	DX_CLK_OUT_155_622+	DX_CLK_OUT_155_622+	Y21		

Table 17. Low-Speed SONET Interface

Signal Name STS-48/STM-16 Mode	Signal Name STS-12/STM-4 Mode	Signal Name STS-3/STM-1 Mode	Pin	Signal Type	Signal Description
DX48_PCLK_OUT-	DX_CLK_OUT_155-	DX_CLK_OUT_155-	M23	LVPECL Output	DX_CLK_OUT_155 (DX48_PCLK_OUT) is always a 155.52 MHz clock. **CLK_155_MODE=0:** DX_CLK_OUT (DX48_PCLK_OUT) is divided down from a 622.08 MHz SYS_CLK_IN. **CLK_155_MODE=1:** DX_CLK_OUT (DX48_PCLK_OUT) and SYS_CLK_IN are both 155.52 MHz.
DX48_PCLK_OUT+	DX_CLK_OUT_155+	DX_CLK_OUT_155+	L22		
SYS_CLK_IN-			V25	LVPECL Input	SYS_CLK_IN is a clock signal used by the Pointer Processor to synchronize data on both the Mux and Demux sides of the Missouri. **STS-3/STM-1 Mode:** 155.52 MHz **Mixed STS-3/STM-1 & STS-12/STM-4 Mode:** 622.08 MHz **STS-12/STM-4 Mode:** 622.08 Mhz **STS-48/STM-16 Mode:** 155.52 Mhz
SYS_CLK_IN+			V23		
SYS_SYNC_IN			Y23	LVTTL (65 Ohm, Internal pull-up)	SYS_SYNC_IN is used to align frames from multiple Missouris so that they can be multiplexed into a STS-192/STM-64.

Table 17. Low-Speed SONET Interface

Signal Name STS-48/STM-16 Mode	Signal Name STS-12/STM-4 Mode	Signal Name STS-3/STM-1 Mode	Pin	Signal Type	Signal Description
SYS_SYNC_OUT			Y25	LVTTL (50 Ohm)	SYS_SYNC_OUT is a Frame Sync Output signal that feeds other Missouris SYS_SYNC_IN inputs. SYS_SYNC_OUT is pulsed high once every 77760 cycles when SYS_CLK_IN is 622.08 Mhz or 19440 cycles when SYS_CLK_IN is 155.52 MHz.

Table 18. High-Speed SONET Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
DX_DATA_IN[15]- DX_DATA_IN[15]+ DX_DATA_IN[14]- DX_DATA_IN[14]+ DX_DATA_IN[13]- DX_DATA_IN[13]+ DX_DATA_IN[12]- DX_DATA_IN[12]+ DX_DATA_IN[11]- DX_DATA_IN[11]+ DX_DATA_IN[10]- DX_DATA_IN[10]+ DX_DATA_IN[9]- DX_DATA_IN[9]+ DX_DATA_IN[8]- DX_DATA_IN[8]+ DX_DATA_IN[7]- DX_DATA_IN[7]+ DX_DATA_IN[6]- DX_DATA_IN[6]+ DX_DATA_IN[5]- DX_DATA_IN[5]+ DX_DATA_IN[4]- DX_DATA_IN[4]+ DX_DATA_IN[3]- DX_DATA_IN[3]+ DX_DATA_IN[2]- DX_DATA_IN[2]+ DX_DATA_IN[1]- DX_DATA_IN[1]+ DX_DATA_IN[0]- DX_DATA_IN[0]+	AD05 AE04 AC06 AE06 Y07 U09 AB07 AA08 AC08 AD07 AA09 Y09 AA10 AB09 AC10 AE11 AE12 AE10 AB11 AC11 U11 W10 AA11 AC12 W12 AA12 AB13 AE13 V13 Y13 AA13 W13	I	LVPECL	**DX_DATA_IN[N]:** Two byte-wide data input stream for Demultiplexer STS-48/STM-16 input data. DX_DATA_IN[15] is the MSB.
DX_CLK_IN- DX_CLK_IN+	AC14 AE14	I	LVPECL	**DEMUX CLOCK INPUT:** Demultiplexer 155.52 MHz clock.
DX_FRAME_IN- DX_FRAME_IN+	AD13 AC13	I	LVPECL	**DEMUX FRAME INDICATOR:** Frame position indication signal is active high and indicates the SONET frame position on the DX_DATA_IN[15:0] bus.

Table 18. High-Speed SONET Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
MX_DATA_OUT[15]- MX_DATA_OUT[15]+ MX_DATA_OUT[14]- MX_DATA_OUT[14]+ MX_DATA_OUT[13]- MX_DATA_OUT[13]+ MX_DATA_OUT[12]- MX_DATA_OUT[12]+ MX_DATA_OUT[11]- MX_DATA_OUT[11]+ MX_DATA_OUT[10]- MX_DATA_OUT[10]+ MX_DATA_OUT[9]- MX_DATA_OUT[9]+ MX_DATA_OUT[8]- MX_DATA_OUT[8]+ MX_DATA_OUT[7]- MX_DATA_OUT[7]+ MX_DATA_OUT[6]- MX_DATA_OUT[6]+ MX_DATA_OUT[5]- MX_DATA_OUT[5]+ MX_DATA_OUT[4]- MX_DATA_OUT[4]+ MX_DATA_OUT[3]- MX_DATA_OUT[3]+ MX_DATA_OUT[2]- MX_DATA_OUT[2]+ MX_DATA_OUT[1]- MX_DATA_OUT[1]+ MX_DATA_OUT[0]- MX_DATA_OUT[0]+	W15 AA16 AC16 AA15 AD15 AC15 AE15 AE16 AD17 AE17 AE18 AC17 AA18 Y17 AC19 AE19 AD19 AE20 AC20 AA19 AC21 AE21 AB21 AD23 AA21 AB23 AC24 AA22 AE24 AE22 AC23 AE23	I	LVPECL	**MUX_ DATA_OUT:** Two byte-wide data output stream for multiplexer STS-48/STM-16 data. MX_DATA_OUT[15] is the MSB.
MX_CLK_OUT- MX_CLK_OUT+	W17 AB19	O	LVPECL	**MUX CLOCK OUT:** MX_CLK_OUT is the 155.52 MHz transmit clock to the line side. It provides timing for the transmit data bus and frame-position indication outputs.

Table 19. Mux Protection Switching Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
MX_PROT_DATA_IN[1]	U02	I	LVCMOS (65 Ohm, Internal pull-down)	**MX_ PROT_DATA_IN[N]:** Two byte-wide data input stream for multiplexer APS PROT interface. MX_PROT_DATA_IN[16] is the MSB.
MX_PROT_DATA_IN[2]	U04	I		
MX_PROT_DATA_IN[3]	W02	I		
MX_PROT_DATA_IN[4]	U08	I		
MX_PROT_DATA_IN[5]	T03	I		
MX_PROT_DATA_IN[6]	T07	I		
MX_PROT_DATA_IN[7]	R02	I		
MX_PROT_DATA_IN[8]	R04	I		
MX_PROT_DATA_IN[9]	R06	I		
MX_PROT_DATA_IN[10]	R08	I		
MX_PROT_DATA_IN[11]	P03	I		
MX_PROT_DATA_IN[12]	P07	I		
MX_PROT_DATA_IN[13]	N02	I		
MX_PROT_DATA_IN[14]	N04	I		
MX_PROT_DATA_IN[15]	M11	I		
MX_PROT_DATA_IN[16]	N08	I		

Table 19. Mux Protection Switching Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
MX_PROT_DATA_OUT[1]	U01	O	LVCMOS (35 Ohm)	**MX_ PROT_DATA_OUT[N]:** Two byte-wide data output stream for multiplexer APS PROT interface. MX_PROT_DATA_OUT[16] is the MSB.
MX_PROT_DATA_OUT[2]	U03	O		
MX_PROT_DATA_OUT[3]	AA02	O		
MX_PROT_DATA_OUT[4]	U07	O		
MX_PROT_DATA_OUT[5]	T01	O		
MX_PROT_DATA_OUT[6]	T05	O		
MX_PROT_DATA_OUT[7]	R01	O		
MX_PROT_DATA_OUT[8]	R03	O		
MX_PROT_DATA_OUT[9]	R05	O		
MX_PROT_DATA_OUT[10]	R07	O		
MX_PROT_DATA_OUT[11]	P01	O		
MX_PROT_DATA_OUT[12]	P05	O		
MX_PROT_DATA_OUT[13]	N01	O		
MX_PROT_DATA_OUT[14]	N03	O		
MX_PROT_DATA_OUT[15]	N05	O		
MX_PROT_DATA_OUT[16]	N07	O		
MX_PROT_CLK_OUT- MX_PROT_CLK_OUT+	U06 U05	O	LVDS	**MUX Protection Clock OUT:** MX_PROT_CLK_OUT is a 155.52 MHz clock signal (non-inverted by default) for APS PROT OUT Data and SYNC signals.
MX_PROT_CLK_IN- MX_PROT_CLK_IN+	V03 V01	I	LVDS	**MUX Protection Clock IN:** MX_PROT_CLK_IN is a 155.52 MHz clock signal for APS PROT IN Data and SYNC signals.
MX_PROT_SYNC_OUT	V05	O	LVCMOS (35 Ohm)	**MUX Protection SYNC Out:** MX_PROT_SYNC_OUT is a byte delineation signal for the APS PROT OUT interface. The 0 to 1 transition of this signal indicates that the first A1 byte is on bits 16:9 of the MX_PROT_DATA_OUT bus.
MX_PROT_SYNC_IN	V07	I	LVCMOS (65 Ohm, Internal pull-down)	**MUX Protection SYNC IN:** MX_PROT_SYNC_IN is a byte delineation signal for the APS PROT IN interface. The 0 to 1 transition of this signal indicates that the first A1 byte is on bits 16:9 of the MX_PROT_DATA_IN bus.

Table 19. Mux Protection Switching Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
MX_PROT_PRTY_OUT	T09	O	LVCMOS (35 Ohm)	**MUX Protection Parity Out:** MX_PROT_PRTY_OUT is an output that provides a parity bit (odd by default) for the MX APS Protection OUT interface.
MX_PROT_PRTY_IN	N09	I	LVCMOS (65 Ohm, Internal pull-down)	**MUX Protection Parity IN:** MX_PROT_PRTY_IN is an input used to perform a parity check (odd by default) across the MX APS Protection IN interface.
RX_REF_CLK_OUT	R09	O	LVCMOS (65 Ohm)	**Reference Clock Output:** RX_REF_CLK_OUT provides a reference clock signal output that can be generated via other input clock sources to the Missouri.

Table 20. Demux Protection Switching Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
DX_PROT_DATA_IN[1]	L02	I	LVCMOS (65 Ohm, Internal pull-down)	**DX_ PROT_DATA_IN[N]:** Two byte-wide data input stream for Demux APS PROT interface. DX_PROT_DATA_IN[16] is the MSB.
DX_PROT_DATA_IN[2]	L04	I		
DX_PROT_DATA_IN[3]	L06	I		
DX_PROT_DATA_IN[4]	L08	I		
DX_PROT_DATA_IN[5]	K03	I		
DX_PROT_DATA_IN[6]	K07	I		
DX_PROT_DATA_IN[7]	J02	I		
DX_PROT_DATA_IN[8]	J04	I		
DX_PROT_DATA_IN[9]	J06	I		
DX_PROT_DATA_IN[10]	J08	I		
DX_PROT_DATA_IN[11]	H03	I		
DX_PROT_DATA_IN[12]	H07	I		
DX_PROT_DATA_IN[13]	G02	I		
DX_PROT_DATA_IN[14]	G04	I		
DX_PROT_DATA_IN[15]	G06	I		
DX_PROT_DATA_IN[16]	G08	I		

Table 20. Demux Protection Switching Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
DX_PROT_DATA_OUT[1]	L01	O	LVCMOS (35 Ohm)	**DX_ PROT_DATA_OUT[N]:** Two byte-wide data output stream for Demux APS PROT interface. DX_PROT_DATA_OUT[16] is the MSB.
DX_PROT_DATA_OUT[2]	L03	O		
DX_PROT_DATA_OUT[3]	L05	O		
DX_PROT_DATA_OUT[4]	L07	O		
DX_PROT_DATA_OUT[5]	K01	O		
DX_PROT_DATA_OUT[6]	K05	O		
DX_PROT_DATA_OUT[7]	J01	O		
DX_PROT_DATA_OUT[8]	J03	O		
DX_PROT_DATA_OUT[9]	J05	O		
DX_PROT_DATA_OUT[10]	J07	O		
DX_PROT_DATA_OUT[11]	H01	O		
DX_PROT_DATA_OUT[12]	H05	O		
DX_PROT_DATA_OUT[13]	G01	O		
DX_PROT_DATA_OUT[14]	G03	O		
DX_PROT_DATA_OUT[15]	G05	O		
DX_PROT_DATA_OUT[16]	G07	O		
DX_PROT_CLK_OUT- DX_PROT_CLK_OUT+	M01 M03	O	LVDS	**DEMUX Protection Clock OUT:** DX_PROT_CLK_OUT is a 155.52 MHz clock signal (non-inverted by default) for APS PROT OUT Data and SYNC signals.
DX_PROT_CLK_IN- DX_PROT_CLK_IN+	N06 N10	I	LVDS	**DEMUX Protection Clock IN:** DX_PROT_CLK_IN is a 155.52 MHz clock signal for APS PROT IN Data and SYNC signals.
DX_PROT_SYNC_OUT	M05	O	LVCMOS (35 Ohm)	**DEMUX Protection SYNC Out:** DX_PROT_SYNC_OUT is a byte delineation signal for the APS PROT OUT interface. The 0 to 1 transition of this signal indicates that the first A1 byte is on bits 16:9 of the DX_PROT_DATA_OUT bus.
DX_PROT_SYNC_IN	M07	I	LVCMOS (65 Ohm, Internal pull-down)	**DEMUX Protection SYNC IN:** DX_PROT_SYNC_IN is a byte delineation signal for the APS PROT IN interface. The 0 to 1 transition of this signal indicates that the first A1 byte is on bits 16:9 of the DX_PROT_DATA_IN bus.

Table 20. Demux Protection Switching Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
DX_PROT_PRTY_OUT	M09	O	LVCMOS (35 Ohm)	**DEMUX Protection Parity Out:** DX_PROT_PRTY_OUT is an output that provides a parity bit (odd by default) for the DX APS Protection Out interface.
DX_PROT_PRTY_IN	L09	I	LVCMOS (65 Ohm, Internal pull-down)	**DEMUX Protection Parity IN:** DX_PROT_PRTY_IN is an input used to perform a parity check (odd by default) across the DX APS Protection IN interface.

Table 21. Drop/Insert Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
MX_TOH_DATA_OUT[1]	AB25	O	LVTTL (65 Ohm)	**MUX Transport Overhead DATA Output:** MX_TOH_DATA_OUT[i] is Multiplexer Serial TOH/SOH Output Data consisting of 17 bytes of TOH data plus 10 stuff bytes, ST#. Data ordering is as follows: ST1,E1,F1,D1-D3,ST2,ST3,ST4,ST5,K1,K2,D4-D12,ST6,ST7,E2,ST8,ST9,ST10. All bytes are expected to be received in MSB to LSB order.
MX_TOH_DATA_OUT[2]	AC22	O		
MX_TOH_DATA_OUT[3]	U25	O		
MX_TOH_DATA_OUT[4]	R20	O		
MX_TOH_DATA_OUT[5]	K21	O		
MX_TOH_DATA_OUT[6]	J22	O		
MX_TOH_DATA_OUT[7]	D23	O		
MX_TOH_DATA_OUT[8]	E20	O		
MX_TOH_DATA_OUT[9]	J17	O		
MX_TOH_DATA_OUT[10]	L16	O		
MX_TOH_DATA_OUT[11]	F15	O		
MX_TOH_DATA_OUT[12]	J15	O		
MX_TOH_DATA_OUT[13]	E10	O		
MX_TOH_DATA_OUT[14]	F07	O		
MX_TOH_DATA_OUT[15]	E05	O		
MX_TOH_DATA_OUT[16]	C04	O		

Table 21. Drop/Insert Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
MX_TOH_SYNC_OUT[1]	AC25	O	LVTTL (65 Ohm)	**MUX Transport Overhead SYNC OUT:** MX_TOH_SYNC_OUT[i] are byte delineation signals for the MX_TOH_DATA_OUT[i] TOH/SOH output signals.
MX_TOH_SYNC_OUT[2]	W24	O		
MX_TOH_SYNC_OUT[3]	U17	O		
MX_TOH_SYNC_OUT[4]	R24	O		
MX_TOH_SYNC_OUT[5]	J18	O		
MX_TOH_SYNC_OUT[6]	H19	O		
MX_TOH_SYNC_OUT[7]	C23	O		
MX_TOH_SYNC_OUT[8]	C22	O		
MX_TOH_SYNC_OUT[9]	L17	O		
MX_TOH_SYNC_OUT[10]	A16	O		
MX_TOH_SYNC_OUT[11]	G15	O		
MX_TOH_SYNC_OUT[12]	J14	O		
MX_TOH_SYNC_OUT[13]	E09	O		
MX_TOH_SYNC_OUT[14]	C07	O		
MX_TOH_SYNC_OUT[15]	A07	O		
MX_TOH_SYNC_OUT[16]	B03	O		

Table 21. Drop/Insert Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
MX_TOH_CLK_OUT[1]	AA20	O	LVTTL (65 Ohm)	**MUX Transport Overhead Clock OUT:** MX_TOH_CLK_OUT[i] are 1.728 MHz output clocks for the MX_TOH_SYNC_OUT[i] and MX_TOH_DATA_OUT[i] signals.
MX_TOH_CLK_OUT[2]	U23	O		
MX_TOH_CLK_OUT[3]	U19	O		
MX_TOH_CLK_OUT[4]	L20	O		
MX_TOH_CLK_OUT[5]	K17	O		
MX_TOH_CLK_OUT[6]	G22	O		
MX_TOH_CLK_OUT[7]	C25	O		
MX_TOH_CLK_OUT[8]	F19	O		
MX_TOH_CLK_OUT[9]	G17	O		
MX_TOH_CLK_OUT[10]	A17	O		
MX_TOH_CLK_OUT[11]	H15	O		
MX_TOH_CLK_OUT[12]	J12	O		
MX_TOH_CLK_OUT[13]	D09	O		
MX_TOH_CLK_OUT[14]	D07	O		
MX_TOH_CLK_OUT[15]	C05	O		
MX_TOH_CLK_OUT[16]	A02	O		

Table 21. Drop/Insert Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
DX_TOH_DATA_INS[1]	AD25	I	LVTTL (65 Ohm)	**DEMUX Transport Overhead DATA Insert:** DX_TOH_DATA_INS[i] is Demultiplexer Serial TOH/SOH Insert Data consisting of 17 bytes of TOH data plus 10 stuff bytes, ST#. Data ordering is as follows: ST1,E1,F1,D1-D3,ST2,ST3,ST4,ST5,K1,K2,D4-D12,ST6,ST7,E2,ST8,ST9,ST10. All bytes are expected to be received in MSB to LSB order.
DX_TOH_DATA_INS[2]	AA24	I		
DX_TOH_DATA_INS[3]	U24	I		
DX_TOH_DATA_INS[4]	T25	I		
DX_TOH_DATA_INS[5]	H21	I		
DX_TOH_DATA_INS[6]	J21	I		
DX_TOH_DATA_INS[7]	G23	I		
DX_TOH_DATA_INS[8]	G25	I		
DX_TOH_DATA_INS[9]	G18	I		
DX_TOH_DATA_INS[10]	G16	I		
DX_TOH_DATA_INS[11]	E15	I		
DX_TOH_DATA_INS[12]	J16	I		
DX_TOH_DATA_INS[13]	G10	I		
DX_TOH_DATA_INS[14]	C08	I		
DX_TOH_DATA_INS[15]	F05	I		
DX_TOH_DATA_INS[16]	A05	I		
DX_TOH_SYNC_INS	T15	O	LVTTL (65 Ohm)	**DEMUX Transport Overhead SYNC Insert:** DX_TOH_SYNC_INS is a byte delineation signal for the DX_TOH_DATA_INS[i] TOH/SOH Insert signals.
DX_TOH_CLK_INS	U15	O	LVTTL (65 Ohm)	**DEMUX Transport Overhead Clock Insert:** DX_TOH_CLK_INS is a 1.728 MHz output clock signal for DX_TOH_SYNC_OUT and DX_TOH_DATA_OUT.
MX_TOH_DATA_INS	V15	I	LVTTL (65 Ohm)	**Transmit Transport Overhead Data:** Serialized Transport Overhead data consisting of 17 bytes of TOH data plus 10 stuff bytes, ST#. Data ordering is as follows: ST1,E1,F1,D1-D3,ST2,ST3,ST4,ST5,K1,K2,D4-D12,ST6,ST7,E2,ST8,ST9,ST10. All bytes are expected to be received in MSB to LSB order.

Table 21. Drop/Insert Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
MX_TOH_SYNC_INS	Y15	O	LVTTL (65 Ohm)	**MUX Transport Overhead SYNC INS:** MX_TOH_SYNC_INS is a byte delineation signal for the MX_TOH_DATA_INS TOH/SOH Insert signal.
MX_TOH_CLK_INS	AB15	O	LVTTL (65 Ohm)	**Transmit Transport Overhead Clock:** MX_TOH_CLK_INS is a 1.728 MHz output clock signal for MX_TOH_SYNC_INS and DX_TOH_DATA_INS.
DX_TOH_DATA_OUT	U16	O	LVTTL (65 Ohm)	**Receive Transport Overhead Data:** Serialized Transport Overhead data consisting of 17 bytes of TOH data plus 10 stuff bytes, ST#. Data ordering is as follows: ST1,E1,F1,D1-D3,ST2,ST3,ST4,ST5,K1,K2,D4-D12,ST6,ST7,E2,ST8,ST9,ST10. All bytes are provided in MSB to LSB order.
DX_TOH_SYNC_OUT	W16	O	LVTTL (65 Ohm)	**DEMUX Transport Overhead SYNC OUT:** DX_TOH_SYNC_OUT is a byte delineation signal for the DX_TOH_DATA_OUT TOH/SOH output signal.
DX_TOH_CLK_OUT	R16	O	LVTTL (65 Ohm)	**Receive Transport Overhead Clock:** DX_TOH_CLK_OUT is a 1.728 MHz output clock for DX_TOH_CLK_OUT and DX_TOH_DATA_OUT.

Table 22. Microprocessor Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
ADDR[12] ADDR[11] ADDR[10] ADDR[9] ADDR[8] ADDR[7] ADDR[6] ADDR[5] ADDR[4] ADDR[3] ADDR[2] ADDR[1] ADDR[0]	W01 Y01 AA01 AB01 AC01 AD01 AE01 W03 AC03 AA03 AA05 AB03 AE03	I	LVTTL (65 Ohm)	**ADDRESS BUS:** Allows host microprocessor to perform register selection within the S4802. ADDR[12] is the MSB.
APS_INTB	V11	O	LVTTL (65 Ohm)	**APS INTERRUPT**: Active-low output from the S4802 triggered by an APS event. APS_INTB is an open-drain output, which is tri-stated when the interrupt is acknowledged by accessing the interrupt.

Table 22. Microprocessor Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
BUSMODE	W11	I	LVTTL (65 Ohm)	**BUS INTERFACE MODE:** This signal allows the data transfer operations to be compatible with most microprocessor interfaces. **Busmode=1:** Data transfer occurs in “Intel mode” (RDB, WRB, RDYB). **Busmode=0:** Data transfer occurs in “Motorola mode” (DSB, RWB, DTACKB).
CSN	AD11	I	LVTTL (65 Ohm)	**CHIP SELECT**: Active-low chip select to the S4802 used to validate the address bus for read-and-write transfers.
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	AC02 Y03 AE02 W04 AA04 AC04 W05 Y05 AD03 AB05 W06 AA06 W07 AA07 W08 AE08	I/O	LVTTL (65 Ohm)	**DATA BUS:** Allows transfer of data between host microprocessor and the S4802. D[15] is the MSB.
INTB	Y11	O	LVTTL (65 Ohm)	**INTERRUPT**: Active-low output from the S4802 triggered by an event that caused one of the internal interrupts to become activated. INTB is an open-drain output that is tri-stated when the interrupt is acknowledged by accessing the interrupt.
RDB/DSB	U10	I	LVTTL (65 Ohm)	**READ DATA BUS/DATA STROBE:** If *BUSMODE*=1, the *RDB/DSB* input is low to enable data to be read from the addressed location on the data bus. If *BUSMODE*=0, the *RDB/DSB* input is low to enable data to be read from or to strobe-write data into the S4802.
RDYB/DTACKB	R10	O	LVTTL (65 Ohm)	**READY/DATA ACKNOWLEDGE:** *RDYB/DTACKB* goes low to acknowledge the end-of-data transfers over the data bus. The *RDYB/DTACKB* signal is a tri-stated output and operates the same for both *BUSMODE* settings.
RSTB	AE09	I	LVTTL (65 Ohm)	**RESET:** Active low input to reset the S4802.

Table 22. Microprocessor Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
SYNCMODE	AD09	I	LVTTL (65 Ohm)	**SYNC MODE:** Selects the mode of operation of the Microprocessor interface. **SYNCMODE=1:** 16-bit synchronous operation. **SYNCMODE=0:** 8-bit asynchronous operation.
uPCLK	AC09	I	LVTTL (65 Ohm)	**Microprocessor Clock:** Microprocessor system clock.
WRB/RWB	W09	I	LVTTL (65 Ohm)	**WRITE/READ-WRITE DATA BUS:** WRB/RWB is high to enable data to be read from the addressed location on the data bus. WRB/RWB is low to enable data to be written to the addressed location on the data bus.

Table 23. GPIO/Alarm/LOS/RDI Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
GPIO[15] GPIO[14] GPIO[13] GPIO[12] GPIO[11] GPIO[10] GPIO[9] GPIO[8] GPIO[7] GPIO[6] GPIO[5] GPIO[4] GPIO[3] GPIO[2] GPIO[1] GPIO[0]	G09 H09 J09 K09 H11 P09 L10 T11 D11 F11 K11 L14 P11 E11 G11 L12	I/O	LVTTL (65 Ohm)	**GENERAL PURPOSE I/O:** The GPIO register allows the user to define each grouping (GPIO[0,1], GPIO[2,3], GPIO[4,5], GPIO[6,7] , GPIO[8,9], GPIO[10,11], GPIO[12,13], GPIO[14,15]) as either input or output bits. These bits can be used for user-defined input control. GPIO[15] is the MSB.
DX_ALARM_OUT	AA17	O	LVTTL (65 Ohm)	**DEMUX ALARM OUT SIGNAL:** Reports SONET Demultilpexer alarms, OOF, LOF, LOC, LAIS, and LOS.
DX_LOSEXT	W18	I	LVTTL (65 Ohm)	**DEMUX ALARM INPUT SIGNAL:** Demultiplexer loss-of-input signal.

Table 23. GPIO/Alarm/LOS/RDI Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
MX_ALARM_OUT[1] MX_ALARM_OUT[2] MX_ALARM_OUT[3] MX_ALARM_OUT[4] MX_ALARM_OUT[5] MX_ALARM_OUT[6] MX_ALARM_OUT[7] MX_ALARM_OUT[8] MX_ALARM_OUT[9] MX_ALARM_OUT[10] MX_ALARM_OUT[11] MX_ALARM_OUT[12] MX_ALARM_OUT[13] MX_ALARM_OUT[14] MX_ALARM_OUT[15] MX_ALARM_OUT[16]	R12 U12 T13 U13 R14 U14 W14 AA14 P15 N16 P17 T17 V17 AB17 R18 AC18	O	LVTTL (65 Ohm)	**MUX ALARM OUT SIGNAL:** Reports SONET Multiplexer alarms for MX tributary [i], OOF, LOF, LOC, LAIS, and LOS.
MX_LOSEXT[1] MX_LOSEXT[2] MX_LOSEXT[3] MX_LOSEXT[4] MX_LOSEXT[5] MX_LOSEXT[6] MX_LOSEXT[7] MX_LOSEXT[8] MX_LOSEXT[9] MX_LOSEXT[10] MX_LOSEXT[11] MX_LOSEXT[12] MX_LOSEXT[13] MX_LOSEXT[14] MX_LOSEXT[15] MX_LOSEXT[16]	V19 R19 N17 K19 H23 E21 B25 A25 C17 B17 B15 J11 J10 E06 E04 A04	I	LVTTL (65 Ohm)	**MUX ALARM INPUT SIGNAL:** Reports loss-of-signal on multiple tributary [i] input.

Table 24. Test Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
TCK	A03	I	LVTTL (Internal pull-up)	**TEST CLOCK:** JTAG input clock used to sample data on the TDI and TDO pins.
TDI	C01	I	LVTTL (65 Ohm, Internal pull-up)	**TEST DATA IN:** Input pin for serial data stream to be sent to the S4802.
TDO	C03	O	LVTTL (65 Ohm)	**TEST DATA OUT:** Output pin for serial data stream sent from the S4802.

Table 24. Test Interface

Pin Signal Name	Pin #	(I/O)	Signal Type	Signal Description
TMS	E01	I	LVTTL (65 Ohm, Internal pull-up)	**TEST MODE SELECT:** Controls the operating mode of the JTAG interface. Should be left high when JTAG interface is not in use.
TRSTB	F03	I	LVTTL (65 Ohm, Internal pull-up)	**TEST PORT RESET:** Active-low input used to reset the JTAG interface. Must be pulsed low after power up (or tied low via a 220 Ohm resistor if unused) for the device to operate correctly.
TRISTATE_EN	B01	I	LVTTL (65 Ohm, Internal pull-down)	**TRI-STATE ENABLE:** When TRISTATE_EN is brought high, all output and input/output pins on the S4802 are tri-stated. Provide 220 Ohm pull-down to ground.

Table 25. Power, Ground, No Connect, and External Pull Down

Chip Signal Name	Pin #	Signal Description
VDD_2.5	H02, M02, V02, B04, F04, Y04, AD04, M06, P06, F08, Y08, D10, M10, P10, AB10, L11, R11, K12, N12, T12, M13, P13, B14, K14, N14, T14, AD14, L15, R15, D16, M16, P16, AB16, F18, Y18, M20, P20, B22, F22, Y22, AD22, H24, M24, V24, A23, AC05, C21, A19, E03, C19, M25, E25, E23, M19, M21, E14, A21, W23	2.5V power supply
VDD_3.3	D02, P02, AB02, K04, T04, D06, H06, V06, AB06, B08, K08, T08, AD08, H10, V10, B12, F12, Y12, AD12, F14, Y14, H16, V16, B18, K18, T18, AD18, D20, H20, V20, AB20, K22, T22, D24, P24, AB24	3.3V power supply
Ground	B02, F02, K02, T02, Y02, AD02, D04, H04, M04, P04, V04, AB04, B06, F06, K06, T06, Y06, AD06, D08, H08, M08, P08, V08, AB08, B10, F10, K10, T10, Y10, AD10, N11, D12, H12, M12, P12, V12, AB12, L13, N13, R13, D14, H14, M14, P14, V14, AB14, N15, B16, F16, K16, T16, Y16, AD16, D18, H18, M18, P18, V18, AB18, B20, F20, K20, T20, W20, Y20, AD20, D22, H22, M22, P22, V22, AB22, B24, F24, K24, T24, Y24, AD24, P23, AE05, AA23, AA25	Ground
NO CONNECT	B19, D01, F01, C02, E02, D03, V09, C10, K15, M17, AE25, G19, D21, F13, C13, M15, G12, E12, AC07, AE07, G14, J13, K13, Y19, AD21	Leave disconnected
UNUSED	W25	Provide a 220 Ohm pull-down to Ground

Note: All internal (weak) pull-up and pull-down resistors are 14 kOhm and 12 kOhm, respectively.

All Missouri LVPECL outputs have push-pull structures instead of the usual open-emitter output found on ECL devices. No external pull-down resistors are needed on the Missouri's LVPECL outputs.

The Missouri's LVDS and LVPECL inputs have the same structure. All LVDS inputs on the Missouri are LVPECL-tolerant, hence LVPECL inputs are really LVPECL-tolerant LVDS inputs. LVPECL outputs should be attenuated through 33 Ohm series resistors, on each side, when interfacing to LVDS inputs.

9.0 Input and Output Descriptions

Table 26. Demultiplexer Side Inputs

Signal Name	Clock Reference	Description
DX_CLK_IN		Demultiplexer 155.52 MHz Clock.
DX_DATA_IN_[15:0]	DX_CLK_IN↑	Two byte-wide STS-48/STM-16 data input.
DX_FRAME_IN		Frame Position Indicator. Must be tied low if internal framer is being used (**DX_FRMR_INH**=0).
DX_LOSEXT		Demultiplexer loss of input signal.
DX_PROT_CLK_IN		Clk Signal for the DX Protection Input Data and Frame Sync signals
DX_PROT_PRTY_IN	DX_PROT_CLK_IN↑	Parity signal for the DX Protection input interface
DX_PROT_SYNC_IN	DX_PROT_CLK_IN↑	Byte delineation signal for the DX Protection input interface
DX_PROT_DATA_IN_[1:16]	DX_PROT_CLK_IN↑	Data for DX Protection input interface
DX_TOH_DATA_INS_[1:16]	DX_TOH_CLK_INS↑	Demultiplexer Serial TOH/SOH Insert data.

Table 27. Multiplexer Side Inputs

Signal Name	Clock Reference	Description
MX_CLK_IN_[1:16]		For STS-12/STM-1 signals, *MX_CLK_IN_[i],* i=1,5,9,13 are used, and they are 622.08 MHz STS-12/STM-4 clocks. Otherwise, *MX_CLK_IN_[i]* are155.52 MHz STS-3/STM-1 clocks.
MX_DATA_IN_[1:16]	MX_CLK_IN_[1:16]↑	For STS-12/STM-1 signals, *MX_DATA_IN_[i], i*=1,5,9,13 are used, and they are serial STS-12/STM-4 signals. Otherwise they are all serial STS-3/STM-1 signals.
MX48_PCLK_IN		Clock for STS-48 parallel data. Pin mapped to MX_CLK_IN_[2].
MX48_PDATA_IN_[15:0]	MX48_PCLK_IN↑	Pins used for STS-48 parallel data. MX48_PDATA_IN bits 15:0 are mapped, respectively to: MX_CLK_IN_[3], MX_DATA_IN_[3], MX_CLK_IN_[4], MX_DATA_IN_[4], MX_CLK_IN_[6], MX_DATA_IN_[6], MX_CLK_IN_[7], MX_DATA_IN_[7], MX_CLK_IN_[8], MX_DATA_IN_[8], MX_CLK_IN_[10], MX_DATA_IN_[10], MX_CLK_IN_[11], MX_DATA_IN_[11], MX_CLK_IN_[12], MX_DATA_IN_[12].
MX_LOSEXT_[1:16]		Multiplexer loss of input signals.
MX_PROT_CLK_IN		Clk Signal for the Protection input Data and Frame Sync signals
MX_PROT_PRTY_IN	MX_PROT_CLK_IN↑	Parity signal for the MX Protection input interface
MX_PROT_SYNC_IN	MX_PROT_CLK_IN↑	Byte delineation signal for the MX Protection input interface
MX_PROT_DATA_IN_[1:16]	MX_PROT_CLK_IN↑	Data for MX Protection input interface.
MX_TOH_DATA_INS	MX_TOH_CLK_INS↑	Multiplexer Serial TOH/SOH Insert data.

Table 28. Common I/O

Signal Name	Clock Reference	Description
SYS_CLK_IN		A 622.08 MHz clock signal used by both the Mux and Demux side of the Missouri The Pointer Processors in the Multiplexer and Demultiplexer Side synchronizes the data to this clock.
SYS_SYNC_OUT		Frame Sync Output signal that feeds other Missouri *SYS_SYNC_IN* input signals.
SYS_SYNC_IN	async (sampled by SYS_CLK_IN↑)	Used to align frames from multiple Missouris so that they can be multiplexed into a STS-192/STM-64.
RSTB		Active low Master Reset Signal.
TS_EN		Input tristate enable. Active high input that tristates all LVTTL output and bi-directional signals.
TCK		JTAG test clock signal.
TMS	TCK↑	JTAG test mode select.
TDI	TCK↑	JTAG test data input.
TRSTB		JTAG test reset signal.

Table 28. Common I/O

Signal Name	Clock Reference	Description
TDO	TCK↓	JTAG test data output.
RX_REF_CLK_OUT		Reference clock output (see section 3.11).
GPIO0-GPIO15		General Purpose I/O. Tied to registers for microprocessor access. Can be defined as I or O through control registers. Defaults as input (to avoid possible contention on power-up) and is pulled up (to avoid possible floating input).

Table 29. Demultiplexer Side Outputs

Signal Name	Clock Reference	Description
DX_CLK_OUT_155_622		For STS-12/STM-4 signals, *DX_CLK_OUT_155_622* is 622.08 MHz, otherwise it is155.52 MHz.
DX_CLK_OUT_155		*DX_CLK_OUT_155* is 155.52 MHz.
DX_DATA_OUT_[1:16]	DX_CLK_OUT_155_622↓[a] DX_CLK_OUT_155↓	For STS-12/STM-4 signals, only *DX_DATA_OUT_[i[i= 1,5,9,13* are active, and they are serial STS-12/STM-4 signals. Otherwise, all are active as serial STS-3/STM-1 signals.
DX48_PCLK_OUT		Clock to accompany *DX48_PDATA_OUT*. Mapped to pin *DX_CLK_OUT_155.*
DX48_PDATA_OUT_[15:0]	DX48_PCLK_OUT↑	Pins used for STS-48 parallel data. DX48_PDATA_OUT bits 15:0 are mapped, respectively to: DX_DATA_OUT[1], [5], [9], [13], [2], [3], [4], [6], [7], [8], [10], [11], [12], [14], [15], [16].
DX_TOH_SYNC_OUT	DX_TOH_CLK_OUT↑	Byte delineation signal for the Demux TOH/SOH Serial Drop Signal.
DX_TOH_CLK_OUT		Demultiplexer Serial TOH/SOH Drop 1.728 MHz Clock.
DX_TOH_DATA_OUT	DX_TOH_CLK_OUT↑	Demultiplexer TOH/SOH Serial Drop Data.
DX_ALARM_OUT		Indicates Received Multiplexer Alarm conditions.
DX_PROT_CLK_OUT		Clock Signal for the DX Protection Output Data and Frame Sync signals.
DX_PROT_PRTY_OUT	DX_PROT_CLK_OUT↑[a]	Indicates Parity across DX Protection Output interface.
DX_PROT_SYNC_OUT	DX_PROT_CLK_OUT↑[a]	Byte delineation signal for the DX Protection Output interface.
DX_PROT_DATA_OUT_[1:16]	DX_PROT_CLK_OUT↑[a]	Data for Protection Output interface.
DX_TOH_CLK_INS		Demultiplexer Serial TOH/SOH Insert 1.728 MHz Clock.
DX_TOH_SYNC_INS	DX_TOH_CLK_INS↑	Sync pulse for DX_TOH_DATA_INS.

a. Note that the sense of *DX_CLK_OUT_155*, *DX_CLK_OUT_155_622*, and *DX_PROT_CLK_OUT* can be inverted by setting the **DX_CLK_OUT_INV_[1:2]** and **DX_PROT_CLK_OUT_INV** bits high, respectively. The edge sensitivity of *DX_CLK_OUT_155* and *DX_CLK_OUT_155_622* are shown for the default, inverted signals (**DX_CLK_OUT_INV_[1:2]** = "11"). The edge sensitivity will be the opposite of that shown in this table for the alternate, non-inverted signals (**DX_CLK_OUT_INV_[1:2]** = "00"). The edge sensitivity of the *DX_PROT_CLK_OUT* clock is shown for the default, non-inverted signal (**DX_PROT_CLK_OUT_INV** = 0). The edge sensitivity will be the opposite of that shown in this table for the alternate, inverted clock (**DX_PROT_CLK_OUT_INV** = 1).

Table 30. Multiplexer Side Outputs

Signal Name	Clock Reference	Description
MX_ALARM_OUT_[1:16]		Multiplexer Alarm Out indication signals.
MX_CLK_OUT		Multiplexer Output Clock (155.52 Mhz).
MX_DATA_OUT_[15:0]	MX_CLK_OUT↑[a]	Two byte-wide STS-48/STM-16 data.
MX_TOH_SYNC_OUT_[1:16]	MX_TOH_CLK_OUT_[i]↑	Byte delineation signal for the TOH/SOH Output signal.
MX_TOH_CLK_OUT_[1:16]		Multiplexer Serial TOH/SOH Insert 1.728 MHz Clock.
MX_TOH_DATA_OUT_[1:16]	MX_TOH_CLK_OUT_[i]↑	Multiplexer TOH Data stream.
MX_TOH_SYNC_INS	MX_TOH_CLK_INS↑	Byte delineation signal for the mux TOH/SOH Serial Insert Signal.
MX_TOH_CLK_INS		Multiplexer Serial TOH/SOH Drop1.728 MHz Clock.
MX_PROT_CLK_OUT		Clk Signal for the Protection Output Data and Frame Sync signals.

Table 30. Multiplexer Side Outputs

Signal Name	Clock Reference	Description
MX_PROT_SYNC_OUT	MX_PROT_CLK_OUT↓a	Byte delineation signal for the Protection Ouput interface.
MX_PROT_DATA_OUT_[1:16]	MX_PROT_CLK_OUT↑[a]	Data for Protection Output interface.
MX_PROT_PRTY_OUT	MX_PROT_CLK_OUT↑[a]	Indicates Parity across Protection Output interface.

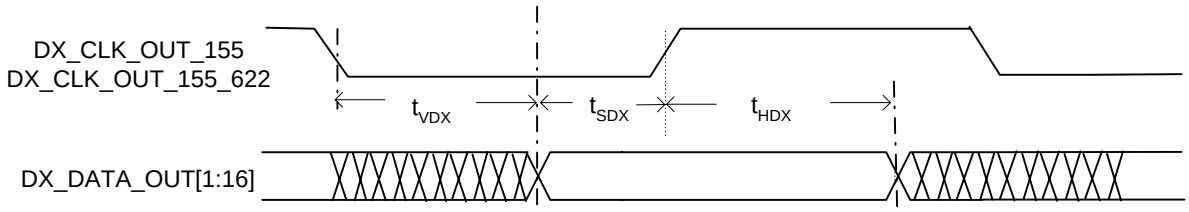
a. Note that the sense of *MX_CLK_OUT* and *MX_PROT_CLK_OUT* can be inverted by setting the **MX_CLK_OUT_INV** and **MX_PROT_CLK_OUT_INV** bits high, respectively. The edge sensitivity of *MX_CLK_OUT* is shown for the default, inverted signal (**MX_CLK_OUT_INV** = 1). The edge sensitivity will be the opposite of that shown in this table for the alternate, non-inverted signals (**MX_CLK_OUT_INV** = 0). The edge sensitivity of the *MX_PROT_CLK_OUT* clock is shown for the default, non-inverted signal (**MX_PROT_CLK_OUT_INV** = 0). The edge sensitivity will be the opposite of that shown in this table for the alternate, inverted clock (**MX_PROT_CLK_OUT_INV** = 1).

10.0 AC Electrical Characteristics

Notes on LVPECL Timing

1. When a set-up time is specified on LVPECL signal between an input and a clock, the set-up time is the time in picoseconds or nanoseconds from the 50% point of the input to the 50% point of the clock.
2. When a hold time is specified on LVPECL signal between an input and a clock, the hold time is the time in picoseconds or nanoseconds from the 50% point of the clock to the 50% point of the input.

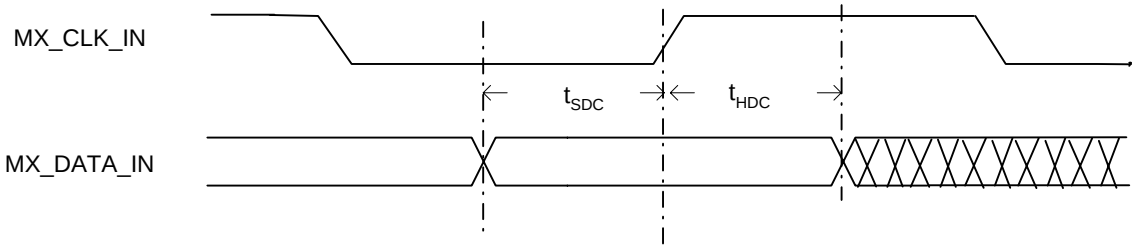
10.1 Low Speed Serial Interface Demux Timing



Label	Parameter	Min	Nom	Max	Units
622 Mb/s Operation					
Freq.	DX_CLK_OUT_155_622		622.08		MHz
	DX_CLK_OUT_155_622 duty cycle	45		55	%
155 Mb/s Operation					
Freq.	DX_CLK_OUT_155 frequency		155.52		MHz
	DX_CLK_OUT_155 duty cycle	45		55	%
622/155 Mb/s Operation					
t_{VDX}	DX_DATA_OUT[1:16] prop delay w.r.t. DX_CLK_OUT_155_622/ DX_CLK_OUT_155 low			440	ps
t_{SDX}	DX_DATA_OUT[1:16] setup time w.r.t. DX_CLK_OUT_155_622/ DX_CLK_OUT_155	400			ps
t_{HDX}	DX_DATA_OUT[1:16] hold time w.r.t. DX_CLK_OUT_155_622/ DX_CLK_OUT_155	400			ps

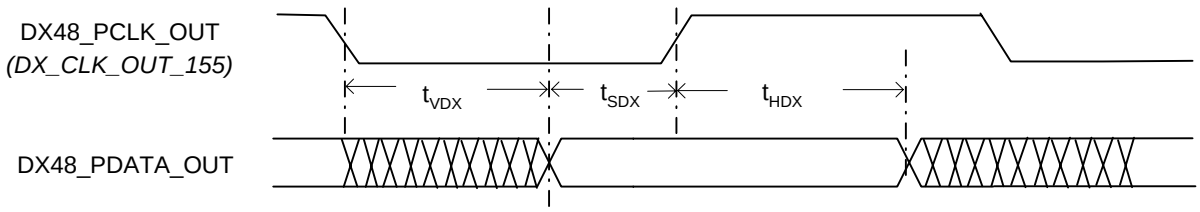
Note that the timing diagram was drawn based on the default *inverted* clock (**DX_CLK_OUT_INV_[1:2]** = 1). The edge sensitivity of *DX_DATA_OUT[1:15]* would be set on the *opposite* edge of that shown in the figure if the *non-inverted* clock was used (**DX_CLK_OUT_INV_[1:2]** = “00”).

10.2 Low-Speed Serial Interface Mux Timing



Label	Parameter	Min	Nom	Max	Units
622 Mb/s Operation					
Freq.	MX_CLK_IN		622.08		MHz
	MX_CLK_IN duty cycle	45		55	%
t_{SDC}	Setup MX_DATA_IN w.r.t. MX_CLK_IN	450			ps
t_{HDC}	Hold MX_DATA_IN w.r.t. MX_CLK_IN	450			ps
155 Mb/s Operation					
Freq.	MX_CLK_IN		155.52		MHz
	MX_CLK_IN duty cycle	45		55	%
t_{SDC}	Setup MX_DATA_IN w.r.t. MX_CLK_IN	1.5			ns
t_{HDC}	Hold MX_DATA_IN w.r.t. MX_CLK_IN	1.5			ns

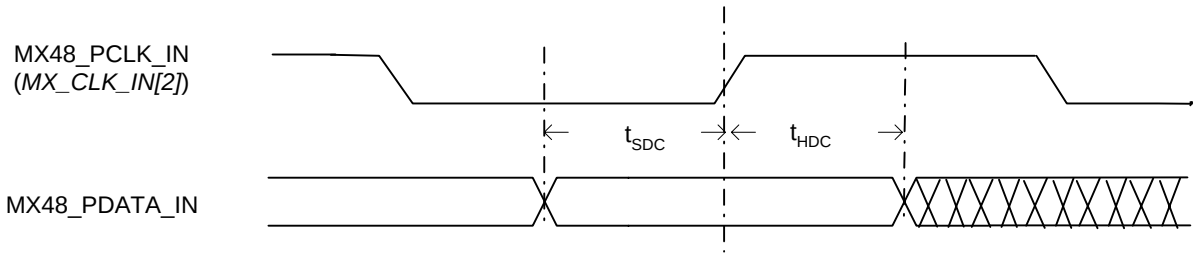
10.3 Low Speed Parallel Interface (OC-48) Demux Timing



Label	Parameter	Min	Nom	Max	Units
Freq.	DX48_PCLK_OUT		155.52		MHz
	DX48_PCLK_OUT duty cycle	45		55	%
t_{VDX}	DX48_PDATA_OUT prop delay w.r.t. DX48_PCLK_OUT low			440	ps
t_{SDX}	DX48_PDATA_OUT setup time w.r.t. DX48_PCLK_OUT	2*			ns
t_{HDX}	DX48_PDATA_OUT hold time w.r.t. DX48_PCLK_OUT	2*			ns

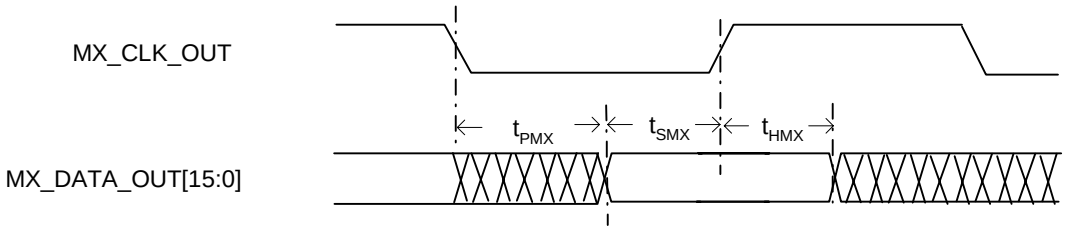
Note: * See AN-S4802-05 App. Note (System Design Considerations when using the S4802 in OC-48 Mode on the Low Speed Side.

10.4 Low-Speed Parallel Interface (OC-48) Mux Timing



Label	Parameter	Min	Nom	Max	Units
Freq.	MX48_PCLK_IN		155.52		MHz
	MX48_PCLK_IN duty cycle	45		55	%
t_{SDC}	Setup MX48_PDATA_IN w.r.t. MX48_PCLK_IN	1.5			ns
t_{HDC}	Hold MX48_PDATA_IN w.r.t. MX48_PCLK_IN	1.5			ns

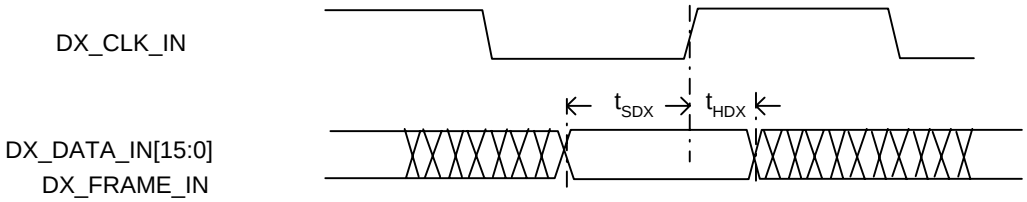
10.5 High-Speed Interface Mux Timing



Label	Parameter	Min	Nom	Max	Units
Freq.	MX_CLK_OUT		155.52		MHz
	MX_CLK_OUT duty cycle	45		55	%
t_{PMX}	MX_DATA_OUT prop delay w.r.t. MX_CLK_OUT	-1		1	ns
t_{SMX}	Setup MX_DATA_OUT w.r.t. MX_CLK_OUT	2			ns
t_{HMX}	Hold MX_DATA_OUT w.r.t. MX_CLK_OUT	2			ns

Note that the timing diagram was drawn based on the default *inverted* clock (**MX_CLK_OUT_INV** = 1). The edge sensitivity of *MX_DATA_OUT[15:0]* would be set on the *opposite* edge of that shown in the figure if the *non-inverted* clock was used (**MX_CLK_OUT_INV** = 0).

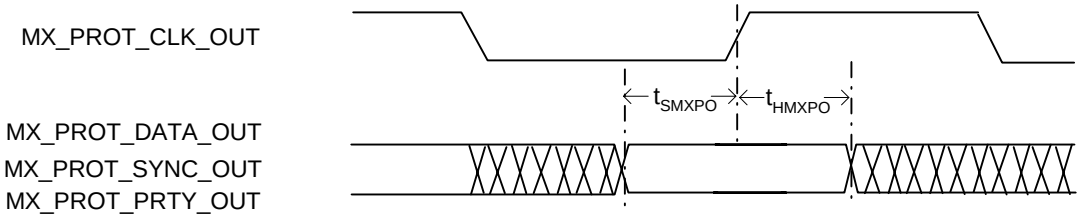
10.6 High-Speed Interface Demux Timing



Label	Parameter	Min	Nom	Max	Units
Freq.	DX_CLK_IN		155.52		MHz
	DX_CLK_IN duty cycle	45		55	%

Label	Parameter	Min	Nom	Max	Units
t_{SDX}	Setup time w.r.t. DX_CLK_IN	1.5			ns
t_{HDX}	Hold time w.r.t. DX_CLK_IN	0.5			ns

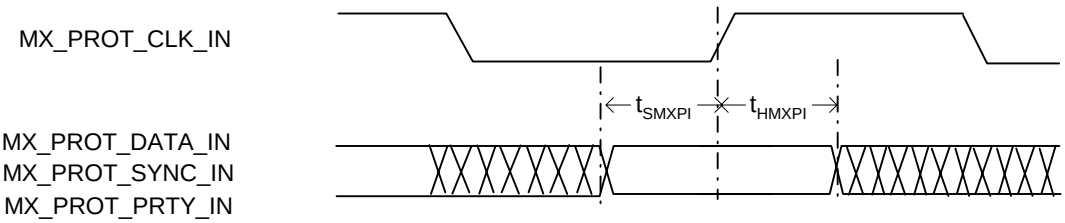
10.7 Protection Switching Mux Output Timing



Label	Parameter	Min	Nom	Max	Units
Freq.	MX_PROT_CLK_OUT		155.52		MHz
	MX_PROT_CLK_OUT duty cycle	45		55	%
t_{SMXPO}	Setup MX_DATA_OUT, MX_PROT_SYNC_OUT, MX_PROT_PTRY_OUT w.r.t. MX_PROT_CLK_OUT	1.8			ns
t_{HMXPO}	Hold MX_DATA_OUT, MX_PROT_SYNC_OUT, MX_PROT_PTRY_OUT w.r.t. MX_PROT_CLK_OUT	2			ns

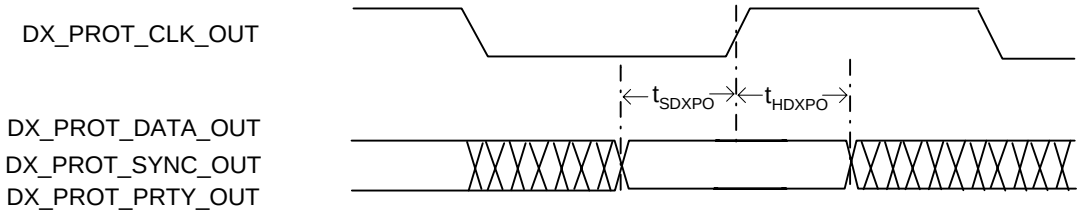
Note that the timing diagram was drawn based on the default *non-inverted* clock (**MX_PROT_CLK_OUT_INV** = 0). The edge sensitivity of *MX_PROT_DATA_OUT*, *MX_PROT_SYNC_OUT*, and *MX_PROT_PTRY_OUT* would be set on the *opposite* edge of that shown in the figure if the *non-inverted* clock was used (**MX_PROT_CLK_OUT_INV** = 1).

10.8 Protection Switching Mux Input Timing



Label	Parameter	Min	Nom	Max	Units
Freq.	MX_PROT_CLK_IN		155.52		MHz
	MX_PROT_CLK_IN duty cycle	45		55	%
t_{SMXPI}	Setup time w.r.t. to MX_PROT_CLK_IN	1.5			ns
t_{HMXPI}	Hold time w.r.t. to MX_PROT_CLK_IN	1.0			ns

10.9 Protection Switching Demux Output Timing

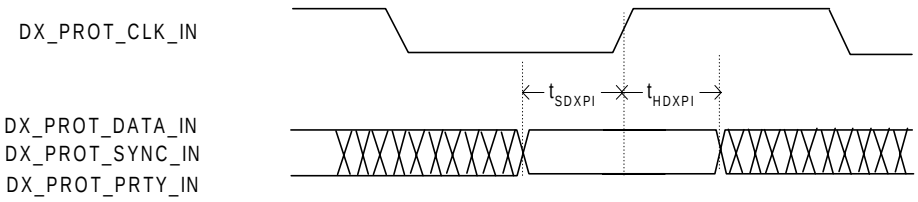


Label	Parameter	Min	Nom	Max	Units
Freq.	DX_PROT_CLK_OUT		155.52		MHz
	DX_PROT_CLK_OUT duty cycle	45		55	%
t_{SDXPO}	Setup MX_DATA_OUT w.r.t. MX_CLK_OUT	1.8			ns
t_{HDXPO}	Hold MX_DATA_OUT w.r.t. MX_CLK_OUT	2			ns

Note that the timing diagram was drawn based on the default *non-inverted* clock (**DX_PROT_CLK_OUT_INV** = 0).

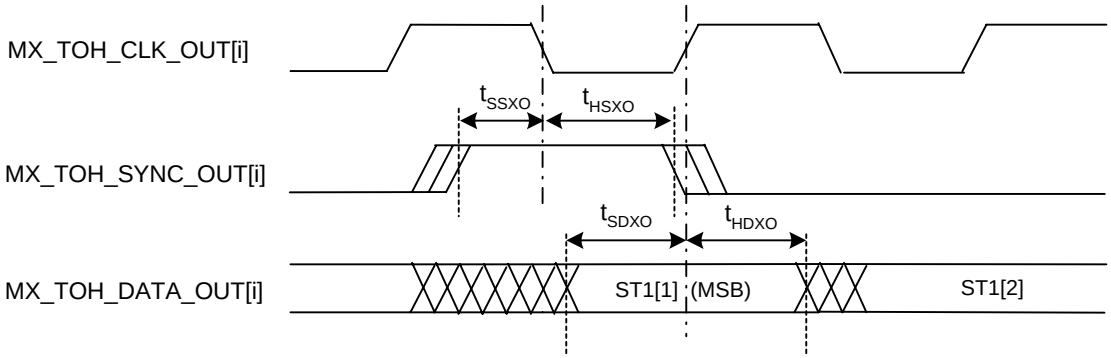
The edge sensitivity of *DX_PROT_DATA_OUT*, *DX_PROT_SYNC_OUT*, and *DX_PROT_PTRY_OUT* would be set on the *opposite* edge of that shown in the figure if the *inverted* clock was used (**DX_PROT_CLK_OUT_INV** = 1).

10.10 Protection Switching Demux Input Timing



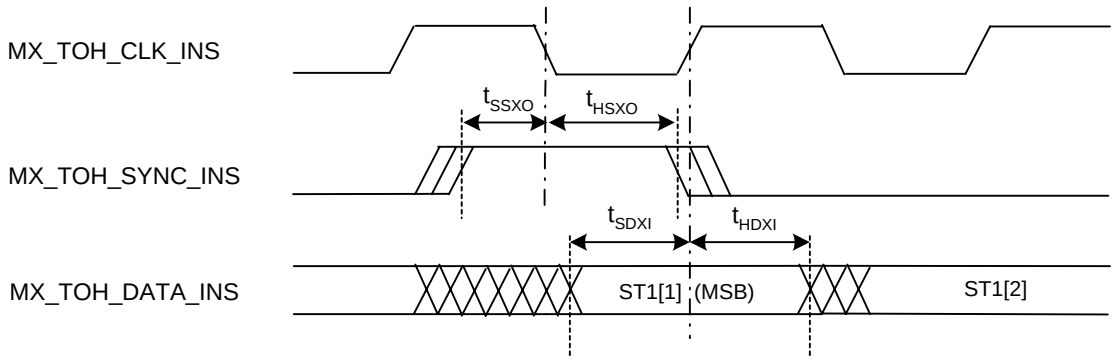
Label	Parameter	Min	Nom	Max	Units
Freq.	DX_PROT_CLK_IN		155.52		MHz
	DX_PROT_CLK_IN duty cycle	45		55	%
t_{SDXPI}	Setup time w.r.t. to DX_PROT_CLK_IN	1.5			ns
t_{HDXPI}	Hold time w.r.t. to DX_PROT_CLK_IN	1.0			ns

10.11 Mux TOH Drop Timing



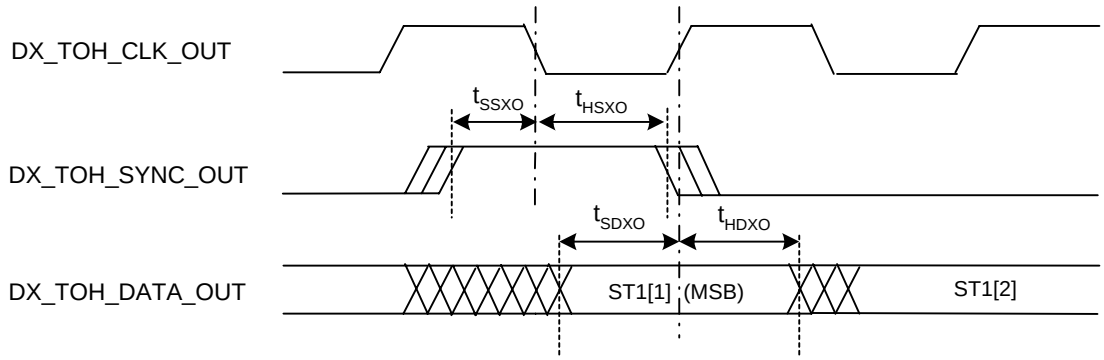
Label	Parameter	Min	Nom	Max	Units
Freq.	MX_TOH_CLK_OUT[i]		1.728		MHz
t_{SSXO}	MX_TOH_SYNC_OUT[i] setup time w.r.t. falling-edge of MX_TOH_CLK_OUT[i]	100			ns
t_{HSXO}	MX_TOH_SYNC_OUT[i] hold time w.r.t. falling-edge of MX_TOH_CLK_OUT[i]	100			ns
t_{SDXO}	MX_TOH_DATA_OUT[i] setup time w.r.t. rising-edge of MX_TOH_CLK_OUT[i]	100			ns
t_{HDXO}	MX_TOH_DATA_OUT[i] hold time w.r.t. rising-edge of MX_TOH_CLK_OUT[i]	100			ns

10.12 Mux TOH Insert Timing



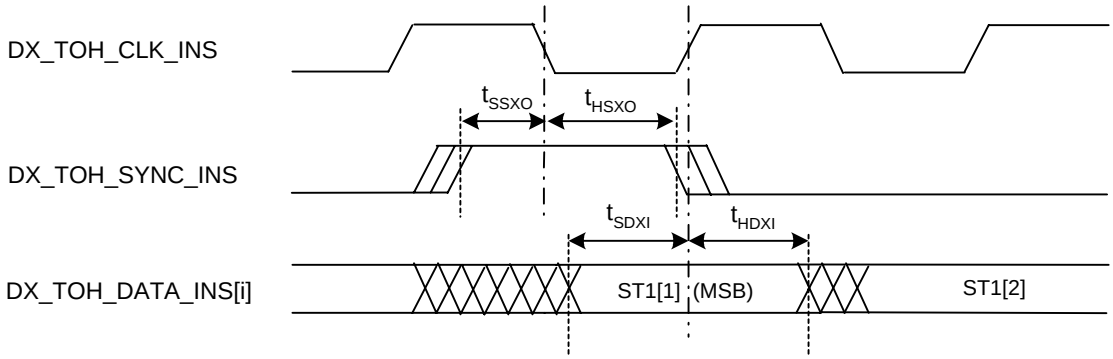
Label	Parameter	Min	Nom	Max	Units
Freq.	MX_TOH_CLK_INS		1.728		MHz
t_{SSXO}	MX_TOH_SYNC_INS setup time w.r.t. falling-edge of MX_TOH_CLK_INS	100			ns
$t_{\mathbf{HSXO}}$	MX_TOH_SYNC_INS hold time w.r.t. falling-edge of MX_TOH_CLK_INS	100			ns
t_{SDXI}	MX_TOH_DATA_INS setup time w.r.t. to rising-edge of MX_TOH_CLK_INS	100			ns
t_{HDXI}	MX_TOH_DATA_INS hold time w.r.t. to rising-edge of MX_TOH_CLK_INS	100			ns

10.13 Demux TOH Drop Timing



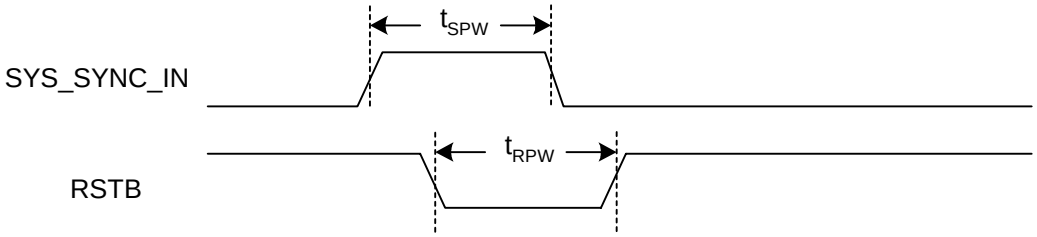
Label	Parameter	Min	Nom	Max	Units
Freq.	DX_TOH_CLK_OUT		1.728		MHz
t_{SSXO}	DX_TOH_SYNC_OUT setup time w.r.t. falling-edge of DX_TOH_CLK_OUT	100			ns
$t_{\mathbf{HS}XO}$	DX_TOH_SYNC_OUT hold time w.r.t. falling-edge of DX_TOH_CLK_OUT	100			ns
$t_{\mathbf{SD}XO}$	DX_TOH_DATA_OUT setup time w.r.t. rising-edge of DX_TOH_CLK_OUT	100			ns
$t_{\mathbf{HD}XO}$	DX_TOH_DATA_OUT hold time w.r.t. rising-edge of DX_TOH_CLK_OUT	100			ns

10.14 Demux TOH Insert Timing



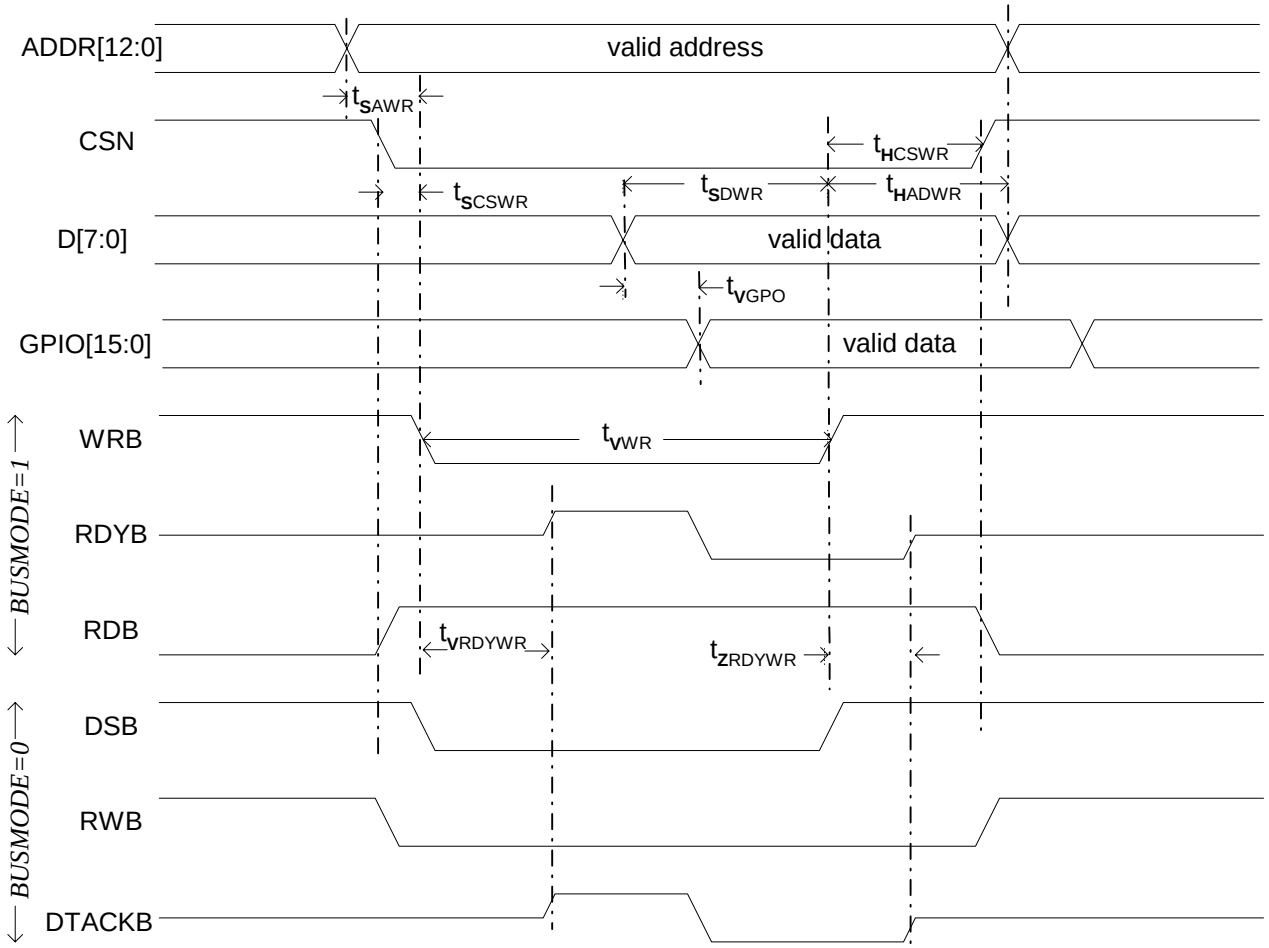
Label	Parameter	Min	Nom	Max	Units
Freq.	DX_TOH_CLK_INS		1.728		MHz
t_{SSXO}	DX_TOH_SYNC_INS setup time w.r.t. falling-edge of DX_TOH_CLK_INS	100			ns
t_{HSXO}	DX_TOH_SYNC_INS hold time w.r.t. falling-edge of DX_TOH_CLK_INS	100			ns
t_{SDXI}	DX_TOH_DATA_INS[i] setup time w.r.t. rising-edge of DX_TOH_CLK_INS	100			ns
t_{HDXI}	DX_TOH_DATA_INS[i] hold time w.r.t. rising-edge of DX_TOH_CLK_INS	100			ns

10.15 System Reset and Synchronization Timing



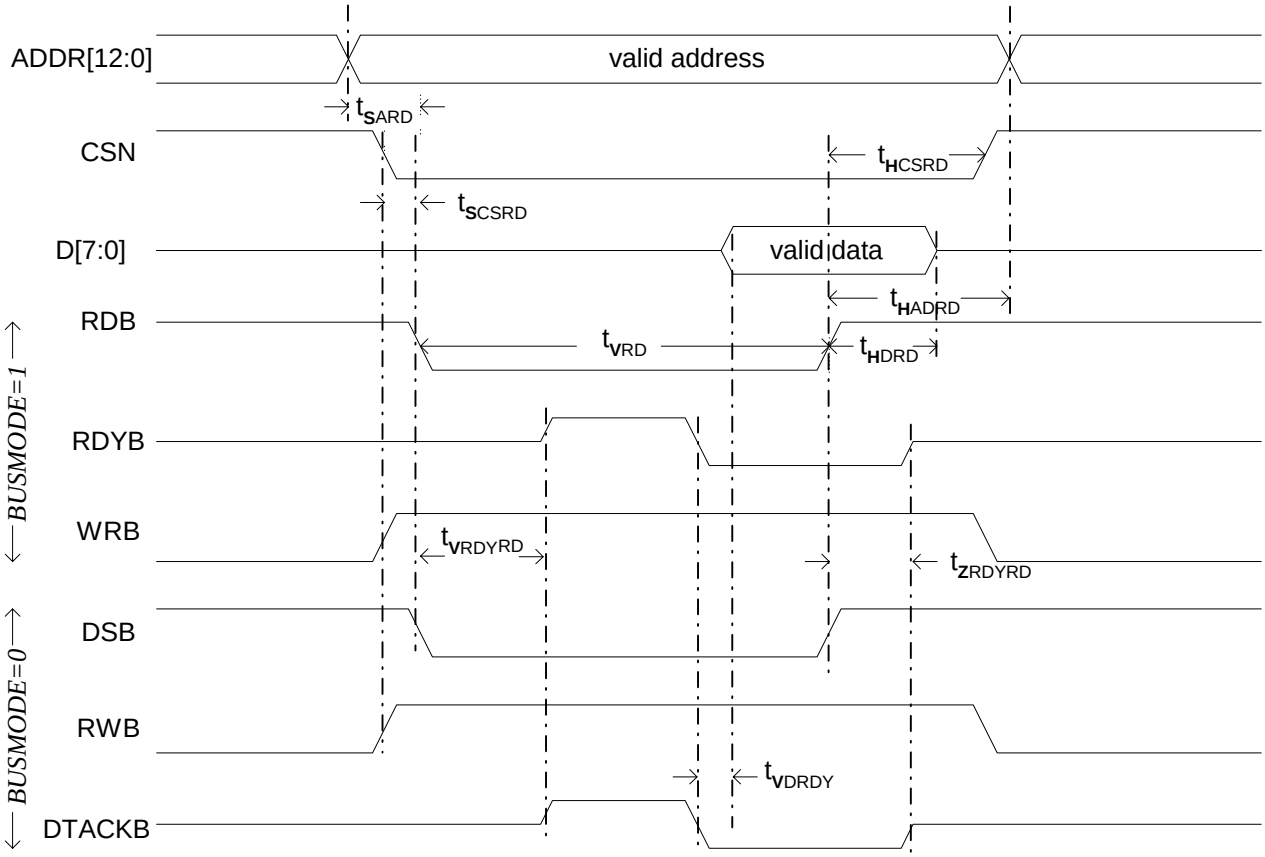
Label	Parameter	Min	Nom	Max	Units
t_{SPW}	SYS_SYNC_IN pulse width	20			ns
t_{RPW}	RSTB pulse width	200			ns

10.16 Microprocessor Interface Write Timing (Asynchronous Mode)



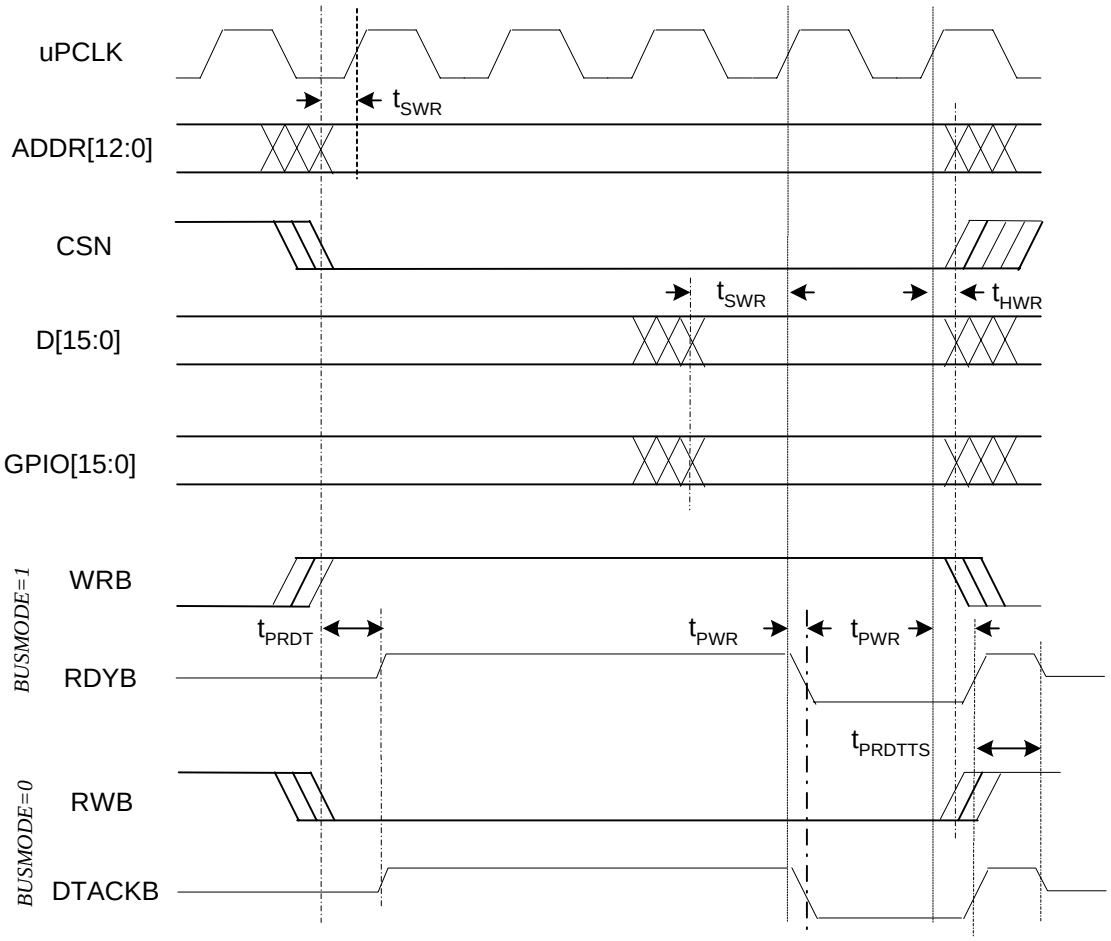
Label	Parameter	Min	Max	Units
t_{SAWR}	Setup addr to write (WRB,DSB) assert	10		ns
t_{SCSWR}	Setup chip select (CSN,RWB) to write (WRB,DSB) assert	5		ns
t_{VWR}	Valid write (WRB,DSB) pulse width	50		ns
t_{SDWR}	Setup data to write (WRB,DSB) deassert	15		ns
t_{HADWR}	Hold addr/data from write (WRB,DSB) deassert	4		ns
t_{VRDYWR}	Valid RDYB,DTACKB from write (WRB,DSB) assert	0	15	ns
t_{ZRDYWR}	Tri-state RDYB,DTACKB from write (WRB,DSB) deassert	0	10	ns
t_{HCSWR}	Hold chip select (CSB,RWB) from write (WRB,DSB) deassert	0		ns
t_{VGPO}	GPIO output valid after D[15:0] written	0	8	ns

10.17 Microprocessor Interface Read Timing (Asynchronous Mode)



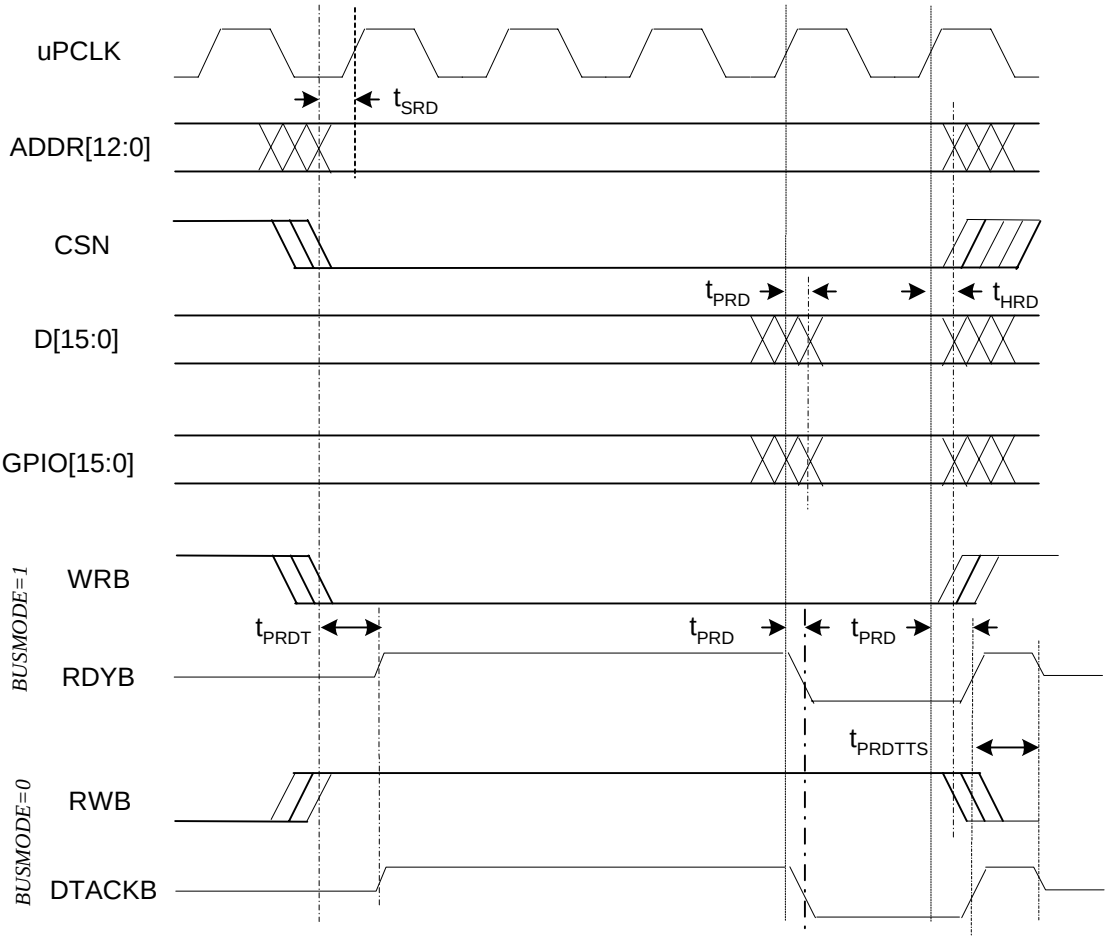
Label	Parameter	Min	Max	Units
t_{SARD}	Setup addr to read (RDB,DSB) assert	10		ns
t_{SCSRD}	Setup chip select (CSN,RWB) to read (RDB,DSB) assert	5		ns
t_{HCSRD}	Hold chip select (CSN,RWB) from read (RDB,DSB) deassert	5		ns
t_{VRD}	Valid read (RDB,DSB) pulse width	50		ns
t_{VDRDY}	Valid data from RDYB/DTACKB assert		10	ns
t_{HADRD}	Hold addr from read (RDB,DSB) deassert	4		ns
t_{VRDYRD}	Valid RDYB,DTACKB from read (RDB,DSB) assert		15	ns
t_{ZRDYRD}	Tri-state RDYB,DTACKB from read (RDB,DSB) deassert	10		ns
t_{HDRD}	Hold data from read (RDB,DSB) deassert	15		ns

10.18 Microprocessor Interface Write Timing (Synchronous Mode)



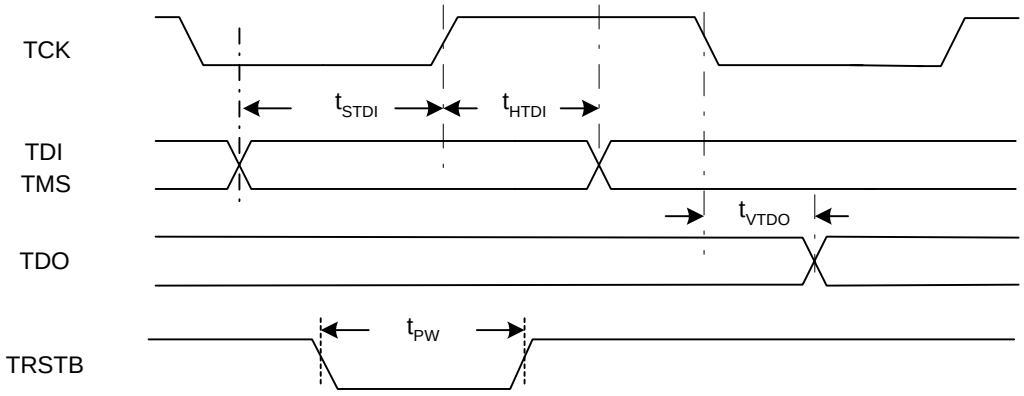
Label	Parameter	Min	Nom	Max	Units
Freq.	uPCLK	25		52	MHz
t_{SWR}	Setup time w.r.t. uPCLK	6			ns
t_{HWR}	Hold time w.r.t. uPCLK	2			ns
t_{PWR}	RDYB, DTACKB propagation delay w.r.t. uPCLK	5		11	ns
t_{PRDT}	Propagation delay w.r.t. CSN asserted			20	ns
t_{PRDTTS}	Propagation delay to tri-state			20	ns

10.19 Microprocessor Interface Read Timing (Synchronous Mode)



Label	Parameter	Min	Nom	Max	Units
Freq.	uPCLK	25		52	MHz
t_{SRD}	Setup time w.r.t. uPCLK	6			ns
t_{HRD}	Hold time w.r.t. uPCLK	2			ns
t_{PRD}	Propagation delay w.r.t. uPCLK	5		11	ns
t_{PRDT}	Propagation delay w.r.t. CSN asserted			20	ns
t_{PRDTTS}	Propagation delay to tri-state			20	ns

10.20 JTAG Interface Timing



Label	Parameter	Min	Max	Units
Freq.	TCK		1	MHz
t_{STDI}	TDI, TMS setup time w.r.t. TCK	50		ns
t_{HTDI}	TDI, TMS hold time w.r.t. TCK	50		ns
t_{VTDO}	TDO output propagation time w.r.t. TCK	2	50	ns
t_{PW}	TRSTB pulse width	200		ns

11.0 Mechanical Packaging Information

The Missouri is packaged in a 624 CBGA package.

Notes:
1. Mechanical drawing is not to scale.
2. Square outline conforms to JEDEC MO-156.

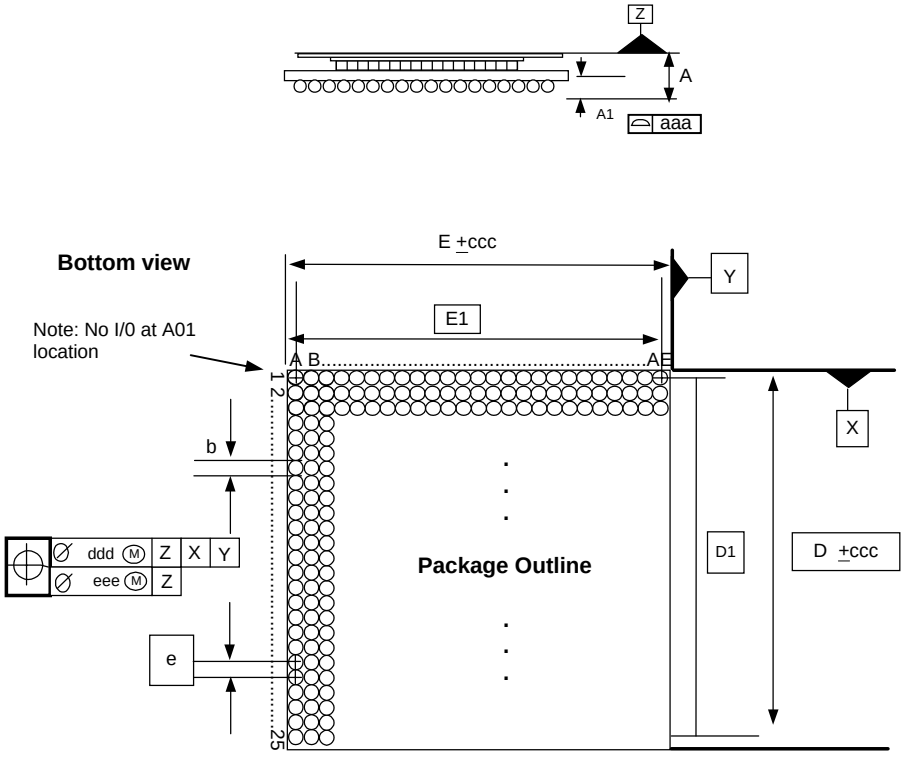


Table 31. Mechanical Specifications

Dimensions	Dimensions and Tolerances	
A (DLA)	Min[2]	4.92
	Max[3]	5.52
A1	Nom	0.90
b	Min	0.82
	Max	0.93
e	Basic	1.27
aaa		0.15
ccc		0.20
ddd		0.30
eee		0.10
D		32.50
D1		30.48
E		32.50
E1		30.48
M[4]		25 x 25

1. All Dimensions are in millimeters
2. Minimum package thickness is calculated using the nominal thickness of all parts. The nominal thickness of a 8-layer package was used for the package thickness.
3. Maximum package thickness is calculated using the nominal thickness of all parts. The nominal thickness of a 12-layer package was used for the package thickness.
4. M = the I/O matrix size.
5. Device is depopulated by 1 I/O at the A01 corner of the array.

Table 32. Thermal Performance

Theta $_{JC}$(^{o}C/W)	Thermal Performance Theta $_{JA}$(^{o}C/W) @ Airflow					
	0 FPM	100 FPM	200 FPM	300 FPM	400 FPM	600 FPM
.47	11.8	10.6	9.4	8.5	7.7	6.7

Table 33. Ordering Information

Part Number	Package Description
S4802CBI12	624 Ceramic Ball Grid Array (CBGA)

12.0 DC Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Level	Units
Supply Voltage on VDD_3.3	-0.6 to 4.75	V
Supply Voltage on VDD_2.5	-0.6 to 3.60	V
Supply current on VDD_3.3	0.24	A
Supply current on VDD_2.5	2.80	A
Power Dissipation	8.5	W
Operating Temperature	-40 to 85	^{o}C
Storage Temperature	-65 to 150	^{o}C
Junction Temperature	125	^{o}C
Voltage on any pin (LVTTL)	-0.6 to 4.2	V
Voltage on any pin (LVCMOS)	-0.6 to 3.6	V
Voltage on any pin (LVDS)	0 to 3.6	V
Voltage on any pin (LVPECL)	0 to 3.6	V
Static Discharge Protection	3000	kV

Note: Exposure to these values for extended periods of time may effect device reliability.

12.2 Power Supply

Label	Parameter	Min	Nom	Max	Units
VDD_3.3	3.3 V Power Supply Voltage	3.135	3.3	3.465	V
ICC_3.3	3.3 V Power Supply Current		0.55		A
VDD_2.5	2.5 V Power Supply Voltage	2.375	2.5	2.625	V
ICC_2.5	2.5 V Power Supply Current		1.68		A

12.3 LVTTL I/O Specifications

Label	Parameter	Min	Nom	Max	Units	Comments
V_{OH}	Output Voltage High	2.4		*	V	Max V_{OH} = VDD_3.3 + 0.3V
V_{OL}	Output Voltage Low			0.4	V	
V_{IH}	Input Voltage High	2.0		*	V	Max V_{IH} = VDD_3.3 + 0.6V
V_{IL}	Input Voltage Low	0		0.8	V	
I_{OH}	Output Current High	9 12 19 40			mA	65 Ohm Driver 50 Ohm Driver 35 Ohm Driver 20 Ohm Driver
I_{OL}	Output Current Low	6 8 12 25			mA	65 Ohm Driver 50 Ohm Driver 35 Ohm Driver 20 Ohm Driver

12.4 LVCMOS I/O Specifications

Label	Parameter	Min	Nom	Max	Units	Comments
V_{OH}	Output Voltage High	2.0		*	V	Max V_{OH} = VDD_2.5 + 0.6V
V_{OL}	Output Voltage Low			0.4	V	
V_{IH}	Input Voltage High	1.7		*	V	Max V_{IH} = VDD_2.5 + 0.6V
V_{IL}	Input Voltage Low	0		0.7	V	
I_{OH}	Output Current High	5 7 10 19			mA	65 Ohm Driver 50 Ohm Driver 35 Ohm Driver 20 Ohm Driver
I_{OL}	Output Current Low	7 9 13 26			mA	65 Ohm Driver 50 Ohm Driver 35 Ohm Driver 20 Ohm Driver

12.5 LVDS I/O Specifications

Label	Parameter	Min	Nom	Max	Units	Comments
V_{IH}	Input Voltage High			VDD_2.5 +0.4	V	On chip 100 Ohm Terminator. See Figure 5.
V_{IL}	Input Voltage Low	-0.4			V	On chip 100 Ohm Terminator. See Figure 5.
V_{ICM}	Input Common Mode Voltage	0		VDD_2.5	V	See Figure 5.
ΔVindiff	Diff. Delta input voltage	0.2			V	Peak-to-Peak Differential.
ΔVinsingle	Single Ended Delta input voltage	0.1			V	Peak-to-Peak Single-Ended. See Figure 5.
R_I	Input Impedance	80	100	120	ohm	Differential Input Impedance
V_{OH}	Output Voltage High	1.34	1.45	1.557	V	See Figure 4.
V_{OL}	Output Voltage Low	0.96	1.05	1.12	V	See Figure 4.
ΔVoutdiff	Diff. Delta output voltage	676	808	960	mV	Peak-to-Peak Differential
ΔVoutsingle	Single Ended Delta output voltage	338	404	480	mV	Peak-to-Peak Single-Ended. See Figure 4.
R_O	Output Impedance	66	-	125	ohm	Differential Output Impedance

12.6 LVPECL I/O Specifications

Label	Parameter	Min	Nom	Max	Units	Comments
V_{IH}	Input Voltage High			VDD_2.5 +0.4	V	On chip 100 Ohm Terminator. See Figure 5.
V_{IL}	Input Voltage Low	-0.4			V	On chip 100 Ohm Terminator. See Figure 5.
V_{ICM}	Input Common Mode Voltage	0		VDD_2.5	V	See Figure 5.
ΔVindiff	Diff. Ended Delta input voltage	0.2			V	Peak-to-Peak Differential
ΔVinsingle	Single Ended Delta input voltage	0.1			V	Peak-to-Peak Single-Ended. See Figure 5.
R_I	Input Impedance	80	100	120	ohm	Differential Input Impedance
V_{OH}	Output Voltage High	VDD_3.3-1.15		VDD_3.3-.70	V	See Figure 4.
V_{OL}	Output Voltage Low	VDD_3.3-1.950		VDD_3.3-1.465	V	See Figure 4.
ΔVoutdiff	Diff. Delta output voltage	1.18	1.62	2.12	V	Peak-to-Peak Differential
ΔVoutsingle	Single Ended Delta output voltage	.59	0.81	1.06	V	Peak-to-Peak Single-Ended. See Figure 4.
R_O	Output Impedance	50	60	70	ohm	Differential Output Impedance

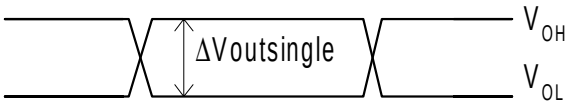


Figure 4. LVDS and LVPECL Outputs

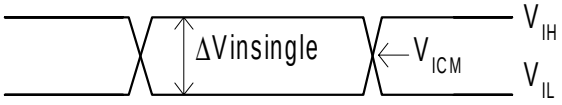


Figure 5. LVDS and LVPECL Inputs

13.0 Register Map and Descriptions

The following sections describe the register bits accessible through the Microprocessor interface. Register addresses that contain at least 1 but fewer than 16 bits (shown as blank bit fields in the tables) return 0 in the undefined bit fields when read. The Missouri data output response to read requests of register addresses that are not shown in the tables is not defined.

When the registers in the following tables are reset, they are forced low (logic 0), unless stated otherwise.

13.1 Register Map Descriptions

13.1.1 Multiplex Common Provisioning and Summary Status (0x0000 - 0x01FF)

13.1.1.1 Software Reset - Addr 0x0000

When the **MX_PROV_RESET** bit is written to a 1, all multiplex side provisioning (read/write) registers (except the byte containing the **MX_PROV_RESET** bit) are reset. These registers are held in their default state until **MX_PROV_RESET** is written to 0 or a hardware reset occurs. These registers include all mux side provisioning and mask registers, but do not include delta, event, or second event bits.

When the **MX_STATE_RESET** bit is written to a 1, all mux side status, monitoring, delta, event, second event and counter registers (the read only registers) and all mux side state machines are reset to their default states. This group should consist of all registers NOT reset by **MX_PROV_RESET**. The mux side of the core remains inactive until the **MX_STATE_RESET** bit is written to 0 (or a hardware reset occurs). The byte containing the **MX_STATE_RESET** bit is not reset by this operation.

The **CNT_LOAD** register bit is used for testing only to preload performance-monitoring counters. When **CNT_LOAD** transitions from 0 to 1, the following registers are preloaded to the specified values:

Table 34. Preload Values When CNT_LOAD Is Set

Register	Value
MX/DX_B1_ERRCNT_[15:0]	0xFFE0
MX/DX_B2_ERRCNT_[21:0]	0x3FFF80
MX/DX_M1_ERRCNT_[21:0]	0x3FFF80
MX/DX_PI_POSCNT_x_[7:0]	0x1C
MX/DX_PG_POSCNT_x_[7:0]	0x1C
MX/DX_PI_NEGCNT_x_[7:0]	0x1C
MX/DX_PG_NEGCNT_x_[7:0]	0x1C

13.1.1.2 Device Version Number - Addr 0x0001

The device version number, **DEV_VER_[7:0]**. **See User Note 14.1.7.1 for important information.**

13.1.1.3 Summary Interrupt - Addr 0x0002

The **MX_SUM_INT** bit is high (logic 1) if any of its contributing bits is high and the corresponding Mask bit is low. On reset, the **MX_SUM_INT** bit is low, because all mask bits are all forced high and all delta and event bits are forced low on reset.

The logic equation for **MX_SUM_INT** is:

MX_SUM_INT = (**MX_TOH_SUMD_[1]** && !**MX_TOH_SUMD_[1]_MASK**) ||
(**MX_TOH_SUMD_[2]** && !**MX_TOH_SUMD_[2]_MASK**) || ... ||
(**MX_TOH_SUMD_[16]** && !**MX_TOH_SUMD_[16]_MASK**) ||
(**MX_TOH_SECE_SUM_[1]** && !**MX_TOH_SECE_SUM_[1]_MASK**) || ... ||
(**MX_TOH_SECE_SUM_[16]** && !**MX_TOH_SECE_SUM_[16]_MASK**) ||
(**MX_PTR_INT_CONCAT_SUMD**&& !**MX_PTR_INT_CONCAT_SUMD_MASK**) ||
(**MX_PTR_INT_PAIS_SUMD** && !**MX_PTR_INT_PAIS_SUMD_MASK**) ||
(**MX_PTR_INT_LOP_SUMD** && !**MX_PTR_INT_LOP_SUMD_MASK**) ||
(**MX_PTR_INT_JUSCNT_SECE_SUM** && !**MX_PTR_INT_JUSCNT_SECE_SUM_MASK**) ||
(**MX_PTR_GEN_JUSCNT_SECE_SUM** && !**MX_PTR_GEN_JUSCNT_SECE_SUM_MASK**) ||
(**MX_PTR_GEN_FIFO_SUME** && !**MX_PTR_GEN_FIFO_SUME_MASK**) ||
(**MX_APS_PROT_PRTY_E** && !**MX_APS_PROT_PRTY_E_MASK**) ||
(**MX_PROT_FIFO_ERR_E** && !**MX_PROT_FIFO_ERR_E_MASK**) ||
(**GPIO_SUMD** && !**GPIO_SUMD_MASK**)

The **MX_APS_INT_[i]** bit is high (logic 1) if any of its contributing delta bits are high and the corresponding Mask bit is low. On reset, the **MX_APS_INT_[i]** bits are low, because all mask bits are all forced high and all delta bits are forced low on reset.

The logic equation for **MX_APS_INT_[i]** is:

MX_APS_INT_[i] = (**MX_K1_[i]_D** && !**MX_K1_[i]_D_MASK**) ||
(**MX_K2_[i]_D** && !**MX_K2_[i]_D_MASK**) ||
(**MX_K1_UNSTAB_[i]_D** && !**MX_K1_UNSTAB_[i]_D_MASK**)|

13.1.1.4 Interrupt Mask - Addr 0x000E

The **MX_SUM_INT_MASK** bit is used to disable the Multiplex side contribution to the Missouri interrupt output *(INTB)*. If **MX_SUM_INT_MASK** is set (logic 1), then the *INTB* output is held low (logic 0). **MX_SUM_INT_MASK** is set upon device reset.

13.1.1.5 Summary Status and Masks - Addr 0x0007 through 0x000B and 0x0010 through 0x0017

The summary delta and summary event bits contribute to the **MX_SUM_INT** bit if their corresponding mask bits are not set. The tributary mask bits are used to mask delta and event bits associated with the Pointer Processor. On reset, all mask bits are set high, and all delta and event bits are forced low.

The **MX_TOH_SUMD_[i]** bits are a function of the Multiplexer TOH/SOH delta bits and their respective masks bits. The logic equations for these bits are:

MX_TOH_SUMD_[i] = (**MX_LOS_[i]_D** && !**MX_LOS_[i]_D_MASK**) ||
(**MX_LOC_[i]_D** && !**MX_LOC_[i]_D_MASK**) ||
(**MX_OOF_[i]_D** && !**MX_OOF_[i]_D_MASK**) ||
(**MX_LOF_[i]_D** && !**MX_LOF_[i]_D_MASK**) ||
(**MX_J0_OOF_[i]_D** && !**MX_J0_OOF_[i]_D_MASK**) ||

(**MX_J0_[i]_D** && !**MX_J0_[i]_D_MASK**) ||

(**MX_B2_ERR_SF_[i]_D** && !**MX_B2_ERR_SF_[i]_D_MASK**) ||

(**MX_B2_ERR_SD_[i]_D** && !**MX_B2_ERR_SD_[i]_D_MASK**) ||

(**MX_LAIS_[i]_D** && !**MX_LAIS_[i]_D_MASK**) ||

(**MX_LRDI_[i]_D** && !**MX_LRDI_[i]_D_MASK**) ||

(**MX_K1_[i]_D** && !**MX_K1_[i]_D_MASK**) ||

(**MX_K1_UNSTAB_[i]_D** && !**MX_K1_UNSTAB_[i]_D_MASK**) ||

(**MX_K2_[i]_D** && !**MX_K2_[i]_D_MASK**) ||

(**MX_S1_[i]_D** && !**MX_S1_[i]_D_MASK**)||

(**MX_LOSEXT_[i]_D** && !**MX_LOSEXT_[i]_D_MASK**)

The **MX_TOH_SECE_SUM_[i]** bits are a function of the Multiplexer TOH/SOH second event bits and their respective masks bits. The logic equations for these bits are:

MX_TOH_SECE_SUM_[i] = (**MX_OOF_[i]_SECE** && !**MX_OOF_SECE_[i]_MASK**) ||

(**MX_LOF_[i]_SECE** && !**MX_LOF_[i]_SECE_MASK**) ||

(**MX_B1ERR_[i]_SECE** && !**MX_B1ERR_[i]_SECE_MASK**) ||

(**MX_B2ERR_[i]_SECE** && !**MX_B2ERR_[i]_SECE_MASK**) ||

(**MX_S1FAIL_[i]_SECE** && !**MX_S1FAIL_[i]_SECE_MASK**) ||

(**MX_M1ERR_[i]_SECE** && !**MX_M1ERR_[i]_SECE_MASK**)

MX_PTR_INT_CONCAT_SUMD are a function of the Pointer Interpreter delta bits and the concatenation masks. The logic equation for this bit is:

MX_PTR_INT_CONCAT_SUMD = (**MX_CONCAT_[19]_D** && !**MX_CONCAT_[19]_D_MASK**) ||

(**MX_CONCAT_[18]_D** && !**MX_CONCAT_[18]_D_MASK**) ||

(**MX_CONCAT_[17]_D** && !**MX_CONCAT_[17]_D_MASK**) ||

(**MX_CONCAT_[16]_D** && !**MX_CONCAT_[16]_D_MASK**) ||...||

(**MX_CONCAT_[1]_D** && !**MX_CONCAT_[1]_D_MASK**) ||

(**MX_CONCAT_[0]_D** && !**MX_CONCAT_[0]_D_MASK**)

MX_PTR_INT_PAIS_SUMD is a function of the Pointer Interpreter delta bits and the tributary masks. The logic equation for this bit is:

MX_PTR_INT_PAIS_SUMD = (**MX_PAIS_[1]_[1]_D** && !**MX_TRIB_MASK_[1]_[1]**) ||

(**MX_PAIS_[1]_[2]_D** && !**MX_TRIB_MASK_[1]_[2]**) ||

(**MX_PAIS_[1]_[3]_D** && !**MX_TRIB_MASK_[1]_[3]**) ||

(**MX_PAIS_[2]_[1]_D** && !**MX_TRIB_MASK_[2]_[1]**) ||

(**MX_PAIS_[2]_[2]_D** && !**MX_TRIB_MASK_[2]_[2]**) ||

... || (**MX_PAIS_[16]_[1]_D** && !**MX_TRIB_MASK_[16]_[1]**) ||

(**MX_PAIS_[16]_[2]_D** && !**MX_TRIB_MASK_[16]_[2]**) ||

(**MX_PAIS_[16]_[3]_D** && !**MX_TRIB_MASK_[16]_[3]**)

MX_PTR_INT_LOP_SUMD are a function of the Pointer Interpreter delta bits and the tributary masks. The logic equation for this bit is:

MX_PTR_INT_LOP_SUMD = (**MX_LOP_[1]_[1]_D** && !**MX_TRIB_MASK_[1]_[1]**) ||

(**MX_LOP_[1]_[2]_D** && !**MX_TRIB_MASK_[1]_[2]**) ||

(**MX_LOP_[1]_[3]_D** && !**MX_TRIB_MASK_[1]_[3]**) ||

(**MX_LOP_[2]_[1]_D** && !**MX_TRIB_MASK_[2]_[1]**) ||

(**MX_LOP_[2]_[1]_D** && !**MX_TRIB_MASK_[2]_[2]**) ||

... || (**MX_LOP_[16]_[1]_D** && !**MX_TRIB_MASK_[16]_[1]**) ||

(**MX_LOP_[16]_[2]_D** && !**MX_TRIB_MASK_[16]_[2]**) ||

(**MX_LOP_[16]_[3]_D** && !**MX_TRIB_MASK_[16]_[3]**)

MX_PTR_INT_JUSCNT_SECE_SUM is a function of the Pointer Interpreter event bits and the tributary masks. The logic equation for this bit is:

MX_PTR_INT_JUSCNT_SECE_SUM =

((**MX_PI_POSCNT_SECE_[1]_[1] || MX_PI_NEGCNT_SECE_[1]_[1]**) &&
!**MX_TRIB_MASK_[1]_[1])||**

((**MX_PI_POSCNT_SECE_[1]_[2]** || **MX_PI_NEGCNT_SECE_[1]_[2]**) &&
!**MX_TRIB_MASK_[1]_[2]**) ||

((**MX_PI_POSCNT_SECE_[1]_[3]** || **MX_PI_NEGCNT_SECE_[1]_[3]**) &&
!**MX_TRIB_MASK_[1]_[3]**) ||

((**MX_PI_POSCNT_SECE_[2]_[1]** || **MX_PI_NEGCNT_SECE_[2]_[1]**) &&
!**MX_TRIB_MASK_[2]_[1]**) ||

((**MX_PI_POSCNT_SECE_[2]_[1]** || **MX_PI_NEGCNT_SECE_[2]_[1]**) &&
!**MX_TRIB_MASK_[2]_[1]**) ||

... || ((**MX_PI_POSCNT_SECE_[16]_[1]** || **MX_PI_NEGCNT_SECE_[16]_[1]**) &&
!**MX_TRIB_MASK_[16]_[1]**) ||

((**MX_PI_POSCNT_SECE_[16]_[2]** && || **MX_PI_NEGCNT_SECE_[16]_[2]**)
!**MX_TRIB_MASK_[16]_[2]**) ||

((**MX_PI_POSCNT_SECE_[16]_[3]** || **MX_PI_NEGCNT_SECE_[16]_[3]**) &&
!**MX_TRIB_MASK_[16]_[3]**)

MX_PTR_GEN_JUSCNT_SECE_SUM is a function of the Pointer Generator event bits and the tributary masks. The logic equation for this bit is:

MX_PTR_GEN_JUSCNT_SECE_SUM =

((**MX_PG_POSCNT_SECE_[1]_[1]** || **MX_PG_NEGCNT_SECE_[1]_[1]**) &&
!**MX_TRIB_MASK_[1]_[1]**) ||

((**MX_PG_POSCNT_SECE_[1]_[2]** || **MX_PG_NEGCNT_SECE_[1]_[2]**) &&
!**MX_TRIB_MASK_[1]_[2]**) ||

((**MX_PG_POSCNT_SECE_[1]_[3]** || **MX_PG_NEGCNT_SECE_[1]_[3]**) &&
!**MX_TRIB_MASK_[1]_[3]**) ||

((**MX_PG_POSCNT_SECE_[2]_[1]** || **MX_PG_NEGCNT_SECE_[2]_[1]**) &&
!**MX_TRIB_MASK_[2]_[1]**) ||

((**MX_PG_POSCNT_SECE_[2]_[2]** || **MX_PG_NEGCNT_SECE_[2]_[2]**) &&
!**MX_TRIB_MASK_[2]_[2]**) ||

... || ((**MX_PG_POSCNT_SECE_[16]_[1]** || **MX_PG_NEGCNT_SECE_[16]_[1]**) &&
!**MX_TRIB_MASK_[16]_[1]**) ||

((**MX_PG_POSCNT_SECE_[16]_[2]** && || **MX_PG_NEGCNT_SECE_[16]_[2]**)
!**MX_TRIB_MASK_[16]_[2]**) ||

((**MX_PG_POSCNT_SECE_[16]_[3]** || **MX_PG_NEGCNT_SECE_[16]_[3]**) &&
!**MX_TRIB_MASK_[16]_[3]**)

MX_PTR_GEN_FIFO_SUME is a function of the Pointer Generator event bits and the tributary masks. The logic equation for this bit is:

MX_PTR_GEN_FIFO_SUME =

((**MX_PG_FIFO_[1]_[1]_E**) && !**MX_TRIB_MASK_[1]_[1]**) ||
((**MX_PG_FIFO_[1]_[2]_E**) && !**MX_TRIB_MASK_[1]_[2]**) ||
((**MX_PG_FIFO_[1]_[3]_E**) && !**MX_TRIB_MASK_[1]_[3]**) ||
((**MX_PG_FIFO_[2]_[1]_E**) && !**MX_TRIB_MASK_[2]_[1]**) ||
((**MX_PG_FIFO_[2]_[2]_E**) && !**MX_TRIB_MASK_[2]_[2]**) ||
... || ((**MX_PG_FIFO_[16]_[1]_E**) && !**MX_TRIB_MASK_[16]_[1]**) ||
((**MX_PG_FIFO_[16]_[2]_E**) !**MX_TRIB_MASK_[16]_[2]**) ||
((**MX_PG_FIFO_[16]_[3]_E**) && !**MX_TRIB_MASK_[16]_[3]**)

GPIO_SUMD is a function of the General Purpose I/O delta bits and their masks. The logic equation for this bit is:

GPIO_SUMD = (**GPIO0_D** && !**GPIO0_MASK**) ||
(**GPIO1_D** && !**GPIO1_MASK**) || ...||
(**GPIO15_D** && !**GPIO15_MASK**)

If a parity event occurs the **MX_APS_PROT_PRTY_E** register bit is set. The **MX_APS_PROT_PRTY_E** bit can be masked by setting the **MX_APS_PROT_PRTY_E_MASK** bit.

13.1.1.6 Mux Configuration registers - Addr 0x0018 through 0x01FF

If **MX_LINE_CONFIG_[4]**=1, the Missouri interfaces on it “Low-Speed” side to an STS-48/STM-16 signal. If **MX_LINE_CONFIG_[3:0]**=1, then the Missouri interfaces to STS-12/STM-4 signals on quadrant 1-4, respectively, otherwise it interfaces to STS-3/STM-1 signals.

LOF_INH is a test feature that disables the contribution of LOF to creation of downstream AIS-P, for faster initialization of the device during simulation. It should be left at its default value of 0 for normal operation.

If the **MX_APS_PROT_PRTY_OUT** bit is high, even parity is used for the outgoing *MX_PROT_PRTY_OUT*, else it is odd.

DX_TO_MX_LS_LOOP_[i] controls the loopback of the Demux side to the Mux side at the Low Speed interface. The default mode of operation is to have this loopback disabled (**DX_TO_MX_LS_LOOP_[i]** = 0). For an STS-48 interface, **DX_TO_MX_LS_LOOP_[1]** controls the loopback of the entire signal.

The **MX_CONFIG_[20:0]** and **MX_CONFIG_AUTO** registers determine the structure of the generated signal.

If **MX_CONFIG_AUTO =** 1 the **MX_CONFIG_[20:0]** is ignored.

When **RX_REF_CLK_FREQ_[1:0]** = 00, 01, 10 and 11, the *RX_REF_CLK_OUT* signal operates at 8 kHz, 19.44 MHz, 38.88 MHz and 77.76 MHz respectively. **RX_REF_CLK_SEL_[4:0]** selects the clock source (see section 3.11).

MX_IN_INH_[i] disables *MX_DATA_IN_[i]* and *MX_CLK_IN_[i]*. **MX_OUT_INH** inhibits *MX_DATA_OUT* and *MX_CLK_OUT*. **MX_PROT_OUT_INH** inhibits *MX_PROT_DATA_OUT, MX_PROT_SYNC_OUT, MX_PROT_PRTY_OUT* and *MX_PROT_CLK_OUT* (LVDS). **MX_PROT_IN_INH** inhibits *MX_PROT_DATA_IN, MX_PROT_SYNC_IN, MX_PROT_PRTY_IN* and *MX_PROT_CLK_IN* (see section 3.12).

The **MUXSEL_x_[7:0]** bits are used to select the data streams that feed the mux frame generation blocks.

The **MX_BIT_BLKCNT_[i]** bit provisions performance-monitoring counters to count bit errors or block errors.

13.1.1.7 General Purpose I/O Deltas, Masks, Status, Control, Parity Error Masks - Addr 0x001C

through 0x0023

GPIO0 through **GPIO15** contain General Purpose Input/Output register that are tied directly to Missouri pins *GPIO0* through *GPIO15*. These are grouped in blocks of 2 in the register maps, each group of 2 is controlled by a **GPIOCTLx** register.

GPIOCTL1 = 1 designates that **GPIO0** and **GPIO1** are to be General Purpose Inputs, else they are outputs.

GPIOCTL2 = 1 designates that **GPIO2** and **GPIO3** are to be General Purpose Inputs, else they are outputs.

GPIOCTL3 = 1 designates that **GPIO4** and **GPIO5** are to be General Purpose Inputs, else they are outputs.

GPIOCTL4 = 1 designates that**GPIO6** and **GPIO7** are to be General Purpose Inputs, else they are outputs.

GPIOCTL5 = 1 designates that **GPIO8** and **GPIO9** are to be General Purpose Inputs, else they are outputs.

GPIOCTL6 = 1 designates that **GPIO10** and **GPIO11** are to be General Purpose Inputs, else they are outputs.

GPIOCTL7 = 1 designates that **GPIO12** and **GPIO13** are to be General Purpose Inputs, else they are outputs.

GPIOCTL8 = 1 designates that **GPIO14** and **GPIO15** are to be General Purpose Inputs, else they are outputs.

If **GPIOx** is provisioned as an input, the **GPIOx_D** delta bit is written to 1 whenever there is a change in **GPIOx**.

See User Note 14.1.8.2 for important information.

13.1.2 Multiplexer Side (0x0200 - 0x05FF)

13.1.2.1 TOH/SOH Deltas, Second Events, and Masks - Addr 0x0200 through 0x0206

The delta and second event bits contribute to the **MX_TOH_SUMD_[i]** and **MX_TOH_SECE_SUM_[i]** summary status bits in registers 0x1007-0x100B. The contribution of any of the bits can be removed by setting the corresponding mask bit. On reset, the delta and second event bits are cleared, and the mask bits are set high.

13.1.2.2 TOH/SOH Provisioning - Addr 0x0208 through 0x020B

The **MX_K2_CONSEC_[i]** register is used in monitoring the received K2 byte (see section 4.4.4). On reset this register is set to “0101” (decimal 5). Note that **MX_K2_CONSEC_[i]** is only defined for values between 2-15.

The **MX_LOF_ALG_[i]** bit determines which of 2 algorithms is used to clear the **MX_LOF_[i]** status bit. Descrambling is inhibited if **MX_DSCRINH_[i]** is high (see section 3.3.1). On reset, these bits are cleared.

MX_LOS_INH_[i] controls the LOS contribution to LRDI and PAIS. **MX_LOSEXT_LEVEL_[i]** controls the polarity of its external input signal, *MX_LOSEXT_[i]* (see section 4.9.3.7).

MX_LOSEXT_INH_[i], MX_LOSEXT_DELAY_INH_[i], MX_LOS_ALL_ZERO_INH_[i] control the contributors to the LOS monitor (see section 4.2.2).

MX_SDH_J0_[i] and **MX_SDH_S1_[i]** determine whether the multiplexer side performs J0 and S1 processing in SONET or SDH mode (see section 4.4).

MX_OOF/LOF/LOC/LAIS/LOS_ALARM_INH_[i] registers determine which alarms (OOF, LOF, LAIS, LOC, or LOS) contribute to the *MX_ALARM_OUT_[i]* pins (see section 4.5.2).

13.1.2.3 TOH/SOH Status - Addr 0x020C through 0x0223

The bits in these registers hold the current state of the TOH/SOH Receiver Monitor (see sections 3.4 through section 4.4). On reset, all bits in these registers are cleared, except for **MX_OOF_[i]**, **MX_LOF_[i]**, **MX_B2_ERR_SF_[i]**, and **MX_B2_ERR_SD_[i]**.

13.1.2.4 B2 Signal Fail and Signal Degrade Parameters - Addr 0x0224 through 0x022F

These registers contain the algorithm parameters for the B2 based Signal Fail and Signal Degrade Monitors (see section 3.4.3.2). On reset, all of the parameter values are set to decimal 1.

13.1.2.5 B1, B2, and M1 Error Counters - Addr 0x0230 through 0x023A

These registers contain the latched results of error counters (see section 3.4.1, section 3.4.3, and section 4.4.6). On reset, these registers are cleared.

The SONET/SDH TOH/SOH Monitoring register map for SONET/SDH signal [1] is illustrated in Table 37. Identical maps exist for Signals [2], [3] ... [16].

13.1.3 Multiplexer Side (0x0600 - 0x07FF)

13.1.3.1 Pointer Interpreter Provisioning - Addr 0x0602 and 0x0606

The **MX_CONCAT_[20:0]_D** bits are set to 1 whenever there is a change of their associated status bits. The **MX_CONCAT_[20:0]_D_MASK** bits are set to 1 to disable the contribution of the associated delta bit to the **MX_PTR_INT_CONCAT_SUMD** interrupt.

13.1.3.2 Pointer Interpreter Provisioning - Addr 0x0704

The **MX_SS_EN_[i]** bits determine whether or not the SS-bits are used in the Pointer Interpreter algorithms (see sections 3.6.2 and 3.6.3). **MX_SDH_PI_[i]** determine whether the Receive Side performs SONET or SDH pointer interpretation (see section 3.6.3).

13.1.3.3 Pointer Interpreter Status - Addr 0x0608

The **MX_CONCAT_[20:0]** bits report the received signal configuration as indicated by the H1H2 bytes (see section 3.6.1).

13.1.3.4 Pointer Interpreter Deltas - Addr [0x0700,0x07F0]

The delta bits contribute to the **MX_PTR_INT_PAIS_SUMD** and **MX_PTR_INT_LOP_SUMD** summary status bits (see section 3.6.2). On reset, the delta bits are cleared.

13.1.3.5 Pointer Interpreter Status - Addr [0x0704-8,0x07F4-8]

These registers hold the current state of the Pointer Interpreter (see section 3.6.2). On reset, **MX_LOP_x**, **MX_PAIS_x**, and both bits of **MX_PTR_STATE_x_[1:0]**, for x = [1,1], [5,1], [9,1], and [13,1] are cleared, and all bits of the 44 remaining **MX_PTR_STATE_x_[1:0]** are also cleared, indicating 16 STS-3c or AU-4 normal pointers.

13.1.4 Multiplexer Side (0x0900 - 0x09FF)

13.1.4.1 Pointer Generator Deltas - Addr [0x0900, 0x09F0] and [0x0902,0x09F2]

If a FIFO overflows or underflows, the **MX_PG_FIFO_x_E** event bit is set. The FIFO is then recentered, and the Pointer Generator continues normal operation.

If for tributary x, there has been at least 1 positive or negative justification in the previous second, the **MX_PG_POSCNT_SECE_x** or **MX_PG_NEGCNT_SECE_x** bit is set.

13.1.4.2 Pointer Generator Provisioning - Addr [0x0904, 0x09F4] and [0x0905,0x09F5]

If **MX_FAST_AIS_x** = 1 and the last frame received for tributary **x** contained only H-bytes, the Missouri inserts PAIS for tributary **x**. **MX_SF_PAIS_INH_[i]** controls the SF contribution to PAIS insertion.

MX_SDH_PG_[i] is used to select between SDH (1) and SONET (0) modes for pointer generation (see section 3.6.4.2).

The user may force PAIS generation for tributary **x** by setting **MX_PAIS_GEN_x** = 1 (if tributary **x** is in operation based on the value of **MX_CONCAT** or **MX_CONFIG** (see section 3.6.2.2).

The Pointer Generators can also insert Unequipped. If **MX_PAIS_GEN_x** = 0, and **MX_UNEQ_GEN_x** = 1, the entire SPE/VC is generated with all-0s.

13.1.4.3 Pointer Generator Provisioning - Addr [0x0908-D, 0x09F8-D]

The Pointer Processors contain 5-bit pointer generator justification counters that count every positive or negative justification. When the performance-monitoring counters are latched, the values of these counters are latched to the **MX_PG_POSCNT_x_[4:0]** and **MX_PG_NEGCNT_x_[4:0]** registers, and the justification counters are cleared.

13.1.5 Multiplexer Side (0x0A00 - 0x0A1F)

MX_A1A2_ERR, **MX_A1A2_ERR_PAT_[15:0]**, **MX_A1A2_ERR_NUM_[2:0]**, **MX_B1_INV**, **MX_B2_INV**, and **MX_M1_ERRCNT_[i]** control the generation of errors in the A1, A2, B1, B2, and M1 bytes in the SONET/SDH signal (see section 4.9.3.1, section 4.9.3.3, section 4.9.3.6, and section 4.9.3.9).

Automatic generation of LRDI and LREI are inhibited if **MX_LRDI_INH** and **MX_LREI_INH** are high. Scrambling of the SONET/SDH signal is disabled if **MX_SCRINH** is high (see section 4.9.3.7 and section 4.9.4).

If **MX_LAIS_GEN** is high, the entire SONET/SDH signal is generated as all-ones, except for the first three rows of Section Overhead (see section 4.9.3.7).

MX_K1K2_APS and **MX_K2_3LSB** registers are used to select the source of the K1 and K2 bytes; either the register map (0) or the TOH serial channel (1) (see section 4.9.3.4).

The **MX_J0_[15:0]_[7:0]**, **MX_K1GEN_[7:0]**, **MX_K2GEN_[7:0]**, and **MX_S1GEN_[7:0]** registers are used in the generation of J0, K1, K2, and S1 bytes (see section 4.9.3.2, section 4.9.3.7, and section 4.9.3.8).

MX_FRAME_IN_INH enables/inhibits the use of the *SYS_SYNC_IN* signal as the frame sync reference for the Missouri (see section 3.9.1).

13.1.6 Demultiplexer Common Provisioning and Summary Status (0x1000 - 0x11FF)

13.1.6.1 Software Reset - Addr 0x1000

When the **DX_PROV_RESET** bit is written to a 1, all multiplex side provisioning (read/write) registers (except the byte containing the **DX_PROV_RESET** bit) are reset. These registers are held in their default state until **DX_PROV_RESET** is written to 0 or a hardware reset occurs. These registers include all mux side provisioning and mask registers, but do not include delta, event, or second event bits.

When the **DX_STATE_RESET** bit is written to a 1, all mux side status, monitoring, delta, event, second event and counter registers (the read only registers) and all mux side state machines are reset to their default states. This group should consist of all registers NOT reset by **DX_PROV_RESET**. The mux side of the core remains inactive until the **DX_STATE_RESET** bit is written to 0 (or a hardware reset occurs). The byte containing the **DX_STATE_RESET** bit is not reset by this operation. **See User Note 14.1.6.2 for important information.**

The hardware reset input, *RSTB*, produces the same result as writing a 1 to both **DX_PROV_RESET** and **DX_STATE_RESET**, except that the hardware reset forces both **DX_PROV_RESET** and **DX_STATE_RESET** to 0, and the device begins operation when *RSTB* goes high (logic 1).

The **MASTER_RESET** register bit produces the same result as writing a 1 to **MX_** and **DX_PROV_RESET** as well as **MX_** and **DX_STATE_RESET**. The Missouri begins operation when **MASTER_RESET** is written to 0 (or a hardware reset occurs).

The **CNT_LOAD** register bit is used for testing only to preload performance-monitoring counters. When **CNT_LOAD** transitions from 0 to 1, the following registers are preloaded to the specified values:

Table 35. Preload Values When CNT_LOAD Is Set

Register	Value
MX/DX_B1_ERRCNT_[15:0]	0xFFE0
MX/DX_B2_ERRCNT_[21:0]	0x3FFF80
MX/DX_M1_ERRCNT_[21:0]	0x3FFF80
MX/DX_PI_POSCNT_x_[7:0]	0x1C
MX/DX_PG_POSCNT_x_[7:0]	0x1C
MX/DX_PI_NEGCNT_x_[7:0]	0x1C
MX/DX_PG_NEGCNT_x_[7:0]	0x1C

The **LATCH_CNT** register bit can be used to latch **_SECE** registers and to transfer performance-monitoring counter values to holding registers so that they can be read by the Controller (see section 2.3). It is cleared on reset.

Setting **SHORT_FRAME**=1 places the Missouri in a test mode where it produces/processes ‘short’ SONET frames only. This is for device verification only.

13.1.6.2 Summary Interrupt - Addr 0x1002

The **DX_SUM_INT** bit is high (logic 1) if any of its contributing bits is high and the corresponding Mask bit is low. On reset, the **DX_SUM_INT** bit is low, because all mask bits are all forced high and all delta and event bits are forced low on reset.

The logic equation for **DX_SUM_INT** is:

DX_SUM_INT = (**DX_TOH_SUMD** && !**DX_TOH_SUMD_MASK**) ||
(**DX_TOH_SECE_SUM** && !**DX_TOH_SECE_SUM_MASK**) ||
(**DX_PTR_INT_CONCAT_SUMD** && !**DX_PTR_INT_CONCAT_SUMD_MASK**) ||
(**DX_PTR_INT_PAIS_SUMD** && !**DX_PTR_INT_PAIS_SUMD_MASK**) ||
(**DX_PTR_INT_LOP_SUMD** && !**DX_PTR_INT_LOP_SUMD_MASK**) ||
(**DX_PTR_INT_JUSCNT_SECE_SUM** && !**DX_PTR_INT_JUSCNT_SECE_SUM_MASK**) ||
(**DX_PTR_GEN_JUSCNT_SECE_SUM** && !**DX_PTR_GEN_JUSCNT_SECE_SUM_MASK**) ||
(**DX_PTR_GEN_FIFO_SUME** && !**DX_PTR_GEN_FIFO_SUME_MASK**) ||
(**DX_APS_PROT_PRTY_E** && !**DX_APS_PROT_PRTY_E_MASK**) ||
(**DX_PROT_FIFO_ERR_E** && !**DX_PROT_FIFO_ERR_E_MASK**) ||
(**LATCH_E** && !**LATCH_E_MASK**)

The **DX_APS_INT** bit is high (logic 1) if any of its contributing delta bits is high and the corresponding Mask bit is low. On reset, the **DX_APS_INT** bit is low, because all mask bits are all forced high and all delta bits are forced low on reset.

The logic equation for **DX_APS_INT** is:

DX_APS_INT = (**DX_K1_D** && !**DX_K1_D_MASK**) ||
(**DX_K2_D** && !**DX_K2_D_MASK**) ||
(**DX_K1_UNSTAB_D** && !**DX_K1_UNSTAB_D_MASK**)

If a parity event occurs the **DX_APS_PROT_PRTY_E** register bit is set. The **DX_APS_PROT_PRTY_E** bit can be masked by setting the **DX_APS_PROT_PRTY_E_MASK** bit.

The microprocessor is notified via **LATCH_E** when a pulse occurs on LATCH_EVENT.

13.1.6.3 Interrupt Mask - Addr 0x100E through 0x100F

The **DX_SUM_INT_MASK** bit is used to disable the Demultiplex side contribution to the Missouri interrupt output, *INTB*. If it is active (logic 1), the *INTB* output is held low (logic 0). It is set on reset.

When **DX_APS_INT_MASK** =1, it is used to mask the **DX_APS_INT** register bit. The **DX_APS_INT** bit is used on the demultiplex side to contribute to the Missouri interrupt output, *APS_INTB*.

When **LATCH_E_MASK** =1, it is used to mask the **LATCH_E** register bit. The **LATCH_E** is used to contribute to the **DX_SUM_INT** bit.

When **DX_TOH_SUMD_MASK** =1, it is used to mask the **DX_TOH_SUMD** register bit. The **DX_TOH_SUMD** register bit contributes to the **DX_SUM_INT** bit.

When **DX_TOH_SECE_SUM_MASK** = 1, it is used to mask the **DX_TOH_SECE_SUM** register bit. The **DX_TOH_SECE_SUM** register bit contributes to the **DX_SUM_INT** bit.

13.1.6.4 Summary Status and Masks - Addr 0x1008 and 0x1014

The summary delta and summary event bits contribute to the **DX_SUM_INT** bit if their corresponding mask bits are not set. The tributary mask bits are used to mask delta and event bits associated with the Pointer Processor. On reset, all mask bits are set high, and all delta and event bits are forced low.

The **DX_TOH_SUMD** bit is a function of the Multiplexer TOH/SOH delta bits and their respective masks bits. The logic equation for this bit is:

DX_TOH_SUMD = (**DX_LOS_D** && !**DX_LOS_D_MASK**) ||
(**DX_LOC_D** && !**DX_LOC_D_MASK**) ||

(**DX_OOF_D** && !**DX_OOF_D_MASK**) ||
(**DX_LOF_D** && !**DX_LOF_D_MASK**) ||
(**DX_J0_OOF_D** && !**DX_J0_OOF_D_MASK**) ||
(**DX_J0_D** && !**DX_J0_D_MASK**) ||
(**DX_B2_ERR_SF_D** && !**DX_B2_ERR_SF_D_MASK**) ||
(**DX_B2_ERR_SD_D** && !**DX_B2_ERR_SD_D_MASK**) ||
(**DX_LAIS_D** && !**DX_LAIS_D_MASK**) ||
(**DX_LRDI_D** && !**DX_LRDI_D_MASK**) ||
(**DX_K1_D** && !**DX_K1_D_MASK**) ||
(**DX_K1_UNSTAB_D** && !**DX_K1_UNSTAB_D_MASK**) ||
(**DX_K2_D** && !**DX_K2_D_MASK**) ||
(**DX_S1_D** && !**DX_S1_D_MASK**) ||
(**DX_LOSEXT_D** && !**DX_LOSEXT_D_MASK**)

The **DX_TOH_SECE_SUM** bits are a function of the Multiplexer TOH/SOH second event bits and their respective masks bits. The logic equation for this bit is:

DX_TOH_SECE_SUM = (**DX_OOF_SECE** && !**DX_OOF_SECE_MASK**) ||
(**DX_LOF_SECE** && !**DX_LOF_SECE_MASK**) ||
(**DX_B1ERR_SECE** && !**DX_B1ERR_SECE_MASK**) ||
(**DX_B2ERR_SECE** && !**DX_B2ERR_SECE_MASK**) ||
(**DX_S1FAIL_SECE** && !**DX_S1FAIL_SECE_MASK**) ||
(**DX_M1ERR_SECE** && !**DX_M1ERR_SECE_MASK**)

DX_PTR_INT_CONCAT_SUMD is a function of the Pointer Interpreter delta bits and the concatenation masks. The logic equation for this bit is:

DX_PTR_INT_CONCAT_SUMD = (**DX_CONCAT_[20]_D** && !**DX_CONCAT_[20]_D_MASK**) ||
(**DX_CONCAT_[19]_D** && !**DX_CONCAT_[19]_D_MASK**) ||
(**DX_CONCAT_[18]_D** && !**DX_CONCAT_[18]_D_MASK**) ||
(**DX_CONCAT_[17]_D** && !**DX_CONCAT_[17]_D_MASK**) ||
(**DX_CONCAT_[16]_D** && !**DX_CONCAT_[16]_D_MASK**) ||...||
(**DX_CONCAT_[1]_D** && !**DX_CONCAT_[1]_D_MASK**) ||
(**DX_CONCAT_[0]_D** && !**DX_CONCAT_[0]_D_MASK**)

DX_PTR_INT_PAIS_SUMD is a function of the Pointer Interpreter delta bits and the DX tributary masks. The logic equation for this bit is:

DX_PTR_INT_PAIS_SUMD = (**DX_PAIS_[1]_[1]_D** && !**DX_TRIB_MASK_[1]_[1]**) ||
(**DX_PAIS_[1]_[2]_D** && !**DX_TRIB_MASK_[1]_[2]**) ||
(**DX_PAIS_[1]_[3]_D** && !**DX_TRIB_MASK_[1]_[3]**) ||
(**DX_PAIS_[2]_[1]_D** && !**DX_TRIB_MASK_[2]_[1]**) ||
(**DX_PAIS_[2]_[2]_D** && !**DX_TRIB_MASK_[2]_[2]**) ||
... || (**DX_PAIS_[16]_[3]_D** && !**DX_TRIB_MASK_[16]_[3]**) ||

DX_PTR_INT_LOP_SUMD is a function of the Pointer Interpreter delta bits and the DX tributary masks. The logic equation for this bit is:

DX_PTR_INT_LOP_SUMD = (**DX_LOP_[1]_[1]_D** && !**DX_TRIB_MASK_[1]_[1]**) ||

(**DX_LOP_[1]_[2]_D** && !**DX_TRIB_MASK_[1]_[2]**) ||

(**DX_LOP_[1]_[3]_D** && !**DX_TRIB_MASK_[1]_[3]**) ||

(**DX_LOP_[2]_[1]_D** && !**DX_TRIB_MASK_[2]_[1]**) ||

(**DX_LOP_[2]_[2]_D** && !**DX_TRIB_MASK_[2]_[2]**) ||

... || (**DX_LOP_[16]_[3]_D** && !**DX_TRIB_MASK_[16]_[3]**) ||

DX_PTR_INT_JUSCNT_SECE_SUM is a function of the Pointer Interpreter event bits and the DX tributary masks. The logic equation for this bit is:

DX_PTR_INT_JUSCNT_SECE_SUM =

((**DX_PI_POSCNT_SECE_[1]_[1] || DX_PI_NEGCNT_SECE_[1]_[1]**) &&
!**DX_TRIB_MASK_[1]_[1])||**

((**DX_PI_POSCNT_SECE_[1]_[2]** || **DX_PI_NEGCNT_SECE_[1]_[2]**) &&
!**DX_TRIB_MASK_[1]_[2]**) ||

((**DX_PI_POSCNT_SECE_[1]_[3]** || **DX_PI_NEGCNT_SECE_[1]_[3]**) &&
!**DX_TRIB_MASK_[1]_[3]**) ||

((**DX_PI_POSCNT_SECE_[2]_[1]** || **DX_PI_NEGCNT_SECE_[2]_[1]**) &&
!**DX_TRIB_MASK_[2]_[1]**) ||

((**DX_PI_POSCNT_SECE_[2]_[2]** || **DX_PI_NEGCNT_SECE_[2]_[2]**) &&
!**DX_TRIB_MASK_[2]_[2]**) ||

... || ((**DX_PI_POSCNT_SECE_[16]_[2]** || **DX_PI_NEGCNT_SECE_[16]_[2]**) &&
!**DX_TRIB_MASK_[16]_[2]**) ||

((**DX_PI_POSCNT_SECE_[16]_[3]** && || **DX_PI_NEGCNT_SECE_[16]_[3]**)
!**DX_TRIB_MASK_[16]_[3]**)

DX_PTR_GEN_JUSCNT_SECE_SUM is a function of the Pointer Generator event bits and the DX tributary masks. The logic equation for this bit is:

DX_PTR_GEN_JUSCNT_SECE_SUM =

((**DX_PG_POSCNT_SECE_[1]_[1]** || **DX_PG_NEGCNT_SECE_[1]_[1]**) &&
!**DX_TRIB_MASK_[1]_[1]**) ||

((**DX_PG_POSCNT_SECE_[1]_[2]** || **DX_PG_NEGCNT_SECE_[1]_[2]**) &&
!**DX_TRIB_MASK_[1]_[2]**) ||

((**DX_PG_POSCNT_SECE_[1]_[3]** || **DX_PG_NEGCNT_SECE_[1]_[3]**) &&
!**DX_TRIB_MASK_[1]_[3]**) ||

((**DX_PG_POSCNT_SECE_[2]_[1]** || **DX_PG_NEGCNT_SECE_[2]_[1]**) &&
!**DX_TRIB_MASK_[2]_[1]**) ||

((**DX_PG_POSCNT_SECE_[2]_[2]** || **DX_PG_NEGCNT_SECE_[2]_[2]**) &&
!**DX_TRIB_MASK_[2]_[2]**) ||

... || ((**DX_PG_POSCNT_SECE_[16]_[2]** || **DX_PG_NEGCNT_SECE_[16]_[2]**) &&
!**DX_TRIB_MASK_[16]_[2]**) ||

((**DX_PG_POSCNT_SECE_[16]_[3]** && || **DX_PG_NEGCNT_SECE_[16]_[3]**)
!**DX_TRIB_MASK_[16]_[3]**)

DX_PTR_GEN_FIFO_SUME is a function of the Pointer Generator event bits and the DX tributary masks. The logic equation for this bit is:

DX_PTR_GEN_FIFO_SUME =

((**DX_PG_FIFO_[1]_[1]_E**) && !**DX_TRIB_MASK_[1]_[1]**) ||
((**DX_PG_FIFO_[1]_[2]_E**) && !**DX_TRIB_MASK_[1]_[2]**) ||
((**DX_PG_FIFO_[1]_[3]_E**) && !**DX_TRIB_MASK_[1]_[3]**) ||
((**DX_PG_FIFO_[2]_[1]_E**) && !**DX_TRIB_MASK_[2]_[1]**) ||
((**DX_PG_FIFO_[2]_[2]_E**) && !**DX_TRIB_MASK_[2]_[2]**) ||
... || ((**DX_PG_FIFO_[16]_[2]_E**) && !**DX_TRIB_MASK_[16]_[2]**) ||
((**DX_PG_FIFO_[16]_[3]_E**) !**DX_TRIB_MASK_[16]_[3]**)

13.1.6.5 Configuration, Provisioning, and Interface Type - Addr 0x1018 through 0x11FF

The **DX_CONFIG_[20:0]** and **DX_CONFIG_AUTO** registers determine the structure of the generated signal.

If **DX_CONFIG_AUTO = 1** the **DX_CONFIG_[20:0]** is ignored.

If the **CNT_SEC_EN** bit is high, the performance-monitoring counters are latched on the rising edge of SEC_EVENT (see section 2.3).

The Missouri contains a 16-bit B1 error counter that either counts every B1 bit error (if **DX_BIT_BLKCNT** = 0) or every frame with at least 1 B1 bit error (if **DX_BIT_BLKCNT** = 1). On reset, this register is cleared.

The Missouri *SYS_CLK_IN* input clock signal can accept a 622.08 MHz signal when **CLK_155_MODE** = 0. If **CLK_155_MODE** =1, then it accepts a 155.52 MHz input clock signal.

If **DX_LINE_CONFIG_[4]**=1, the Missouri interfaces on it “Low-Speed” side to an STS-48/STM-16 signal. If **DX_LINE_CONFIG_[3:0]**=1, then the Missouri interfaces to STS-12/STM-4 signals on quadrant 1-4, respectively, otherwise it interfaces to STS-3/STM-1 signals.

The **DX_APS_PROT_PRTY_OUT** register bit is used to set outgoing APS parity. If **DX_APS_PROT_PRTY_OUT** = 0 odd parity is used for the *DX_PRTY_PROT_OUT*, else it is even.

DX_IN_INH disables *DX_DATA_IN* and *DX_CLK_IN* and *DX_FRAME_IN*. **DX_OUT_INH_[i]** inhibits *DX_DATA_OUT_[i]* (but not *DX_CLK_OUT_166* or *DX_CLK_OUT_155_622)*. **DX_CLK_OUT_INH_[1]** and **DX_CLK_OUT_INH_[2]** inhibits *DX_CLK_OUT_155_622* and *DX_CLK_OUT_155*, respectively**.** **DX_PROT_OUT_INH** inhibits *DX_PROT_DATA_OUT, DX_PROT_SYNC_OUT, DX_PROT_PRTY_OUT* and *DX_PROT_CLK_OUT*. **DX_PROT_IN_INH** inhibits *DX_PROT_DATA_IN, DX_PROT_SYNC_IN, DX_PROT_PRTY_IN* and *DX_PROT_CLK_IN* (see section 4.10).

The **DMUXSEL_x_[7:0]** bits are used to select the data streams that feed the demux frame generation blocks.

13.1.7 Demultiplexer Side (0x1200 - 0x123F)

13.1.7.1 TOH/SOH Deltas, Second Events, and Masks - Addr 0x1200 through 0x1206

The delta and second event bits contribute to the **DX_TOH_SUMD** and **DX_TOH_SECE_SUM** summary status bits. The contribution of any of the bits can be removed by setting the corresponding mask bit. On reset, the delta and second event bits are cleared, and the mask bits are set high.

13.1.7.2 TOH/SOH Provisioning - Addr 0x1208 through 0x120B

The **DX_K2_CONSEC** register is used in monitoring the received K2 byte (see section 4.4.4). On reset this register is set to “0101” (decimal 5). Note that **DX_K2_CONSEC** is only defined for values between 2-15.

The **DX_LOF_ALG** bit determines which of 2 algorithms is used to clear the **DX_LOF** status bit. Descrambling is inhibited if **DX_DSCRINH** is high (see section 4.3.1). On reset, these bits are cleared.

DX_LOS_INH controls the LOS contribution to LRDI and PAIS. **DX_LOSEXT_LEVEL** controls the polarity of *DX_LOSEXT* (see section 4.9.3.7).

DX_LOSEXT_INH, DX_LOSEXT_DELAY_INH, DX_LOS_ALL_ZERO_INH control the contributors to the LOS monitor (see section 4.2.2).

DX_FIN_BYTE_TYPE_[1:0] and **DX_FRMR_INH** control the framer bypass functionality of the Missouri (see section 4.3.2).

DX_SDH_J0 and **DX_SDH_S1** determine whether the multiplexer side performs J0 and S1 processing in SONET or SDH mode (see section 4.4).

DX_OOF/LOF/LOC/LAIS/LOS_ALARM_INH registers determine which alarms (OOF, LOF, LAIS, LOC, or LOS) contribute to the *DX_ALARM_OUT* pin (see section 4.5.2).

13.1.7.3 TOH/SOH Status - Addr 0x120C through 0x1223

The bits in these registers hold the current state of the TOH/SOH Receiver Monitor (see sections 3.4 through section 4.4). On reset, all bits in these registers are cleared, except for **DX_OOF**, **DX_LOF**, **DX_B2_ERR_SF**, and **DX_B2_ERR_SD**.

13.1.7.4 B2 Signal Fail and Signal Degrade Parameters - Addr 0x1224 through 0x122F

These registers contain the algorithm parameters for the B2 based Signal Fail and Signal Degrade Monitors (see section 4.4.3). On reset, all of the parameter values are set to decimal 1.

13.1.7.5 B1, B2, and M1 Error Counters - Addr 0x1230 through 0x123A

These registers contain the latched results of error counters (see section 4.4.1, section 4.4.3, and section 4.4.6). On reset, these registers are cleared.

13.1.8 Demultiplexer Side (0x1600 - 0x17FF)

13.1.8.1 Pointer Interpreter Provisioning - Addr 0x1602 and 0x1606

The **DX_CONCAT_[20:0]_D** bits are set to 1 whenever there is a change of their associated status bits. The **DX_CONCAT_[20:0]_D_MASK** bits are set to 1 to disable the contribution of the associated delta bit to the **DX_PTR_INT_CONCAT_SUMD** interrupt.

13.1.8.2 Pointer Interpreter Provisioning - Addr 0x160B

The **DX_SS_EN_[i]** bits determine whether or not the SS-bits are used in the Pointer Interpreter algorithms (see section 3.6.2 and section 3.6.3). **DX_SDH_PI_[i]** determine whether the Receive Side performs SONET or SDH pointer interpretation (see section 3.6.3).

13.1.8.3 Pointer Interpreter Status - Addr 0x1608 to 0x160A

The **DX_CONCAT_[20:0]** bits report the received signal configuration as indicated by the H1H2 bytes (see section 3.6.1).

13.1.8.4 Pointer Interpreter Deltas - Addr [0x1700,0x1702]

The delta bits contribute to the **DX_PTR_INT_PAIS_SUMD** and **DX_PTR_INT_LOP_SUMD** summary status bits in transmit register 0x1006 (see section 3.6.2). On reset, the delta bits are cleared.

13.1.8.5 Pointer Interpreter Status - Addr [0x1700 - 0x17F8]

These registers hold the current state of the Pointer Interpreter (see section 3.6.2). On reset, **DX_LOP_x**, **DX_PAIS_x**, and both bits of **DX_PTR_STATE_x_[1:0]** for x = [1,1], [5,1], [9,1], and [13,1] are cleared, and all bits of the 44 remaining **DX_PTR_STATE_x_[1:0]** are also cleared, indicating 16 STS-3c or AU-4 normal pointers.

13.1.9 Demultiplexer Side (0x1800 - 0x19FF)

13.1.9.1 Pointer Generator Event Bits - Addr [0x1900,0x19F0] and [0x1902,0x19F2]

If for tributary x, there has been at least 1 positive or negative justification in the previous second, the **DX_PG_POSCNT_SECE_x** or **DX_PG_NEGCNT_SECE_x** bit is set.

The DX Pointer Generator contains 5-bit pointer generator justification counters that count every positive or negative justification. When the performance-monitoring counters are latched, the values of these counters are latched to the **DX_PG_POSCNT_x_[4:0]** and **DX_PG_NEGCNT_x_[4:0]** registers, and the justification counters are cleared.

If a DX Pointer Generator FIFO overflows or underflows, the **DX_PG_FIFO_x_E** event bit is set. The FIFO is then recentered, and the Pointer Generator continues normal operation.

13.1.9.2 Pointer Generator Provisioning - Addr [0x1904-5,0x19F4-5]

If **DX_FAST_AIS_x** = 1 and the last frame received for tributary **x** contains all-ones in its H-bytes, the Missouri inserts PAIS for tributary **x**. **DX_SF_PAIS_INH** controls the SF contribution to PAIS insertion.

DX_SDH_PG_[i] is used to select between SDH (1) and SONET (0) modes for pointer generation (see section 4.6.4.2).

The user may force PAIS generation for tributary **x** by setting **DX_PAIS_GEN_x** = 1 (if tributary **x** is in operation based on the value of **DX_CONCAT** or **DX_CONFIG**, see section 3.6.2.2).

The Pointer Generators can also insert Unequipped. If **DX_PAIS_GEN_x** = 0, and **DX_UNEQ_GEN_x** = 1, the entire SPE/VC is generated with all-zeros. The pointer value used for unequipped insertion must be a valid pointer value; the specific value is not specified. An NDF does not need to be generated when the unequipped signal insertion is removed (**DX_UNEQ_GEN_x** is cleared).

13.1.10 Demultiplexer Side (0x1A00 - 0x1BFF)

DX_A1A2_ERR_[i], **DX_A1A2_ERR_PAT_[i]_[15:0]**, **DX_A1A2_ERR_NUM_[i]_[2:0]**, **DX_B1_INV_[i]**, **DX_B2_INV_[i]**, and **DX_M1_ERRCNT_[21:0]** control the generation of errors in the A1, A2, B1, B2, and M1 bytes in SONET/SDH signal i (see section 4.9.3.1, section 4.9.3.3, section 4.9.3.6, and section 4.9.3.9).

Automatic generation of LRDI and LREI are inhibited if **DX_LRDI_INH_[i]** and **DX_LREI_INH_[i]** are high. Scrambling of the SONET/SDH signal is disabled if **DX_SCRINH_[i]** is high (see section 4.9.3.7 and section 4.9.4).

If **DX_LAIS_GEN_[i]** is high, the entire SONET/SDH signal i is generated as all-ones, except for the first three rows of Section Overhead (see section 4.9.3.7).

DX_K1K2_APS_[i] and **DX_K2_3LSB_[i]** registers are used to select the source of the K1 and K2 bytes; either from the register map (0) or the TOH serial channel (1) (see section 3.9.3.4).

The **DX_J0_[i]_[15:0]_[7:0]**, **DX_K1GEN_[i]_[7:0]**, **DX_K2GEN_[i]_[7:0]**, and **DX_S1GEN_[i]_[7:0]** registers are used in the generation of J0, K1, K2, and S1 bytes (see section 4.9.3.2, section 4.9.3.7, and section 4.9.3.8).

DX_FRAME_IN_INH enables/inhibits the use of the *SYS_SYNC_IN* signal as the frame sync reference for DX side of the Missouri (see section 3.9.1).

The SONET/SDH TOH/SOH Provisioning and Scrambler Inhibit register map for SONET/SDH signal [1] is illustrated in Table 45. Identical maps exist for Signals [2], [3] ... [16].

13.1.11 Device ID (0x1FFF)

13.1.11.1 Device Identification Code - Addr - 0x1FFF

This register holds a device identification number for the Missouri, **DEV_ID_[7:0]**.

13.2 Register Map

13.2.1 Multiplex Common Provisioning and Summary Status (Addresses 0x0000 through 0x01FF)

Table 36. Mux Side Configuration and Summary Status Map

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset Control (Read/Write)									
0000	0x00							MX_STATE_ RESET	MX_PROV_ RESET
0001		Unused							
Device Version Number (Read Only)									
0002	0x01	DEV_VER_[7:0]							
0003		Unused							
Mux Side Summary Interrupt (Read Only) and Summary Delta/Event (Read Only / cleared by microprocessor)									
0004	0x00								MX_SUM_ INT
0005	0x00	MX_APS_ INT_[16]	MX_APS_ INT_[15]	MX_APS_ INT_[14]	MX_APS_ INT_[13]	MX_APS_ INT_[12]	MX_APS_ INT_[11]	MX_APS_ INT_[10]	MX_APS_ INT_[9]
0006	0x00	MX_APS_ INT_[8]	MX_APS_ INT_[7]	MX_APS_ INT_[6]	MX_APS_ INT_[5]	MX_APS_ INT_[4]	MX_APS_ INT_[3]	MX_APS_ INT_[2]	MX_APS_ INT_[1]
0007	0x00	MX_TOH_SUM D_[8]	MX_TOH_SUM D_[7]	MX_TOH_SUM D_[6]	MX_TOH_ SUMD_[5]	MX_TOH_ SUMD_[4]	MX_TOH_ SUMD_[3]	MX_TOH_ SUMD_[2]	MX_TOH_ SUMD_[1]
0008	0x00	MX_TOH_ SUMD_[16]	MX_TOH_ SUMD_[15]	MX_TOH_ SUMD_[14]	MX_TOH_ SUMD_[13]	MX_TOH_ SUMD_[12]	MX_TOH_ SUMD_[11]	MX_TOH_ SUMD_[10]	MX_TOH_ SUMD_[9]
0009	0x00	MX_TOH_ SECE_ SUM_[8]	MX_TOH_ SECE_ SUM_[7]	MX_TOH_ SECE_ SUM_[6]	MX_TOH_ SECE_ SUM_[5]	MX_TOH_ SECE_ SUM_[4]	MX_TOH_ SECE_ SUM_[3]	MX_TOH_ SECE_ SUM_[2]	MX_TOH_ SECE_ SUM_[1]
000A	0x00	MX_TOH_ SECE_ SUM_[16]	MX_TOH_ SECE_ SUM_[15]	MX_TOH_ SECE_ SUM_[14]	MX_TOH_ SECE_ SUM_[13]	MX_TOH_ SECE_ SUM_[12]	MX_TOH_ SECE_ SUM_[11]	MX_TOH_ SECE_ SUM_[10]	MX_TOH_ SECE_ SUM_[9]
000B	0x00	MX_APS_ PROT_PRTY_ E	GPIO_SUMD	MX_PTR_GEN _FIFO_SUME	MX_PTR_INT_ CONCAT_ SUMD	MX_PTR_INT_ PAIS_ SUMD	MX_PTR_INT_ LOP_ SUMD	MX_PTR_INT_ JUSCNT_ SECE_ SUM	MX_PTR_GEN _JUSCNT_ SECE_ SUM
000C	0x00		MX_PROT_ FIFO_ERR_E	Reserved					
000D		Unused							
Mux Side Summary Interrupt and GPIO Summary Masks (Read/Write)									
000E	0x01								MX_SUM_ INT_MASK

Table 36. Mux Side Configuration and Summary Status Map

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
000F	0xFF	MX_APS_ INT_MASK _[16]	MX_APS_ INT_MASK _[15]	MX_APS_ INT_MASK _[14]	MX_APS_ INT_MASK _[13]	MX_APS_ INT_MASK _[12]	MX_APS_ INT_MASK _[11]	MX_APS_ INT_MASK _[10]	MX_APS_ INT_MASK _[9]
0010	0xFF	MX_APS_ INT_MASK _[8]	MX_APS_ INT_MASK _[7]	MX_APS _INT_MASK _[6]	MX_APS_ INT_MASK _[5]	MX_APS_ INT_MASK _[4]	MX_APS_ INT_MASK _[3]	MX_APS_ INT_MASK _[2]	MX_APS_ INT_MASK _[1]
0011	0xFF	MX_TOH_ SUMD_MASK_ [16]	MX_TOH_ SUMD_MASK_ [15]	MX_TOH_ SUMD_MASK_ [14]	MX_TOH_ SUMD_MASK_ [13]	MX_TOH_ SUMD_MASK_ [12]	MX_TOH_ SUMD_MASK_ [11]	MX_TOH_ SUMD_MASK_ [10]	MX_TOH_ SUMD_MASK_ [9]
0012	0xFF	MX_TOH_ SUMD_MASK_ [8]	MX_TOH_ SUMD_MASK_ [7]	MX_TOH_ SUMD_MASK_ [6]	MX_TOH_ SUMD_MASK_ [5]	MX_TOH_ SUMD_MASK_ [4]	MX_TOH_ SUMD_MASK_ [3]	MX_TOH_ SUMD_MASK_ [2]	MX_TOH_ SUMD_MASK_ [1]
0013	0xFF	MX_TOH_ SECE_SUM_ MASK_[16]	MX_TOH_ SECE_SUM_ MASK_[15]	MX_TOH_ SECE_SUM _MASK_[14]	MX_TOH_ SECE_SUM_ MASK_[13]	MX_TOH_ SECE_SUM_ MASK_[12]	MX_TOH_ SECE_SUM_ MASK_[11]	MX_TOH_ SECE_SUM_ MASK_[10]	MX_TOH_ SECE_SUM_ MASK_[9]
0014	0xFF	MX_TOH_ SECE_SUM_ MASK_[8]	MX_TOH_ SECE_SUM_ MASK_[7]	MX_TOH_ SECE_SUM_ MASK_[6]	MX_TOH_ SECE_SUM_ MASK_[5]	MX_TOH_ SECE_SUM_ MASK_[4]	MX_TOH_ SECE_SUM _MASK_[3]	MX_TOH_ SECE_SUM_ MASK_[2]	MX_TOH_ SECE_SUM_ MASK_[1]
0015	0xFF	MX_APS_ PROT_PRTY_ E_MASK	GPIO_SUMD_ MASK	MX_PTR_GEN _FIFO_SUME_ MASK	MX_PTR_INT_ CONCAT_ SUMD_ MASK	MX_PTR_INT_ PAIS_ SUMD_ MASK	MX_PTR_INT_ LOP_ SUMD_ MASK	MX_PTR_INT_ JUSCNT_ SECE_ SUM_ MASK	MX_PTR_GEN _JUSCNT_ SECE_ SUM_ MASK
0016	0x60		MX_PROT_ FIFO_ERR_E_ MASK	Reserved					
0017		Unused							
Configuration, GPIO Provisioning (Read/Write)									
0018	0x00				MX_LINE_CONFIG_[4:0]				
0019	0x00	LOF_INH	MX_APS_ PROT_PRTY_ OUT	Reserved	Reserved				
001A	0x00	MX_CONFIG_[7:0]							
001B	0x00	MX_CONFIG_[15:8]							
001C	0x00			MX_CONFIG_ AUTO	MX_CONFIG_[20:16]				
001D		Unused							
001E	0xFF	GPIOCTL8	GPIOCTL7	GPIOCTL6	GPIOCTL5	GPIOCTL4	GPIOCTL3	GPIOCTL2	GPIOCTL1
001F	0x00		RX_REF_CLK_FREQ_[1:0]		RX_REF_CLK_SEL_[4:0]				
0020		Unused							
0021	0x00	MX_OUT_INH	Unused	MX_PROT_ OUT_INH	MX_PROT_IN_ INH	Unused			
0022	0x01			MX_PROT_ CLK_OUT_INV					MX_CLK_ OUT_INV
0023-0027		Unused							
MX Configuration Status (Read Only)									
0028	0x00			Reserved			Reserved		

Table 36. Mux Side Configuration and Summary Status Map

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0029-002F		Unused							
GPIO Delta Bits (Read Only, Cleared by microprocessor)									
0030	0x00	GPIO7_D	GPIO6_D	GPIO5_D	GPIO4_D	GPIO3_D	GPIO2_D	GPIO1_D	GPIO0_D
0031	0x00	GPIO15_D	GPIO14_D	GPIO13_D	GPIO12_D	GPIO11_D	GPIO10_D	GPIO9_D	GPIO8_D
Mask Bits (Read/Write)									
0032	0xFF	GPIO7_ MASK	GPIO6_ MASK	GPIO5_ MASK	GPIO4_ MASK	GPIO3 _MASK	GPIO2_ MASK	GPIO1_ MASK	GPIO0_ MASK
0033	0xFF	GPIO15_ MASK	GPIO14_ MASK	GPIO13_ MASK	GPIO12_ MASK	GPIO11 _MASK	GPIO10_ MASK	GPIO9_ MASK	GPIO8_ MASK
General Purpose Inputs/Outputs									
0034	0x00	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
0035	0x00	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8
0036-00FF		Unused							
Tributary Configuration Provisioning (Read/Write)									
0100	0x07						MX_TRIB_ MASK_[1]_[1]	MX_TRIB_ MASK_[2]_[1]	MX_TRIB_ MASK_[3]_[1]
0101	0x00	DX_TO_MX_LS _LOOP_[1]	MX_BIT_ BLKCNT_[1]	MX_IN_INH_[1]	Unused				
0102	0x00	MUXSEL_[1]_[1]_[7:0]							
0103	0x01	MUXSEL_[1]_[2]_[7:0]							
0104	0x02	MUXSEL_[1]_[3]_[7:0]							
0105-010F		Unused							
0110	0x07						MX_TRIB_ MASK_[4]_[1]	MX_TRIB_ MASK_[5]_[1]	MX_TRIB_ MASK_[6]_[1]
0111	0x00	DX_TO_MX_LS _LOOP_[2]	MX_BIT_ BLKCNT_[2]	MX_IN_INH_[2]	Unused				
0112	0x04	MUXSEL_[2]_[1]_[7:0]							
0113	0x05	MUXSEL_[2]_[2]_[7:0]							
0114	0x06	MUXSEL_[2]_[3]_[7:0]							
0115-011F		Unused							
0120	0x07						MX_TRIB_ MASK_[7]_[1]	MX_TRIB_ MASK_[8]_[1]	MX_TRIB_ MASK_[9]_[1]
0121	0x00	DX_TO_MX_LS _LOOP_[3]	MX_BIT_ BLKCNT_[3]	MX_IN_INH_[3]	Unused				
0122	0x08	MUXSEL_[3]_[1]_[7:0]							
0123	0x09	MUXSEL_[3]_[2]_[7:0]							
0124	0x0A	MUXSEL_[3]_[3]_[7:0]							
0125-012F		Unused							
0130	0x07						MX_TRIB_ MASK_[10]_[1]	MX_TRIB_ MASK_[11]_[1]	MX_TRIB_ MASK_[12]_[1]
0131	0x00	DX_TO_MX_LS _LOOP_[4]	MX_BIT_ BLKCNT_[4]	MX_IN_INH_[4]	Unused				
0132	0x0C	MUXSEL_[4]_[1]_[7:0]							

Table 36. Mux Side Configuration and Summary Status Map

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0133	0x0D	MUXSEL_[4]_[2]_[7:0]							
0134	0x0E	MUXSEL_[4]_[3]_[7:0]							
0135-013F		Unused							
0140	0x07						MX_TRIB_MASK_[13]_[1]	MX_TRIB_MASK_[14]_[1]	MX_TRIB_MASK_[15]_[1]
0141	0x00	DX_TO_MX_LS_LOOP_[5]	MX_BIT_BLKCNT_[5]	MX_IN_INH_[5]	Unused				
0142	0x10	MUXSEL_[5]_[1]_[7:0]							
0143	0x11	MUXSEL_[5]_[2]_[7:0]							
0144	0x12	MUXSEL_[5]_[3]_[7:0]							
0145-014F		Unused							
0150	0x07						MX_TRIB_MASK_[16]_[1]	MX_TRIB_MASK_[1]_[2]	MX_TRIB_MASK_[2]_[2]
0151	0x00	DX_TO_MX_LS_LOOP_[6]	MX_BIT_BLKCNT_[6]	MX_IN_INH_[6]	Unused				
0152	0x14	MUXSEL_[6]_[1]_[7:0]							
0153	0x15	MUXSEL_[6]_[2]_[7:0]							
0154	0x16	MUXSEL_[6]_[3]_[7:0]							
0155-015F		Unused							
0160	0x07						MX_TRIB_MASK_[3]_[2]	MX_TRIB_MASK_[4]_[2]	MX_TRIB_MASK_[5]_[2]
0161	0x00	DX_TO_MX_LS_LOOP_[7]	MX_BIT_BLKCNT_[7]	MX_IN_INH_[7]	Unused				
0162	0x18	MUXSEL_[7]_[1]_[7:0]							
0163	0x19	MUXSEL_[7]_[2]_[7:0]							
0164	0x1A	MUXSEL_[7]_[3]_[7:0]							
0165-016F		Unused							
0170	0x07						MX_TRIB_MASK_[6]_[2]	MX_TRIB_MASK_[7]_[2]	MX_TRIB_MASK_[8]_[2]
0171	0x00	DX_TO_MX_LS_LOOP_[8]	MX_BIT_BLKCNT_[8]	MX_IN_INH_[8]	Unused				
0172	0x1C	MUXSEL_[8]_[1]_[7:0]							
0173	0x1D	MUXSEL_[8]_[2]_[7:0]							
0174	0x1E	MUXSEL_[8]_[3]_[7:0]							
0175-017F		Unused							
0180	0x07						MX_TRIB_MASK_[9]_[2]	MX_TRIB_MASK_[10]_[2]	MX_TRIB_MASK_[11]_[2]
0181	0x00	DX_TO_MX_LS_LOOP_[9]	MX_BIT_BLKCNT_[9]	MX_IN_INH_[9]	Unused				
0182	0x20	MUXSEL_[9]_[1]_[7:0]							
0183	0x21	MUXSEL_[9]_[2]_[7:0]							
0184	0x22	MUXSEL_[9]_[3]_[7:0]							

Table 36. Mux Side Configuration and Summary Status Map

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0185-018F		Unused							
0190	0x07						MX_TRIB_MASK_[12]_[2]	MX_TRIB_MASK_[13]_[2]	MX_TRIB_MASK_[14]_[2]
0191	0x00	DX_TO_MX_LS_LOOP_[10]	MX_BIT_BLKCNT_[10]	MX_IN_INH_[10]	Unused				
0192	0x24	MUXSEL_[10]_[1]_[7:0]							
0193	0x25	MUXSEL_[10]_[2]_[7:0]							
0194	0x26	MUXSEL_[10]_[3]_[7:0]							
0195-019F		Unused							
01A0	0x07						MX_TRIB_MASK_[15]_[2]	MX_TRIB_MASK_[16]_[2]	MX_TRIB_MASK_[1]_[3]
01A1	0x00	DX_TO_MX_LS_LOOP_[11]	MX_BIT_BLKCNT_[11]	MX_IN_INH_[11]	Unused				
01A2	0x28	MUXSEL_[11]_[1]_[7:0]							
01A3	0x29	MUXSEL_[11]_[2]_[7:0]							
01A4	0x2A	MUXSEL_[11]_[3]_[7:0]							
01A5-01AF		Unused							
01B0	0x07						MX_TRIB_MASK_[2]_[3]	MX_TRIB_MASK_[3]_[3]	MX_TRIB_MASK_[4]_[3]
01B1	0x00	DX_TO_MX_LS_LOOP_[12]	MX_BIT_BLKCNT_[12]	MX_IN_INH_[12]	Unused				
01B2	0x2C	MUXSEL_[12]_[1]_[7:0]							
01B3	0x2D	MUXSEL_[12]_[2]_[7:0]							
01B4	0x2E	MUXSEL_[12]_[3]_[7:0]							
01B5-01BF		Unused							
01C0	0x07						MX_TRIB_MASK_[5]_[3]	MX_TRIB_MASK_[6]_[3]	MX_TRIB_MASK_[7]_[3]
01C1	0x00	DX_TO_MX_LS_LOOP_[13]	MX_BIT_BLKCNT_[13]	MX_IN_INH_[13]	Unused				
01C2	0x30	MUXSEL_[13]_[1]_[7:0]							
01C3	0x31	MUXSEL_[13]_[2]_[7:0]							
01C4	0x32	MUXSEL_[13]_[3]_[7:0]							
01C5-01CF		Unused							
01D0	0x07						MX_TRIB_MASK_[8]_[3]	MX_TRIB_MASK_[9]_[3]	MX_TRIB_MASK_[10]_[3]
01D1	0x00	DX_TO_MX_LS_LOOP_[14]	MX_BIT_BLKCNT_[14]	MX_IN_INH_[14]	Unused				
01D2	0x34	MUXSEL_[14]_[1]_[7:0]							
01D3	0x35	MUXSEL_[14]_[2]_[7:0]							
01D4	0x36	MUXSEL_[14]_[3]_[7:0]							
01D5-01DF		Unused							

Table 36. Mux Side Configuration and Summary Status Map

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01E0	0x07						MX_TRIB_ MASK_[11]_[3]	MX_TRIB_ MASK_[12]_[3]	MX_TRIB_ MASK_[13]_[3]
01E1	0x00	DX_TO_MX_LS _LOOP_[15]	MX_BIT_ BLKCNT_[15]	MX_IN_INH_ [15]	Unused				
01E2	0x38	MUXSEL_[15]_[1]_[7:0]							
01E3	0x39	MUXSEL_[15]_[2]_[7:0]							
01E4	0x3A	MUXSEL_[15]_[3]_[7:0]							
01E5-01EF		Unused							
01F0	0x07						MX_TRIB_ MASK_[14]_[3]	MX_TRIB_ MASK_[15]_[3]	MX_TRIB_ MASK_[16]_[3]
01F1	0x00	DX_TO_MX_LS _LOOP_[16]	MX_BIT_ BLKCNT_[16]	MX_IN_INH_ [16]	Unused				
01F2	0x3C	MUXSEL_[16]_[1]_[7:0]							
01F3	0x3D	MUXSEL_[16]_[2]_[7:0]							
01F4	0x3E	MUXSEL_[16]_[3]_[7:0]							
01F5-01FF		Unused							

13.2.2 Multiplexer Side (Addresses 0x0200 through 0x05FF)

Table 37. Multiplexer Side Register Address Map for SONET/SDH TOH/SOH Monitoring

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Signal 1 TOH/SOH Delta and Second Event Bits (Read Only, Cleared by microprocessor)									
0200	0x00	MX_B2_ERR_ SF_[1]_D	MX_B2_ERR_ SD_[1]_D	MX_ LAIS_[1]_D	MX_ LRDI_[1]_D	MX_K1_[1]_D	MX_K1_ UNSTAB_[1]_D	MX_K2_[1]_D	MX_S1_[1]_D
0201	0x00		MX_ LOSEXT_[1]_D	MX_ LOS_[1]_D	MX_ LOC_[1]_D	MX_ OOF_[1]_D	MX_ LOF_[1]_D	MX_J0_OOF_ [1]_D	MX_J0_[1]_D
0202	0x00			MX_OOF_ [1]_SECE	MX_LOF_ [1]_SECE	MX_B1ERR_ [1]_SECE	MX_B2ERR_ [1]_SECE	MX_S1FAIL_ [1]_SECE	MX_M1ERR_ [1]_SECE
0203		Unused							
TOH/SOH Masks and Provisioning Bits (Read/Write)									
0204	0xFF	MX_B2_ERR_ SF_[1]_D_ MASK	MX_B2_ERR_ SD_[1]_D_ MASK	MX_ LAIS_[1]_D_ MASK	MX_ LRDI_[1]_D_ MASK	MX_K1_[1]_D_ MASK	MX_K1_ UNSTAB_[1]_ D_MASK	MX_K2_[1]_D_ MASK	MX_S1_[1]_D_ MASK
0205	0x7F		MX_ LOSEXT_[1]_D _MASK	MX_ LOS_[1]_D_ MASK	MX_ LOC_[1]_D_ MASK	MX_ OOF_[1]_D_ MASK	MX_ LOF_[1]_D_ MASK	MX_J0_ OOF_[1]_D_ MASK	MX_J0_[1]_D _MASK
0206	0x3F			MX_OOF_ [1]_SECE_ MASK	MX_LOF_ [1]_SECE_ MASK	MX_B1ERR_ [1]_SECE_ MASK	MX_B2ERR_ [1]_SECE_ MASK	MX_S1FAIL_ [1]_SECE_ MASK	MX_M1ERR_ [1]_SECE_ MASK
0207		Unused							
0208	0x50	MX_K2_CONSEC_[1]_[3:0]						MX_LOF_ ALG_[1]	MX_DSCRINH _[1]

Table 37. Multiplexer Side Register Address Map for SONET/SDH TOH/SOH Monitoring

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0209	0x88	MX_LOSEXT_INH_[1]	MX_LOSEXT_LEVEL_[1]	MX_LOS_INH_[1]	Reserved	MX_LOSEXT_DELAY_INH_[1]	MX_LOS_ALL_ZERO_INH_[1]	MX_SDH_S1_[1]	MX_SDH_J0_[1]
020A	0x00			Reserved					
020B	0x00				MX_LOS_ALARM_INH_[1]	MX_LAIS_ALARM_INH_[1]	MX_LOC_ALARM_INH_[1]	MX_LOF_ALARM_INH_[1]	MX_OOF_ALARM_INH_[1]
TOH/SOH Status (Read Only)									
020C	0xC0	MX_B2_ERR_SF_[1]	MX_B2_ERR_SD_[1]	MX_LAIS_[1]	MX_LRDI_[1]		MX_K1_UNSTAB_[1]		
020D	0x0C		MX_LOSEXT_[1]	MX_LOS_[1]	MX_LOC_[1]	MX_OOF_[1]	MX_LOF_[1]	MX_J0_OOF_[1]	
020E-020F		Unused							
0210	0x00	MX_J0_[1]_[0]_[7:0]							
0211	0x00	MX_J0_[1]_[1]_[7:0]							
0212	0x00	MX_J0_[1]_[2]_[7:0]							
0213-021D	0x00								
021E	0x00	MX_J0_[1]_[14]_[7:0]							
021F	0x00	MX_J0_[1]_[15]_[7:0]							
0220		Unused							
0221	0x00					MX_S1_[1]_[3:0]			
0222	0x00	MX_K2_[1]_[7:0]							
0223	0x00	MX_K1_[1]_[7:0]							
Signal Fail & Signal Degrade Parameters (Read/Write)									
0224	0x01	MX_B2_BLOCK_SF_[1]_[7:0]							
0225		Unused							
0226	0x01	MX_B2_THRESH_SET_SF_[1]_[7:0]							
0227	0x01			MX_B2_GROUP_SET_SF_[1]_[5:0]					
0228	0x01	MX_B2_THRESH_CLR_SF_[1]_[7:0]							
0229	0x01			MX_B2_GROUP_CLR_SF_[1]_[5:0]					
022A	0x01	MX_B2_BLOCK_SD_[1]_[7:0]							
022B	0x00	MX_B2_BLOCK_SD_[1]_[15:8]							
022C	0x01			MX_B2_THRESH_SET_SD_[1]_[5:0]					
022D	0x01			MX_B2_GROUP_SET_SD_[1]_[5:0]					
022E	0x01			MX_B2_THRESH_CLR_SD_[1]_[5:0]					
022F	0x01			MX_B2_GROUP_CLR_SD_[1]_[5:0]					
Performance Monitoring Counters (Read Only)									
0230	0x00	MX_B1_ERRCNT_[1]_[7:0]							
0231	0x00	MX_B1_ERRCNT_[1]_[15:8]							
0232		Unused							
0233		Unused							
0234	0x00	MX_B2_ERRCNT_[1]_[7:0]							
0235	0x00	MX_B2_ERRCNT_[1]_[15:8]							
0236	0x00			MX_B2_ERRCNT_[1]_[21:16]					
0237		Unused							
0238	0x00	MX_M1_ERRCNT_[1]_[7:0]							
0239	0x00	MX_M1_ERRCNT_[1]_[15:8]							
023A	0x00			MX_M1_ERRCNT_[1]_[21:16]					

Table 37. Multiplexer Side Register Address Map for SONET/SDH TOH/SOH Monitoring

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
023B-023F		Unused							
Signal 2 TOH/SOH Delta and Second Event Bits (Read Only, Cleared by microprocessor)									
0240-027F		Same as 0x0200 through 0x023F							
Signal 3 -15 TOH/SOH Delta and Second Event Bits (Read Only, Cleared by microprocessor)									
0280-05BF		Same as 0x0200 through 0x023F							
Signal 16TOH/SOH Delta and Second Event Bits (Read Only, Cleared by microprocessor)									
05C0-05FF		Same as 0x0200 through 0x023F							

13.2.3 Multiplexer Side (Addresses 0x0600 through 0x07FF)

Table 38. Mux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
0600	0x00	MX_CONCAT_[7:0]_D							
0601	0x00	MX_CONCAT_[15:8]_D							
0602	0x00				MX_CONCAT_[20:16]_D				
0603		Unused							
Pointer Interpreter Delta Bits (Read/Write)									
0604	0xFF	MX_CONCAT_[7:0]_D_MASK							
0605	0xFF	MX_CONCAT_[15:8]_D_MASK							
0606	0x1F				MX_CONCAT_[20:16]_D_MASK				
0607		Unused							
Pointer Interpreter Status Bits (Ready Only)									
0608	0x00	MX_CONCAT_[7:0]							
0609	0x00	MX_CONCAT_[15:8]							
060A	0x00				MX_CONCAT_[20:16]				
060B-06FF		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
0700	0x00			MX_LOP_[1]_[1]_D	MX_PAIS_[1]_[1]_D	MX_LOP_[2]_[1]_D	MX_PAIS_[2]_[1]_D	MX_LOP_[3]_[1]_D	MX_PAIS_[3]_[1]_D
0701	0x00			MX_PI_NEGCNT_SECE_[1]_[1]	MX_PI_POSCNT_SECE_[1]_[1]	MX_PI_NEGCNT_SECE_[2]_[1]	MX_PI_POSCNT_SECE_[2]_[1]	MX_PI_NEGCNT_SECE_[3]_[1]	MX_PI_POSCNT_SECE_[3]_[1]
0702-0703		Unused							
Tributary [1] Pointer Interpreter Configuration Bits (Read/Write)									
0704	0x00		MX_SDH_PI_[1]	MX_SS_EN_[1]					
0705		Unused							

Table 38. Mux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pointer Interpreter Status Bits (Read Only)									
0706	0x00			MX_PTR_STATE_[1]_[1]_[1:0]		MX_PTR_STATE_[1]_[2]_[1:0]		MX_PTR_STATE_[1]_[3]_[1:0]	
0707	0x00			MX_LOP _[1]_[1]	MX_PAIS _[1]_[1]	MX_LOP _[2]_[1]	MX_PAIS _[2]_[1]	MX_LOP _[3]_[1]	MX_PAIS _[3]_[1]
Tributary [1] Pointer Interpreter Counter Bits (Read Only)									
0708	0x00				MX_PI_POSCNT_[1]_[1]_[4:0]				
0709	0x00				MX_PI_NEGCNT_[1]_[1]_[4:0]				
070A	0x00				MX_PI_POSCNT_[1]_[2]_[4:0]				
070B	0x00				MX_PI_NEGCNT_[1]_[2]_[4:0]				
070C	0x00				MX_PI_POSCNT_[1]_[3]_[4:0]				
070D	0x00				MX_PI_NEGCNT_[1]_[3]_[4:0]				
070E-070F		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
0710	0x00			MX_LOP_ [4]_[1]_D	MX_PAIS_ [4]_[1]_D	MX_LOP_ [5]_[1]_D	MX_PAIS _[5]_[1]_D	MX_LOP _[6]_[1]_D	MX_PAIS_ [6]_[1]_D
0711	0x00			MX_PI_ NEGCNT_ SECE_[4]_[1]	MX_PI_ POSCNT_ SECE_[4]_[1]	MX_PI_ NEGCNT_ SECE_[5]_[1]	MX_PI_ POSCNT_ SECE_[5]_[1]	MX_PI_ NEGCNT_ SECE_[6]_[1]	MX_PI_ POSCNT_ SECE_[6]_[1]
0712-0713		Unused							
Tributary [2] Pointer Interpreter Configuration Bits (Read/Write)									
0714	0x00		MX_SDH_ PI_[2]	MX_SS_ EN_[2]					
0715		Unused							
Pointer Interpreter Status Bits (Read Only)									
0716	0x00			MX_PTR_STATE_[2]_[1]_[1:0]		MX_PTR_STATE_[2]_[2]_[1:0]		MX_PTR_STATE_[2]_[3]_[1:0]	
0717	0x00			MX_LOP _[4]_[1]	MX_PAIS _[4]_[1]	MX_LOP _[5]_[1]	MX_PAIS _[5]_[1]	MX_LOP _[6]_[1]	MX_PAIS _[6]_[1]
Tributary [2] Pointer Interpreter Counter Bits (Read Only)									
0718	0x00				MX_PI_POSCNT_[2]_[1]_[4:0]				
0719	0x00				MX_PI_NEGCNT_[2]_[1]_[4:0]				
071A	0x00				MX_PI_POSCNT_[2]_[2]_[4:0]				
071B	0x00				MX_PI_NEGCNT_[2]_[2]_[4:0]				
071C	0x00				MX_PI_POSCNT_[2]_[3]_[4:0]				
071D	0x00				MX_PI_NEGCNT_[2]_[3]_[4:0]				
071E-071F		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
0720	0x00			MX_LOP _[7]_[1]_D	MX_PAIS_ [7]_[1]_D	MX_LOP _[8]_[1]_D	MX_PAIS_ [8]_[1]_D	MX_LOP _[9]_[1]_D	MX_PAIS_ [9]_[1]_D
0721	0x00			MX_PI_ NEGCNT_ SECE_[7]_[1]	MX_PI_ POSCNT_ SECE_[7]_[1]	MX_PI_ NEGCNT_ SECE_[8]_[1]	MX_PI_ POSCNT_ SECE_[8]_[1]	MX_PI_ NEGCNT_ SECE_[9]_[1]	MX_PI_ POSCNT_ SECE_[9]_[1]
0722-0723		Unused							
Tributary [3] Pointer Interpreter Configuration Bits (Read/Write)									
0724	0x00		MX_SDH_ PI_[3]	MX_SS_ EN_[3]					

Table 38. Mux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0725		Unused							
Pointer Interpreter Status Bits (Read Only)									
0726	0x00			MX_PTR_STATE_[3]_[1]_[1:0]		MX_PTR_STATE_[3]_[2]_[1:0]		MX_PTR_STATE_[3]_[3]_[1:0]	
0727	0x00			MX_LOP _[7]_[1]	MX_PAIS _[7]_[1]	MX_LOP _[8]_[1]	MX_PAIS _[8]_[1]	MX_LOP _[9]_[1]	MX_PAIS _[9]_[1]
Tributary [3] Pointer Interpreter Counter Bits (Read Only)									
0728	0x00				MX_PI_POSCNT_[3]_[1]_[4:0]				
0729	0x00				MX_PI_NEGCNT_[3]_[1]_[4:0]				
072A	0x00				MX_PI_POSCNT_[3]_[2]_[4:0]				
072B	0x00				MX_PI_NEGCNT_[3]_[2]_[4:0]				
072C	0x00				MX_PI_POSCNT_[3]_[3]_[4:0]				
072D	0x00				MX_PI_NEGCNT_[3]_[3]_[4:0]				
072E-072F		Unused145							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
0730	0x00			MX_LOP _[10]_[1]_D	MX_PAIS_ [10]_[1]_D	MX_LOP _[11]_[1]_D	MX_PAIS_ [11]_[1]_D	MX_LOP _[12]_[1]_D	MX_PAIS_ [12]_[1]_D
0731	0x00			MX_PI_ NEGCNT_ SECE_[10]_[1]	MX_PI_ POSCNT_ SECE_[10]_[1]	MX_PI_ NEGCNT_ SECE_[11]_[1]	MX_PI_ POSCNT_ SECE_[11]_[1]	MX_PI_ NEGCNT_ SECE_[12]_[1]	MX_PI_ POSCNT_ SECE_[12]_[1]
0732-0733		Unused							
Tributary [4] Pointer Interpreter Configuration Bits (Read/Write)									
0734	0x00		MX_SDH_ PI_[4]	MX_SS_ EN_[4]					
0735		Unused							
Pointer Interpreter Status Bits (Read Only)									
0736	0x00			MX_PTR_STATE_[4]_[1]_[1:0]		MX_PTR_STATE_[4]_[2]_[1:0]		MX_PTR_STATE_[4]_[3]_[1:0]	
0737	0x00			MX_LOP _[10]_[1]	MX_PAIS _[10]_[1]	MX_LOP _[11]_[1]	MX_PAIS _[11]_[1]	MX_LOP _[12]_[1]	MX_PAIS _[12]_[1]
Tributary [4] Pointer Interpreter Counter Bits (Read Only)									
0738	0x00				MX_PI_POSCNT_[4]_[1]_[4:0]				
0739	0x00				MX_PI_NEGCNT_[4]_[1]_[4:0]				
073A	0x00				MX_PI_POSCNT_[4]_[2]_[4:0]				
073B	0x00				MX_PI_NEGCNT_[4]_[2]_[4:0]				
073C	0x00				MX_PI_POSCNT_[4]_[3]_[4:0]				
073D	0x00				MX_PI_NEGCNT_[4]_[3]_[4:0]				
073E-073F		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
0740	0x00			MX_LOP _[13]_[1]_D	MX_PAIS_ [13]_[1]_D	MX_LOP _[14]_[1]_D	MX_PAIS_ [14]_[1]_D	MX_LOP _[15]_[1]_D	MX_PAIS_ [15]_[1]_D
0741	0x00			MX_PI_ NEGCNT_ SECE_[13]_[1]	MX_PI_ POSCNT_ SECE_[13]_[1]	MX_PI_ NEGCNT_ SECE_[14]_[1]	MX_PI_ POSCNT_ SECE_[14]_[1]	MX_PI_ NEGCNT_ SECE_[15]_[1]	MX_PI_ POSCNT_ SECE_[15]_[1]
0742-0743		Unused							
Tributary [5] Pointer Interpreter Configuration Bits (Read/Write)									

Table 38. Mux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0744	0x00		MX_SDH_PI_[5]	MX_SS_EN_[5]					
0745		Unused							
Pointer Interpreter Status Bits (Read Only)									
0746	0x00			MX_PTR_STATE_[5]_[1]_[1:0]		MX_PTR_STATE_[5]_[2]_[1:0]		MX_PTR_STATE_[5]_[3]_[1:0]	
0747	0x00			MX_LOP_[13]_[1]	MX_PAIS_[13]_[1]	MX_LOP_[14]_[1]	MX_PAIS_[14]_[1]	MX_LOP_[15]_[1]	MX_PAIS_[15]_[1]
Tributary [5] Pointer Interpreter Counter Bits (Read Only)									
0748	0x00				MX_PI_POSCNT_[5]_[1]_[4:0]				
0749	0x00				MX_PI_NEGCNT_[5]_[1]_[4:0]				
074A	0x00				MX_PI_POSCNT_[5]_[2]_[4:0]				
074B	0x00				MX_PI_NEGCNT_[5]_[2]_[4:0]				
074C	0x00				MX_PI_POSCNT_[5]_[3]_[4:0]				
074D	0x00				MX_PI_NEGCNT_[5]_[3]_[4:0]				
074E-074F		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
0750	0x00			MX_LOP_[16]_[1]_D	MX_PAIS_[16]_[1]_D	MX_LOP_[1]_[2]_D	MX_PAIS_[1]_[2]_D	MX_LOP_[2]_[2]_D	MX_PAIS_[2]_[2]_D
0751	0x00			MX_PI_NEGCNT_SECE_[16]_[1]	MX_PI_POSCNT_SECE_[16]_[1]	MX_PI_NEGCNT_SECE_[1]_[2]	MX_PI_POSCNT_SECE_[1]_[2]	MX_PI_NEGCNT_SECE_[2]_[2]	MX_PI_POSCNT_SECE_[2]_[2]
0752-0753		Unused							
Tributary [6] Pointer Interpreter Configuration Bits (Read/Write)									
0754	0x00		MX_SDH_PI_[6]	MX_SS_EN_[6]					
0755		Unused							
Pointer Interpreter Status Bits (Read Only)									
0756	0x00			MX_PTR_STATE_[6]_[1]_[1:0]		MX_PTR_STATE_[6]_[2]_[1:0]		MX_PTR_STATE_[6]_[3]_[1:0]	
0757	0x00			MX_LOP_[16]_[1]	MX_PAIS_[16]_[1]	MX_LOP_[1]_[2]	MX_PAIS_[1]_[2]	MX_LOP_[2]_[2]	MX_PAIS_[2]_[2]
Tributary [6] Pointer Interpreter Counter Bits (Read Only)									
0758	0x00				MX_PI_POSCNT_[6]_[1]_[4:0]				
0759	0x00				MX_PI_NEGCNT_[6]_[1]_[4:0]				
075A	0x00				MX_PI_POSCNT_[6]_[2]_[4:0]				
075B	0x00				MX_PI_NEGCNT_[6]_[2]_[4:0]				
075C	0x00				MX_PI_POSCNT_[6]_[3]_[4:0]				
075D	0x00				MX_PI_NEGCNT_[6]_[3]_[4:0]				
075E-075F		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
0760	0x00			MX_LOP_[3]_[2]_D	MX_PAIS_[3]_[2]_D	MX_LOP_[4]_[2]_D	MX_PAIS_[4]_[2]_D	MX_LOP_[5]_[2]_D	MX_PAIS_[5]_[2]_D
0761	0x00			MX_PI_NEGCNT_SECE_[3]_[2]	MX_PI_POSCNT_SECE_[3]_[2]	MX_PI_NEGCNT_SECE_[4]_[2]	MX_PI_POSCNT_SECE_[4]_[2]	MX_PI_NEGCNT_SECE_[5]_[2]	MX_PI_POSCNT_SECE_[5]_[2]
0762-0763		Unused							

Table 38. Mux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Tributary [7] Pointer Interpreter Configuration Bits (Read/Write)									
0764	0x00		MX_SDH_ PI_[7]	MX_SS_ EN_[7]					
0765		Unused							
Pointer Interpreter Status Bits (Read Only)									
0766	0x00			MX_PTR_STATE_[7]_[1]_[1:0]		MX_PTR_STATE_[7]_[2]_[1:0]		MX_PTR_STATE_[7]_[3]_[1:0]	
0767	0x00			MX_LOP _[3]_[2]	MX_PAIS _[3]_[2]	MX_LOP _[4]_[2]	MX_PAIS _[4]_[2]	MX_LOP _[5]_[2]	MX_PAIS _[5]_[2]
Tributary [7] Pointer Interpreter Counter Bits (Read Only)									
0768	0x00				MX_PI_POSCNT_[7]_[1]_[4:0]				
0769	0x00				MX_PI_NEGCNT_[7]_[1]_[4:0]				
076A	0x00				MX_PI_POSCNT_[7]_[2]_[4:0]				
076B	0x00				MX_PI_NEGCNT_[7]_[2]_[4:0]				
076C	0x00				MX_PI_POSCNT_[7]_[3]_[4:0]				
076D	0x00				MX_PI_NEGCNT_[7]_[3]_[4:0]				
076E-076F		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
0770	0x00			MX_LOP _[6]_[2]_D	MX_PAIS_ [6]_[2]_D	MX_LOP _[7]_[2]_D	MX_PAIS_ [7]_[2]_D	MX_LOP _[8]_[2]_D	MX_PAIS_ [8]_[2]_D
0771	0x00			MX_PI_ NEGCNT_ SECE_[6]_[2]	MX_PI_ POSCNT_ SECE_[6]_[2]	MX_PI_ NEGCNT_ SECE_[7]_[2]	MX_PI_ POSCNT_ SECE_[7]_[2]	MX_PI_ NEGCNT_ SECE_[8]_[2]	MX_PI_ POSCNT_ SECE_[8]_[2]
0772-0773		Unused							
Tributary [8] Pointer Interpreter Configuration Bits (Read/Write)									
0774	0x00		MX_SDH_ PI_[8]	MX_SS_ EN_[8]					
0775		Unused							
Pointer Interpreter Status Bits (Read Only)									
0776	0x00			MX_PTR_STATE_[8]_[1]_[1:0]		MX_PTR_STATE_[8]_[2]_[1:0]		MX_PTR_STATE_[8]_[3]_[1:0]	
0777	0x00			MX_LOP _[6]_[2]	MX_PAIS _[6]_[2]	MX_LOP _[7]_[2]	MX_PAIS _[7]_[2]	MX_LOP _[8]_[2]	MX_PAIS _[8]_[2]
Tributary [8] Pointer Interpreter Counter Bits (Read Only)									
0778	0x00				MX_PI_POSCNT_[8]_[1]_[4:0]				
0779	0x00				MX_PI_NEGCNT_[8]_[1]_[4:0]				
077A	0x00				MX_PI_POSCNT_[8]_[2]_[4:0]				
077B	0x00				MX_PI_NEGCNT_[8]_[2]_[4:0]				
077C	0x00				MX_PI_POSCNT_[8]_[3]_[4:0]				
077D	0x00				MX_PI_NEGCNT_[8]_[3]_[4:0]				
077E-077F		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
0780	0x00			MX_LOP _[9]_[2]_D	MX_PAIS_ [9]_[2]_D	MX_LOP _[10]_[2]_D	MX_PAIS_ [10]_[2]_D	MX_LOP _[11]_[2]_D	MX_PAIS_ [11]_[2]_D
0781	0x00			MX_PI_ NEGCNT_ SECE_[9]_[2]	MX_PI_ POSCNT_ SECE_[9]_[2]	MX_PI_ NEGCNT_ SECE_[10]_[2]	MX_PI_ POSCNT_ SECE_[10]_[2]	MX_PI_ NEGCNT_ SECE_[11]_[2]	MX_PI_ POSCNT_ SECE_[11]_[2]

Table 38. Mux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0782-0783		Unused							
Tributary [9] Pointer Interpreter Configuration Bits (Read/Write)									
0784	0x00		MX_SDH_PI_[9]	MX_SS_EN_[9]					
0785		Unused							
Pointer Interpreter Status Bits (Read Only)									
0786	0x00			MX_PTR_STATE_[9]_[1]_[1:0]		MX_PTR_STATE_[9]_[2]_[1:0]		MX_PTR_STATE_[9]_[3]_[1:0]	
0787	0x00			MX_LOP_[9]_[2]	MX_PAIS_[9]_[2]	MX_LOP_[10]_[2]	MX_PAIS_[10]_[2]	MX_LOP_[11]_[2]	MX_PAIS_[11]_[2]
Tributary [9] Pointer Interpreter Counter Bits (Read Only)									
0788	0x00				MX_PI_POSCNT_[9]_[1]_[4:0]				
0789	0x00				MX_PI_NEGCNT_[9]_[1]_[4:0]				
078A	0x00				MX_PI_POSCNT_[9]_[2]_[4:0]				
078B	0x00				MX_PI_NEGCNT_[9]_[2]_[4:0]				
078C	0x00				MX_PI_POSCNT_[9]_[3]_[4:0]				
078D	0x00				MX_PI_NEGCNT_[9]_[3]_[4:0]				
078E-078F		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
0790	0x00			MX_LOP_[12]_[2]_D	MX_PAIS_[12]_[2]_D	MX_LOP_[13]_[2]_D	MX_PAIS_[13]_[2]_D	MX_LOP_[14]_[2]_D	MX_PAIS_[14]_[2]_D
0791	0x00			MX_PI_NEGCNT_SECE_[12]_[2]	MX_PI_POSCNT_SECE_[12]_[2]	MX_PI_NEGCNT_SECE_[13]_[2]	MX_PI_POSCNT_SECE_[13]_[2]	MX_PI_NEGCNT_SECE_[14]_[2]	MX_PI_POSCNT_SECE_[14]_[2]
0792-0793		Unused							
Tributary [10] Pointer Interpreter Configuration Bits (Read/Write)									
0794	0x00		MX_SDH_PI_[10]	MX_SS_EN_[10]					
0795		Unused							
Pointer Interpreter Status Bits (Read Only)									
0796	0x00			MX_PTR_STATE_[10]_[1]_[1:0]		MX_PTR_STATE_[10]_[2]_[1:0]		MX_PTR_STATE_[10]_[3]_[1:0]	
0797	0x00			MX_LOP_[12]_[2]	MX_PAIS_[12]_[2]	MX_LOP_[13]_[2]	MX_PAIS_[13]_[2]	MX_LOP_[14]_[2]	MX_PAIS_[14]_[2]
Tributary [10] Pointer Interpreter Counter Bits (Read Only)									
0798	0x00				MX_PI_POSCNT_[10]_[1]_[4:0]				
0799	0x00				MX_PI_NEGCNT_[10]_[1]_[4:0]				
079A	0x00				MX_PI_POSCNT_[10]_[2]_[4:0]				
079B	0x00				MX_PI_NEGCNT_[10]_[2]_[4:0]				
079C	0x00				MX_PI_POSCNT_[10]_[3]_[4:0]				
079D	0x00				MX_PI_NEGCNT_[10]_[3]_[4:0]				
079E-079F		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
07A0	0x00			MX_LOP_[15]_[2]_D	MX_PAIS_[15]_[2]_D	MX_LOP_[16]_[2]_D	MX_PAIS_[16]_[2]_D	MX_LOP_[1]_[3]_D	MX_PAIS_[1]_[3]_D

Table 38. Mux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07A1	0x00			MX_PI_ NEGCNT_ SECE_[15]_[2]	MX_PI_ POSCNT_ SECE_[15]_[2]	MX_PI_ NEGCNT_ SECE_[16]_[2]	MX_PI_ POSCNT_ SECE_[16]_[2]	MX_PI_ NEGCNT_ SECE_[1]_[3]	MX_PI_ POSCNT_ SECE_[1]_[3]
07A2-07A3		Unused							
Tributary [11] Pointer Interpreter Configuration Bits (Read/Write)									
07A4	0x00		MX_SDH_ PI_[11]	MX_SS_ EN_[11]					
07A5		Unused							
Pointer Interpreter Status Bits (Read Only)									
07A6	0x00			MX_PTR_STATE_[11]_[1]_[1:0]		MX_PTR_STATE_[11]_[2]_[1:0]		MX_PTR_STATE_[11]_[3]_[1:0]	
07A7	0x00			MX_LOP _[15]_[2]	MX_PAIS _[15]_[2]	MX_LOP _[16]_[2]	MX_PAIS _[16]_[2]	MX_LOP _[1]_[3]	MX_PAIS _[1]_[3]
Tributary [11] Pointer Interpreter Counter Bits (Read Only)									
07A8	0x00				MX_PI_POSCNT_[11]_[1]_[4:0]				
07A9	0x00				MX_PI_NEGCNT_[11]_[1]_[4:0]				
07AA	0x00				MX_PI_POSCNT_[11]_[2]_[4:0]				
07AB	0x00				MX_PI_NEGCNT_[11]_[2]_[4:0]				
07AC	0x00				MX_PI_POSCNT_[11]_[3]_[4:0]				
07AD	0x00				MX_PI_NEGCNT_[11]_[3]_[4:0]				
07AE-07AF		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
07B0	0x00			MX_LOP _[2]_[3]_D	MX_PAIS_ [2]_[3]_D	MX_LOP _[3]_[3]_D	MX_PAIS_ [3]_[3]_D	MX_LOP _[4]_[3]_D	MX_PAIS_ [4]_[3]_D
07B1	0x00			MX_PI_ NEGCNT_ SECE_[2]_[3]	MX_PI_ POSCNT_ SECE_[2]_[3]	MX_PI_ NEGCNT_ SECE_[3]_[3]	MX_PI_ POSCNT_ SECE_[3]_[3]	MX_PI_ NEGCNT_ SECE_[4]_[3]	MX_PI_ POSCNT_ SECE_[4]_[3]
07B2-07B3		Unused							
Tributary [12] Pointer Interpreter Configuration Bits (Read/Write)									
07B4	0x00		MX_SDH_ PI_[12]	MX_SS_ EN_[12]					
07B5		Unused							
Pointer Interpreter Status Bits (Read Only)									
07B6	0x00			MX_PTR_STATE_[12]_[1]_[1:0]		MX_PTR_STATE_[12]_[2]_[1:0]		MX_PTR_STATE_[12]_[3]_[1:0]	
07B7	0x00			MX_LOP _[2]_[3]	MX_PAIS _[2]_[3]	MX_LOP _[3]_[3]	MX_PAIS _[3]_[3]	MX_LOP _[4]_[3]	MX_PAIS _[4]_[3]
Tributary [12] Pointer Interpreter Counter Bits (Read Only)									
07B8	0x00				MX_PI_POSCNT_[12]_[1]_[4:0]				
07B9	0x00				MX_PI_NEGCNT_[12]_[1]_[4:0]				
07BA	0x00				MX_PI_POSCNT_[12]_[2]_[4:0]				
07BB	0x00				MX_PI_NEGCNT_[12]_[2]_[4:0]				
07BC	0x00				MX_PI_POSCNT_[12]_[3]_[4:0]				
07BD	0x00				MX_PI_NEGCNT_[12]_[3]_[4:0]				
07BE-07BF		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									

Table 38. Mux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07C0	0x00			MX_LOP _[5]_[3]_D	MX_PAIS_ [5]_[3]_D	MX_LOP _[6]_[3]_D	MX_PAIS_ [6]_[3]_D	MX_LOP _[7]_[3]_D	MX_PAIS_ [7]_[3]_D
07C1	0x00			MX_PI_ NEGCNT_ SECE_[5]_[3]	MX_PI_ POSCNT_ SECE_[5]_[3]	MX_PI_ NEGCNT_ SECE_[6]_[3]	MX_PI_ POSCNT_ SECE_[6]_[3]	MX_PI_ NEGCNT_ SECE_[7]_[3]	MX_PI_ POSCNT_ SECE_[7]_[3]
07C2-07C3		Unused							
Tributary [13] Pointer Interpreter Configuration Bits (Read/Write)									
07C4	0x00		MX_SDH_ PI_[13]	MX_SS_ EN_[13]					
07C5		Unused							
Pointer Interpreter Status Bits (Read Only)									
07C6	0x00			MX_PTR_STATE_[13]_[1]_[1:0]		MX_PTR_STATE_[13]_[2]_[1:0]		MX_PTR_STATE_[13]_[3]_[1:0]	
07C7	0x00			MX_LOP _[5]_[3]	MX_PAIS _[5]_[3]	MX_LOP _[6]_[3]	MX_PAIS _[6]_[3]	MX_LOP _[7]_[3]	MX_PAIS _[7]_[3]
Tributary [13] Pointer Interpreter Counter Bits (Read Only)									
07C8	0x00				MX_PI_POSCNT_[13]_[1]_[4:0]				
07C9	0x00				MX_PI_NEGCNT_[13]_[1]_[4:0]				
07CA	0x00				MX_PI_POSCNT_[13]_[2]_[4:0]				
07CB	0x00				MX_PI_NEGCNT_[13]_[2]_[4:0]				
07CC	0x00				MX_PI_POSCNT_[13]_[3]_[4:0]				
07CD	0x00				MX_PI_NEGCNT_[13]_[3]_[4:0]				
07CE-07CF		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
07D0	0x00			MX_LOP _[8]_[3]_D	MX_PAIS_ [8]_[3]_D	MX_LOP _[9]_[3]_D	MX_PAIS_ [9]_[3]_D	MX_LOP _[10]_[3]_D	MX_PAIS_ [10]_[3]_D
07D1	0x00			MX_PI_ NEGCNT_ SECE_[8]_[3]	MX_PI_ POSCNT_ SECE_[8]_[3]	MX_PI_ NEGCNT_ SECE_[9]_[3]	MX_PI_ POSCNT_ SECE_[9]_[3]	MX_PI_ NEGCNT_ SECE_[10]_[3]	MX_PI_ POSCNT_ SECE_[10]_[3]
07D2-07D3		Unused							
Tributary [14] Pointer Interpreter Configuration Bits (Read/Write)									
07D4	0x00		MX_SDH_ PI_[14]	MX_SS_ EN_[14]					
07D5		Unused							
Pointer Interpreter Status Bits (Read Only)									
07D6	0x00			MX_PTR_STATE_[14]_[1]_[1:0]		MX_PTR_STATE_[14]_[2]_[1:0]		MX_PTR_STATE_[14]_[3]_[1:0]	
07D7	0x00			MX_LOP _[8]_[3]	MX_PAIS _[8]_[3]	MX_LOP _[9]_[3]	MX_PAIS _[9]_[3]	MX_LOP _[10]_[3]	MX_PAIS _[10]_[3]
Tributary [14] Pointer Interpreter Counter Bits (Read Only)									
07D8	0x00				MX_PI_POSCNT_[14]_[1]_[4:0]				
07D9	0x00				MX_PI_NEGCNT_[14]_[1]_[4:0]				
07DA	0x00				MX_PI_POSCNT_[14]_[2]_[4:0]				
07DB	0x00				MX_PI_NEGCNT_[14]_[2]_[4:0]				
07DC	0x00				MX_PI_POSCNT_[14]_[3]_[4:0]				
07DD	0x00				MX_PI_NEGCNT_[14]_[3]_[4:0]				
07DE-07DF		Unused							

Table 38. Mux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
07E0	0x00			MX_LOP _[11]_[3]_D	MX_PAIS_ [11]_[3]_D	MX_LOP _[12]_[3]_D	MX_PAIS_ [12]_[3]_D	MX_LOP _[13]_[3]_D	MX_PAIS_ [13]_[3]_D
07E1	0x00			MX_PI_ NEGCNT_ SECE_[11]_[3]	MX_PI_ POSCNT_ SECE_[11]_[3]	MX_PI_ NEGCNT_ SECE_[12]_[3]	MX_PI_ POSCNT_ SECE_[12]_[3]	MX_PI_ NEGCNT_ SECE_[13]_[3]	MX_PI_ POSCNT_ SECE_[13]_[3]
07E2-07E3		Unused							
Tributary [15] Pointer Interpreter Configuration Bits (Read/Write)									
07E4	0x00		MX_SDH_ PI_[15]	MX_SS_ EN_[15]					
07E5		Unused							
Pointer Interpreter Status Bits (Read Only)									
07E6	0x00			MX_PTR_STATE_[15]_[1]_[1:0]		MX_PTR_STATE_[15]_[2]_[1:0]		MX_PTR_STATE_[15]_[3]_[1:0]	
07E7	0x00			MX_LOP _[11]_[3]	MX_PAIS _[11]_[3]	MX_LOP _[12]_[3]	MX_PAIS _[12]_[3]	MX_LOP _[13]_[3]	MX_PAIS _[13]_[3]
Tributary [15] Pointer Interpreter Counter Bits (Read Only)									
07E8	0x00				MX_PI_POSCNT_[15]_[1]_[4:0]				
07E9	0x00				MX_PI_NEGCNT_[15]_[1]_[4:0]				
07EA	0x00				MX_PI_POSCNT_[15]_[2]_[4:0]				
07EB	0x00				MX_PI_NEGCNT_[15]_[2]_[4:0]				
07EC	0x00				MX_PI_POSCNT_[15]_[3]_[4:0]				
07ED	0x00				MX_PI_NEGCNT_[15]_[3]_[4:0]				
07EE-07EF		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
07F0	0x00			MX_LOP _[14]_[3]_D	MX_PAIS_ [14]_[3]_D	MX_LOP _[15]_[3]_D	MX_PAIS_ [15]_[3]_D	MX_LOP _[16]_[3]_D	MX_PAIS_ [16]_[3]_D
07F1	0x00			MX_PI_ NEGCNT_ SECE_[14]_[3]	MX_PI_ POSCNT_ SECE_[14]_[3]	MX_PI_ NEGCNT_ SECE_[15]_[3]	MX_PI_ POSCNT_ SECE_[15]_[3]	MX_PI_ NEGCNT_ SECE_[16]_[3]	MX_PI_ POSCNT_ SECE_[16]_[3]
07F2-07F3		Unused							
Tributary [16] Pointer Interpreter Configuration Bits (Read/Write)									
07F4	0x00		MX_SDH_ PI_[16]	MX_SS_ EN_[16]					
07F5		Unused							
Pointer Interpreter Status Bits (Read Only)									
07F6	0x00			MX_PTR_STATE_[16]_[1]_[1:0]		MX_PTR_STATE_[16]_[2]_[1:0]		MX_PTR_STATE_[16]_[3]_[1:0]	
07F7	0x00			MX_LOP _[14]_[3]	MX_PAIS _[14]_[3]	MX_LOP _[15]_[3]	MX_PAIS _[15]_[3]	MX_LOP _[16]_[3]	MX_PAIS _[16]_[3]
Tributary [16] Pointer Interpreter Counter Bits (Read Only)									
07F8	0x00				MX_PI_POSCNT_[16]_[1]_[4:0]				
07F9	0x00				MX_PI_NEGCNT_[16]_[1]_[4:0]				
07FA	0x00				MX_PI_POSCNT_[16]_[2]_[4:0]				
07FB	0x00				MX_PI_NEGCNT_[16]_[2]_[4:0]				
07FC	0x00				MX_PI_POSCNT_[16]_[3]_[4:0]				
07FD	0x00				MX_PI_NEGCNT_[16]_[3]_[4:0]				

Table 38. Mux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07FE-07FF		Unused							

13.2.4 Multiplexer Side (Addresses 0x0900 through 0x09FF)

Table 39. Mux Side Register Address Map for SONET/SDH Pointer Generator

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0800-08FF		Unused							
Tributary [1] Pointer Generator Event Bits (Read Only, cleared by microprocessor)									
0900	0x00			MX_PG_NEGCNT_SECE_[1]_[1]	MX_PG_POSCNT_SECE_[1]_[1]	MX_PG_NEGCNT_SECE_[1]_[2]	MX_PG_POSCNT_SECE_[1]_[2]	MX_PG_NEGCNT_SECE_[1]_[3]	MX_PG_POSCNT_SECE_[1]_[3]
0901		Unused							
0902	0x00						MX_PG_FIFO_[1]_[1]_E	MX_PG_FIFO_[1]_[2]_E	MX_PG_FIFO_[1]_[3]_E
0903		Unused							
Tributary [1] Pointer Generator Configuration Bits (Read/Write)									
0904	0x00		MX_SF_PAIS_INH_[1]	MX_UNEQ_GEN_[1]_[1]	MX_PAIS_GEN_[1]_[1]	MX_UNEQ_GEN_[1]_[2]	MX_PAIS_GEN_[1]_[2]	MX_UNEQ_GEN_[1]_[3]	MX_PAIS_GEN_[1]_[3]
0905	0x00		MX_SDH_PG_[1]	MX_FAST_AIS_[1]_[1]		MX_FAST_AIS_[1]_[2]		MX_FAST_AIS_[1]_[3]	
0906-0907		Unused							
Tributary [1] Pointer Generator Counter Bits (Read Only)									
0908	0x00				MX_PG_POSCNT_[1]_[1]_[4:0]				
0909	0x00				MX_PG_NEGCNT_[1]_[1]_[4:0]				
090A	0x00				MX_PG_POSCNT_[1]_[2]_[4:0]				
090B	0x00				MX_PG_NEGCNT_[1]_[2]_[4:0]				
090C	0x00				MX_PG_POSCNT_[1]_[3]_[4:0]				
090D	0x00				MX_PG_NEGCNT_[1]_[3]_[4:0]				
090E-090F		Unused							
Tributary [2] Pointer Generator Event Bits (Read Only, cleared by microprocessor)									
0910	0x00			MX_PG_NEGCNT_SECE_[2]_[1]	MX_PG_POSCNT_SECE_[2]_[1]	MX_PG_NEGCNT_SECE_[2]_[2]	MX_PG_POSCNT_SECE_[2]_[2]	MX_PG_NEGCNT_SECE_[2]_[3]	MX_PG_POSCNT_SECE_[2]_[3]
0911		Unused							
0912	0x00						MX_PG_FIFO_[2]_[1]_E	MX_PG_FIFO_[2]_[2]_E	MX_PG_FIFO_[2]_[3]_E
0913		Unused							
Tributary [2] Pointer Generator Configuration Bits (Read/Write)									
0914	0x00		MX_SF_PAIS_INH_[2]	MX_UNEQ_GEN_[2]_[1]	MX_PAIS_GEN_[2]_[1]	MX_UNEQ_GEN_[2]_[2]	MX_PAIS_GEN_[2]_[2]	MX_UNEQ_GEN_[2]_[3]	MX_PAIS_GEN_[2]_[3]
0915	0x00		MX_SDH_PG_[2]	MX_FAST_AIS_[2]_[1]		MX_FAST_AIS_[2]_[2]		MX_FAST_AIS_[2]_[3]	

Table 39. Mux Side Register Address Map for SONET/SDH Pointer Generator

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0916-0917		Unused							
Tributary [2] Pointer Generator Counter Bits (Read Only)									
0918	0x00				MX_PG_POSCNT_[2]_[1]_[4:0]				
0919	0x00				MX_PG_NEGCNT_[2]_[1]_[4:0]				
091A	0x00				MX_PG_POSCNT_[2]_[2]_[4:0]				
091B	0x00				MX_PG_NEGCNT_[2]_[2]_[4:0]				
091C	0x00				MX_PG_POSCNT_[2]_[3]_[4:0]				
091D	0x00				MX_PG_NEGCNT_[2]_[3]_[4:0]				
091E-091F		Unused							
0920-09EF		. . ..							
Tributary [16] Pointer Generator Event Bits (Read Only, cleared by microprocessor)									
09F0	0x00			MX_PG_NEGCNT_SECE_[16]_[1]	MX_PG_POSCNT_SECE_[16]_[1]	MX_PG_NEGCNT_SECE_[16]_[2]	MX_PG_POSCNT_SECE_[16]_[2]	MX_PG_NEGCNT_SECE_[16]_[3]	MX_PG_POSCNT_SECE_[16]_[3]
09F1		Unused							
09F2	0x00						MX_PG_FIFO_[16]_[1]_E	MX_PG_FIFO_[16]_[2]_E	MX_PG_FIFO_[16]_[3]_E
09F3		Unused							
Tributary [16] Pointer Generator Configuration Bits (Read/Write)									
09F4	0x00		MX_SF_PAIS_INH_[16]	MX_UNEQ_GEN_[16]_[1]	MX_PAIS_GEN_[16]_[1]	MX_UNEQ_GEN_[16]_[2]	MX_PAIS_GEN_[16]_[2]	MX_UNEQ_GEN_[16]_[3]	MX_PAIS_GEN_[16]_[3]
09F5	0x00		MX_SDH_PG_[16]	MX_FAST_AIS_[16]_[1]		MX_FAST_AIS_[16]_[2]		MX_FAST_AIS_[16]_[3]	
09F6-09F7		Unused							
Tributary [16] Pointer Generator Counter Bits (Read Only)									
09F8	0x00				MX_PG_POSCNT_[16]_[1]_[4:0]				
09F9	0x00				MX_PG_NEGCNT_[16]_[1]_[4:0]				
09FA	0x00				MX_PG_POSCNT_[16]_[2]_[4:0]				
09FB	0x00				MX_PG_NEGCNT_[16]_[2]_[4:0]				
09FC	0x00				MX_PG_POSCNT_[16]_[3]_[4:0]				
09FD	0x00				MX_PG_NEGCNT_[16]_[3]_[4:0]				
09FE-09FF		Unused							

13.2.5 Multiplexer Side (Addresses 0x0A00 through 0x0A1F)

Table 40. Mux Side Register Address Map for SONET/SDH TOH/SOH Provisioning and Scrambler Inhibit

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SONET/SDH Line/MS AIS Generation Control, Scrambler Inhibit, and TOH/SOH Provisioning (Read/Write)									

Table 40. Mux Side Register Address Map for SONET/SDH TOH/SOH Provisioning and Scrambler Inhibit

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0A00	0x00	MX_A1A2_ ERR	MX_A1A2_ERR_NUM_[2:0]			MX_B1_INV	MX_B2_INV	MX_M1GEN_ ERR	MX_SCRINH
0A01	0x00	MX_LAIS_GEN	Reserved	MX_K1K2_APS	MX_K2_3LSB			LRDI_INH	MX_LREI_INH
0A02	0x00	MX_A1A2_ERR_PAT_[7:0]							
0A03	0x00	MX_A1A2_ERR_PAT_[15:8]							
0A04	0x01	MX_J0_[0]_[7:0]							
0A05	0x01	MX_J0_[1]_[7:0]							
0A06	0x01	MX_J0_[2]_[7:0]							
0A07	0x01	MX_J0_[3]_[7:0]							
0A08	0x01	MX_J0_[4]_[7:0]							
0A09	0x01	MX_J0_[5]_[7:0]							
0A0A	0x01	MX_J0_[6]_[7:0]							
0A0B	0x01	MX_J0_[7]_[7:0]							
0A0C	0x01	MX_J0_[8]_[7:0]							
0A0D	0x01	MX_J0_[9]_[7:0]							
0A0E	0x01	MX_J0_[10]_[7:0]							
0A0F	0x01	MX_J0_[11]_[7:0]							
0A10	0x01	MX_J0_[12]_[7:0]							
0A11	0x01	MX_J0_[13]_[7:0]							
0A12	0x01	MX_J0_[14]_[7:0]							
0A13	0x01	MX_J0_[15]_[7:0]							
0A14	0x00	MX_K2GEN_[7:0]							
0A15	0x00	MX_K1GEN_[7:0]							
0A16	0x00	MX_S1GEN_[7:0]							
0A17	0x00	MX_FRAME_IN _INH	Reserved	Reserved		Reserved			
0A18- 0A1F		Unused							

13.2.6 Demultiplexer Common Provisioning and Summary Status (Addresses 0x1000 through 0x11FF)

Table 41. Demux Side Configuration and Summary Status Map

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset Control (Read/Write)									
1000	0x00			MASTER_ RESET	SHORT_ FRAME	CNT_ LOAD	LATCH_ CNT	DX_STATE_ RESET	DX_PROV_ RESET
1001		Unused							
Demux Side Summary Interrupt (Read Only) and Summary Delta/Event (Read Only / cleared by microprocessor)									
1002	0x00		LATCH_E					DX_APS_INT	DX_SUM_ INT
1003	0x00			Reserved	Reserved			DX_TOH_ SUMD	DX_TOH_ SECE_SUM
1004-1007		Unused							
1008	0x00	DX_APS_ PROT_PRTY_ E	DX_PROT_ FIFO_ERR_E	DX_PTR_GEN _FIFO_ SUME	DX_PTR_INT_ CONCAT_ SUMD	DX_PTR_INT_ PAIS_ SUMD	DX_PTR_INT_ LOP_ SUMD	DX_PTR_INT_ JUSCNT_ SECE_ SUM	DX_PTR_GEN _JUSCNT_ SECE_ SUM
1009-100D		Unused							
Demux Side Summary Interrupt Summary Masks (Read/Write)									
100E	0x43		LATCH_E_ MASK					DX_APS_INT_ MASK	DX_SUM_ INT_MASK
100F	0x33			Reserved	Reserved			DX_TOH_ SUMD_MASK	DX_TOH_ SECE_SUM_ MASK
1010-1013		Unused							
1014	0xFF	DX_APS_ PROT_PRTY_ E_MASK	DX_PROT_ FIFO_ERR_E_ MASK	DX_PTR_GEN _FIFO_SUME_ MASK	DX_PTR_INT_ CONCAT_ SUMD_ MASK	DX_PTR_INT_ PAIS_ SUMD_ MASK	DX_PTR_INT_ LOP_ SUMD_ MASK	DX_PTR_INT_ JUSCNT_ SECE_ SUM_ MASK	DX_PTR_GEN _JUSCNT_ SECE_ SUM_ MASK
1015-1017		Unused							
Configuration, Loopback Provisioning (Read/Write)									
1018	0x00	DX_BIT_ BLKCNT	CNT_SEC_EN	CLK_155_ MODE	DX_LINE_CONFIG_[4:0]				
1019	0x00	Reserved	DX_APS_ PROT_PRTY_ OUT		MX_TO_DX_ HS_LOOP				SYS_SYNC_IN _RESYNC
101A	0x00	DX_CONFIG_[7:0]							
101B	0x00	DX_CONFIG_[15:8]							
101C	0x00			DX_CONFIG_ AUTO	DX_CONFIG_[20:16]				
101D	0x00	Unused							
101E	0x00	Reserved							
1020	0x08	Reserved							

Table 41. Demux Side Configuration and Summary Status Map

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1021	0x00	Unused	DX_IN_INH	DX_PROT_OUT_INH	DX_PROT_IN_INH	DX_CLK_OUT_INH_[1:2]		Reserved	Reserved
1022	0x0F			DX_PROT_CLK_OUT_INV		DX_CLK_OUT_INV_[1:2]		Reserved	Reserved
1023-102F		Unused							
DX Configuration Status (Read Only)									
1030	0x00			Reserved	Reserved				
1031	0x00						Reserved		
1032-10FF		Unused							
Tributary Configuration Provisioning (Read/Write)									
1100	0x07						DX_TRIB_MASK_[1]_[1]	DX_TRIB_MASK_[2]_[1]	DX_TRIB_MASK_[3]_[1]
1101	0x00	Reserved	DX_OUT_INH_[1]	Reserved	Unused				
1102	0x00	DMUXSEL_[1]_[1]_[7:0]							
1103	0x01	DMUXSEL_[1]_[2]_[7:0]							
1104	0x02	DMUXSEL_[1]_[3]_[7:0]							
1105-110F		Unused							
1110	0x07						DX_TRIB_MASK_[4]_[1]	DX_TRIB_MASK_[5]_[1]	DX_TRIB_MASK_[6]_[1]
1111	0x00	Reserved	DX_OUT_INH_[2]	Reserved	Unused				
1112	0x04	DMUXSEL_[2]_[1]_[7:0]							
1113	0x05	DMUXSEL_[2]_[2]_[7:0]							
1114	0x06	DMUXSEL_[2]_[3]_[7:0]							
1115-111F		Unused							
1120	0x07						DX_TRIB_MASK_[7]_[1]	DX_TRIB_MASK_[8]_[1]	DX_TRIB_MASK_[9]_[1]
1121	0x00	Reserved	DX_OUT_INH_[3]	Reserved	Unused				
1122	0x08	DMUXSEL_[3]_[1]_[7:0]							
1123	0x09	DMUXSEL_[3]_[2]_[7:0]							
1124	0x0A	DMUXSEL_[3]_[3]_[7:0]							
1125-112F		Unused							
1130	0x07						DX_TRIB_MASK_[10]_[1]	DX_TRIB_MASK_[11]_[1]	DX_TRIB_MASK_[12]_[1]
1131	0x00	Reserved	DX_OUT_INH_[4]	Reserved	Unused				
1132	0x0C	DMUXSEL_[4]_[1]_[7:0]							
1133	0x0D	DMUXSEL_[4]_[2]_[7:0]							
1134	0x0E	DMUXSEL_[4]_[3]_[7:0]							
1135-113F		Unused							

Table 41. Demux Side Configuration and Summary Status Map

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1140	0x07						DX_TRIB_MASK_[13]_[1]	DX_TRIB_MASK_[14]_[1]	DX_TRIB_MASK_[15]_[1]
1141	0x00	Reserved	DX_OUT_INH_[5]	Reserved	Unused				
1142	0x10	DMUXSEL_[5]_[1]_[7:0]							
1143	0x11	DMUXSEL_[5]_[2]_[7:0]							
1144	0x12	DMUXSEL_[5]_[3]_[7:0]							
1145-114F		Unused							
1150	0x07						DX_TRIB_MASK_[16]_[1]	DX_TRIB_MASK_[1]_[2]	DX_TRIB_MASK_[2]_[2]
1151	0x00	Reserved	DX_OUT_INH_[6]	Reserved	Unused				
1152	0x14	DMUXSEL_[6]_[1]_[7:0]							
1153	0x15	DMUXSEL_[6]_[2]_[7:0]							
1154	0x16	DMUXSEL_[6]_[3]_[7:0]							
1155-115F		Unused							
1160	0x07						DX_TRIB_MASK_[3]_[2]	DX_TRIB_MASK_[4]_[2]	DX_TRIB_MASK_[5]_[2]
1161	0x00	Reserved	DX_OUT_INH_[7]	Reserved	Unused				
1162	0x18	DMUXSEL_[7]_[1]_[7:0]							
1163	0x19	DMUXSEL_[7]_[2]_[7:0]							
1164	0x1A	DMUXSEL_[7]_[3]_[7:0]							
1165-116F		Unused							
1170	0x07						DX_TRIB_MASK_[6]_[2]	DX_TRIB_MASK_[7]_[2]	DX_TRIB_MASK_[8]_[2]
1171	0x00	Reserved	DX_OUT_INH_[8]	Reserved	Unused				
1172	0x1C	DMUXSEL_[8]_[1]_[7:0]							
1173	0x1D	DMUXSEL_[8]_[2]_[7:0]							
1174	0x1E	DMUXSEL_[8]_[3]_[7:0]							
1175-117F		Unused							
1180	0x07						DX_TRIB_MASK_[9]_[2]	DX_TRIB_MASK_[10]_[2]	DX_TRIB_MASK_[11]_[2]
1181	0x00	Reserved	DX_OUT_INH_[9]	Reserved	Unused				
1182	0x20	DMUXSEL_[9]_[1]_[7:0]							
1183	0x21	DMUXSEL_[9]_[2]_[7:0]							
1184	0x22	DMUXSEL_[9]_[3]_[7:0]							
1185-118F		Unused							
1190	0x07						DX_TRIB_MASK_[12]_[2]	DX_TRIB_MASK_[13]_[2]	DX_TRIB_MASK_[14]_[2]
1191	0x00	Reserved	DX_OUT_INH_[10]	Reserved	Unused				
1192	0x24	DMUXSEL_[10]_[1]_[7:0]							

Table 41. Demux Side Configuration and Summary Status Map

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1193	0x25	DMUXSEL_[10]_[2]_[7:0]							
1194	0x26	DMUXSEL_[10]_[3]_[7:0]							
1195-119F		Unused							
11A0	0x07						DX_TRIB_MASK_[15]_[2]	DX_TRIB_MASK_[16]_[2]	DX_TRIB_MASK_[1]_[3]
11A1	0x00	Reserved	DX_OUT_INH_[11]	Reserved	Unused				
11A2	0x28	DMUXSEL_[11]_[1]_[7:0]							
11A3	0x29	DMUXSEL_[11]_[2]_[7:0]							
11A4	0x2A	DMUXSEL_[11]_[3]_[7:0]							
11A5-11AF		Unused							
11B0	0x07						DX_TRIB_MASK_[2]_[3]	DX_TRIB_MASK_[3]_[3]	DX_TRIB_MASK_[4]_[3]
11B1	0x00	Reserved	DX_OUT_INH_[12]	Reserved	Unused				
11B2	0x2C	DMUXSEL_[12]_[1]_[7:0]							
11B3	0x2D	DMUXSEL_[12]_[2]_[7:0]							
11B4	0x2E	DMUXSEL_[12]_[3]_[7:0]							
11B5-11BF		Unused							
11C0	0x07						DX_TRIB_MASK_[5]_[3]	DX_TRIB_MASK_[6]_[3]	DX_TRIB_MASK_[7]_[3]
11C1	0x00	Reserved	DX_OUT_INH_[13]	Reserved	Unused				
11C2	0x30	DMUXSEL_[13]_[1]_[7:0]							
11C3	0x31	DMUXSEL_[13]_[2]_[7:0]							
11C4	0x32	DMUXSEL_[13]_[3]_[7:0]							
11C5-11CF		Unused							
11D0	0x07						DX_TRIB_MASK_[8]_[3]	DX_TRIB_MASK_[9]_[3]	DX_TRIB_MASK_[10]_[3]
11D1	0x00	Reserved	DX_OUT_INH_[14]	Reserved	Unused				
11D2	0x34	DMUXSEL_[14]_[1]_[7:0]							
11D3	0x35	DMUXSEL_[14]_[2]_[7:0]							
11D4	0x36	DMUXSEL_[14]_[3]_[7:0]							
11D5-11DF		Unused							
11E0	0x07						DX_TRIB_MASK_[11]_[3]	DX_TRIB_MASK_[12]_[3]	DX_TRIB_MASK_[13]_[3]
11E1	0x00	Reserved	DX_OUT_INH_[15]	Reserved	Unused				
11E2	0x38	DMUXSEL_[15]_[1]_[7:0]							
11E3	0x39	DMUXSEL_[15]_[2]_[7:0]							
11E4	0x3A	DMUXSEL_[15]_[3]_[7:0]							
11E5-11EF		Unused							

Table 41. Demux Side Configuration and Summary Status Map

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
11F0	0x07						DX_TRIB_ MASK_[14]_[3]	DX_TRIB_ MASK_[15]_[3]	DX_TRIB_ MASK_[16]_[3]
11F1	0x00	Reserved	DX_OUT_INH_ [16]	Reserved	Unused				
11F2	0x3C	DMUXSEL_[16]_[1]_[7:0]							
11F3	0x3D	DMUXSEL_[16]_[2]_[7:0]							
11F4	0x3E	DMUXSEL_[16]_[3]_[7:0]							
11F5-11FF		Unused							

13.2.7 Demultiplexer Side (Addresses 0x1200 through 0x123F)

Table 42. Demux Side Register Address Map for SONET/SDH TOH/SOH Monitoring

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TOH/SOH Delta and Second Event Bits (Read Only, Cleared by microprocessor)									
1200	0x00	DX_B2_ERR_ SF_D	DX_B2_ERR_ SD_D	DX_ LAIS_D	DX_ LRDI_D	DX_K1_D	DX_K1_ UNSTAB_D	DX_K2_D	DX_S1_D
1201	0x00		DX_ LOSEXT_D	DX_ LOS_D	DX_ LOC_D	DX_ OOF_D	DX_ LOF_D	DX_J0_OOF_D	DX_J0_D
1202	0x00			DX_OOF_ SECE	DX_LOF_ SECE	DX_B1ERR_ SECE	DX_B2ERR_ SECE	DX_S1FAIL _SECE	DX_M1ERR_ SECE
1203		Unused							
TOH/SOH Masks and Provisioning Bits (Read/Write)									
1204	0xFF	DX_B2_ERR_ SF_D_ MASK	DX_B2_ERR_ SD_D_ MASK	DX_ LAIS_D_ MASK	DX_ LRDI_D_ MASK	DX_K1_D_ MASK	DX_K1_ UNSTAB_ D_MASK	DX_K2_D_ MASK	DX_S1_D_ MASK
1205	0x7F		DX_ LOSEXT_D_ MASK	DX_ LOS_D_ MASK	DX_ LOC_D_ MASK	DX_ OOF_D_ MASK	DX_ LOF_D_ MASK	DX_J0_ OOF_D_ MASK	DX_J0_D _MASK
1206	0x3F			DX_OOF_SEC E_ MASK	DX_LOF_SEC E_ MASK	DX_B1ERR_S ECE_ MASK	DX_B2ERR_S ECE_ MASK	DX_S1FAIL_SE CE_ MASK	DX_M1ERR_S ECE_ MASK
1207		Unused							
1208	0x50	DX_K2_CONSEC_[3:0]						DX_LOF_ ALG	DX_DSCRINH
1209	0x88	DX_LOSEXT_ INH	DX_LOSEXT_ LEVEL	DX_LOS_INH	DX_FRMR_ INH	DX_LOSEXT_ DELAY_INH	DX_LOS_ALL ZERO_INH	DX_SDH_ S1	DX_SDH_ J0
120A	0x00			DX_FIN_BYTE_TYPE_[1:0]		Reserved			
120B	0x00				DX_LOS_ ALARM_ INH	DX_LAIS_ ALARM_ INH	DX_LOC_ ALARM_ INH	DX_LOF_ ALARM_ INH	DX_OOF_ ALARM_ INH
TOH/SOH Status (Read Only)									
120C	0xC0	DX_B2_ERR_ SF	DX_B2_ERR_ SD	DX_LAIS	DX_LRDI		DX_K1_UNSTA B		
120D	0x0C		DX_LOSEXT	DX_LOS	DX_LOC	DX_OOF	DX_LOF	DX_J0_OOF	

Table 42. Demux Side Register Address Map for SONET/SDH TOH/SOH Monitoring

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
120E-120F		Unused							
1210	0x00	DX_J0_[0]_[7:0]							
1211	0x00	DX_J0_[1]_[7:0]							
1212	0x00	DX_J0_[2]_[7:0]							
1213-121D	0x00	: : :							
121E	0x00	DX_J0_[14]_[7:0]							
121F	0x00	DX_J0_[15]_[7:0]							
1220		Unused							
1221	0x00					DX_S1_[3:0]			
1222	0x00	DX_K2_[7:0]							
1223	0x00	DX_K1_[7:0]							
Signal Fail & Signal Degrade Parameters (Read/Write)									
1224	0x01	DX_B2_BLOCK_SF_[7:0]							
1225		Unused							
1226	0x01	DX_B2_THRESH_SET_SF_[7:0]							
1227	0x01			DX_B2_GROUP_SET_SF_[5:0]					
1228	0x01	DX_B2_THRESH_CLR_SF_[7:0]							
1229	0x01			DX_B2_GROUP_CLR_SF_[5:0]					
122A	0x01	DX_B2_BLOCK_SD_[7:0]							
122B	0x00	DX_B2_BLOCK_SD_[15:8]							
122C	0x01			DX_B2_THRESH_SET_SD_[5:0]					
122D	0x01			DX_B2_GROUP_SET_SD_[5:0]					
122E	0x01			DX_B2_THRESH_CLR_SD_[5:0]					
122F	0x01			DX_B2_GROUP_CLR_SD_[5:0]					
Performance Monitoring Counters (Read Only)									
1230	0x00	DX_B1_ERRCNT_[7:0]							
1231	0x00	DX_B1_ERRCNT_[15:8]							
1232-1233		Unused							
1234	0x00	DX_B2_ERRCNT_[7:0]							
1235	0x00	DX_B2_ERRCNT_[15:8]							
1236	0x00			DX_B2_ERRCNT_[21:16]					
1237		Unused							
1238	0x00	DX_M1_ERRCNT_[7:0]							
1239	0x00	DX_M1_ERRCNT_[15:8]							
123A	0x00			DX_M1_ERRCNT_[21:16]					
123B-123F		Unused							

13.2.8 Demultiplexer Side (Addresses 0x1600 through 0x17FF)

Table 43. Demux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
1600	0x00	DX_CONCAT_[7:0]_D							
1601	0x00	DX_CONCAT_[15:8]_D							
1602	0x00				DX_CONCAT_[20:16]_D				
1603		Unused							
Pointer Interpreter Delta Bit Masks (Read/Write)									
1604	0xFF	DX_CONCAT_[7:0]_D_MASK							
1605	0xFF	DX_CONCAT_[15:8]_D_MASK							
1606	0x1F				DX_CONCAT_[20:16]_D_MASK				
1607		Unused							
Pointer Interpreter Status Bits (Ready Only)									
1608	0x00	DX_CONCAT_[7:0]							
1609	0x00	DX_CONCAT_[15:8]							
160A	0x00				DX_CONCAT_[20:16]				
160B-16FF		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
1700	0x00			DX_LOP_[1]_[1]_D	DX_PAIS_[1]_[1]_D	DX_LOP_[2]_[1]_D	DX_PAIS_[2]_[1]_D	DX_LOP_[3]_[1]_D	DX_PAIS_[3]_[1]_D
1701	0x00			DX_PI_NEGCNT_SECE_[1]_[1]	DX_PI_POSCNT_SECE_[1]_[1]	DX_PI_NEGCNT_SECE_[2]_[1]	DX_PI_POSCNT_SECE_[2]_[1]	DX_PI_NEGCNT_SECE_[3]_[1]	DX_PI_POSCNT_SECE_[3]_[1]
1702-1703		Unused							
Tributary [1] Pointer Interpreter Configuration Bits (Read/Write)									
1704	0x00		DX_SDH_PI_[1]	DX_SS_EN_[1]					
1705		Unused							
Pointer Interpreter Status Bits (Read Only)									
1706	0x00			DX_PTR_STATE_[1]_[1]_[1:0]		DX_PTR_STATE_[1]_[2]_[1:0]		DX_PTR_STATE_[1]_[3]_[1:0]	
1707	0x00			DX_LOP_[1]_[1]	DX_PAIS_[1]_[1]	DX_LOP_[2]_[1]	DX_PAIS_[2]_[1]	DX_LOP_[3]_[1]	DX_PAIS_[3]_[1]
Tributary [1] Pointer Interpreter Counter Bits (Read Only)									
1708	0x00				DX_PI_POSCNT_[1]_[1]_[4:0]				
1709	0x00				DX_PI_NEGCNT_[1]_[1]_[4:0]				
170A	0x00				DX_PI_POSCNT_[1]_[2]_[4:0]				
170B	0x00				DX_PI_NEGCNT_[1]_[2]_[4:0]				
170C	0x00				DX_PI_POSCNT_[1]_[3]_[4:0]				
170D	0x00				DX_PI_NEGCNT_[1]_[3]_[4:0]				
170E-170F		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
1710	0x00			DX_LOP_[4]_[1]_D	DX_PAIS_[4]_[1]_D	DX_LOP_[5]_[1]_D	DX_PAIS_[5]_[1]_D	DX_LOP_[6]_[1]_D	DX_PAIS_[6]_[1]_D

Table 43. Demux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1711	0x00			DX_PI_ NEGCNT_ SECE_[4]_[1]	DX_PI_ POSCNT_ SECE_[4]_[1]	DX_PI_ NEGCNT_ SECE_[5]_[1]	DX_PI_ POSCNT_ SECE_[5]_[1]	DX_PI_ NEGCNT_ SECE_[6]_[1]	DX_PI_ POSCNT_ SECE_[6]_[1]
1712-1713		Unused							
Tributary [2] Pointer Interpreter Configuration Bits (Read/Write)									
1714	0x00		DX_SDH_ PI_[2]	DX_SS_ EN_[2]					
1715		Unused							
Pointer Interpreter Status Bits (Read Only)									
1716	0x00			DX_PTR_STATE_[2]_[1]_[1:0]		DX_PTR_STATE_[2]_[2]_[1:0]		DX_PTR_STATE_[2]_[3]_[1:0]	
1717	0x00			DX_LOP _[4]_[1]	DX_PAIS _[4]_[1]	DX_LOP _[5]_[1]	DX_PAIS _[5]_[1]	DX_LOP _[6]_[1]	DX_PAIS _[6]_[1]
Tributary [2] Pointer Interpreter Counter Bits (Read Only)									
1718	0x00				DX_PI_POSCNT_[2]_[1]_[4:0]				
1719	0x00				DX_PI_NEGCNT_[2]_[1]_[4:0]				
171A	0x00				DX_PI_POSCNT_[2]_[2]_[4:0]				
171B	0x00				DX_PI_NEGCNT_[2]_[2]_[4:0]				
171C	0x00				DX_PI_POSCNT_[2]_[3]_[4:0]				
171D	0x00				DX_PI_NEGCNT_[2]_[3]_[4:0]				
171E-171F		Unused							
1720-17EF		. . .							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
1720	0x00			DX_LOP _[7]_[1]_D	DX_PAIS_ [7]_[1]_D	DX_LOP _[8]_[1]_D	DX_PAIS_ [8]_[1]_D	DX_LOP _[9]_[1]_D	DX_PAIS_ [9]_[1]_D
1721	0x00			DX_PI_ NEGCNT_ SECE_[7]_[1]	DX_PI_ POSCNT_ SECE_[7]_[1]	DX_PI_ NEGCNT_ SECE_[8]_[1]	DX_PI_ POSCNT_ SECE_[8]_[1]	DX_PI_ NEGCNT_ SECE_[9]_[1]	DX_PI_ POSCNT_ SECE_[9]_[1]
1722-1723		Unused							
Tributary [3] Pointer Interpreter Configuration Bits (Read/Write)									
1724	0x00		DX_SDH_ PI_[3]	DX_SS_ EN_[3]					
1725		Unused							
Pointer Interpreter Status Bits (Read Only)									
1726	0x00			DX_PTR_STATE_[3]_[1]_[1:0]		DX_PTR_STATE_[3]_[2]_[1:0]		DX_PTR_STATE_[3]_[3]_[1:0]	
1727	0x00			DX_LOP _[7]_[1]	DX_PAIS _[7]_[1]	DX_LOP _[8]_[1]	DX_PAIS _[8]_[1]	DX_LOP _[9]_[1]	DX_PAIS _[9]_[1]
Tributary [3] Pointer Interpreter Counter Bits (Read Only)									
1728	0x00				DX_PI_POSCNT_[3]_[1]_[4:0]				
1729	0x00				DX_PI_NEGCNT_[3]_[1]_[4:0]				
172A	0x00				DX_PI_POSCNT_[3]_[2]_[4:0]				
172B	0x00				DX_PI_NEGCNT_[3]_[2]_[4:0]				
172C	0x00				DX_PI_POSCNT_[3]_[3]_[4:0]				
172D	0x00				DX_PI_NEGCNT_[3]_[3]_[4:0]				

Table 43. Demux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
172E-172F		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
1730	0x00			DX_LOP_[10]_[1]_D	DX_PAIS_[10]_[1]_D	DX_LOP_[11]_[1]_D	DX_PAIS_[11]_[1]_D	DX_LOP_[12]_[1]_D	DX_PAIS_[12]_[1]_D
1731	0x00			DX_PI_NEGCNT_SECE_[10]_[1]	DX_PI_POSCNT_SECE_[10]_[1]	DX_PI_NEGCNT_SECE_[11]_[1]	DX_PI_POSCNT_SECE_[11]_[1]	DX_PI_NEGCNT_SECE_[12]_[1]	DX_PI_POSCNT_SECE_[12]_[1]
1732-1733		Unused							
Tributary [4] Pointer Interpreter Configuration Bits (Read/Write)									
1734	0x00		DX_SDH_PI_[4]	DX_SS_EN_[4]					
1735		Unused							
Pointer Interpreter Status Bits (Read Only)									
1736	0x00			DX_PTR_STATE_[4]_[1]_[1:0]		DX_PTR_STATE_[4]_[2]_[1:0]		DX_PTR_STATE_[4]_[3]_[1:0]	
1737	0x00			DX_LOP_[10]_[1]	DX_PAIS_[10]_[1]	DX_LOP_[11]_[1]	DX_PAIS_[11]_[1]	DX_LOP_[12]_[1]	DX_PAIS_[12]_[1]
Tributary [4] Pointer Interpreter Counter Bits (Read Only)									
1738	0x00				DX_PI_POSCNT_[4]_[1]_[4:0]				
1739	0x00				DX_PI_NEGCNT_[4]_[1]_[4:0]				
173A	0x00				DX_PI_POSCNT_[4]_[2]_[4:0]				
173B	0x00				DX_PI_NEGCNT_[4]_[2]_[4:0]				
173C	0x00				DX_PI_POSCNT_[4]_[3]_[4:0]				
173D	0x00				DX_PI_NEGCNT_[4]_[3]_[4:0]				
173E-173F		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
1740	0x00			DX_LOP_[13]_[1]_D	DX_PAIS_[13]_[1]_D	DX_LOP_[14]_[1]_D	DX_PAIS_[14]_[1]_D	DX_LOP_[15]_[1]_D	DX_PAIS_[15]_[1]_D
1741	0x00			DX_PI_NEGCNT_SECE_[13]_[1]	DX_PI_POSCNT_SECE_[13]_[1]	DX_PI_NEGCNT_SECE_[14]_[1]	DX_PI_POSCNT_SECE_[14]_[1]	DX_PI_NEGCNT_SECE_[15]_[1]	DX_PI_POSCNT_SECE_[15]_[1]
1742-1743		Unused							
Tributary [5] Pointer Interpreter Configuration Bits (Read/Write)									
1744	0x00		DX_SDH_PI_[5]	DX_SS_EN_[5]					
1745		Unused							
Pointer Interpreter Status Bits (Read Only)									
1746	0x00			DX_PTR_STATE_[5]_[1]_[1:0]		DX_PTR_STATE_[5]_[2]_[1:0]		DX_PTR_STATE_[5]_[3]_[1:0]	
1747	0x00			DX_LOP_[13]_[1]	DX_PAIS_[13]_[1]	DX_LOP_[14]_[1]	DX_PAIS_[14]_[1]	DX_LOP_[15]_[1]	DX_PAIS_[15]_[1]
Tributary [5] Pointer Interpreter Counter Bits (Read Only)									
1748	0x00				DX_PI_POSCNT_[5]_[1]_[4:0]				
1749	0x00				DX_PI_NEGCNT_[5]_[1]_[4:0]				
174A	0x00				DX_PI_POSCNT_[5]_[2]_[4:0]				
174B	0x00				DX_PI_NEGCNT_[5]_[2]_[4:0]				
174C	0x00				DX_PI_POSCNT_[5]_[3]_[4:0]				

Table 43. Demux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
174D	0x00				DX_PI_NEGCNT_[5]_[3]_[4:0]				
174E-174F		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
1750	0x00			DX_LOP_[16]_[1]_D	DX_PAIS_[16]_[1]_D	DX_LOP_[1]_[2]_D	DX_PAIS_[1]_[2]_D	DX_LOP_[2]_[2]_D	DX_PAIS_[2]_[2]_D
1751	0x00			DX_PI_NEGCNT_SECE_[16]_[1]	DX_PI_POSCNT_SECE_[16]_[1]	DX_PI_NEGCNT_SECE_[1]_[2]	DX_PI_POSCNT_SECE_[1]_[2]	DX_PI_NEGCNT_SECE_[2]_[2]	DX_PI_POSCNT_SECE_[2]_[2]
1752-1753		Unused							
Tributary [6] Pointer Interpreter Configuration Bits (Read/Write)									
1754	0x00		DX_SDH_PI_[6]	DX_SS_EN_[6]					
1755		Unused							
Pointer Interpreter Status Bits (Read Only)									
1756	0x00			DX_PTR_STATE_[6]_[1]_[1:0]		DX_PTR_STATE_[6]_[2]_[1:0]		DX_PTR_STATE_[6]_[3]_[1:0]	
1757	0x00			DX_LOP_[16]_[1]	DX_PAIS_[16]_[1]	DX_LOP_[1]_[2]	DX_PAIS_[1]_[2]	DX_LOP_[2]_[2]	DX_PAIS_[2]_[2]
Tributary [6] Pointer Interpreter Counter Bits (Read Only)									
1758	0x00				DX_PI_POSCNT_[6]_[1]_[4:0]				
1759	0x00				DX_PI_NEGCNT_[6]_[1]_[4:0]				
175A	0x00				DX_PI_POSCNT_[6]_[2]_[4:0]				
175B	0x00				DX_PI_NEGCNT_[6]_[2]_[4:0]				
175C	0x00				DX_PI_POSCNT_[6]_[3]_[4:0]				
175D	0x00				DX_PI_NEGCNT_[6]_[3]_[4:0]				
175E-175F		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
1760	0x00			DX_LOP_[3]_[2]_D	DX_PAIS_[3]_[2]_D	DX_LOP_[4]_[2]_D	DX_PAIS_[4]_[2]_D	DX_LOP_[5]_[2]_D	DX_PAIS_[5]_[2]_D
1761	0x00			DX_PI_NEGCNT_SECE_[3]_[2]	DX_PI_POSCNT_SECE_[3]_[2]	DX_PI_NEGCNT_SECE_[4]_[2]	DX_PI_POSCNT_SECE_[4]_[2]	DX_PI_NEGCNT_SECE_[5]_[2]	DX_PI_POSCNT_SECE_[5]_[2]
1762-1763		Unused							
Tributary [7] Pointer Interpreter Configuration Bits (Read/Write)									
1764	0x00		DX_SDH_PI_[7]	DX_SS_EN_[7]					
1765		Unused							
Pointer Interpreter Status Bits (Read Only)									
1766	0x00			DX_PTR_STATE_[7]_[1]_[1:0]		DX_PTR_STATE_[7]_[2]_[1:0]		DX_PTR_STATE_[7]_[3]_[1:0]	
1767	0x00			DX_LOP_[3]_[2]	DX_PAIS_[3]_[2]	DX_LOP_[4]_[2]	DX_PAIS_[4]_[2]	DX_LOP_[5]_[2]	DX_PAIS_[5]_[2]
Tributary [7] Pointer Interpreter Counter Bits (Read Only)									
1768	0x00				DX_PI_POSCNT_[7]_[1]_[4:0]				
1769	0x00				DX_PI_NEGCNT_[7]_[1]_[4:0]				
176A	0x00				DX_PI_POSCNT_[7]_[2]_[4:0]				
176B	0x00				DX_PI_NEGCNT_[7]_[2]_[4:0]				

Table 43. Demux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
176C	0x00				DX_PI_POSCNT_[7]_[3]_[4:0]				
176D	0x00				DX_PI_NEGCNT_[7]_[3]_[4:0]				
176E-176F		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
1770	0x00			DX_LOP_[6]_[2]_D	DX_PAIS_[6]_[2]_D	DX_LOP_[7]_[2]_D	DX_PAIS_[7]_[2]_D	DX_LOP_[8]_[2]_D	DX_PAIS_[8]_[2]_D
1771	0x00			DX_PI_NEGCNT_SECE_[6]_[2]	DX_PI_POSCNT_SECE_[6]_[2]	DX_PI_NEGCNT_SECE_[7]_[2]	DX_PI_POSCNT_SECE_[7]_[2]	DX_PI_NEGCNT_SECE_[8]_[2]	DX_PI_POSCNT_SECE_[8]_[2]
1772-1773		Unused							
Tributary [8] Pointer Interpreter Configuration Bits (Read/Write)									
1774	0x00		DX_SDH_PI_[8]	DX_SS_EN_[8]					
1775		Unused							
Pointer Interpreter Status Bits (Read Only)									
1776	0x00			DX_PTR_STATE_[8]_[1]_[1:0]		DX_PTR_STATE_[8]_[2]_[1:0]		DX_PTR_STATE_[8]_[3]_[1:0]	
1777	0x00			DX_LOP_[6]_[2]	DX_PAIS_[6]_[2]	DX_LOP_[7]_[2]	DX_PAIS_[7]_[2]	DX_LOP_[8]_[2]	DX_PAIS_[8]_[2]
Tributary [8] Pointer Interpreter Counter Bits (Read Only)									
1778	0x00				DX_PI_POSCNT_[8]_[1]_[4:0]				
1779	0x00				DX_PI_NEGCNT_[8]_[1]_[4:0]				
177A	0x00				DX_PI_POSCNT_[8]_[2]_[4:0]				
177B	0x00				DX_PI_NEGCNT_[8]_[2]_[4:0]				
177C	0x00				DX_PI_POSCNT_[8]_[3]_[4:0]				
177D	0x00				DX_PI_NEGCNT_[8]_[3]_[4:0]				
177E-177F		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
1780	0x00			DX_LOP_[9]_[2]_D	DX_PAIS_[9]_[2]_D	DX_LOP_[10]_[2]_D	DX_PAIS_[10]_[2]_D	DX_LOP_[11]_[2]_D	DX_PAIS_[11]_[2]_D
1781	0x00			DX_PI_NEGCNT_SECE_[9]_[2]	DX_PI_POSCNT_SECE_[9]_[2]	DX_PI_NEGCNT_SECE_[10]_[2]	DX_PI_POSCNT_SECE_[10]_[2]	DX_PI_NEGCNT_SECE_[11]_[2]	DX_PI_POSCNT_SECE_[11]_[2]
1782-1783		Unused							
Tributary [9] Pointer Interpreter Configuration Bits (Read/Write)									
1784	0x00		DX_SDH_PI_[9]	DX_SS_EN_[9]					
1785		Unused							
Pointer Interpreter Status Bits (Read Only)									
1786	0x00			DX_PTR_STATE_[9]_[1]_[1:0]		DX_PTR_STATE_[9]_[2]_[1:0]		DX_PTR_STATE_[9]_[3]_[1:0]	
1787	0x00			DX_LOP_[9]_[2]	DX_PAIS_[9]_[2]	DX_LOP_[10]_[2]	DX_PAIS_[10]_[2]	DX_LOP_[11]_[2]	DX_PAIS_[11]_[2]
Tributary [9] Pointer Interpreter Counter Bits (Read Only)									
1788	0x00				DX_PI_POSCNT_[9]_[1]_[4:0]				
1789	0x00				DX_PI_NEGCNT_[9]_[1]_[4:0]				
178A	0x00				DX_PI_POSCNT_[9]_[2]_[4:0]				

Table 43. Demux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
178B	0x00				DX_PI_NEGCNT_[9]_[2]_[4:0]				
178C	0x00				DX_PI_POSCNT_[9]_[3]_[4:0]				
178D	0x00				DX_PI_NEGCNT_[9]_[3]_[4:0]				
178E-178F		Unused							
[10] Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
1790	0x00			DX_LOP_[12]_[2]_D	DX_PAIS_[12]_[2]_D	DX_LOP_[13]_[2]_D	DX_PAIS_[13]_[2]_D	DX_LOP_[14]_[2]_D	DX_PAIS_[14]_[2]_D
1791	0x00			DX_PI_NEGCNT_SECE_[12]_[2]	DX_PI_POSCNT_SECE_[12]_[2]	DX_PI_NEGCNT_SECE_[13]_[2]	DX_PI_POSCNT_SECE_[13]_[2]	DX_PI_NEGCNT_SECE_[14]_[2]	DX_PI_POSCNT_SECE_[14]_[2]
1792-1793		Unused							
Tributary [10] Pointer Interpreter Configuration Bits (Read/Write)									
1794	0x00		DX_SDH_PI_[10]	DX_SS_EN_[10]					
1795		Unused							
Pointer Interpreter Status Bits (Read Only)									
1796	0x00			DX_PTR_STATE_[10]_[1]_[1:0]		DX_PTR_STATE_[10]_[2]_[1:0]		DX_PTR_STATE_[10]_[3]_[1:0]	
1797	0x00			DX_LOP_[12]_[2]	DX_PAIS_[12]_[2]	X_LOP_[13]_[2]	DX_PAIS_[13]_[2]	DX_LOP_[14]_[2]	DX_PAIS_[14]_[2]
Tributary [10] Pointer Interpreter Counter Bits (Read Only)									
1798	0x00				DX_PI_POSCNT_[10]_[1]_[4:0]				
1799	0x00				DX_PI_NEGCNT_[10]_[1]_[4:0]				
179A	0x00				DX_PI_POSCNT_[10]_[2]_[4:0]				
179B	0x00				DX_PI_NEGCNT_[10]_[2]_[4:0]				
179C	0x00				DX_PI_POSCNT_[10]_[3]_[4:0]				
179D	0x00				DX_PI_NEGCNT_[10]_[3]_[4:0]				
179E-179F		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
17A0	0x00			DX_LOP_[15]_[2]_D	DX_PAIS_[15]_[2]_D	X_LOP_[16]_[2]_D	DX_PAIS_[16]_[2]_D	DX_LOP_[1]_[3]_D	DX_PAIS_[1]_[3]_D
17A1	0x00			DX_PI_NEGCNT_SECE_[15]_[2]	DX_PI_POSCNT_SECE_[15]_[2]	DX_PI_NEGCNT_SECE_[16]_[2]	DX_PI_POSCNT_SECE_[16]_[2]	DX_PI_NEGCNT_SECE_[1]_[3]	DX_PI_POSCNT_SECE_[1]_[3]
17A2-17A3		Unused							
Tributary [11] Pointer Interpreter Configuration Bits (Read/Write)									
17A4	0x00		DX_SDH_PI_[11]	DX_SS_EN_[11]					
17A5		Unused							
Pointer Interpreter Status Bits (Read Only)									
17A6	0x00			DX_PTR_STATE_[11]_[1]_[1:0]		DX_PTR_STATE_[11]_[2]_[1:0]		DX_PTR_STATE_[11]_[3]_[1:0]	
17A7	0x00			DX_LOP_[15]_[2]	DX_PAIS_[15]_[2]	DX_LOP_[16]_[2]	DX_PAIS_[16]_[2]	DX_LOP_[1]_[3]	DX_PAIS_[1]_[3]
Tributary [11] Pointer Interpreter Counter Bits (Read Only)									
17A8	0x00				DX_PI_POSCNT_[11]_[1]_[4:0]				
17A9	0x00				DX_PI_NEGCNT_[11]_[1]_[4:0]				

Table 43. Demux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
17AA	0x00				DX_PI_POSCNT_[11]_[2]_[4:0]				
17AB	0x00				DX_PI_NEGCNT_[11]_[2]_[4:0]				
17AC	0x00				DX_PI_POSCNT_[11]_[3]_[4:0]				
17AD	0x00				DX_PI_NEGCNT_[11]_[3]_[4:0]				
17AE-17AF		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
17B0	0x00			DX_LOP_[2]_[3]_D	DX_PAIS_[2]_[3]_D	DX_LOP_[3]_[3]_D	DX_PAIS_[3]_[3]_D	DX_LOP_[4]_[3]_D	DX_PAIS_[4]_[3]_D
17B1	0x00			DX_PI_NEGCNT_SECE_[2]_[3]	DX_PI_POSCNT_SECE_[2]_[3]	DX_PI_NEGCNT_SECE_[3]_[3]	DX_PI_POSCNT_SECE_[3]_[3]	DX_PI_NEGCNT_SECE_[4]_[3]	DX_PI_POSCNT_SECE_[4]_[3]
17B2-17B3		Unused							
Tributary [12] Pointer Interpreter Configuration Bits (Read/Write)									
17B4	0x00		DX_SDH_PI_[12]	DX_SS_EN_[12]					
17B5		Unused							
Pointer Interpreter Status Bits (Read Only)									
17B6	0x00			DX_PTR_STATE_[12]_[1]_[1:0]		DX_PTR_STATE_[12]_[2]_[1:0]		DX_PTR_STATE_[12]_[3]_[1:0]	
17B7	0x00			DX_LOP_[2]_[3]	DX_PAIS_[2]_[3]	DX_LOP_[3]_[3]	DX_PAIS_[3]_[3]	DX_LOP_[4]_[3]	DX_PAIS_[4]_[3]
Tributary [12] Pointer Interpreter Counter Bits (Read Only)									
17B8	0x00				DX_PI_POSCNT_[12]_[1]_[4:0]				
17B9	0x00				DX_PI_NEGCNT_[12]_[1]_[4:0]				
17BA	0x00				DX_PI_POSCNT_[12]_[2]_[4:0]				
17BB	0x00				DX_PI_NEGCNT_[12]_[2]_[4:0]				
17BC	0x00				DX_PI_POSCNT_[12]_[3]_[4:0]				
17BD	0x00				DX_PI_NEGCNT_[12]_[3]_[4:0]				
17BE-17BF		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
17C0	0x00			DX_LOP_[5]_[3]_D	DX_PAIS_[5]_[3]_D	DX_LOP_[6]_[3]_D	DX_PAIS_[6]_[3]_D	DX_LOP_[7]_[3]_D	DX_PAIS_[7]_[3]_D
17C1	0x00			DX_PI_NEGCNT_SECE_[5]_[3]	DX_PI_POSCNT_SECE_[5]_[3]	DX_PI_NEGCNT_SECE_[6]_[3]	DX_PI_POSCNT_SECE_[6]_[3]	DX_PI_NEGCNT_SECE_[7]_[3]	DX_PI_POSCNT_SECE_[7]_[3]
17C2-17C3		Unused							
Tributary [13] Pointer Interpreter Configuration Bits (Read/Write)									
17C4	0x00		DX_SDH_PI_[13]	DX_SS_EN_[13]					
17C5		Unused							
Pointer Interpreter Status Bits (Read Only)									
17C6	0x00			DX_PTR_STATE_[13]_[1]_[1:0]		DX_PTR_STATE_[13]_[2]_[1:0]		DX_PTR_STATE_[13]_[3]_[1:0]	
17C7	0x00			DX_LOP_[5]_[3]	DX_PAIS_[5]_[3]	DX_LOP_[6]_[3]	DX_PAIS_[6]_[3]	DX_LOP_[7]_[3]	DX_PAIS_[7]_[3]
Tributary [13] Pointer Interpreter Counter Bits (Read Only)									
17C8	0x00				DX_PI_POSCNT_[13]_[1]_[4:0]				

Table 43. Demux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
17C9	0x00				DX_PI_NEGCNT_[13]_[1]_[4:0]				
17CA	0x00				DX_PI_POSCNT_[13]_[2]_[4:0]				
17CB	0x00				DX_PI_NEGCNT_[13]_[2]_[4:0]				
17CC	0x00				DX_PI_POSCNT_[13]_[3]_[4:0]				
17CD	0x00				DX_PI_NEGCNT_[13]_[3]_[4:0]				
17CE-17CF		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
17D0	0x00			DX_LOP_[8]_[3]_D	DX_PAIS_[8]_[3]_D	DX_LOP_[9]_[3]_D	DX_PAIS_[9]_[3]_D	DX_LOP_[10]_[3]_D	DX_PAIS_[10]_[3]_D
17D1	0x00			DX_PI_NEGCNT_SECE_[8]_[3]	DX_PI_POSCNT_SECE_[8]_[3]	DX_PI_NEGCNT_SECE_[9]_[3]	DX_PI_POSCNT_SECE_[9]_[3]	DX_PI_NEGCNT_SECE_[10]_[3]	DX_PI_POSCNT_SECE_[10]_[3]
17D2-17D3		Unused							
Tributary [14] Pointer Interpreter Configuration Bits (Read/Write)									
17D4	0x00		DX_SDH_PI_[14]	DX_SS_EN_[14]					
17D5		Unused							
Pointer Interpreter Status Bits (Read Only)									
17D6	0x00			DX_PTR_STATE_[14]_[1]_[1:0]		DX_PTR_STATE_[14]_[2]_[1:0]		DX_PTR_STATE_[14]_[3]_[1:0]	
17D7	0x00			DX_LOP_[8]_[3]	DX_PAIS_[8]_[3]	DX_LOP_[9]_[3]	DX_PAIS_[9]_[3]	DX_LOP_[10]_[3]	DX_PAIS_[10]_[3]
Tributary [14] Pointer Interpreter Counter Bits (Read Only)									
17D8	0x00				DX_PI_POSCNT_[14]_[1]_[4:0]				
17D9	0x00				DX_PI_NEGCNT_[14]_[1]_[4:0]				
17DA	0x00				DX_PI_POSCNT_[14]_[2]_[4:0]				
17DB	0x00				DX_PI_NEGCNT_[14]_[2]_[4:0]				
17DC	0x00				DX_PI_POSCNT_[14]_[3]_[4:0]				
17DD	0x00				DX_PI_NEGCNT_[14]_[3]_[4:0]				
17DE-17DF		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
17E0	0x00			DX_LOP_[11]_[3]_D	DX_PAIS_[11]_[3]_D	DX_LOP_[12]_[3]_D	DX_PAIS_[12]_[3]_D	DX_LOP_[13]_[3]_D	DX_PAIS_[13]_[3]_D
17E1	0x00			DX_PI_NEGCNT_SECE_[11]_[3]	DX_PI_POSCNT_SECE_[11]_[3]	DX_PI_NEGCNT_SECE_[12]_[3]	DX_PI_POSCNT_SECE_[12]_[3]	DX_PI_NEGCNT_SECE_[13]_[3]	DX_PI_POSCNT_SECE_[13]_[3]
17E2-17E3		Unused							
Tributary [15] Pointer Interpreter Configuration Bits (Read/Write)									
17E4	0x00		DX_SDH_PI_[15]	DX_SS_EN_[15]					
17E5		Unused							
Pointer Interpreter Status Bits (Read Only)									
17E6	0x00			DX_PTR_STATE_[15]_[1]_[1:0]		DX_PTR_STATE_[15]_[2]_[1:0]		DX_PTR_STATE_[15]_[3]_[1:0]	
17E7	0x00			DX_LOP_[11]_[3]	DX_PAIS_[11]_[3]	DX_LOP_[12]_[3]	DX_PAIS_[12]_[3]	DX_LOP_[13]_[3]	DX_PAIS_[13]_[3]
Tributary [15] Pointer Interpreter Counter Bits (Read Only)									

Table 43. Demux Side Register Address Map for SONET/SDH Pointer Interpreter

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
17E8	0x00				DX_PI_POSCNT_[15]_[1]_[4:0]				
17E9	0x00				DX_PI_NEGCNT_[15]_[1]_[4:0]				
17EA	0x00				DX_PI_POSCNT_[15]_[2]_[4:0]				
17EB	0x00				DX_PI_NEGCNT_[15]_[2]_[4:0]				
17EC	0x00				DX_PI_POSCNT_[15]_[3]_[4:0]				
17ED	0x00				DX_PI_NEGCNT_[15]_[3]_[4:0]				
17EE-17EF		Unused							
Pointer Interpreter Delta Bits (Read Only, cleared by microprocessor)									
17F0	0x00			DX_LOP_[14]_[3]_D	DX_PAIS_[14]_[3]_D	DX_LOP_[15]_[3]_D	DX_PAIS_[15]_[3]_D	DX_LOP_[16]_[3]_D	DX_PAIS_[16]_[3]_D
17F1	0x00			DX_PI_NEGCNT_SECE_[14]_[3]	DX_PI_POSCNT_SECE_[14]_[3]	DX_PI_NEGCNT_SECE_[15]_[3]	DX_PI_POSCNT_SECE_[15]_[3]	DX_PI_NEGCNT_SECE_[16]_[3]	DX_PI_POSCNT_SECE_[16]_[3]
17F2-17F3		Unused							
Tributary [16] Pointer Interpreter Configuration Bits (Read/Write)									
17F4	0x00		DX_SDH_PI_[16]	DX_SS_EN_[16]					
17F5		Unused							
Pointer Interpreter Status Bits (Read Only)									
17F6	0x00			DX_PTR_STATE_[16]_[1]_[1:0]		DX_PTR_STATE_[16]_[2]_[1:0]		DX_PTR_STATE_[16]_[3]_[1:0]	
17F7	0x00			DX_LOP_[14]_[3]	DX_PAIS_[14]_[3]	DX_LOP_[15]_[3]	DX_PAIS_[15]_[3]	DX_LOP_[16]_[3]	DX_PAIS_[16]_[3]
Tributary [16] Pointer Interpreter Counter Bits (Read Only)									
17F8	0x00				DX_PI_POSCNT_[16]_[1]_[4:0]				
17F9	0x00				DX_PI_NEGCNT_[16]_[1]_[4:0]				
17FA	0x00				DX_PI_POSCNT_[16]_[2]_[4:0]				
17FB	0x00				DX_PI_NEGCNT_[16]_[2]_[4:0]				
17FC	0x00				DX_PI_POSCNT_[16]_[3]_[4:0]				
17FD	0x00				DX_PI_NEGCNT_[16]_[3]_[4:0]				
17FE-17FF		Unused							

* Designates those registers which use only a single control bit, the bit associated with tributary [i] = 1. This bit controls the corresponding function for all tributaries.

13.2.9 Demultiplexer Side (Addresses 0x1800 through 0x19FF)

Table 44. Demux Side Register Address Map for SONET/SDH Pointer Generator

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1800-18FF		Unused							
Tributary [1] Pointer Generator Event Bits (Read Only, cleared by microprocessor)									

Table 44. Demux Side Register Address Map for SONET/SDH Pointer Generator

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1900	0x00			DX_PG_ NEGCNT_ SECE_[1]_[1]	DX_PG_ POSCNT_ SECE_[1]_[1]	DX_PG_ NEGCNT_ SECE_[1]_[2]	DX_PG_ POSCNT_ SECE_[1]_[2]	DX_PG_ NEGCNT_ SECE_[1]_[3]	DX_PG_ POSCNT_ SECE_[1]_[3]
1901		Unused							
1902	0x00						DX_PG_FIFO_ [1]_[1]_E	DX_PG_FIFO_ [1]_[2]_E	DX_PG_FIFO_ [1]_[3]_E
1903		Unused							
Tributary [1] Pointer Generator Configuration Bits (Read/Write)									
1904	0x00		DX_SF_PAIS_ INH*	DX_UNEQ_ GEN_[1]_[1]	DX_PAIS_GEN _[1]_[1]	DX_UNEQ_ GEN_[1]_[2]	DX_PAIS_GEN _[1]_[2]	DX_UNEQ_ GEN_[1]_[3]	DX_PAIS_GEN _[1]_[3]
1905	0x00		DX_SDH_PG_ [1]	DX_FAST_AIS _[1]_[1]		DX_FAST_AIS _[1]_[2]		DX_FAST_AIS _[1]_[3]	
1906-1907		Unused							
Tributary [1] Pointer Generator Counter Bits (Read Only)									
1908	0x00				DX_PG_POSCNT_[1]_[1]_[4:0]				
1909	0x00				DX_PG_NEGCNT_[1]_[1]_[4:0]				
190A	0x00				DX_PG_POSCNT_[1]_[2]_[4:0]				
190B	0x00				DX_PG_NEGCNT_[1]_[2]_[4:0]				
190C	0x00				DX_PG_POSCNT_[1]_[3]_[4:0]				
190D	0x00				DX_PG_NEGCNT_[1]_[3]_[4:0]				
190E-190F		Unused							
Tributary [2] Pointer Generator Event Bits (Read Only, cleared by microprocessor)									
1910	0x00			DX_PG_ NEGCNT_ SECE_[2]_[1]	DX_PG_ POSCNT_ SECE_[2]_[1]	DX_PG_ NEGCNT_ SECE_[2]_[2]	DX_PG_ POSCNT_ SECE_[2]_[2]	DX_PG_ NEGCNT_ SECE_[2]_[3]	DX_PG_ POSCNT_ SECE_[2]_[3]
1911		Unused							
1912	0x00						DX_PG_FIFO _[2]_[1]_E	DX_PG_FIFO _[2]_[2]_E	DX_PG_FIFO _[2]_[3]_E
1913		Unused							
Tributary [2] Pointer Generator Configuration Bits (Read/Write)									
1914	0x00		Reserved	DX_UNEQ_ GEN_[2]_[1]	DX_PAIS_GEN _[2]_[1]	DX_UNEQ_ GEN_[2]_[2]	DX_PAIS_GEN _[2]_[2]	DX_UNEQ_ GEN_[2]_[3]	DX_PAIS_GEN _[2]_[3]
1915	0x00		DX_SDH_PG_ [2]	DX_FAST_AIS _[2]_[1]		DX_FAST_AIS _[2]_[2]		DX_FAST_AIS _[2]_[3]	
1916-1917		Unused							
Tributary [2] Pointer Generator Counter Bits (Read Only)									
1918	0x00				DX_PG_POSCNT_[2]_[1]_[4:0]				
1919	0x00				DX_PG_NEGCNT_[2]_[1]_[4:0]				
191A	0x00				DX_PG_POSCNT_[2]_[2]_[4:0]				
191B	0x00				DX_PG_NEGCNT_[2]_[2]_[4:0]				
191C	0x00				DX_PG_POSCNT_[2]_[3]_[4:0]				
191D	0x00				DX_PG_NEGCNT_[2]_[3]_[4:0]				
191E-191F		Unused							
1920-19EF	0x00	. . .							
Tributary [16] Pointer Generator Event Bits (Read Only, cleared by microprocessor)									

Table 44. Demux Side Register Address Map for SONET/SDH Pointer Generator

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
19F0	0x00			DX_PG_ NEGCNT_ SECE_[16]_[1]	DX_PG_ POSCNT_ SECE_[16]_[1]	DX_PG_ NEGCNT_ SECE_[16]_[2]	DX_PG_ POSCNT_ SECE_[16]_[2]	DX_PG_ NEGCNT_ SECE_[16]_[3]	DX_PG_ POSCNT_ SECE_[16]_[3]
19F1		Unused							
19F2	0x00						DX_PG_FIFO _[16]_[1]_E	DX_PG_FIFO _[16]_[2]_E	DX_PG_FIFO _[16]_[3]_E
19F3		Unused							
Tributary [16] Pointer Generator Configuration Bits (Read/Write)									
19F4	0x00		Reserved	DX_UNEQ_ GEN_[16]_[1]	DX_PAIS_GEN _[16]_[1]	DX_UNEQ_ GEN_[16]_[2]	DX_PAIS_GEN _[16]_[2]	DX_UNEQ_ GEN_[16]_[3]	DX_PAIS_GEN _[16]_[3]
19F5	0x00		DX_SDH_PG_ [16]	DX_FAST_AIS _[16]_[1]		DX_FAST_AIS _[16]_[2]		DX_FAST_AIS _[16]_[3]	
19F6- 19F7		Unused							
Tributary [16] Pointer Generator Counter Bits (Read Only)									
19F8	0x00				DX_PG_POSCNT_[16]_[1]_[4:0]				
19F9	0x00				DX_PG_NEGCNT_[16]_[1]_[4:0]				
19FA	0x00				DX_PG_POSCNT_[16]_[2]_[4:0]				
19FB	0x00				DX_PG_NEGCNT_[16]_[2]_[4:0]				
19FC	0x00				DX_PG_POSCNT_[16]_[3]_[4:0]				
19FD	0x00				DX_PG_NEGCNT_[16]_[3]_[4:0]				
19FE- 19FF		Unused							

* Designates those registers which use only a single control bit, the bit associated with tributary [i] = 1. This bit controls the corresponding function for all tributaries.

13.2.10 Demultiplexer Side (Addresses 0x1A00 through 0x1BFF)

Table 45. Demux Side Register Address Map for SONET/SDH TOH/SOH Provisioning and Scrambler Inhibit

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Signal 1 SONET/SDH Line/MS AIS Generation Control, Scrambler Inhibit, and TOH/SOH Provisioning (Read/Write)									
1A00	0x00	DX_A1A2_ERR _[1]	DX_A1A2_ERR_NUM_[1]_[2:0]			DX_B1_INV_[1]	DX_B2_INV_[1]	DX_M1GEN_ ERR_[1]	DX_SCRINH _[1]
1A01	0x00	DX_LAIS_GEN _[1]	Reserved	DX_K1K2_ APS_[1]	DX_K2_ 3LSB_[1]			DX_LRDI_INH_ [1]	DX_LREI_INH_ [1]
1A02	0x00	DX_A1A2_ERR_PAT_[1]_[7:0]							
1A03	0x00	DX_A1A2_ERR_PAT_[1]_[15:8]							
1A04	0x01	DX_J0_[1]_[0]_[7:0]							
1A05	0x01	DX_J0_[1]_[1]_[7:0]							
1A06	0x01	DX_J0_[1]_[2]_[7:0]							
1A07	0x01	DX_J0_[1]_[3]_[7:0]							
1A08	0x01	DX_J0_[1]_[4]_[7:0]							
1A09	0x01	DX_J0_[1]_[5]_[7:0]							
1A0A	0x01	DX_J0_[1]_[6]_[7:0]							
1A0B	0x01	DX_J0_[1]_[7]_[7:0]							

Table 45. Demux Side Register Address Map for SONET/SDH TOH/SOH Provisioning and Scrambler Inhibit

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1A0C	0x01	DX_J0_[1]_[8]_[7:0]							
1A0D	0x01	DX_J0_[1]_[9]_[7:0]							
1A0E	0x01	DX_J0_[1]_[10]_[7:0]							
1A0F	0x01	DX_J0_[1]_[11]_[7:0]							
1A10	0x01	DX_J0_[1]_[12]_[7:0]							
1A11	0x01	DX_J0_[1]_[13]_[7:0]							
1A12	0x01	DX_J0_[1]_[14]_[7:0]							
1A13	0x01	DX_J0_[1]_[15]_[7:0]							
1A14	0x00	DX_K2GEN_[1]_[7:0]							
1A15	0x00	DX_K1GEN_[1]_[7:0]							
1A16	0x00	DX_S1GEN_[1]_[7:0]							
1A17	0x00	DX_FRAME_IN_INH**	Reserved	Reserved		Reserved			
1A18-1A1F		Unused							
Signal [2] SONET/SDH Line/MS AIS Generation Control, Scrambler Inhibit, and TOH/SOH Provisioning (Read/Write)									
1A20-1A3F		Same as 0x1A00 through 0x1A1F with i=2, except for **							
Signal [3] SONET/SDH Line/MS AIS Generation Control, Scrambler Inhibit, and TOH/SOH Provisioning (Read/Write)									
1A40-1A5F		Same as 0x1A1F through 0x1A1F with i=3, except for **							
1A60 - 1B9F		. . .							
Signal [16] SONET/SDH Line/MS AIS Generation Control, Scrambler Inhibit, and TOH/SOH Provisioning (Read/Write)									
1BE0-1BFF		Same as 0x1A00 through 0x1A1F with i=16, except for **							

** Only 1 active register - register in map for signal [1] controls all tributaries. Register location in maps for signals [2] through [16] are “Reserved.”

13.2.11 Device ID (Address 0x1FFF)

Table 46. Device Identification Code

Addr	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device Identification Code (Read Only)									
1FFF	0x04	DEV_ID_[7:0]							

14.0 Appendix

14.1 User Notes

14.1.1 Low Speed Line Interface

14.1.1.1 Unmatched propagation delays in OC-48 mode on Low Speed Side data lines

Issue:

When the Missouri's low speed side is configured for OC-48 mode operation, the channels normally associated with serial OC-12 rates (i.e., 1, 5, 9, & 13) have propagation delays much shorter than the other 12 data lines, relative to the SYS_CLK_IN signal.

Description:

The Missouri's low speed side can operate in either serial OC-3 or OC-12 modes or in a parallel OC-48 mode. Four of the data lines are shared between the serial and parallel operation modes. Due to the design implementation of the Missouri, the four data lines DX_DATA_OUT 1,5,9,13 associated with the OC-12 mode, have much shorter propagation delays, relative to the SYS_CLK_IN signal, than the other 12 data lines when the Missouri is configured for OC-48 mode. As a result, there is not enough hold time on channels 1,5,9,13 to ensure that the receiving device can latch the data in with the rising edge of DX_CLK_OUT_155 (DX_CLK_OUT_[2]).

Possible System Implication.

Without adjusting either the DX_DATA_OUT data lines (1,5,9,13) or DX_CLK_OUT_155 (DX_CLK_OUT_[2]) the Missouri cannot work in the OC-48 mode on the low speed side.

Solution or User Workaround:

Use external flip-flops and re-time the DX_DATA_OUT channels (1,5,9,13) to the inverted version of DX_CLK_OUT_155 (DX_CLK_OUT_[2]) signal. This will enable sufficient setup/hold time to enable the four data lines to be latched into the receiving device along with the other 12 data lines.

14.1.2 APS Interface

14.1.2.1 Default settings on the MX/DX_PROT_CLK_OUT_INV register bits are incorrect

Issue:

The default settings on the MX/DX_PROT_CLK_OUT_INV register bits are incorrect. They should default to a Logic "1". If the protection ports are used without software configuring the MX/DX_PROT_CLK_OUT_INV register bits to a Logic "1" after reset, the protection ports may experience data errors.

Description:

The default settings on the protection MX/DX_PROT_CLK_OUT_INV register bits are incorrect. As a result, they provide inadequate Hold timing margins and cause Protection Port data errors.

Possible System Implication:

The MX/DX Protection ports may not transfer data error free if the MX/DX_PROT_CLK_OUT_INV register bits are not set to a Logic “1” after reset. As a result, Automatic Protection Switching may not operate correctly.

Solution or User workaround:

After a hardware (RSTB) or software (MASTER_RESET) reset, the MX/DX_PROT_CLK_OUT_INV register bits should be set to a Logic “1”. This will ensure sufficient Setup and Hold Margin on the Protection Ports data busses.

14.1.2.2 MX Channel #1 is the only contributor to APS_INTB

Issue:

On the MX side of the Missouri, the MX_APS_INT[1] is the only contributor to the APS_INTB.

Description:

On the MX side of the Missouri, the internal signals MX_APS_INT[2:16] do not contribute to the generation of the APS_INT. Only MX_APS_INT[1] contributes to the APS_INT signal.

Possible System Implication:

The APS_INT signal enables system designers to more quickly respond to an APS event (K1/K2 bytes). System designers can still respond to APS events (K1/K2 bytes) via Missouri’s INTB signal. The internal signals MX_APS_INT[1-16] do correctly contribute to the INTB interrupt signal. As a result, system designers will need to use the Missouri’s INTB signal to detect an APS (K1/K2) event.

Solution or User workaround:

SW can still respond quickly to an APS event, by developing the Interrupt Routine to first determine if an APS event has occurred.

14.1.3 Input Line Monitor

14.1.3.1 MX/DX_LOSEXT_DELAY function does not operate correctly

Issue:

The MX/DX_LOSEXT_DELAY function does not operate.

Description:

This function delayed the MX/DX_LOSEXT signal by 3.29 usecs before causing the LOS condition to be reported by the Missouri. The default condition is to have the MX/DX_LOSEXT

signal immediately cause the Missouri to report the LOS condition

Possible System Implication:

The lack of this function should not be an issue since most E/O and SERDES devices already provide a delayed Signal Degrade signal into the MX/DX_LOSEXT input. The default condition of the Missouri is to have the MX/DX_LOSEXT signal immediately cause the report of the LOS condition

Solution or User workaround:

Software should ensure that the MX/DX_LOS_DELAY_INH register bits are always inhibited and System/Board designers should ensure that the signal to the MX/DX_LOSEXT input provides the appropriate delay from when a Fiber Cut/Signal Degrade occurs.

14.1.3.2 LOC Detection Logic is Unreliable

Issue:

The LOC detection logic on all Receive ports is unreliable.

Description:

In some cases, when there is a LOC condition on a Line Interface, the Missouri may not recognize the event.

Possible System Implication:

The system SW may not recognize the fact that an LOC condition has occurred on a Line interface.

Solution or User workaround:

Ultimately the system will want to know if there has been a Fiber Cut/LOS/LOF or OOF condition. A LOC condition is only one of the alarms that will indicate one of these events. The LOSEXT input and the LOS/LOF/OOF alarm signals will also be able to notify the system SW that a Line condition has occurred. The optics/SERDES device can still provide an EXTLOS input to all receive channels to indicate an LOS event, and the Frame Monitor logic will detect a LOF/OOF condition.

14.1.3.3 LEVEL control (DX/MX_LOSEXT_LEVEL) for External LOS does not function properly

Issue:

Level control of MX/DX_LOSEXT_LEVEL register bit for external LOS does not function per the specification.

Description:

The contents of LOSEXT should be (LOSEXT_IN(pin) XOR LOSEXT_LEVEL), however LOSEXT_LEVEL has no effect on LOSEXT. Instead, LOSEXT_LEVEL inverts the sense of the LOSEXT contribution to LOS.

The actual behavior is:

LOSEXT = LOSEXT_IN(pin)

LOS = ((LOSEXT XOR LOSEXT_LEVEL) && !LOSEXT_INH)

This same behavior is present on the sixteen MX and single DX inputs.

Possible System Implication:

There could be a misinterpretation of the DX/MX_LOSEXT registers.

Solution or User Workaround:

Although the above description is not the correct behavior, the user can still control what sense of the external pin (MX/DX_LOSEXT_IN) contributes to MX/DX_LOS and the MX/DX_ALARM_OUT output signals.

14.1.4 TOH Generation

14.1.4.1 RDI does not respond properly upon removal of LOS/LOF/LAIS

Issue:

The RDI condition is not necessarily removed within one frame of the removal of an LOS/LOF/LAIS condition.

Description:

GR253 specifies that the RDI condition should be removed within one frame of removal of received LOS,LOF, or LAIS conditions, provided the 20 frame minimum criterion has been met.

The Missouri always adds the 20 frames of RDI after the removal of the LOS, LOF or LAIS condition, even when the 20 frame minimum has been met.

Possible System Implication:

If the assertion of the RDI condition is brief, then the Missouri properly keeps the condition asserted for 20 frames. If in the case where the assertion of the RDI is relatively long, the Missouri's extension of the RDI condition, as an additional percentage of time, should be negligible.

Solution or User workaround:

There is no work around.

14.1.5 Pointer Processor

14.1.5.1 MX/DX_PG_FIFO_x_E - Pointer Generator FIFO over/underflow condition

Issue:

The DX/MX_PG_FIFO_x_E device register bits do not match the Missouri Product Specification's memory map. The DX/MX_PG_FIFO_x_E register bits indicate if there has been an overflow or underflow condition in the Pointer Generator FIFOs.

Description:

When the Missouri is configured with STS-1 payloads and the Pointer Generator FIFO(s) either overflow or underflow, DX/MX_PG_FIFO_x_E occur at the proper tributary locations in the memory map.

When the Missouri is configured with STS-3c payloads and the Pointer Generator FIFO(s) either overflow or underflow, the DX/MX_PG_FIFO_x_E event bit occurs at the improper tributary location in the memory map. For example, instead of occurring at MX_PG_FIFO_[1]_[1]_E, it occurs at _[1]_[3].

When the Missouri is configured with STS-12c payloads and the Pointer Generator FIFO(s) either overflow or underflow, the DX/MX_PG_FIFO_x_E event bit occurs at the improper tributary location in the memory map. For example, instead of occurring at MX_PG_FIFO_[1]_[1]_E, it occurs at _[4]_[3].

When the Missouri is configured with STS-48c payloads and the Pointer Generator FIFO(s) either overflow or underflow, the DX/MX_PG_FIFO_x_E event bit occurs at the improper tributary location in the memory map. For example, instead of occurring at MX_PG_FIFO_[1]_[1]_E, it occurs at _[16]_[3].

Possible System Implication:

If one or more of the Missouri's Pointer Generator FIFOs have an underflow or overflow condition, the system may not see it or may see it at the wrong tributary location. As a result, the system may not respond correctly to the alarm event.

Solution or User workaround:

Software will need to look at the locations MX/DX_PG_FIFO _[1]_[3], _[2]_[3], ... , [16]_[3] for proper error indications with STS-3c payload types.

Software will need to look at the locations MX/DX_PG_FIFO _[4]_[3], _[8]_[3], ... , [16]_[3] for proper error indications with STS-12c payload types.

Software will need to look at the locations MX/DX_PG_FIFO [16]_[3] for proper error indications with STS-48c payload types.

14.1.5.2 PAIS and LOP reporting for STS-3 inputs is not correct for some input ports

Issue:

The MX Pointer Interpreter reporting for PAIS and LOP is not reliable for STS-3 inputs that arrive on ports 6, 7, 9, 10, 11, 13, 14, and 15.

Description:

The MX Pointer Interpreter reporting for PAIS and LOP is not reliable for STS-3 inputs that arrive on ports 6, 7, 9, 10, 11, 13, 14, and 15. In order for channels 6 and 7 to be reported properly, port 8 must have a clock input. Similarly, channels 9, 10, and 11 require a clock from channel 12; and channels 13, 14, and 15 require a clock from channel 16.

Without these clocks, the reporting of PAIS and LOP for the impacted channels stays at their last state. After reset, these states are inactive in the STS-3 line input mode. The true state can be determined from the PTR_STATE_x registers, but it is the PAIS and LOP registers themselves that contribute to the generation of outgoing PAIS.

Possible System Implication:

The High Speed OC-48 output will output a PAIS/LOP condition for the specific OC-3 tributary even though there is a valid OC-3 signal being fed into the device.

Solution or User workaround:

In order for channels 6 and 7 to be reported properly, port 8 must have a clock input. Similarly, channels 9, 10, and 11 require a clock from channel 12; and channels 13, 14, and 15 require a clock from channel 16.

The other alternative is to perform a MX_STATE_RESET.

14.1.6 Clocking

14.1.6.1 OC-48 mode on Low Speed side requires 155 MHz System clock

Issue:

The S4802 Product Specification indicates that the Missouri can operate off of either a 155 or 622 MHz SYS_CLK_IN signal. The SYS_CLK_IN signal *must* be supplied with a 155 MHz clock signal when the low speed side is configured for STS-48/STM-16.

Description:

The current S4802 Advanced Product Specification indicates that the Missouri can operate off of either a 155 or 622 MHz clock. It further indicates that if all of the inputs are either STS-3/STM-1 signals or a parallel STS-48/STM-16 signal that SYS_CLK_IN *can* be 155 MHz.

To further clarify, in order for the Low Speed to operate correctly in STS-48/STM-16 mode, the SYS_CLK_IN signal *must* be supplied with a 155 MHz clock signal.

Possible System Implication:

Missouri will not operate in STS-48/STM-16 mode on the low speed side if SYS_CLK_IN does not have a 155 MHz clock input.

Solution or User Workaround:

The product specification will need to clarify that when in STS-48/STM-16 mode on the low speed side, the SYS_CLK_IN must be 155 MHz.

14.1.6.2 MX_CLK_OUT Disabled when DX_STATE_RESET asserted

Issue:

Assertion of DX_STATE_RESET disables MX_CLK_OUT

Description:

When the register bit DX_STATE_RESET is asserted MX_CLK_OUT is disabled. The DX_STATE_RESET is used to initialize the internal state machines and counters associated with the demultiplex side of the Missouri device.

Possible System Implication:

If the DX_STATE_RESET is applied, the MX_CLK_OUT will be disabled and the high speed (OC-48) transmit side will be effectively shut down.

Solution or User workaround:

Normally the DX_STATE_RESET register bit does not need to be set. It is typically used for test purposes. If the Missouri requires a reset, either the RSTB signal should be asserted or the MASTER_RESET register bit should be set. Either of these resets will initialize all Missouri state machines and counters and clear all register bits to their default value.

14.1.7 Synchronization

14.1.7.1 MX and DX are not synchronized upon power-up or reset

Issue:

Upon power-up or reset, the internal frame positions on MX and DX of Missouri is not synchronized

Description:

The internal SONET/SDH frame positions on the MX and DX side of Missouri is not synchronized upon power-up or after RSTB pin reset or MX/DX_STATE_RESET software reset.

Possible System Implication:

This problem affects the following loopbacks:

- Lowspeed side MX-to-DX via DX cross-connect selection
- Highspeed side DX-to-MX via MX cross-connect selection

If Missouri is configured in either of the above loopback configuration, then the output frames would be corrupted. The pointer and payload would be shifted relative to the output TOH.

Solution or User workaround:

To overcome this issue, a “resync” operation needs to be performed upon power-up or aforementioned resets for only one time until another power cycle or reset occurs.

A “resync” operation requires the following sequence of events in the following order:

- The register SYS_SYNC_IN_RESYNC at address 0x1019 bit 0 needs to be written from 0 to 1.
- The input pin SYS_SYNC_IN needs to be pulsed from logic ‘0’ to ‘1’ i.e. providing a rising edge.

Once the SYS_SYNC_IN_RESYNC register is written, Missouri is “armed” to look for the next rising edge input from SYS_SYNC_IN pin and succeeding transitions on the pin will be ignored. Once a rising edge is received after the register is provisioned, Missouri will synchronize its internal frame position generator and then flywheel on this frame position.

14.1.8 Miscellaneous

14.1.8.1 JTAG - TRSTB input signal

Issue:

TRSTB must be pulsed low in order for Missouri to operate correctly.

Description:

The TRSTB must be pulsed low in order for Missouri to operate correctly. If the TRSTB is not driven/pulsed low after power up the Missouri will not be able to be initialized via the microprocessor interface. The assertion of TRSTB puts the JTAG circuitry into its test logic reset state.

Possible System Implication:

Missouri will not be able to operate without TRSTB asserted low after power up. As a result, system will not function.

Solution or User workaround:

Supply a logic “0” pulse to TRSTB after power up.

14.1.8.2 Unspecified GPIO behavior in mixed input/output configurations

Issues:

(1) In certain configurations the GPIO registers that are configured as inputs do not update upon logic level change at the corresponding GPIO pin.

(2) In certain configurations the GPIO registers that are configured as outputs change value when other registers are read or written.

Description:

(1) There are 16 GPIOs in the Missouri, namely GPIO[15:0]. The 8 GPIOs, GPIO[15:8], are located at address 0x0035 and the remaining 8 GPIOs, GPIO[7:0] are located at address 0x0034. These GPIO pins can be configured for input or output by provisioning a control register, GPIOCTL[8:1]. If GPIOCTL[n]=1 then an input from the corresponding pin is expected; else it is an output.

If GPIO[11:8] and GPIO[3:0] are configured for input and the remaining GPIOs are configured for output then a read of address 0x0035 or 0x0034 will not return the value currently present at their corresponding pins. Instead the previous value is returned.

In the following configurations this issue does NOT exist:

- GPIO[15:0] set as all inputs/outputs
- GPIO[7:0] set as all inputs/outputs and/or GPIO[15:0] set as all inputs/outputs
- GPIO[15:12] are inputs and GPIO[11:8] are outputs and/or GPIO[7:4] are inputs and GPIO[3:0] are outputs (issue 2)

(2) If GPIO [15:12] are configured as inputs and GPIO[11:0] as outputs, then the values on the output GPIO lines will change as different registers are read or written to. The value coming out of the output GPIO lines will be what is on the uP bus at that instant.

Possible System Implication:

This should be a non-issue since either an appropriate configuration can be selected where there are no problems or the workaround detailed below can be applied.

Solution or User workaround:

(1) To read the correct value from GPIO[11:8] or GPIO[3:0] when the aforementioned problematic configuration is used, first write to the register, 0x0035 or 0x0034, with previous value (returned on first read) and then read the same register upon which the current value presented at the corresponding pins will be returned.

(2) When using GPIO lines are configured as outputs, the entire 8 bits controlled by GPIOCTL8 (i.e., GPIO[15:8]) or GPIOCTL4 (i.e., GPIO[7:0]) should be configured as outputs by setting GPIOCTL[8:5]=”0000” or GPIOCTL[4:1]=”0000,” respectively. SImilarly, when GPIO lines are configured as inputs, the 8-bit word controlled by GPIOCTL8 (i.e., GPIO[15:8]) or GPIOCTL4 (i.e., GPIO[7:0]) should be configured as inputs by setting GPIOCTL[8:5]=”1111” or GPIOCTL[4:1]=”1111,” respectively.

14.1.8.3 Register 0x0102 bit 0 stuck at 1

Issue:

Read from register 0x0102 will always return 1 for bit 0.

Description:

Address 0x0102 is the MUXSEL_[1]_[1] register which provisions the MX cross-connect tributary (1,1).

This register can be written to properly including bit 0. A read to the register returns on bits [7:1] the value that was previously written but bit 0 always returns a 1. However, the correct value is written to bit 0. In other words, bit 0 can still be provisioned to 0 or 1 properly and only the read is affected.

Possible System Implication:

Software will not be able to determine the value provisioned on bit 0 of address 0x0102. The MX cross-connect can be provisioned properly for tributary (1,1) hence there is no system impact.

Solution or User workaround:

Ignore value returned in bit 0 of 0x0102 on a read.

14.1.8.4 Device version register

Issue:

The value of the DEV_VER register (address 0x0002) was not incremented properly to correspond with Missouri respin.

Description:

The following are the DEV_VER register values per Missouri version:

Missouri version	DEV_VER
1.0	00
1.1	00
1.2	01

Possible System Implication:

Software cannot distinguish between version 1.0 and 1.1 of Missouri

Solution or User workaround:

There is no workaround for software to distinguish between v1.0 and v1.1. Software would have to note that the DEV_VER value for Missouri v1.2 is 0x01 instead of the expected 0x02.

Index of Registers

15.0 Index of Registers

KEY:

In this index, primary entries are registers that appear in text and include a definition of the register. Secondary (indented) registers in this index refer to registers in the Memory Map tables.

C

D

Index of Registers

Index of Registers

Index of Registers

Index of Registers

Index of Registers

Index of Registers

G

L

M

Index of Registers

Index of Registers

Index of Registers

Index of Registers

Index of Registers

Index of Registers

Index of Registers

R

S

16. Ordering and Packaging Information

Ordering information for Missouri: S4802CBI12.

Table 47. Part Number decoding of S4802CBI12

Missouri: S4802CBI12	Definition
S	S = Standard (Integrated Circuit)
4802	Missouri model number
CBI	Packaging information: C = Ceramic B = Ball I = Industrial (temperature)
12	Revision number of the Missouri device: 1.2

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