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AKM

=Preliminary=

AK2399

π/4 Shift QPSK MODEM for Digital Cordless Telephone

Overview

The AK2399 is a modem LSI for digital cordless telephones and corresponds to the standard for second-generation cordless telephone systems (RCR STD-28). The modulation part is composed of a base band filter for band limitation (root Nyquist roll-off filter), differential logic circuit, D/A converter, etc. The demodulation circuit is composed of the differential demodulation circuit, the bit synchronization circuit, the clock recovery circuit, etc. The AK2399 additionally includes the RSSI circuit, receiving AFC circuit and an D/A converter for APC, and size reduction for the mobile handset can be realized easily.

Features

Modulation Part
- ☐ Transmission speed: 384 kbps
- ☐ Roll-off filter (digital filter + analog filter)
  - * Root Nyquist characteristic: α = 0.5 (Japan)
  - * Pass band (3 dB): 96 kHz
  - * Stop band attenuation: 60 dB or more (600 kHz detuning)
    65 dB or more (900 kHz and more)
- ☐ Modulation accuracy: 3% rms or less
- ☐ Built-in ramp response circuit
- ☐ Built-in D/A converter
- ☐ Built-in output level adjustment circuit
- ☐ Built-in DC offset voltage adjustment circuit
- ☐ Built-in differential logic circuit corresponding to the π /4 shift QPSK modulation

APC Part (power control)
- ☐ Built-in 9 bit DAC for level setting
- ☐ Built-in 9 bit DAC for level control

Demodulation Part
- ☐ IF input frequency: 10.8 MHz, 1.5 Vp-p
- ☐ Differential demodulation
- ☐ Built-in clock recovery and bit synchronization circuit

RSSI Part
- ☐ Built-in gain/offset adjustment circuit
- ☐ 8 bit ADC
- ☐ 3 comparators

Others
- ☐ Built-in reference voltage generation circuits
- ☐ Master clock: 19.2 MHz
- ☐ Low power supply voltage operation: 2.7 to 3.6 V, single power supply
- ☐ Package: 64 pin LQFP

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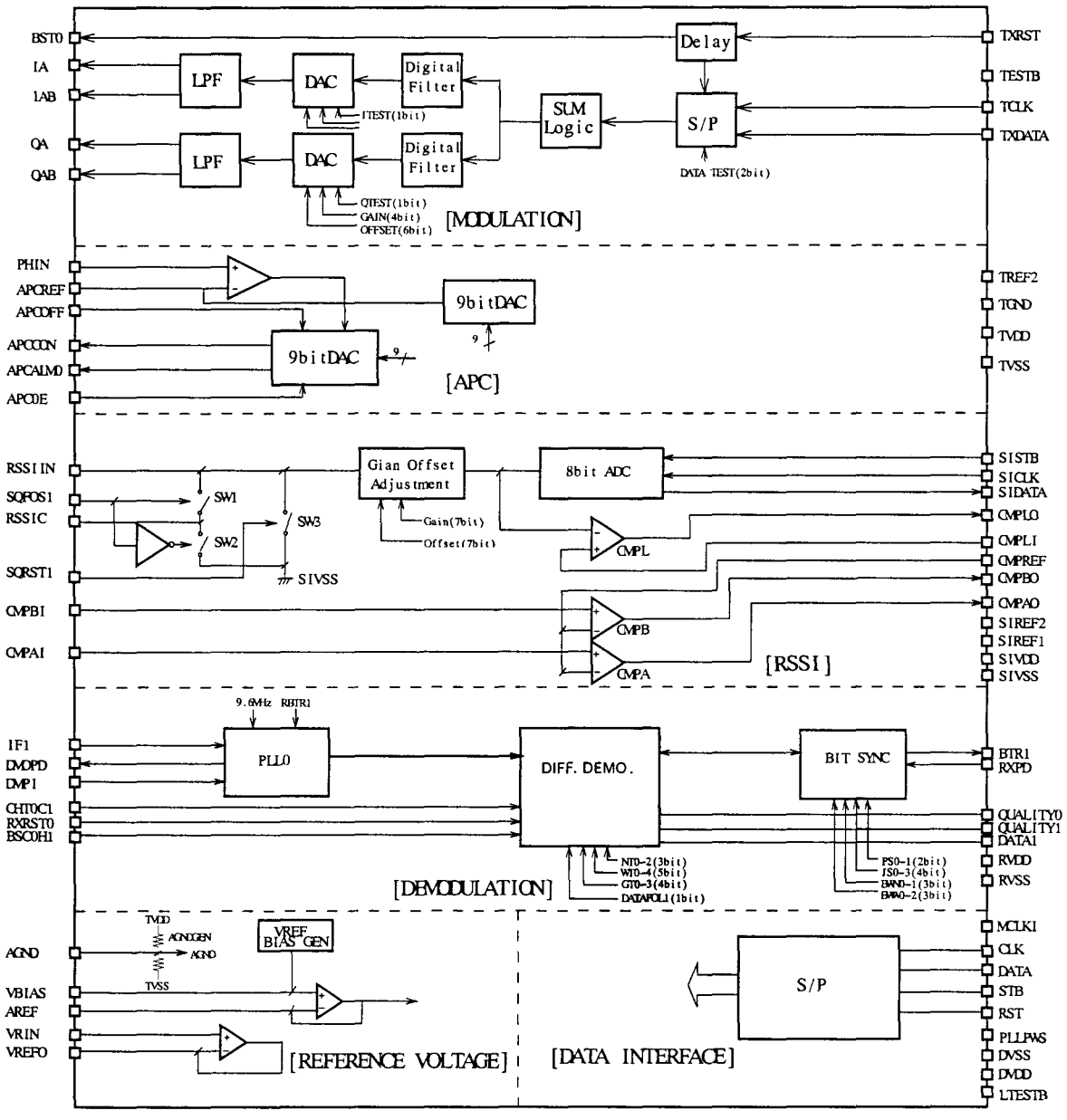
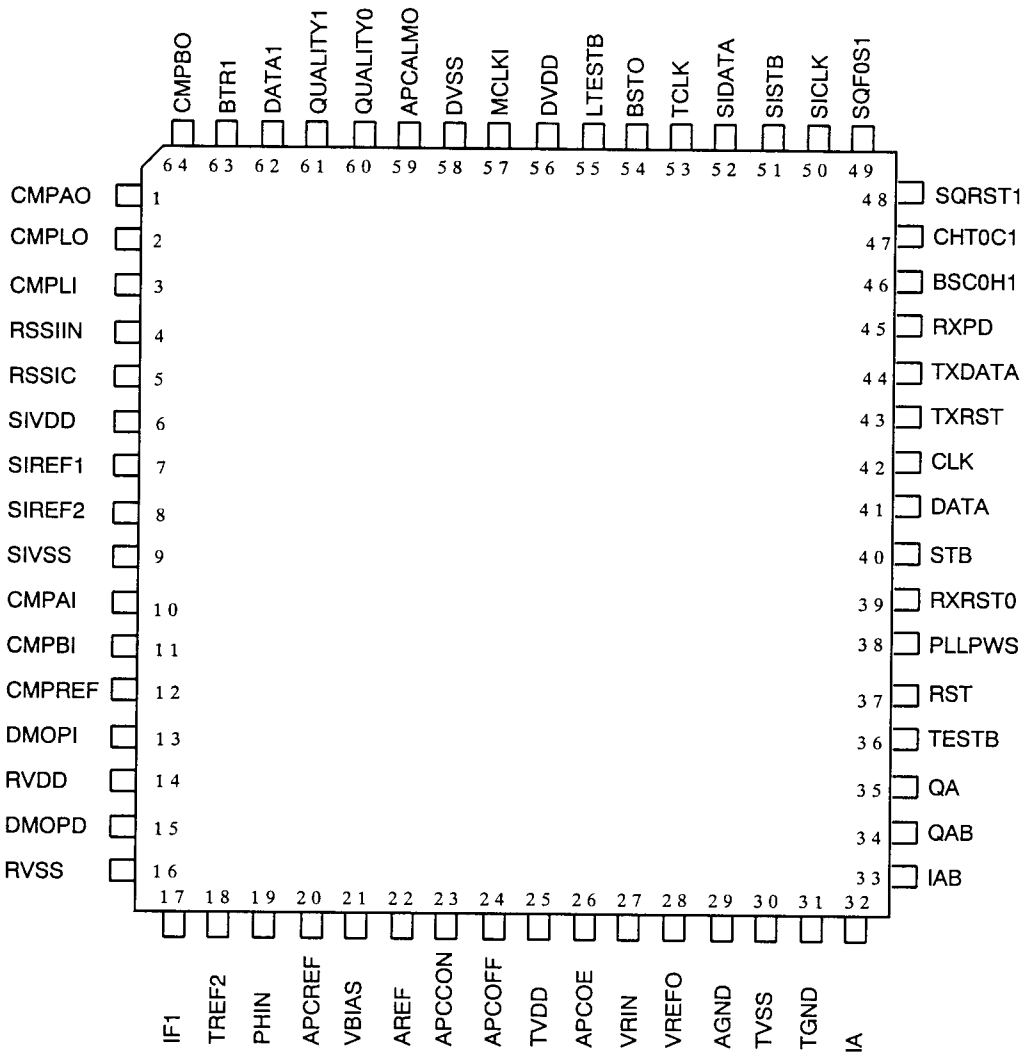
Block Diagram



Pin Configuration

(TOP VIEW)



Pin Functions

Pin No.	Pin Name	I/O	Function	Remark
Data Setting Part				
42	CLK	DI	Clock input pin for data input. This is synchronized to the rise of the clock while the STB input is low level, and the status of the DATA pin is taken in to the shift register.	
41	DATA	DI	Data input pin for control register setting. Data for rewriting the various control registers in the IC are given as input.	
40	STB	DI	Writing enable signal input pin. When this input is made low level, the clock input from the CLK pin is enabled.	
37	RST	DI	Reset signal input pin. Control register resetting is executed by low-level input. After power ON, set to low level once before start of operation.	
38	PLLPWS	DI	Power-down signal input pin. This IC becomes PDO by low-level input, and only the data setting part reaches operation status. By high-level input, this IC reaches a status other than PDO.	
56	DVDD	PWR	Power supply pin for digital circuits.	
58	DVSS	GND	Ground pin for digital circuits.	
System Clock Input				
57	MCLKI	AI2	Main clock input pin. DC cut is executed for the 19.2 MHz clock, and it is given as input. High impedance is obtained with PDO.	Note1

Pin No.	Pin Name	I/O	Function	Remark
RSSI Part				
4	RSSIIN	AI1	RSSI signal input pin. This is the input pin for gain and offset adjustment circuit. This becomes direct input to the SCF circuit in the IC.	Note2
49	SQFOS1	DI	RSSI load adjustment signal input pin. SW1 becomes ON by high-level input, and RSSIC and RSSIIN become connected. SW2 becomes ON by low-level input, and RSSIC and SIVSS becomes connected.	
5	RSSIC	AO	RSSI load connection pin. This is used to adjust the load of RSSIIN by input from SQFOS1. Normally, a capacitor is connected between this and SIVSS.	
48	SQRST1	DI	RSSI reset signal input pin. RSSIIN and SIVSS are connected by high-level input.	
7	SIREF1	AO	RSSI reference level output pins. Output of about 1 V from SIREF1 and output of about 2 V from SIREF2is executed. Connect a capacitor of 1μ between SIREF1/SIREF2 and SIVSS. With PD00, SIREF1 becomeshigh impedance, and SIREF2 becomes low level.	Note3
8	SIREF2	AO		
51	SISTB	DI	A/D conversion start signal input pin. A/D conversion is started by the rise of this input.	
50	SICLK	DI	Clock input signal for A/D data output. Synchronized to the rise of the input clock, the A/D conversion result is put out to SIDATA.	
52	SIDATA	DO1	A/D data output pin. Low-level output is executed for PDn (n = 0 to 2, 4).	Note4
3	CMPLI	AI1	Input pin for electric field strength setting This is connected to the positive input of CMPL.	Note5
10	CMPAI	AI1	Comparator positive input pin. This is connected to the positive input of CMPA and CMPB.	Note5
11	CMPBI	AI1		
12	CMPREF	AI1	Comparison level input pin. This is connected to the negative input of CMPA and CMPB.	Note5
2	CMPLO	DO1	Electric field strength judgement result output pin. High-level output is executed when the output of the gain/offset adjustment circuit is smaller that the input to CMPLI (large RSSIIN input level) . Low-level output is executed for PDn (n=0 to 2, , 4).	Note4
1	CMPAO	DO1	Comparison result output pin. CMPAO/CMPBO becomes high-level when the input level to CMPAI, CMPBI is larger than the input to CMPREF. Low-level output is executed for PDn (n = 0 to 2, 4).	Note4
64	CMPBO	DO1		
6	SIVDD	PWR	Power supply pin for the RSSI part.	
9	SIVSS	GND	Ground power supply pin for the RSSI part.	

Pin No.	Pin Name	I/O	Function	Remark
Demodulation part				
17	IF1	AI2	Limiter signal input pin. DC cut is executed for the output signal from the limiter, and this is given as input. Please use a 220 pF capacitor for the DC cut. High impedance is obtained except for PD30.	Note6
47	CHTOC1	DI	Reception burst types signal input pin. UW = 16 bit mode is obtained with low-level input, and UW = 32 bit mode is obtained with high-level input.	
39	RXRSTO	DI	Demodulation part reset signal input pin. At the time of low-level input, the IC assumes PD00 or PD1X status, and at the time of high-level input, the IC assumes PDn (n = 2 to 4) status and power-down release is executed for the demodulation part.	
45	RXPD	DI	Demodulation part clock stop signal input pin. When RXRST is high level, the IC assumes PD2 or PD4 status with low-level input, and with high-level input, the IC assumes PD3 status and the demodulation part starts operation. When RXRSTO is low level, the status of this input pin is disregarded, and low-level input is assumed.	
46	BSCOH1	DI	Bit synchronization operation control signal input pin. At the time of low-level input, the bit synchronization operation assumes control status, and at the time of high-level input, the bit synchronization operation assumes hold status.	
60 61	QUARITY0 QUARITY1	DO1	Reception data quality signal output pin. The output status changes synchronized to the rise of BTR1. Low-level output is executed for PD0 and PD1. For PD2 and PD4, the output is fixed to high or low.	Note4
62	DATA1	DO1	Reception data output pin. The reception data are put out synchronized to the rise of BTR1. Low-level output is executed for PD0 and PD1. For PD2 and PD4, the output is fixed to high or low.	Note4
63	BTR1	DO1	Reception regeneration clock output pin. Low-level output is executed for PD0 and PD1. For PD2 and PD4, 384 kHz free running clock output is executed. For PD3, regeneration clock output is executed.	Note4
15	DMOPD	DO2	PLL0-VCO charge pump output pin. Output of low level when the VCO oscillation frequency must be speeded up, output of high level when the VCO oscillation frequency must be slowed down, and output of high impedance when the VCO frequency must not be changed.	Note7
13	DMOPI	AI1	PLL0-VCO control input pin. The VCO oscillation frequency slows down with increasing input level.	Note5
14	RVDD	PWR	Power supply for PLL0.	
16	RVSS	GND	Ground for PLL0.	

Pin No.	Pin Name	I/O	Function	
			Modulation part	
43	TXRST	DI	Modulation part reset signal input pin. With high-level input while RXRST0 is high level and RXPD is low level, PD4 is obtained and power-down release is executed. Execute input synchronized to the rise of the TCLK input clock.	
53	TCLK	DI	Transmission clock input. Execute input of a 384 kHz clock.	
44	TXDATA	DI	Transmission data input pin. The input pin status is taken in with the drop of the TCLK input clock.	
36	TESTB	DI	Test mode control pin. The modulation part enters test mode with low-level input. (Pull-up inernaly)	
54	BST0	DO1	Burst indication signal output pin. The burst position during I, Q analog output is indicated. Low-level output is executed for PDX (n = 0 to 3).	Note4
32	IA	AO	$\pi/4$ shift QPSK modulator in-phase component output pin. This is differential output.	Note8
33	IAB	AO	High impedance is obtained for PDn (n=0, 1, 2, 3).	
35	QA	AO	$\pi/4$ shift QPSK modulator quadrature-phase component output pin. This is differential output.	Note8
34	QAB	AO	High impedance is obtained for PDn (n=0, 1, 2, 3).	
23	APCCON	AO	APC control output pin. This is the 9 bit DA output for transmission output level control, and the output level can be changed when it is necessary to change the input level to APCOFF. Power-down occurs for PD0/1 and low level output is executed. During modulation part power-down (PD2, PD3), the output level of the previous burst (PD4) is held.	Note9
26	APCOE	DI	APCCON output conrol pin. APCCON output is always low level when APCOE is level. It takes 10μsec from APCOE release to I, Q stabilization.	
24	APCOFF	AI1	APC output offset input pin. By changing the level to this input, the output level from APCCON can be changed. When the input level to this input pin is increased, the APCCON output level will increase.	Note5
20	APCRFF	AO	APC setting pin. When APCREN1 is "1", the transmission output level setting will become the internal setting, and this pin will become the monitor pin for the 9 bit DA output for transmission output level setting. At this time, power-down is executed and high impedance is obtained. Please set APCREN1 always to 1.	Note4
59	APCALM0	DO1	APC alarm output pin. When the 9 bit DA value for transmission output level control has becomes MAX (1FFH) or MIN (000H), low-level output is executed. For PD0, power-down is executed and high-level output is executed.	Note4

Pin No.	Pin Name	I/O	Function	Remark
Modulation part (continued)				
18	TREF2	AO	Modulation reference level output pin. Output of about 2 V is executed from TREF2. Connect a 1 μ capacitor between TREF2 and TVSS. For PD00, TREF2 becomes low level.	Note10
19	PHIN	AI1	Transmission output level input pin. When the input level is smaller than the level of the APCREF pin, the APCCON output level is increased.	Note5
31	TGND	AO	Modulation part analog ground output pin. Normally, a 1 μ capacitor is connected between this and TVSS. High impedance is obtained for PD0.	Note10
25	TVDD		Power supply pin for the modulation part analog circuit.	
30	TVSS		Ground pin for the modulation part analog circuit.	
Reference voltages				
29	AGND	AO	Reference analog ground output pin. Normally, a 1000 pF capacitor is connected between this and TVSS. High impedance is obtained for PD0.	Note11
22	AREF	AO	Reference level output pin. Output of about 1.2 V is executed. Connect a 0.01 μ capacitor between AREF and TVSS. High impedance is obtained for PD0.	Note12
27	VRIN	AI1	Reference level input level.	Note13
28	VRFE0	AO	Reference buffer output pin. This is the voltage follower output of the VRIN input. High impedance is obtained for PD0.	Note14
21	VBIAS	AO	Bias voltage output pin. Normally, a 47 kΩ resistance is connected between this and TVSS.	Note15
Others				
55	LTESTB	DI	Test Pin. Open at normal usage.	

I/O

AO	Analog output
AI1	Analog input 1
AI2	Analog input 2
DO1	Digital output 1
DO2	Digital output 2
DI	Digital input
PWR	Power supply
GND	Ground

Note1: Input capacitance 11pF max., Input resistance 30k Ω min.
DC cut input is required.
Note2: Input capacitance 53pF max., Input resistance 300k Ω min.
Input to the SCF circuit.
Note3: Load capacitance 1 μ F typ., 1 μ F capacitor is required between this pin and SIVSS.
Note4: Load capacitance 15pF max.
Note5: Input capacitance 11pF max., Input resistance 300k Ω min.
Note6: Input capacitance 11pF max., Input resistance 300k Ω min.
DC cut input via 220pF is required.
Note7: Load capacitance 15pF max. 3 state output.
Note8: Load capacitance 20pF max. Load resistance to analog ground is 5k Ω min.
Note9: Load capacitance 15pF max. Output current +/−150 μ A max.
Note10: Load capacitance 1 μ F typ., 1 μ F capacitor is required between this pin and TVSS.
Note11: Load capacitance 1nF typ.
1000pF capacitor is required between this pin and TVSS.
Note12: Load capacitance 0.01 μ F typ.
0.01 μ F capacitor is required between this pin and TVSS.
Note13: Input capacitance 15pF max., Input resistance 300k Ω min.
Note14: Load capacitance 15pF max. Output current +/−100 μ A max.
Note15: Load capacitance 15pF max. Load resistance 47k Ω typ.
The resister within 5% error is required between this pin and TVSS.

Absolute Maximum Ratings

Item	Symbol	min.	max.	Unit	Remarks
Power supply Voltage (VDD)	DVDD, SIVDD, RVDD, TVDD	-0.3	7.0	V	TVDD >= Other VDD
Ground level (VSS)	DVSS, SIVSS, RVSS, TVSS	0	0	V	Voltage reference level
Input voltage	V_{IN}	-0.3	TVDD+0.3	V	
Input current	I_{IN}	-10	+10	mA	
Storage temperature	T_{stg}	-50	125	℃	
Soldering temperature	T_{sol}		260 x 10	℃xsec	For manual soldering

Recommended Operating Conditions

Item	Symbol	min.	typ.	max.	Unit
Power supply voltage	VDD	2.7		3.6	V
Operation temperature	Ta	-20		70	℃

Electrical Characteristics

1) DC characteristics

Item	Symbol	Pin	Condition	min.	Typ.	max.	Unit
Current consumption	I_{DD00}		PD0		0.1	20	μA
	I_{DD10}		PD1		3.4	8.0	mA
	I_{DD20}		PD2		3.7	8.0	mA
	I_{DD30}		PD3		4.6	10.0	mA
	I_{DD40}		PD4		8.6	18.0	mA
High-level output current	I_{OH}	DO1	VDD-0.5V	-0.5			mA
		DO2	VDD-0.5V	-1			mA
Low-level output current	I_{OL}	DO1 DO2	0.5V	1			mA
High-level output voltage	V_{IH}	DI		0.7VDD		VDD	V
Low-level output voltage	V_{IL}	DI		0		0.3VDD	V
Input leakage current	I_I	DI				±10	μA

Note: The output drive consumption is not included in the current consumption.

2) Switching characteristic C_L = 15 pF

①

Item	Symbol	Pin	min.	typ.	max.	Unit	Remark
Transient time	t_r	DO1 DO2			20	nsec	fig. 1
	t_f	DO1 DO2			20	nsec	fig. 2

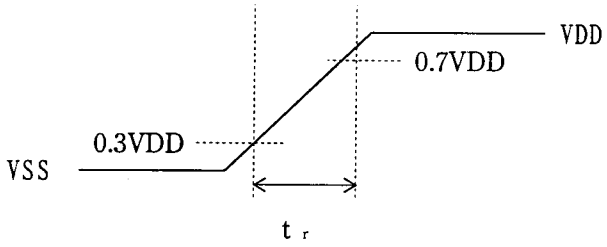


fig.1

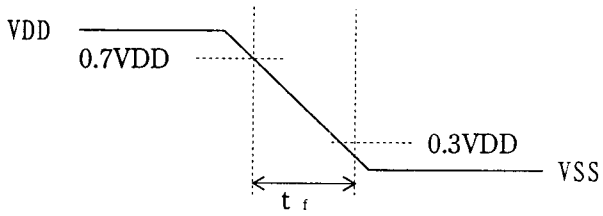
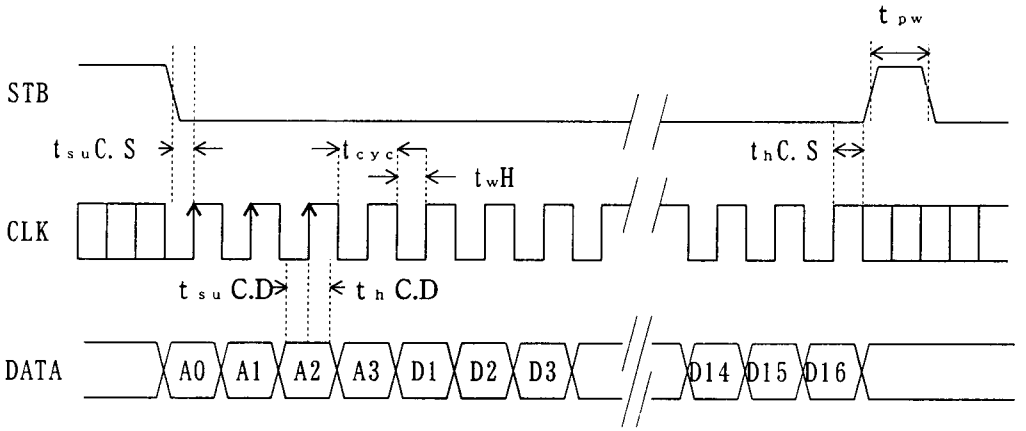


fig.2

② Data setting part

Item	Symbol	Pin	min.	typ.	max.	Unit	Remarks
Clock frequency	f_{CLK}	CLK			1	MHz	fig 3
Reset Pulse width	t_{pwRST}	RST	10			μsec	fig 3.1
Pulse duty	t_{dut}	CLK	40		60	%	fig. 3
Pulse width	t_{pw}	STB	1			μsec	fig. 3
Setup time	t_{suCD}	CLK → DATA	0.25			μsec	fig. 3
	t_{sucs}	CLK → STB	0.25			μsec	fig. 3
Hold time	t_{hCD}	CLK → DATA	0.25			μsec	fig. 3
	t_{hCS}	CLK → STB	0.25			μsec	fig. 3



$f_{CLK} = 1/t_{cyc}$

$t_{cyc} = t_w H/t_{cyc}$

fig.3

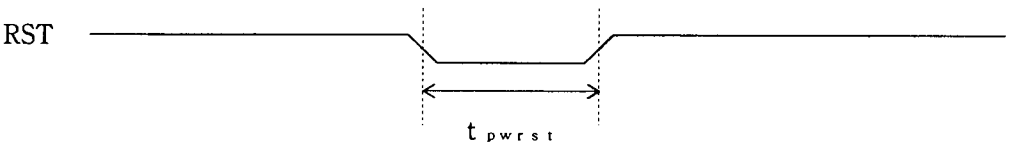


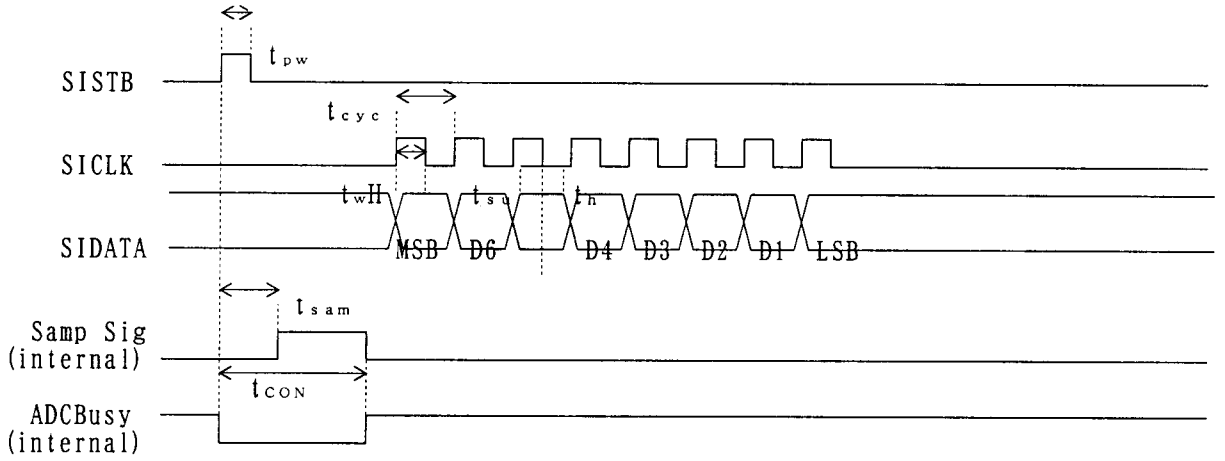
fig.3.1

③ RSSI part

Item	Symbol	Pin	min.	typ.	max.	Unit	Remarks
Clock frequency	f_{CLK}	SICLK			1	MHz	fig. 4
Pulse duty	t_{duty}	SICLK	40		60	%	fig. 4
Pulse width	t_{pw}	SISTB	1			μsec	fig. 4
Setup time	t_{su}	SICLK → SIDATA	0. 25			μsec	fig. 4
Hold time	t_h	SICLK → SIDATA	0. 25			μsec	fig. 4
A/D conversion time	t_{CON}	SISTB →			50	μsec	Note 1 fig. 4
A/D sample time	t_{sam}	SISTB →			10	μsec	Note 2 fig. 4

Note 1: When SICLK input is started before completion of A/D conversion, the A/D conversion taking place will become invalid, and meaningless data will be put out. Accordingly, execute SICLK input after at least 50 μ sec have passed after start of A/D conversion by the rise of SISTB.

Note 2: Design guarantee value ... After completion of A/D conversion, the A/D converter enters sample status.



$f_{CLK} = 1/t_{cyc}$

fig.4

④ Demodulation part

Item	Symbol	Pin	min.	typ.	max.	Unit	Remark
Setup time	t_{su}	BTR1 → DATA1	0.65			μsec	fig. 5
		BTR1 → QUARITY1	0.65			μsec	fig. 5
		BTR1 → QUARITY2	0.65			μsec	fig. 5
Hold time	t_h	BTR1 → DATA1	0.65			μsec	fig. 5
		BTR1 → QUARITY1	0.65			μsec	fig. 5
		BTR1 → QUARITY2	0.65			μsec	fig. 5
Clock frequency	f_{CLK}	BTR1		384		KHz	

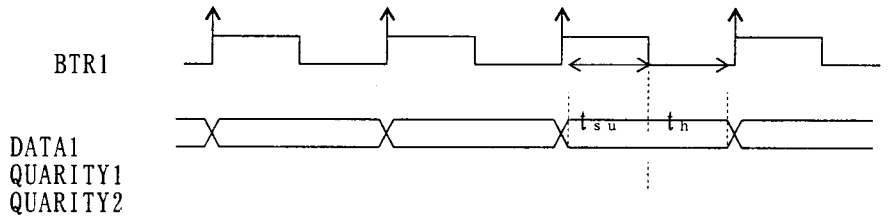


fig.5

⑤ Modulation part

Item	Symbol	Pin	min.	typ.	max.	Unit	Remark
Setup time	t_{suBR}	TCLK → TXRST	0.65			μsec	Note 3 fig. 6
	t_{suBD}	TCLK → TXDATA	0.65			μsec	fig. 6
Hold time	t_{hBD}	TCLK → TXDATA	0.65			μsec	fig. 6
Delay time	t_{dRD}	TXRST → TXDATA		10		Symbol	Note 4 fig. 6
	t_{dRP}	TXRST →		4		Symbol	Note 5 fig. 6
	t_{dPIQ}	→ I·Q			30	μsec	Note 6 fig. 6
	t_{dRO}	TXRST → BSTO		12.5		Symbol	Note 7 fig. 6
	t_{dDIQ}	TXDATA → IQ	4.59	4.66	4.74	Symbol	Note 8 fig. 6
	t_{dRPa}	TXRST →		10		Symbol	Note 9 fig. 6
	t_{dROa}	TXRST → BSTO		6.75		Symbol	Note10 fig. 6
	t_{dRAI}	TXRST → PHIN		119.5		Symbol	Note11 fig. 6
	t_{dRAO}	PHIN → APCOON		8.5		Symbol	Note12 fig. 6

Note 3: Enter TXRST synchronized to the rise of TCLK.
TXRST itself is sampled by the high-speed clock (9.6 MHz) inside the IC and is used inside the IC.
The rise of TCLK, to which TXRST is synchronized, in the following becomes the reference point for the timing of the demodulation part.

Note 4: This is the delay from the rise of TXRST until input of the first data (X1).

Note 5: This is the delay from the rise of TXRST until transmission part power-down release.

Note 6: This is the delay from transmission part power-down release until offset transmission start (analog circuit stabilization).

Note 7: This is the delay from TXRST drop until BSTO output rise.

Note 8: This is the delay from input of the first data (X1) until first symbol transmission. (design guarantee value).

Note 9: This is the delay from TXRST drop until transmission part power-down.

Note 10: This is the delay from TXRST drop until BSTO output drop.

Note 11: This is the delay from TXRST rise until the PHIN input comparator result.
When TXRST is already at low level when the comparator result is to be taken in, the comparator result will not be taken in.

Note 12: After the PHIN input comparator result has been taken in, APCON output level change is executed after the 8, 5 symbol.

Modulation Part Operation Timing

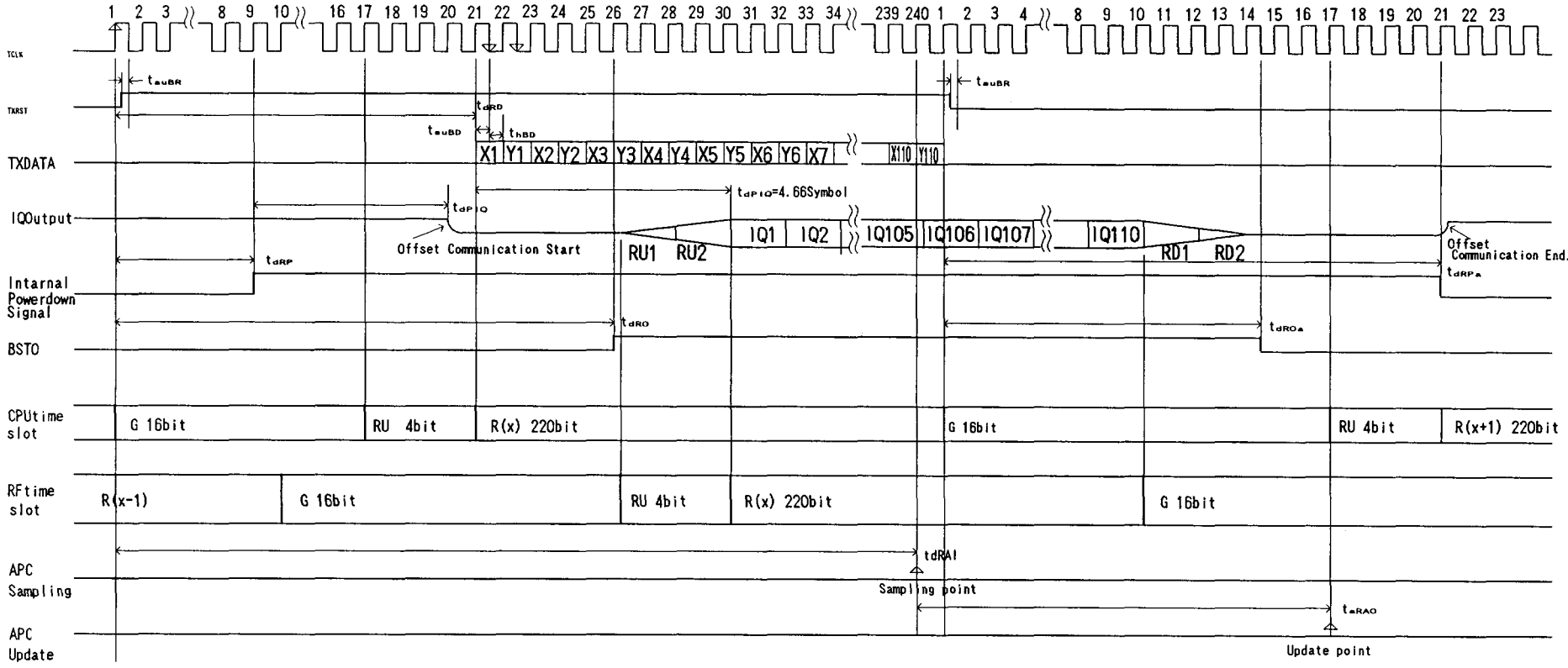


fig. 6

5) Analog characteristics

① RSSI

Item	Pin	Condition	min.	typ.	max.	Unit	Remarks
Switch ON resistance	RSSIIN → SIVSS	RSSIIN = 1/2VDD			5	KΩ	
	RSSIIN → RSSIC	RSSIIN = 1/2VDD			10	KΩ	
	RSSIC → SIVSS	RSSIC = 1/2VDD			10	KΩ	
Input voltage range	RSSIIN		0.1		2.5	V	4 to 86dBμV as the electric field strength
Gain/ offset adjustment circuit stabilization time	RSSI → Internal node			6.7		μsec	Design guarantee value Note 13
Gain adjustment range	RSSI → Internal node		-0.8		-0.6	$\frac{V_{out}}{V_{in}}$	Note 14
Gain adjustment accuracy (ΔLSB)	RSSI → Internal node		+0.005		-.001	$\frac{\Delta V_{out}}{V_{in}}$	
Offset adjustment range	RSSI → Internal node	VRIN=1.2V	+100		+700	mV	Note 15
Offset adjustment accuracy (ΔLSB)	RSSI → Internal node	VRIN=1.2V	-2	6	10	mV	
A/D converter resolution (LSB)	→SIDATA	VRIN=1.2V		7.81		mV	Note 16
A/D conversion error	→SIDATA	SIDATA= 08H to ACH			±3/2	LSB	Note 17

Note 13: This is the operation period for the gain/offset adjustment circuit.
Note 14: Internal voltage changes from 20.2 mV to 24.8 mV can be adjusted to 15.6 mV (AD output code: 2 codes: 2 × 2.0V/256) changes.
(7 bit, 128 steps)
Note 15: After adjustment of the input voltage of 140 mV (20.25 mV/dB × 7 dB) to 700 mV (24.75 nV/dB × 28 dB) at RSSIIN corresponding to the antenna electric field strength of 10 dB μV, adjustment to an AD input voltage of the.84 V (AD output code: 14H) is possible.
(8 bit, 256 steps)
Note 16: SIREF2 (10 × VRIN/6)/256
Note 17: Error for the AD converter by itself (design guarantee value).
The deviation from the expected value when looking at the AD conversion result from RSSIIN after gain/offset adjustment becomes about 4 LSB.

Item	Pin	Condition	min.	typ.	max.	Unit	Remarks
Comparator response time (TD)	Internal node → CMPLO	CMPLI =1.84V			4	μsec	Design guarantee value Note 18, 19 Fig. 7
					10	μsec	Design guarantee value Note 19. 20 Fig. 7
	CMPAI → CMPAO	CMPREF = 1.5V			2	μsec	Note 18 Fig. 7
					10	μsec	Note 19 Fig. 7 Design guarantee value
	CMPBI → CMPBO	CMPREF = 1.5V			2	μsec	Note 18 Fig. 7
					10	μsec	Note 19 Fig. 7 Design guarantee value
Comparator offset	Internal node → CMPLI				±10	mV	Design guarantee value
	CMPBI → CMPAI	CMPREF = 1.5V			±10	mV	
	CMPREF → CMPBI	CMPREF = 1.5V			±10	mV	
Comparator offset temperature drift	Internal node → CMPLI			±10		μV/℃	
	CMPBI → CMPAI			±10		μV/℃	
	CMPREF → CMPBI			±10		μV/℃	
Comparator setting voltage range	CMPLI		1.5	1.84	2.2		Note 19
	CMPREF		0.8		VDD −0.8	V	

Note 18: Value with an input amplitude of 100 mV and an overdrive of 20 mV.

Note 19: Value with an input amplitude of 100 mV and an overdrive of 5 mV.Value

Note 20: 1.84 V is the value corresponding to an electric field strength of 10 dB μ V after gain/offset adjustment.

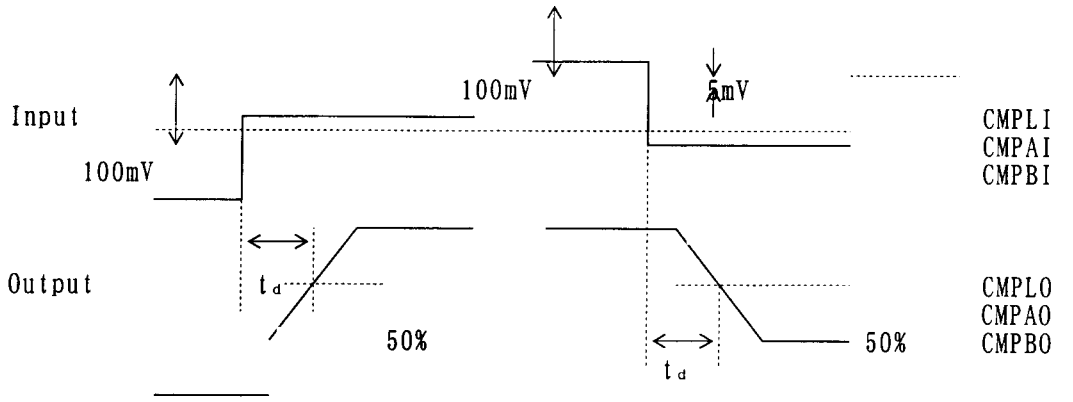


fig.7

Item	Pin	Condition	min.	typ.	max.	Unit	Remark
Output voltage level	SIREF2	CL=1μF	1.76	2.0	2.24	V	
	SIREF1	CL=1μF	0.88	1.0	1.12	V	
Recovery time	SIREF2	CL=1μF			18	msec	Note20
	SIREF1	CL=1μF			18	msec	Note20

Note 20: This is the time from power-down (PD0) release until output level stabilization.

② System Clock Input Part

Item	Pin	Condition	min.	typ.	max.	Unit	Remark
Clock frequency	MCLKI			19.2		MHz	
Input amplitude	MCLKI		0.1		1.5	Vpp	Note21

Note 21: Execute input with DC cut. When a 0.01 μF capacitors used, about 2.5 msec are required from power-down PD0 release until the analog ground level becomes stable.

③ Demodulation part

Item	Pin	Condition	min.	typ.	max.	Unit	Remark
Clock frequency	IFI		10.65	10.8	10.95	MHz	
Input amplitude	IFI		0.1		1.5	Vpp	Note22
Recovery time	IFI	DC cut 220 pF			30	μsec	Note23
PLL0 tie-up time	Internal node				3	msec	
Error between PLL0 steps	Internal node				±10	%	Design guarantee value Note24 fig8
PLL0 output duty error	Internal node				±2	nsec	Design guarantee value Note25 fig8

Note 22: Execute input with DC cut.

Note 23: When a 220 pF capacitor is used for DC cut, this is the time required from power-down PD2X release until operation start.

Note 24: This is the error in regard to the mean value for the delay between the (16) VCO outputs inside the PLL03. (30 X tdn/td1+td2+···td30 :n=1 ~ 30)

Note 25: This is the duty error of the sampling VCO output in PLL0.(twH-twL)

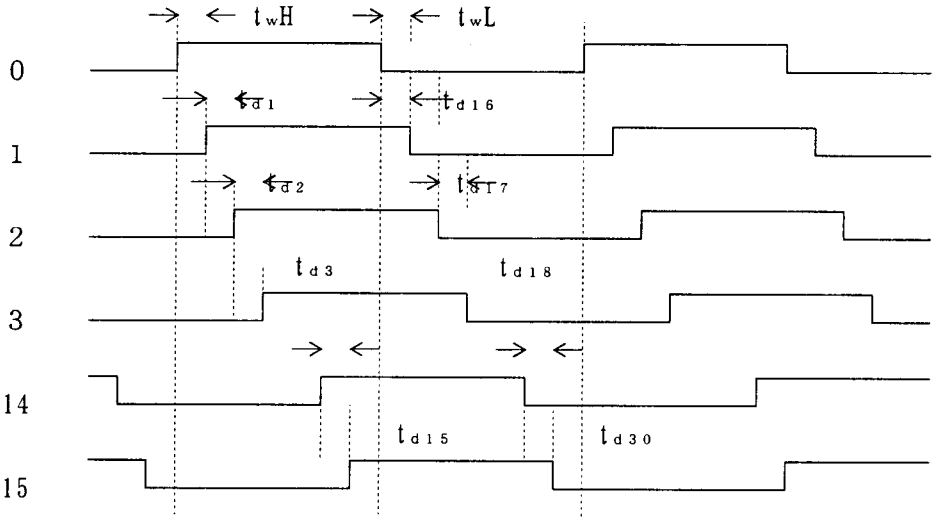


fig.8

④ Modulation part

Item	Pin	Condition	min.	typ.	max.	Unit	Remark
DC output level	IA, IAB QA, QAB	$\frac{IA+IAB}{2}$ $\frac{QA+QAB}{2}$	0.5VDD -0.2	0.5VDD	0.5VDD +0.2	V	
Output amplitude level	IA, IAB QA, QAB	R_L = 5KΩ to analog ground level		0.5		Vpp	Note26
Output amplitude adjustment range	IA, IAB QA, QAB		±14			%	Note27
Leakage power outside the band	IA, IAB QA, QAB	600 kHz detuning ± 96 kHz band			-60	dB	Note28
		900 kHz detuning ± 96 kHz band			-65	dB	Note28
Transmission spurious	IA, IAB QA, QAB	1MHz or more detuning ± 96 kHz band			-60	dB	Note28
Modulation accuracy	IA, IAB QA, QAB				3	%rms	
Output amplitude adjustment range drift	IA, IAB QA, QAB				±200	ppm /℃	
DC offset	IA, IAB QA, QAB	IA-IAB QA-QAB			±20	mV	
DC offset adjustment range	IA, IAB QA, QAB	IA-IAB QA-QAB	±32			mV	Note29

Note 26: This is the value when all input data are "0".

Note 27: This is the relative value in regard to the value at the time of gain adjustment 0 dB. (4 bit, 16 steps)

Note 28: This is the value in regard to two times of the power of 0 to 96 kHz.

Note 29: This is the relative value in regard to the value at the time of offset adjustment 0 mV. (6 bit, 64 steps).

Item	Pin	Condition	min.	typ.	max.	Unit	Remarks
Comparison voltage setting range	APCREF		1.32		1.8	V	Note 30
Comparison voltage temperature drift	APCREF			20		μV/℃	Note 31
Comparison voltage adjustment accuracy (ΔLSB)	APCREF		0.6	1.56	2.4	mV	
Response time (td)	PHIN→ Internal node	APCREF =1.5V			200	μsec	Design guarantee value Note 32 Fig. 9
Output voltage setting range	APCCON	APCOFF=1.2V	1.32		1.8	V	Note 30
Output voltage temperature drift	APCCON	APCOFF=1.2V		20		μV/℃	Note 31
Output voltage adjustment accuracy (ΔLSB)	APCCON		0.6	1.56	2.4	mV	
Offset input range	APCOFF		1.0		1.3	V	Note 33
Output stabilization time	APCCON				20	μsec	
Output voltage level	TREF2	CL=1μF	1.8	2.0	2.2	V	
	TGND	CL=1μF	0.48VDD		0.52VDD	V	
Recovery time	TREF2	CL=1μF			18	msec	Note 34
	TGND	CL=1μF			18	msec	Note 34

Note 30: 9 bit, 512 step setting is possible (typical case).

Note 31: This is the drift from temperature changes after level setting.

Note 32: This is the value for an input amplitude of 50 mV and an overdrive of 75 μ V.
Accordingly, in order to obtain a correct comparison result, it is required to confirm the PHIN input level within 85 symbols after start of symbol transmission.

Note 33: The APCCON output range becomes
0.8 V to 1.6 V with input of 1.0 V to APCOFF,
1.2 V to 2.0 V with input of 1.2 V,to APCOFF and
1.4 V to 2.2 V with input of 1.3 V,to APCOFF.
(typical case)

Note 34: This is the time from power-down (PD0) release until the output level becomes stable.

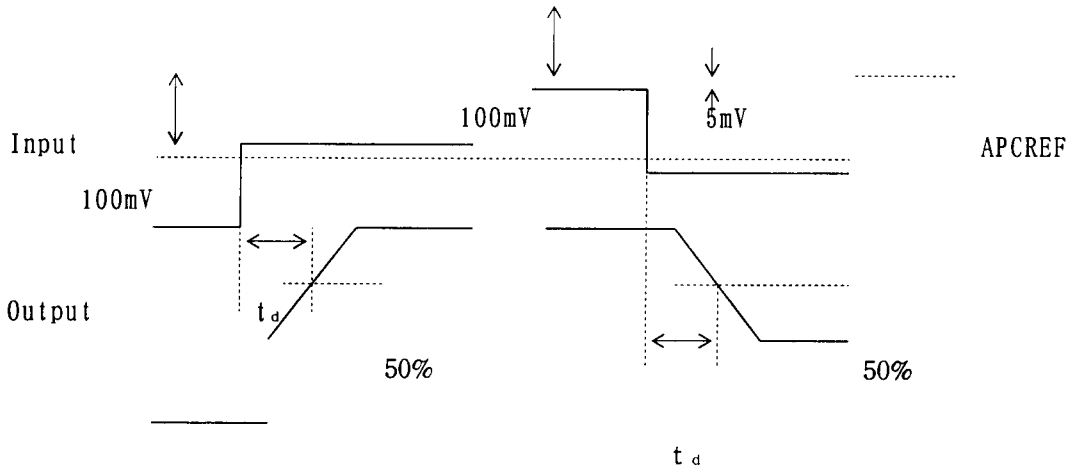


fig.9

⑥ Reference voltage part

Item	Pin	Condition	min.	typ.	max.	Unit	Remark
Analog ground level	AGND		0.48VDD		0.52VDD	V	
Input voltage range	VRIN		1.08	1.2	1.32	V	
Output voltage level	AREF	C_L =0.01μF	1.08	1.2	1.32	V	
	VREFO	VRIN=1.2V	1.18		1.22	V	
Recovery time	AGND	C_L =1000pF			15	msec	Note35
	AREF	C_L =0.01μF			5	msec	Note35
	VREFO	VRIN=1.2V			2	msec	Note35
Output voltage temperature drift	AREF	C_L =0.01μF		290		μV/℃	
	VREFO	VRIN=1.2V		10		μV/℃	

Note 35: This is the time from power-down (PD0) release until the output level becomes stable.

Function Explanation

(1) Data setting part

The setting conditions for the various parts are changed by writing data to the various control registers.

Block	Function
S/P converter	This is the shift register for input of data for change of the various setting conditions in the IC. It is not powered down.

i) Register initialization

By low-level input to the RST pins, the default values are loaded to the registers inside the IC.

ii) Data setting method

The clock input to SCLK is enabled by low-level STB input.
With the first 20 SCLK rises after STB low level, the data pin status is taken into the IC.
After the first 20 SCLK rises, data sampling is prohibited, and the data read into the IC by SCLK high level following the twentieth SCLK rise are transmitted to the specified control registers. This timing is shown in Fig. 10.

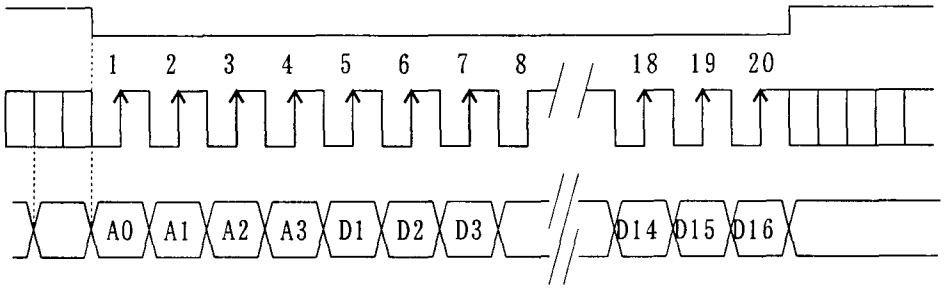
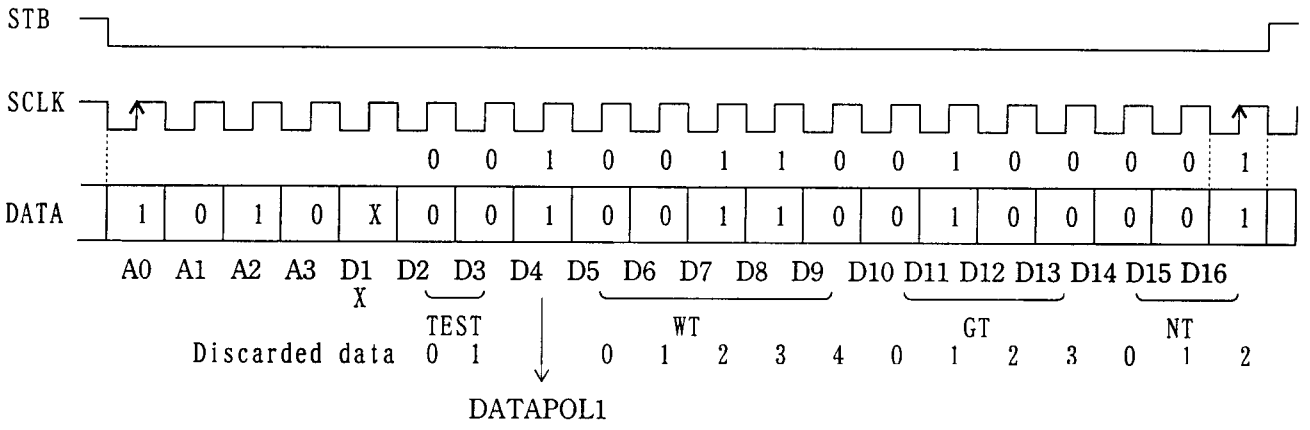


fig. 10

The first 4 bits sampled by SCLK rise indicate the addresses of the control registers where the 16 data sampled afterwards are to be stored.
Even when the required data length is less than 16 bits, SCLK input for the specified number of times is required.
In this case, the not required data are discarded in the IC. As data discarding is executed from first sampled data, input required data with last justified format.
The timing for input of the default value for register 6 is shown in Fig. 11.



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iii) Register MAP

Register Name	Address				Contents															
	A3	A2	A1	A0	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
Register 1	0	0	0	0	Register 1 ~ 5 Not Used															
:	:																			
Register 5	0	1	0	0																
Register 6	0	1	0	1	NT2···NT0			GT3···GT0			WT4···WT0						DATA POL1	×	AFCCAL	×
Register 7	0	1	1	0	TAFCEN1	AFCEN1	JPEN1	BWN2···BWN0			BWW2···BWW0			JS31···JS01				PS11	PS01	×
Register 8	0	1	1	1	RS07···RS00							×	RSG6···RSG0							×
Register 9	1	0	0	0	IDA05···IDA00						IDAG3···IDAG0				×	×	×	×	×	
Register 10	1	0	0	1	QDA05···QDA00						QDAG3···QDAG0				×	×	×	×	×	
Register 11	1	0	1	0	APC9···APC0									×	IQTest Enable	Q TEST	I TEST	TEST Enable	DTEST X	DTEST Y
Register 12	1	0	1	1	APCR9···APCR0									×	APCREN1	APCEN1	×	×	×	×
Register 13	1	1	0	0	Reserved															
:																				
Register 15	1	1	1	1																

Register 6

Demodulation part 1
A0,A1,A2,A3 = 1,0,1,0 Effective data length: 15 bit

Contents	Signal name		Default		Length
				LSB MSB	
Discarded data		D1			1bit
AFCCAL	AFCCAL	D2	0	0	1bit
Discarded data		D3			1bit
Local frequency	DATAPOL1	D4	1	1	1bit
Bit sync wide time	WT0, . . , WT4	D5～D9	12	00110	5bit
Buffer time	GT0, . . , GT3	D10～D13	2	0100	4bit
AFC data sampling time	NT0. . . . NT2	D14～D16	4	001	3bit

AFC Calculation Option : AFCCAL
AFC Calculation Option Selection.
0:The signed absolute data is used for the AFC calculation.
1:The 2's conplement data is used for the AFC caluculation.
Please set to "1" for normal usage.

Local frequency : DATAPOL1
Frequency shift direction setting is executed for the modulation side and the demodulation side.
0: The IF1 input frequency is reversed.
(the frequency shift on the modulation side and the frequency shift on the demodulation side are in opposite directions)
1: The IF1 input frequency is in forward direction.
(the frequency shift on the modulation side and the frequency shift on the demodulation side are in the same direction)

Bit sync wide time : WT0, ... WT4
The bit sync band width between WT reception symbols is made wide band.
(WT = WT0 + 2 × WT1 + 4 × WT2 + 8 × WT3 + 16 × WT4)

Buffer time : GT0, ... GT3
Waiting for AFC data sampling is executed between GT reception symbols.
(GT = GT0 + 2 × GT1 + 4 × GT2 + 8 × GT3)

AFC data sampling time : NT0, NT1, NT2
The AFC quantity is decided by the mean of 2^{NT} reception symbols.
(NT = NT0 + 2 × NT1 + 4 × NT2)

Register 7

Demodulation part 2
A0,A1,A2,A3 = 0,1,1,0 Effective data length: 15 bit

Contents	Signal name	Default		Length
			LSB MSB	
Discarded data	D1			1bit
Bit sync hysteresis width	PS01, PS11 D2, D3	0	00	2bit
Erroneous sync detection level	JS01, . . . , JS31 D4～D7	12	0011	4bit
Bit sync wide band width	BWW0, . . . , BWW2 D8～D10	2	010	3bit
Bit sync narrow band width	BWN0, . . . , BWN2 D11～D13	0	000	3bit
Erroneous sync detection enable	JPEN1 (0: Enable, 1: Disable) D14	1	1	1bit
UW32AFC enable	AFCEN1 (0: Disable, 1: Enable) D15	1	1	1bit
UW16AFC enable	TAFCEN1 (0: Disable, 1: Enable) D16	1	1	1bit

Bit sync hysteresis width : PS01, PS11
The phase direction for correction of the bit sync from the 2^{PS} reception symbol is decided.
(PS = PS01 + 2 × PS11)

Erroneous sync detection threshold value : JS01, ... JS31
The JS reception symbol is decided as the erroneous sync detection threshold value.
(JS = JS01 + 2 × JS11 + 4 × JS21 + 8 × JS31)

Bit sync wide band width : BWW0, BWW1, BWW2
Setting is possible for 0, 1, 2, 3, and 4 (setting is prohibited for 5, 6, and 7).
2^{BWW} is used as the phase width for correction of the bit sync at the time of bit sync wide band.
(BWW = BWW0 + 2 × BWW1 + 4 × BWW2)

Bit sync narrow band width : BWN0, BWN1, BWN2
Setting is possible for 0, 1, 2, 3, and 4 (setting is prohibited for 5, 6, and 7).
2^{BWN} is used as the phase width for correction of the bit sync at the time of bit sync narrow band.
(BWN = BWN0 + 2 × BWN1 + 4 × BWN2)

Erroneous sync detection enable : JPEN1
1: Erroneous sync detection disable
0: Erroneous sync detection enable
Please set to "0" for normal usage.

UW32 enable : AFCEN1
1: AFC enable
0: AFC disable

UW16AFC enable : TAFCEN1
This setting becomes effective when CHTOCH is low level.
1: AFC data sampling is enabled in regard to a burst of UW = 16.
0: AFC data sampling is disabled in regard to a burst of UW = 16.

Register 8

RSSI part
A0,A1,A2,A3 = 1,1,1,0 Effective data length: 15 bit

Contents	Signal name		Default		Length
				LSB MSB	
Discarded data		D1			1bit
RSSI gain	RSG0, . . , RSG6	D2～D8	62	0111110	7bit
RSSI offset	RS00, . . , RS06, RS07	D9～D16	134	01100001	8bit

RSSI gain : RSG0, ... RSG6
The gain of the gain/offset regulator is set.

RSSI gain (typical case)

RSG							Vout	RSG							Vout
0	1	2	3	4	5	6	vin	0	1	2	3	4	5	6	vin
0	0	0	0	0	0	0	-0. 500	0	0	0	0	0	0	1	-0. 701
1	0	0	0	0	0	0	-0. 503								
0	1	0	0	0	0	0	-0. 506								
1	1	0	0	0	0	0	-0. 509								
0	0	1	0	0	0	0	-0. 513	0	0	1	1	1	1	1	-0. 890
								0	1	1	1	1	1	1	-0. 893
								0	1	1	1	1	1	1	-0. 896
1	1	1	1	1	1	0	-0. 698	1	1	1	1	1	1	1	-0. 899

RSSI offset : RSO0, ... RSO7
The offset of the gain/offset regulator is set.

RSSI offset (typical case, VRIN = 1.2 V)

RSO								Offset	RSO								Offset
0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7	
X	0	0	0	0	0	0	0	0. 0mV	X	0	0	0	0	0	0	1	402. 4mV
X	1	0	0	0	0	0	0	6. 3mV									
X	0	1	0	0	0	0	0	12. 6mV									
X	1	1	0	0	0	0	0	18. 9mV	X	0	0	1	1	1	1	1	776. 5mV
									X	1	0	1	1	1	1	1	782. 8mV
									X	0	1	1	1	1	1	1	789. 1mV
X	1	1	1	1	1	1	0	396. 1mV	X	1	1	1	1	1	1	1	795. 4mV

Register 9

Ich
A0,A1,A2,A3 = 0,0,0,1 Effective data length: 10 bit

Contents	Signal name	Default		Length
			LSB MSB	
Discarded data				6bit
Ich DAC gain	IDAG0, . . , IDAG3	0	0000	4bit
Ich DAC offset	IDA00, . . , IDA05	0	000000	6bit

Ich DAC gain : IDAG0, ... IDAG3
The IA−IAB output amplitude (gain) is set.

Ich DAC gain (typical case, in regard to the standard value)

IDAG					IDAG				
0	1	2	3		0	1	2	3	
1	1	1	0	117.5%	1	1	1	1	97.5%
0	1	1	0	115.0%	0	1	1	1	95.0%
1	0	1	0	112.5%	1	0	1	1	92.5%
0	0	1	0	110.0%	0	0	1	1	90.0%
1	1	0	0	107.5%	1	1	0	1	87.5%
0	1	0	0	105.0%	0	1	0	1	85.0%
1	0	0	0	102.5%	1	0	0	1	82.5%
0	0	0	0	100.5%	0	0	0	1	80.0%

Ich DAC offset : IDAO0, ... IDAO5
The offset between the IA−IAB outputs is set.

IchDAC offset (typical case)

IDAO							IDAO						
0	1	2	3	4	5		0	1	2	3	4	5	
1	1	1	1	1	0	40.6mV	1	1	1	1	1	1	-1.3mV
0	1	1	1	1	0	39.3mV	0	1	1	1	1	1	-2.6mV
1	0	1	1	1	0	38.0mV	1	0	1	1	1	1	-3.9mV
0	0	1	1	1	0	36.7mV	0	0	1	1	1	1	-5.2mV
:							:						
0	1	0	0	0	0	2.6mV	0	1	0	0	0	1	-39.3mV
1	0	0	0	0	0	1.3mV	1	0	0	0	0	1	-40.6mV
0	0	0	0	0	0	0.0mV	0	0	0	0	0	1	-41.9mV

Register 10

Qch
A0,A1,A2,A3 = 1,0,0,1 Effective data length: 10 bit

Contents	Signal name	Default		Length
			LSB MSB	
Discarded data				6bit
Qch DAC gain	QDAG0, . . . , QDAG3	0	0000	4bit
Qch DAC offset	QDAO0, . . . , QDAO5	0	000000	6bit

Qch DAC gain : QDAG0, ... QDAG3
The QA−QAB output amplitude (gain) is set.

Qch DAC gain (typical case, in regard to the standard value)

QDAG					QDAG				
0	1	2	3		0	1	2	3	
1	1	1	0	117.5%	1	1	1	1	97.5%
0	1	1	0	115.0%	0	1	1	1	95.0%
1	0	1	0	112.5%	1	0	1	1	92.5%
0	0	1	0	110.0%	0	0	1	1	90.0%
1	1	0	0	107.5%	1	1	0	1	87.5%
0	1	0	0	105.0%	0	1	0	1	85.0%
1	0	0	0	102.5%	1	0	0	1	82.5%
0	0	0	0	100.5%	0	0	0	1	80.0%

Qch DAC offset : QDAO0, ... QDAO5
The offset between the QA−QAB outputs is set.

Qch DAC offset (typical case)

QDAO							QDAO						
0	1	2	3	4	5		0	1	2	3	4	5	
1	1	1	1	1	0	40.6mV	1	1	1	1	1	1	-1.3mV
0	1	1	1	1	0	39.3mV	0	1	1	1	1	1	-2.6mV
1	0	1	1	1	0	38.0mV	1	0	1	1	1	1	-3.9mV
0	0	1	1	1	0	36.7mV	0	0	1	1	1	1	-5.2mV
:							:						
0	1	0	0	0	0	2.6mV	0	1	0	0	0	1	-39.3mV
1	0	0	0	0	0	1.3mV	1	0	0	0	0	1	-40.6mV
0	0	0	0	0	0	0.0mV	0	0	0	0	0	1	-41.9mV

Register 11

Transmission test
A0,A1,A2,A3 = 0,1,0,1 Effective data length: 16 bit

Contents	Signal name	Default		Length
			LSB MSB	
Data test	DTESTY, DTESTX	0	00	2bit
Data test enable	0: Disable, 1: Enable	0	0	1bit
IQ test	ITEST, QTEST	0	00	2bit
IQ test enable	0: Disable, 1: Enable	0	0	1bit
APCDAC data	APC0, . . , APC9	0	0000000000	10bit

Data test : DTESTY, DTESTX
The Y data and the X data at the time of data test are set.

Data test

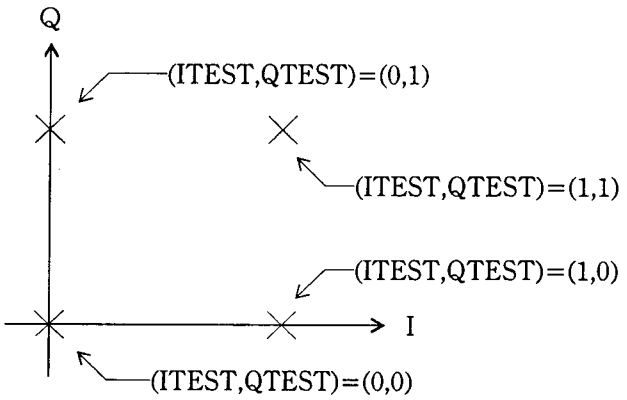
DTEST		IQ shift
X	Y	
0	0	$\pi/4$
1	0	$-\pi/4$
0	1	$3/4\pi$
1	1	$-3/4\pi$

Data test enable

1: Data test enabled
When IQ test enable is "0", the transmission part enters into data test mode when "1" is written to this bit, TESTB is made "L", and TXRST is made "H".
This is not effective when IQ test enable is "1".

0: Data test disabled

IQ test : ITEST, QTEST
The I data and the Q data at the time of IQ test are set.



IQ test enable

1: IQ test enabled
When data test enable is "0", the transmission part enters into IQ test mode when "1" is written to this bit, TESTB is made "L", and TXRST is made "H".
This is not effective when data test enable is "1".
0: IQ test disabled

APCDAC data : APC0, ... APC9
The 9 bit DA data for transmission output control are set.
The output level of the APCCON pin is changed by this setting.

APCCON output level (TYPICAL case, VRIN=APCOFF=1.2V)

APC										APCCON output level (V)
0	1	2	3	4	5	6	7	8	9	
X	0	0	0	0	0	0	0	0	0	1.2000V
X	1	0	0	0	0	0	0	0	0	1.2016V
X	0	1	0	0	0	0	0	0	0	1.2031V
:										
X	0	0	0	0	0	0	0	0	1	1.6000V
:										
X	1	0	1	1	1	1	1	1	1	1.9953V
X	0	1	1	1	1	1	1	1	1	1.9968V
X	1	1	1	1	1	1	1	1	1	1.9984V

Register 12

Transmission part APC
A0,A1,A2,A3,=1,1,0,1 Effective data length: 12 bit

Contents	Signal name	Default		Length
			LSB MSB	
Discarded data				4bit
APC enable	APCEN1 (0: Disable, 1: Enable)	1	1	1bit
APC reference enable	APCREN1 (0: Disable, 1: Enable)	1	1	1bit
APCREF data	APCR0, ... APCR9	0	0000000000	10bit

APC enable : APCEN1

1: Control status
The DAC set value for transmission output level control is based on the result of the PHIN−APCREF comparison executed at the time of burst transmission (PD4), it is updated after conclusion of the burst transmission, and the APCCON output level changes.

0: Hold status
The DAC set value for transmission output level control is not updated according to the result of the PHIN−APCREF comparison executed at the time of burst transmission (PD4).
Accordingly, the APCCON output level holds the same level before and after burst transmission.

Change of the DAC set value for transmission output level control by rewriting the APCDAC data is effective independent of the status of APCEN1, and the APCCON output level changes with rewriting of the APCDAC data.

APC reference enable : APCREN1

1: Operation possible status
The 9 bit DAC for transmission output level setting shifts between operation and power−down status depending on the power−down mode setting.

0: Power−down status
The 9 bit DAC for transmission output level setting is placed into power−down status independent of the power−down mode setting.
The transmission output level setting becomes an external setting, and the APCREF pin becomes the input pin for transmission output level setting.

APCREF data : APCR0, ... APCR9
9 bit data setting for transmission output level setting is executed.
The output level of the APCREF pin is changed by this setting.

APCREF output level (typical case)

APCR										APCREF output level (V)
0	1	2	3	4	5	6	7	8	9	
X	0	0	0	0	0	0	0	0	0	1.2000V
X	1	0	0	0	0	0	0	0	0	1.2016V
X	0	1	0	0	0	0	0	0	0	1.2031V
:										
X	0	0	0	0	0	0	0	0	1	1.6000V
:										
X	1	0	1	1	1	1	1	1	1	1.9953V
X	0	1	1	1	1	1	1	1	1	1.9968V
X	1	1	1	1	1	1	1	1	1	1.9984V

Others
(A0, A1, A2, A3) = (0, 0, 1, 1 to 1, 1, 1, 1) are reserved by the IC.

(2) RSSI part

After execution of gain and offset adjustment for the input from RSSI IN, A/D conversion is executed, and output is made as an 8 bit digital signal.
This block is composed of a gain and offset adjustment circuit, an 8 bit A/D converter, 3 comparators, and a reference voltage generation circuit for the A/D converter.

Block	Function
Gain and offset adjustment circuit	This is the circuit for execution of gain and offset adjustment in regard to the RSSI IN input. Gain 7 bit and offset 7 bit adjustment are possible by control register. Power-down release is executed for PD3.
A/D converter	After the gain/offset adjustment circuit, this circuit executes A/D conversion of the RSSI signal to 8 bit digital values. Power-down release is executed for PD3.
CMPL	The output from the gain/offset adjustment circuit and the CMPLI input are compared. Power-down release is executed for PD3.
CMPA, CMPB	Comparison is executed between external input levels. Power-down release is executed for PD3.
Reference AMP	The reference level for the A/D converter of the RSSI part is put out. Power-down release is executed for PDn (n=1 to 4).

i) RSSI signal input pin
This pin is the direct input pin to the gain/offset adjustment circuit (SCF peak hold circuit).
In regard to this pin, a load of max. 40 pF is connected on the inside of the IC via a switch, and this switch repeats ON and OFF at a period of 300 kHz.
Accordingly, sufficient attention must be paid to the output impedance of the external device supplying a signal to the RSSIIN pin.

ii) Gain/offset adjustment circuit
This circuit is an inversion amplifier by SCF, and gain adjustment is executed by SIREF1 output level reference. Accordingly, the offset amount at the VSS reference is changed by gain adjustment.
The offset adjustment amount is produced by dividing the SIREF2 output level. Accordingly, the offset adjustment range and the adjustment accuracy change when the VRIN input level is changed.

iii) 8 bit A/D converter
The input voltage range of the A/D converter is given by the SIREF2 output level. Accordingly, the resolution changes when the VRIN input level is changed.
The A/D converter starts A/D conversion by the rise of SISTB.
Sampling is completed within 10 μ sec of the rise of SISTB, and A/D conversion is completed within 50 μ sec.
Accordingly, in order to obtain correct A/D conversion results, it is required that SICLK input is executed 50 μ sec or more after the rise of SISTB.
In case of input of SICLK before completion of A/D conversion, the A/D conversion being executed becomes ineffective, and meaningless data will be put out.
A further rise of SISTB before completion of A/D conversion also will be disregarded.
The A/D conversion result output from the SIDATA pin is executed synchronized to the rise of SICLK, and output is made from the MSB side. (Refer to Fig. 4.)

A/D converter input voltage	Output code MSB LSB
1992.2mV ~ 2000.0mV	0 0 0 0 0 0 0 0
1984.3mV ~ 1999.2mV	0 0 0 0 0 0 0 1
1976.6mV ~ 1984.3mV	0 0 0 0 0 0 1 0
1968.8mV ~ 1976.6mV	0 0 0 0 0 0 1 1
:	:
23.4mV ~ 31.3mV	1 1 1 1 1 1 0 0
15.6mV ~ 23.4mV	1 1 1 1 1 1 0 1
7.8mV ~ 15.6mV	1 1 1 1 1 1 1 0
0mV ~ 7.8mV	1 1 1 1 1 1 1 1

Note: The A/D converter output code becomes larger with increasing RSSIIN input voltage. However,
as the gain/offset adjustment circuit is an inversion amplifier, the A/D converter itself operates so that the output code becomes larger with decreasing input voltage.

(3) Demodulation part

Clock regeneration from the input signal and data demodulation are executed.
This block is composed of PLL0, selector, differential demodulation circuit, and bit synchronization circuit.

Block	Function
PLL0	10.8 MHz is resolved to 5 bit phase information. Power-down release is executed for PDn (n = 1 to 4).
Differential demodulation circuit	The signal from the selector is demodulated to the original data. Setting by control register is possible for the buffer time(16 steps), the bit synchronization wide time (32 steps), the AFC data sampling time (8 steps, however at the time of CHT0C1=1), UW32AFC operation enable, and UW16AFC operation enable (however, at the time of CHT0C1 = 0), and bit synchronization control setting is executed by external input separate by reception burst types. Power-down release is executed for PDn (n = 2 to 4), and operation is started for PD3.
Bit synchronization circuit	The reception data clock is regenerated on the basis of the signal from the differential demodulation circuit. Control register setting is executed for the bit synchronization wide band (8 steps, however, 5, 6, and 7 are prohibited), the bit synchronization narrow band (8 steps, however, 5, 6, and 7 are prohibited), the bit synchronization hysteresis width (4 steps), the erroneous sync detection level (16 steps), and erroneous sync detection enable. Power-down release is executed for PDn (n = 2 to 4), and operation is started for PD3.

i) PLL0
This is a ring oscillator composed of 16 delay elements. The oscillation frequency is locked to 10.8 MHz, and phase information (5 bit) is obtained with any desired timing.

ii) Delay detection circuit
The phase information handed over from the selector is used as the basis for decoding of the received signal, for reception quality output, and for AFC operation.
By selection of the reception local frequency, decoding of the received signal becomes possible for equipment with the frequency shift direction for the received signal in the opposite direction of the transmission side by DATAPOL=0 and for equipment with the same direction by DATAPOL=1.
In the case of AFCEN1=1 and CHT0C1=1 (UW=32), the AFC operation is executed using the mean value for the AFC amount estimated from the reception data from the reception burst start time (rise of BSC0H1) until [time set by NT0, ... NT2: 2^{NT} symbol] after [time set by WT0, ... WT4: WT symbol] + [time set by GT0, ... GT3: GT symbol].
However, there are the limits of WT + GT + $2^{NT} \leqq 32$, WT $\geqq$ 1, and GT $\geqq$ 1.
In the case of AFCEN1=and, TAFCEN1=1, and CHT0C1=0 (UW=16), the AFC operation is executed so that the mean value of the AFC amount estimated for the reception data from reception burst start (drop of BSC0H1) until 64 symbols after [time set by GT0, ... GT3: GT symbol] becomes effective in regard to the next reception burst. However, there is the limit of GT $\geqq$ 1.
AFC operation is not executed in the case of AFCEN1=0.
In the case of AFCEN1=1 and TAFCEN1=0, the AFC amount is not updated at the time of CHT0C1=0. However, the AFC operation itself is executed.

iii) Bit sync circuit

At the time of RXPD=1, reception data clock regeneration is executed on the basis of the signal from the delay detection circuit.
In the case of CHT0C1=1, bit sync operation is executed for the time from reception burst start (drop of BSC0H1) until [time set by WT0, ... WT4: WT symbol] for each reception symbol with [phase width set by BWW0, ... BWW2: 2^{BWW}] as the correction phase width, and for the remaining BSC0H1=0, bit sync operation is executed for each [time set by PS01, PS11: 2^{PS} symbol] with [phase width set by BWN0, ... BWN2: 2^{BWN}] as the correction phase width.
In the case of CHT0C1=0, bit sync operation is executed for each [time set by PS01, PS11: 2^{PS} symbol] with the period from reception burst start (drop of BSC0H1) until phase width set by BWN0,... BWN2: 2^{BWN}] as the correction phase width.

In the case of BSC0H1=1, bit sync operation is not executed and the phase of the reception regeneration clock becomes fixed. At this time, the reception regeneration clock reaches free-running status.
In the case of JSEN1=1, erroneous sync detection is executed using the [erroneous sync detection threshold JS set by JS01, ... JS31].
In the case of JSEN1=0, erroneous sync detection is not executed.
At the time of RXPD=0, bit sync operation is not executed in the same way as at the time of BSC0H1=1, and the phase of the reception regeneration clock becomes fixed. At this time also, the reception regeneration clock reaches free-running status.

(4) Modulation part

I and Q signal are formed from the entered digital data. This block is composed of delay circuit, S/P converter, SUM logic, digital filter, DAC, LPF, analog ground AMP, reference AMP, and APC circuit.

Block	Function
Delay circuit	The transmission operation timing is controlled on the basis of the external input signal. Power-down release is executed for PDn (n = 2 to 4).
S/P converter	The entered 384 kbps serial data are separated into two 192 kbps data. Power-down release is executed for PD4.
SUM Logic	Differential encoding is executed for the data from the S/P converter. Power-down release is executed for PD4.
Digital Filter	This is a root Nyquist filter. Power-down release is executed for PD4.
DAC	This is a DAC for conversion of the signal from the digital filter to an analog signal. 6 bit offset adjustment and 4 bit gain adjustment are possible by control register. Power-down release is executed for PD4.
APC	Transmission output control is executed. This is composed of a 9 bit DA for transmission output level setting and a 9 bit DA for comparator transmission output level control. Control register setting is possible for the 9 bit data in regard to the two DAs, APC enable, and APC reference enable. The 9 bit DA for transmission output level control executes power-down release for PDn (n = 1 to 4), and it reaches control status at the time of APCEN1 ="1" and hold status at the time of APCEN1 = "0". In hold status. Output level change is not executed after burst output. The 9 bit DA for transmission output level setting reaches operation possible status at the time of APCREN1= "1", and power-down release occurs at the time of PDn (n = 1 to 4). At the time of APCREN1 ="0", power-down status is obtained at all times.
Reference AMP	The reference level for the modulation part is put out. Power-down release is executed for PDn (n = 1 to 4).
Analog Ground AMP	The analog ground level for the modulation part is put out. Power-down release is executed for PDn (n = 1 to 4).

i) Operation timing for the modulation part (refer to Fig. 6)

Operation of the modulation part is started by sampling the high level of TXRST (given as input synchronized to the rise of TCLK) by the high-speed clock (9.6 MHz) in the IC.
When TCLK[1] is used as the TCLK rise synchronized to the TXRST high-level change, the modulation part is released from power-down status at TCLK[9] (t dRP). Afterwards, max. 30 μ sec (t dPIQ) are required until the modulation part becomes stable.
Then the first TXD data are given as input to the IC (t dRD) at TCLK[21], and these data are sampled by the TCLK drop following TCLK[21]. The delay from TCLK[2] until the first symbol transmission (symbol delay) is about 4.66 symbols (t dDIQ).
Before symbol transmission, the signal for indication of the transmission burst position (BSTO) is made high level at TCLK[26] (t dRO). This is about 0.85 μ sec before actual start of transmission (ramp-up).
The TXRST low-level given as input synchronized to the TCLK rise is sampled by the high-speed clock (9.6 MHz) in the IC to start the sequence for stop of the modulation part.
This start is generated 240 clocks after the normal TXRST change to high level. With TCLK[1A] as the TCLK rise to which the TXRST change to low level is synchronized, following TXDATA sampling is prohibited, and ramp down is completed about 34.65 μ sec (6.66 symbols) later.
About 0.45 μ sec after ramp-down completion, BSTO drop occurs 6.75 symbols after TCLK[1A] (t dROa).
3.25 symbols after this, the modulation part executes power-down 10 symbols after TCLK[1A] (t dRPa) and offset transmission is stopped.

ii) APC operation

Output at the level specified by the initial set value (register APC0 to 9) (1.2 V at the time of APCOFF 1.2 V setting) starts with release from the first power-down (PD0) after power ON.
Afterwards, for each burst transmission execution, the result of the comparison of the signal indicating the transmission level (PHIN) with the reference transmission level is taken in to (TCLK[1])A]) 119.5 symbols after the rise of TCLK (TCLK[1]) synchronized to the change of TXRST to high level, and 8.5 symbols (t dRAO) later, APCCON output level change is executed on the basis of the comparison result.
When TXRST already is low level at the time when the comparison result is taken in, the comparison result will not be taken in, and accordingly, the APCCON output level change 8.5 symbols later also will not be executed.
Afterwards, in case of recovery from power-down PDn (n = 0 to 3), start is executed from the output of the level changed last (result of the change at the time of the burst transmission directly before power-down).

(5) Reference voltage part

The voltage and current used as reference in the IC are supplied.
This is composed of AGNDGEN and VRF–BIAS GEN.

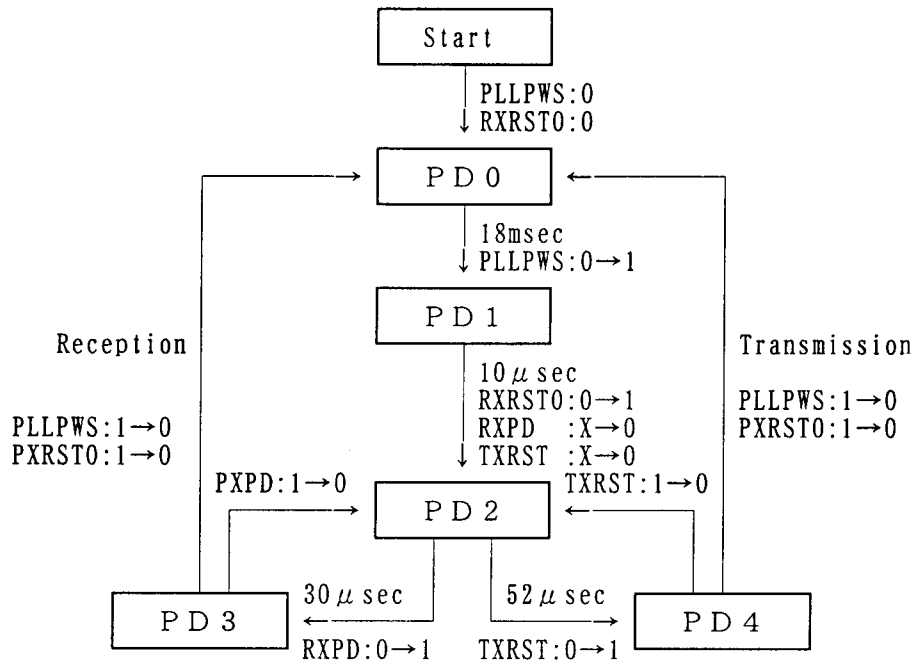
Block	Function
AGNDGEN	The reference level in regard to the analog ground AMP of the various IC parts is supplied. Power-down release is executed for PDn (n = 1 to 4).
VREF-BIAS GEN	The reference voltage supplied to the various IC parts is produced. Power-down release is executed for PDn (n = 1 to 4).

(6) Power–down mode

i) Power–down mode

	PLLPWS	RXRST0	RXPD	TXRST	
PD0	0	0	×	×	Standby status 'a' while waiting Data setting part ON
PD1	1	0	×	×	Standby status 'b0' while waiting PD0 + PLL0 + AGNDAMP
PD2	1	1	0	0	Standby status '0' at the time of a call PD1 + APC(Hold) ON + reception part(clock mask, BTR free running) ON
PD3	1	1	1	×	Reception status '0' at the time of a call PD1 + APC(Hold) ON + reception part (BTR sync) ON
PD4	1	1	0	1	Transmission status '0' at the time of a call PD2 (APC operation) + transmission part ON

ii) Power−down mode shift and shift time



PD0 −> PD1 : Shift time from the PLLPWS setting
This is mainly the time required for AGNDGEN and analog ground AMP stabilization.

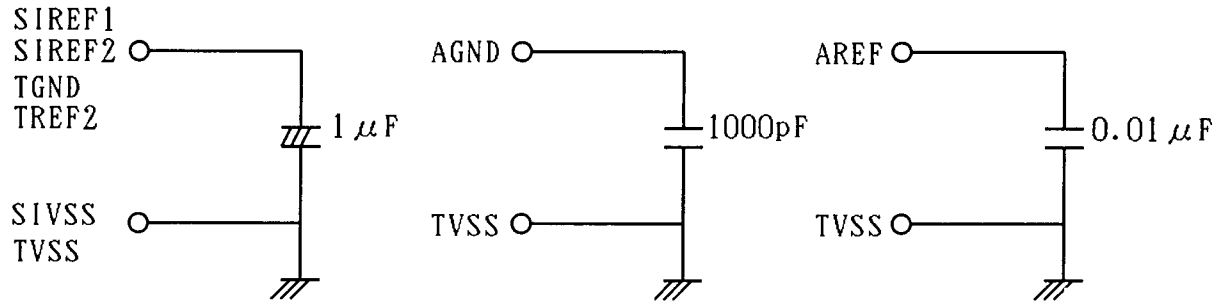
PD1 −> PD2 : This is mainly the time required for APCCON ouput stabilization.

PD2 −> PD3 : Shift time from the RXPD setting
This is mainly the time required for IF1 input part operation.

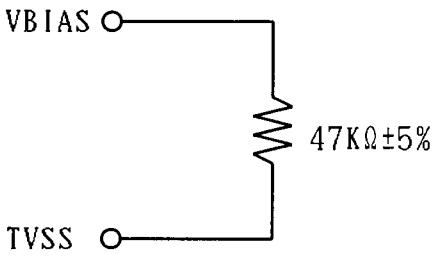
PD2 −> PD4 : Shift time from the TXRST setting
This is mainly the time required for DAC and LPF stabilization.

Recommended Circuit Examples

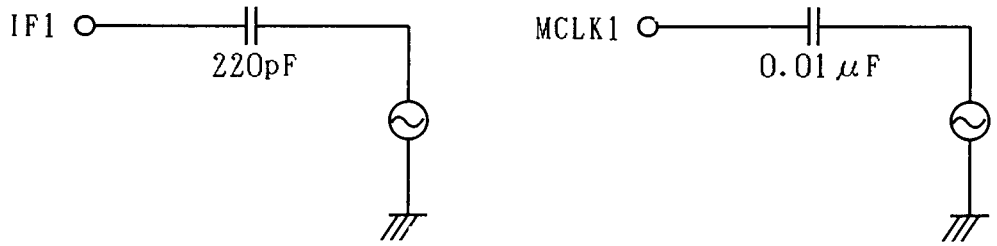
1) Capacitor for analog ground



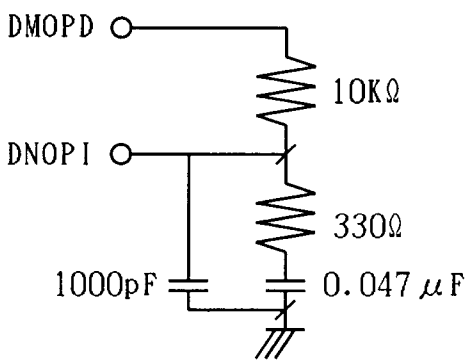
2) Resistor for VBIAS



3) DC cut capacitor



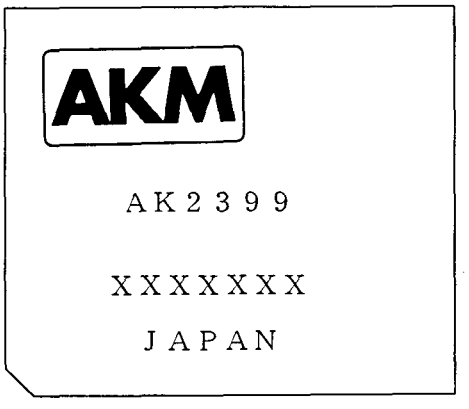
4) PLL0 loop filter

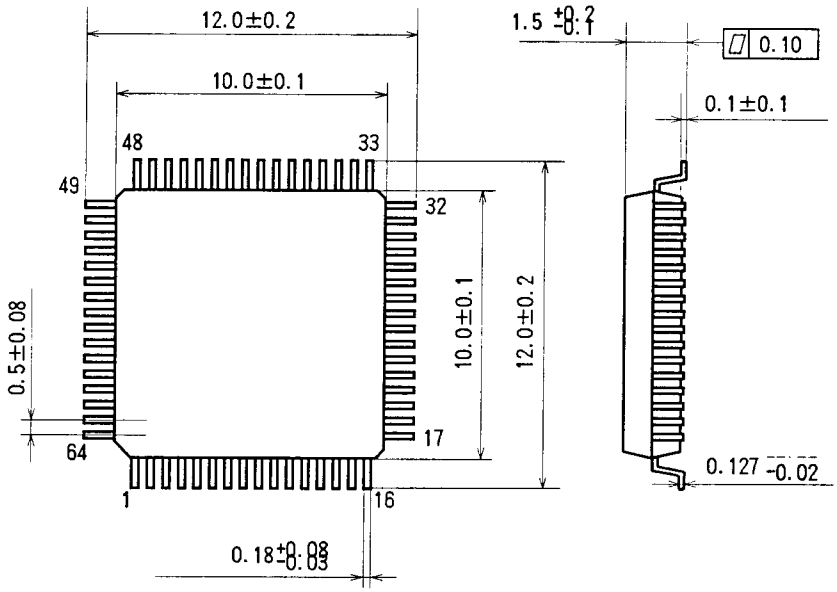


Package

■ Marking

(1) Indication of pin 1 (the bevelled corner becomes pin 1)
(2) Date code: XXXXXXX (7 digits)
(3) Marketing code: AK2399
(4) Manufacturing country name indication: JAPAN
(5) Asahi Kasei logo





■ External dimensions of the package

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