Features

- Fully Synchronous to Positive Clock Edge
- Four Banks controlled by BS0/BS1 (Bank Select)
- Programmable CAS Latency: 2, 3
- Programmable Burst Length: 1, 2, 4, 8, Full page
- Programmable Wrap: Sequential or Interleave
- Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Dual Data Mask for byte control (x16)
- Auto Refresh and Self Refresh
- 64ms refresh period (4K cycle)
- JEDEC standard 3.3V Power Supply
- LVTTL compatible
- Package: 54-pin TSOP (II)

Description

The NT5SV8M16FS and NT5SV8M16FT are four-bank Synchronous DRAMs organized as 1Mbit x 16 I/O x 4 Bank. These synchronous devices achieve high-speed data transfer rates of up to 166MHz by employing a pipeline chip architecture that synchronizes the output data to a system clock.

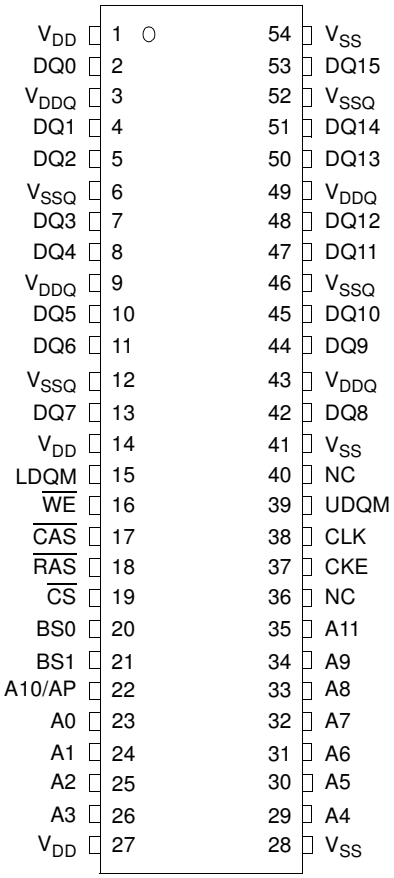
The device is designed to comply with all JEDEC standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address, and data input/output (I/O or DQ) circuits are synchronized with the positive edge of an externally supplied clock.

$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and $\overline{CS}$ are pulsed signals which are examined at the positive edge of each externally applied clock (CK). Internal chip operating modes are defined by combinations of these signals and a command decoder initiates the necessary timings for each operation. A fourteen bit address bus accepts address data in the conventional $\overline{RAS}$/$\overline{CAS}$ multiplexing style. Twelve row addresses (A0-A11) and two bank select addresses (BS0, BS1) are strobed with $\overline{RAS}$. Eight column addresses (A0-A8) plus bank select addresses and A10 are strobed with $\overline{CAS}$.

Prior to any access operation, the $\overline{CAS}$ latency, burst length, and burst sequence must be programmed into the device by address inputs A0-A7, BS0, BS1 during a mode register set cycle. In addition, it is possible to program a multiple burst sequence with single write cycle for write through cache operation.

Operating the four memory banks in an interleave fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate of up to 166MHz is possible depending on burst length, $\overline{CAS}$ latency, and speed grade of the device. Simultaneous operation of both decks of a stacked device is allowed, depending on the operation being done. Auto Refresh (CBR) and Self Refresh operation are supported.

Pin Assignments for Planar Components (Top View)



54-pin Plastic TSOP(II)

Pin Description

CLK	Clock Input	DQ0-DQ15	Data Input/Output
CKE	Clock Enable	LDQM, UDQM	Data Mask
$\overline{CS}$	Chip Select	V_{DD}	Power supply
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	V_{DDQ}	Output Power for DQs
$\overline{WE}$	Write Enable	V_{SSQ}	Ground for DQs
BS1, BS0	Bank Select	NC	No Connection
A0 - A11	Address Inputs	—	—

Input/Output Functional Description

Symbol	Type	Polarity	Function
CLK	Input	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Active High	Activates the CLK signal when high and deactivates the CLK signal when low. By deactivating the clock, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{CS}$	Input	Active Low	$\overline{CS}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BS0, BS1	Input	—	Selects which bank is to be active.
A0 - A11	Input	—	During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A7 defines the column address (CA0-CA7) when sampled at the rising clock edge. A10 is used to invoke auto-precharge operation at the end of the burst read or write cycle. If A10 is high, auto-precharge is selected and BS0, BS1 defines the bank to be precharged. If A10 is low, auto-precharge is disabled. During a Precharge command cycle, A10 is used in conjunction with BS0, BS1 to control which bank(s) to precharge. If A10 is high, all banks will be precharged regardless of the state of BS. If A10 is low, then BS0 and BS1 are used to define which bank to precharge.
DQ0 - DQ15	Input-Output	—	Data Input/Output pins operate in the same manner as on conventional DRAMs.
LDQM UDQM	Input	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In x16 products, LDQM and UDQM control the lower and upper byte I/O buffers, respectively.
V_{DD}, V_{SS}	Supply	—	Power and ground for the input buffers and the core logic.
V_{DDQ} V_{SSQ}	Supply	—	Isolated power supply and ground for the output buffers to provide improved noise immunity.

Ordering Information

Organization	Part Number	Speed Grade	Power Supply	Package
		Clock Frequency@CAS Latency		
8M x 16	N2SV12816FT-6K	166MHz@CL3	3.3 V	54-PIN TSOP II
	N2SV12816FT-75B	133MHz@CL3		
	N2SV12816FS-6K	166MHz@CL3	3.3 V	54-PIN TSOP II Green
	N2SV12816FS-75B	133MHz@CL3		

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Power Supply Voltage	-1.0 to +4.6	V	1
V_{DDQ}	Power Supply Voltage for Output	-1.0 to +4.6	V	1
V_{IN}	Input Voltage	-1.0 to +4.6	V	1
V_{OUT}	Output Voltage	-1.0 to +4.6	V	1
T_A	Operating Temperature (ambient)	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +150	°C	1
P_D	Power Dissipation	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0°C to 70°C)

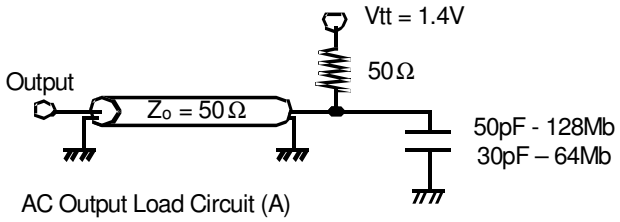
Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	3.0	3.3	3.6	V	
V_{DDQ}	Supply Voltage for Output	3.0	3.3	3.6	V	
V_{IH}	Input High Voltage	2.0	3.0	V_{DD} + 0.3	V	1
V_{IL}	Input Low Voltage	-0.3	0	0.8	V	2
V_{OH}	Output Level (LVTTL) Output “H” Level Voltage	2.4	—	—	V	I_{OH} = -2.0mA
V_{OL}	Output Level (LVTTL) Output “L” Level Voltage (	—	—	0.4	V	I_{OL} = 2.0mA

1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The overshoot voltage duration is ≤ 3ns.

Capacitance (T_A = 23°C, f = 1MHz, V_{DD} = 3.3V, V_{REF}=1.4+/-200mV)

Symbol	Parameter	Min.	64Mb Max.	128Mb Max.	Units
C_{IN}	Input Capacitance (A0-A11, BS0, BS1, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, DQM)	2.5	5.0	3.8	pF
C_{ADD}	Address	2.5	5.0	3.8	pF
C_{CLK}	Input Clock (CLK)	2.5	4.0	3.5	pF
C_{OUT}	Output Capacitance (DQ0 - DQ15)	4.0	6.5	6.0	pF

AC Output Load Circuit



AC Output Load Circuit (A)

AC Operating Test Conditions (Vdd=3.3+/-0.3V, TA=0 to 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf=1/1	ns
Output timing measurement reference level	1.4	V

Operating, Standby, and Refresh Currents (T_A = 0 to +70°C, V_{DD} = 3.3V ±0.3V)

Parameter	Symbol	Test Condition	-6K (6ns)	-75B (7ns)	Units	Notes
Operating Current	I_{CC1}	1 bank operation $t_{RC} = t_{RC}(min)$, t_{CK} = min Active-Precharge command cycling without burst operation	130	90	mA	1, 2, 3
Precharge Standby Current in Power Down Mode	I_{CC2P}	$\overline{CKE} \le V_{IL}(max)$, t_{CK} = min, $\overline{CS} = V_{IH}(min)$	4	4	mA	1
	I_{CC2PS}	$\overline{CKE} \le V_{IL}(max)$, t_{CK} = Infinity, $\overline{CS} = V_{IH}(min)$	4	4	mA	1
Precharge Standby Current in Non-Power Down Mode	I_{CC2N}	$\overline{CKE} \ge V_{IH}(min)$, t_{CK} = min, $\overline{CS} = V_{IH}$ (min)	20	20	mA	1, 5
	I_{CC2NS}	CKE ≥ V_{IH}(min), t_{CK} = Infinity,	10	10	mA	1, 7
No Operating Current (Active state: 4 bank)	I_{CC3N}	$\overline{CKE} \ge V_{IH}(min)$, t_{CK} = min, $\overline{CS} = V_{IH}$ (min)	35	35	mA	1, 5
	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CK} = min,	5	5	mA	1, 6
Operating Current (Burst Mode)	I_{CC4}	t_{CK} = min, Read/ Write command cycling, Multiple banks active, gapless data, BL = 4	150	110	mA	1, 3, 4
Auto (CBR) Refresh Current	I_{CC5}	t_{CK} = min, $t_{RC} = t_{RC}(min)$ CBR command cycling	220	200	mA	1
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	4	4	mA	1

1. Currents given are valid for a single device. The total current for a stacked device depends on the operation being performed on the other deck.
2. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t_{CK} and t_{RC}. Input signals are changed up to three times during t_{RC}(min).
3. The specified values are obtained with the output open.
4. Input signals are changed once during t_{CK}(min).
5. Input signals are changed once during three clock cycles.
6. Active Standby Current will be higher if Clock Suspend is entered during a burst read cycle (add 1mA per DQ).
7. Input signals are stable.

AC Timing Parameters

Symbol	Parameter	-6K (166)		-75B (133)		Units
		Min.	Max.	Min.	Max.	
t_{CK3}	Clock Cycle Time, $\overline{CAS}$ Latency = 3	6	—	7.5	—	ns
t_{CK2}	Clock Cycle Time, $\overline{CAS}$ Latency = 2	10	—	10	—	ns
t_{AC3}	Clock Access Time, $\overline{CAS}$ Latency = 3	—	5	—	5.4	ns
t_{AC2}	Clock Access Time, $\overline{CAS}$ Latency = 2	—	6	—	6	ns
t_{OH3}	Output data Hold Time, , $\overline{CAS}$ Latency = 3	2.5	—	3	—	ns
t_{OH2}	Output data Hold Time, , $\overline{CAS}$ Latency = 2	3	—	3	—	ns
t_{LZ}	Data Out to Low Impedance time	0	—	0	—	ns
t_{HZ}	Data Out to High Impedance time	3	7	3	7	ns
t_{WR}	Write Recovery Time	2	—	2	—	CLK
t_{CKH}	Clock High Pulse Width	2.5	—	2.5	—	ns
t_{CKL}	Clock Low Pulse Width	2.5	—	2.5	—	ns
t_{IS}	Input Set-up Time	1.5	—	1.5	—	ns
t_{IH}	Input Hold Time	1	—	0.8	—	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	18	—	20	—	ns
t_{RC}	Bank Cycle Time	60	—	65	—	ns
t_{RAS}	Active Command Period	42	100K	45	100K	ns
t_{RP}	Precharge Time	18	—	20	—	ns
t_{RRD}	Bank to Bank Delay Time	12	—	15	—	ns
t_{CDL}	Last data into new column address delay	1	—	1	—	CLK
t_{CCD}	Column address to column address delay	1	—	1	—	CLK

Package Dimensions (54 lead; Thin Small Outline Package)

Unit : Millimeters