PBM 397 02
DUAL CMOS CODEC/FILTER

General

A monolithic circuit containing A/D- and D/A-conversion and PCM-coding for two separate telephone lines, to be manufactured in a 5 V single supply CMOS process.

Features Complete CODEC and filtering system for two telephone lines including:

- free operational amplifier for gain adjust in both directions
- internal precision voltage reference
- antialiasfiltering
- smoothing filtering
- sinx/x correlation
- A-law/μ-law pin selectable
- auto power down mode
- power on reset
- common serial digital I/O both channels
- separate frame sync each channel
- 24 pin VSOP package

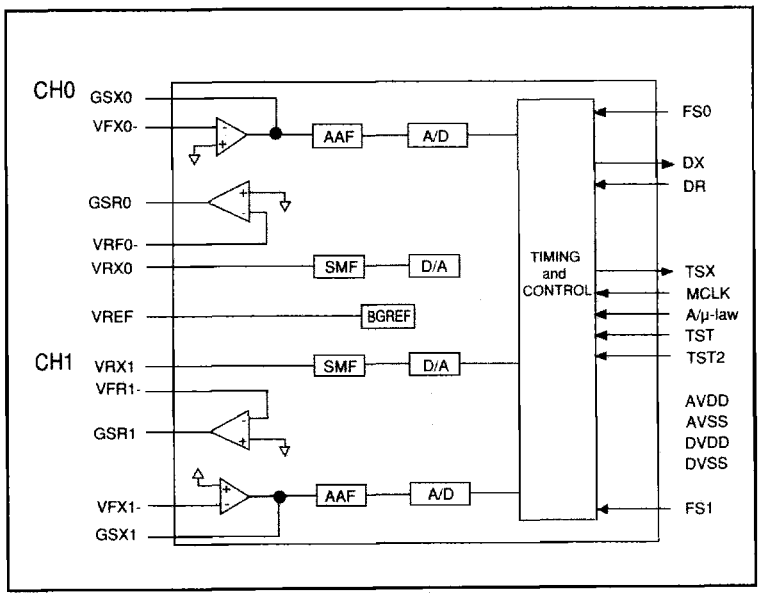

Fig. 1 Block Diagram

Pin description

Pin No	Pin Name	I/O	TTL	Function
1	AVDD	-		Analogue positive supply voltage. Systems analogue +5 V supply.
2	TST2	I		Test pin. Tie to logic high for normal operation. The device enters test mode with TST2 low.
3	VFX0-	I		Transmit analogue input Negative input of transmit input amplifier channel 0
4	GSX0	O		Output of transmit input amplifier channel 0
5	VRX0	O		Receive analogue output unamplified, Channel 0
6	VFR0-	I		Negative input of receive output amplifier channel 0
7	GSR0	O		Amplified receive analogue output channel 0
8	TST	I		Test pin. Tie to logic high in normal operation. With TST low, the device enters power down mode.
9	FS0	I	X	Frame sync input for channel 0
10	MCLK	I	X	Master clock.
11	TSX	O		Open drain output pulsing low during digital transmission cycle.
12	DVDD	-		Digital positive supply voltage. Systems digital +5 V supply.
13	DVSS	-		Digital negative supply voltage. Systems digital ground
14	DX	O		Serial output of digital transmit data.
15	DR	I	X	Serial input of digital receive data.
16	FS1	I	X	Frame sync input for channel 1
17	ALAWN	I	X	Selects A-law or µ-law companding scheme. Logic zero selects A-law.
18	GSR1	O		Amplified receive analogue output channel 1
19	VFR1-	I		Negative input of receive output amplifier channel 1
20	VRX1	O		Receive analogue output unamplified, Channel 1
21	GSX1	O		Output of transmit input amplifier channel 1
22	VFX1-	I		Transmit analogue input Negative input of transmit input amplifier channel 1
23	VREF	O		Band gap stabilized internal reference voltage performing zero level (analogue ground) to the data conversion respective channel. Internally connected to the positive inputs of transmit input and receive output amplifiers. External capacitor 1.0 µF or larger recommended
24	AVSS	-		Analogue negative supply voltage. Systems analogue grond.

Absolute Maximum Ratings

Quantity	Value	Unit
Supply voltage any VDD to AVSS	-0.3...+6.5	V
Voltage DVSS to AVSS	-0.1...+0.1	V
Voltage any pin to AVSS	-0.3...+6.5	V
	and	
	< AVDD+0.3	V
Max current at any pin except supply voltage pins	-10...+10	mA
(Latch-up immunity)		
Operating temperature	0...+85	°C
Storage temperature	-55...+125	°C
Lead temperature, soldering 10 seconds	+300	°C

Recommended Operating Conditions

Quantity	Value	Unit
AVDD Supply Voltage	4.75..5.25	V
DVDD Supply Voltage	4.75..AVDD	V
Ambient Operating Temperature	0...+85	°C
Master Clock Frequency	2.048	MHz

Electrical characteristics

Unless otherwise noted, the specification applies for TA = 0 to +85 ∞C,
DVDD = AVDD = 5 V ± 5%, DVSS = AVSS = 0 V and MCLK = 2.048 MHz.

Power dissipation

Quantity	Conditions	Min	Typ	Max	Unit
Power dissipation	Outputs unloaded	60	80		mW

Digital Interface

Quantity	Conditions	Min	Typ	Max	Unit
Input Low Voltage				0.8	V
Input High Voltage		2.0			V
Output Low Voltage	IL = 3.2 mA			0.4	V
Output High Voltage	IL = 3.2 mA	2.4			V
Input Current		-10		+10	mA
Input Capacitance				5	pF
Output Current	Tri-state mode	-10		+10	µA

Analogue Interface Transmit Input Amplifier

Quantity	Conditions	Min	Typ	Max	Unit
Input Leakage Current	0.6 V < V < 4.2 V	-100		+100	nA
Input Resistance		10			MΩ
Input Voltage	Relative AVSS	2.3	2.4	2.5	V
Voltage Gain		5000			V/V
Unity-Gain Bandwidth		1.0	2.0		MHz
Offset Voltage		-20		+20	mV
Load Resistance		10			kΩ
Load Capacitance				50	pF
Output Voltage Swing			3.6		Vpp
Output resistance				10	Ω
Power Supply Rejection Ratio	0-60kHz	tbd			dB

Analogue Interface Receive Output

Quantity	Conditions	Min	Typ	Max	Unit
Output Resistance				10	Ω
Output Voltage	0 dBm0 PCM code	2.3	2.4	2.5	V
Output Voltage Swing			3.6		Vpp
Load Resistance		10			kΩ
Load Capacitance				50	pF

Analogue Interface Receive Output Amplifier

Quantity	Conditions	Min	Typ	Max	Unit
Input Leakage Current	0.6 V < V < 4.2V	-100		+100	nA
Input Resistance		10			MΩ
Input Voltage		2.3	2.4	2.5	V
Voltage Gain		5000			V/V
Unity-Gain Bandwidth		1.0	2.0		MHz
Offset Voltage		-20		+20	mV
Load Resistance		10			kΩ
Load Capacitance				50	pF
Output Voltage Swing			3.6		Vpp
Output Resistance				10	Ω
Power Supply Rejection Ratio	0 - 60 kHz	tbd			dB

Transmission characteristics

Unless otherwise noted, the specification applies for TA = 0 to +85 °C, DVDD = AVDD = 5 V ± 5%, DVSS = AVSS = 0 V and MCLK = 2.048 MHz. Analog input is a 0 dBm0, 1020 Hz sine wave; transmit input amplifier set for unity gain. Digital input is a code sequence for 0 dBm0, 1020 Hz sine wave. Conditions and values should be measured related to the system analogue ground, i.e. AVSS, see Typical Application.

Absolute Gain

Quantity	Conditions	Min	Typ	Max	Unit
Analogue Input Level	0 dBm0		0.849		Vrms
Absolute Transmit Gain		-0.25		+0.25	dB
Absolute Transmit Gain	@VDD=5V,T=25°C	-0.15		+0.15	dB
Analogue Output Level	0 dBm0		0.849		Vrms
Absolute Receive Gain		-0.25		+0.25	dB
Absolute Receive Gain	@VDD=5V,T=25°C	-0.15		+0.15	dB
Maximum Overload Level	3.14 dBm0		1.219		Vrms

Gain Tracking

Quantity	Conditions	Min	Typ	Max	Unit
Transmit Gain Tracking Error					
Reference Level:	+3 dBm0 to -40 dBm0	-0.2		+0.2	dB
-10 dBm0 sine wave	-40 dBm0 to -50 dBm0	0.4		+0.4	dB
	-50 dBm0 to -55 dBm0	-1.2		+1.2	dB
Receive Gain Tracking Error					
Reference Input: sine wave	+3 dBm0 to -40 dBm0	-0.2		+0.2	dB
-10 dBm0 PCM code	-40 dBm0 to -50 dBm0	-0.4		+0.4	dB
	-50 dBm0 to -55 dBm0	-1.2		+1.2	dB

Frequency response

Quantity	Conditions	Min	Typ	Max	Unit
Transmit Gain Relative Gain	f = 50 Hz			-30	dB
	f = 60 Hz			-26	dB
	f = 200 Hz	-1.8		0	dB
	f = 300 Hz - 3000 Hz	-0.15		+0.15	dB
	f = 3400 Hz	-0.8		0	dB
	f ≥ 4000 Hz			tbd	dB
Receive Gain Relative Gain	f = 0 Hz - 3000 Hz	-0.15		+0.15	dB
	f = 3400 Hz	-0.8		0	dB
	f ≥ 4000 Hz			tbd	dB

Distorsion

Quantity	Conditions	Min	Typ	Max	Unit
Transmit Signal to Distortion	0 dBm0 - -30 dBm0	36			dB
	-30 dBm0 - -40 dBm0	30			dB
	-40 dBm0 - -45 dBm0	25			dB
Receive Signal to Distortion	0 dBm0 - -30 dBm0	36			dB
	-30 dBm0 - -40 dBm0	30			dB
	-40 dBm0 - -45 dBm0	25			dB
Single Frequency Distortion:					
Transmit				-46	dB
Recieve				-46	dB
Intermodulation Distortion	Two frequencies in the range 300 Hz - 3400 Hz at - 6 dBm0			-42	dB

Envelope Delay Distorsion

Quantity	Conditions	Min	Typ	Max	Unit
Transmit Delay, Absolute	f = 1600Hz			315	us
Transmit Delay, Relative	f = 500 Hz - 600 Hz			220	us
	f = 600 Hz - 1000 Hz			145	us
	f = 1000 Hz - 2600 Hz			75	us
	f = 2600 Hz - 2800 Hz			105	us
	f = 2800 Hz - 3000 Hz			155	us
Receive Delay, Absolute	f = 1600 Hz			200	us
Receive Delay, Relative	f = 500 Hz - 1000 Hz	-40			us
	f = 1000 Hz - 1600 Hz	-30			us
	f = 1600 Hz - 2600 Hz			90	us
	f = 2600 Hz - 2800 Hz			125	us
	f = 2800 Hz - 3000 Hz			175	us

Noise

Quantity	Conditions	Min	Typ	Max	Unit
Transmit Noise, Psophometric					
Weighted, A-law			tbd	tbd	dBm0p
Transmit Noise, C Message					
Weighted, u-law			5	10	dBrnC0
Receive Noise, Psophometric					
Weighted, A-law			-85	-80	dBm0p
Receive Noise, C Message					
Weighted, u-law			5	10	dBrnC0
Noise, Single Frequency	VFXIN = 0 Vrms, DR = DX			-53	dBm0
PSRR, Transmit	DVDD = AVDD =				
	= 5.0 V + 0.1 Vrms				
	f = 0 Hz - 50000 Hz	tbd			dB
PSRR, Receive	PCM code is pos. zero				
	DVDD = AVDD =				
	5.0 V + 0.1 Vrms				
	f = 0 Hz - 50000 Hz	tbd			dB
Spurious Out-of-Band	Input: 0 dBm0,				
Signals at VRX Output	300 Hz -- 3400 Hz				
	PCM code applied				
	4.6 kHz - 7.6 kHz			tbd	dB
	7.6 kHz - 8.4 kHz			tbd	dB
	8.4 kHz - 100 kHz			tbd	dB

Interchannel Crosstalk

Quantity	Conditions	Min	Typ	Max	Unit
Transmit to Receive	0 dBm0 at VFXIN			-75	dB
Channel under test	Idle PCM code				
Receive to Transmit	0 dBm0 code level			-75	dB
Channel under test	VFXIN = 0 Vrms				
Transmit to Transmit	0 dBm0 at VFXIN			-75	dB
Channel under test	VFXIN = 0 Vrms				
Receive to Receive	0 dBm0 code level			-75	dB
Channel under test	Idle PCM code				

Intrachannel Crosstalk

Quantity	Conditions	Min	Typ	Max	Unit
Transmit to Receive	0 dBm0 at VFXIN			-75	dB
	Idle PCM code				
Receive to Transmit	VFXIN = 0 Vrms			-75	dB
	0 dBm0 code level				

Timing and Control specification

Power on Reset

Power on reset is implemented for the power supply related power up. During the typical 20 ms initialization sequence, any input on FSn (n=0,1) will not be taken notice of.

Long/Short Frame Sync

Long or short frame sync timing mode is defined by the first frame sync pulse after power up. This apply to power supply related power up as well as power up after power down.

Long frame sync timing is selected if first frame sync is two or more MCLK pulses. Otherwise short frame sync timing is selected.

Time Slot Assignment

Both FS0 and FS1 must be derived from MCLK and both should have a periodicity of 256 MCLK cycles.

Time slot 0 is determined by the slot defined by FS0 or FS1 whichever comes first. If the other channel is to be used, FS for other channel must be delayed from the first by a multiple of 8 MCLK cycles.

In order to change channel/s/ in use and time slot of each channel in use , the device must be reset to power down (TST pin low or absence of FS0 and FS1), before channels and time slots can be selected as described above.

Auto Power Down Mode

The device enters powerdown mode if either TST pin is low or the FS0 or FS1 defining time slot 0, is not present within 500µs (i.e. 4 time frames).

Power down is not guaranteed if MCLK is lost unless the device was already in power down mode due to the absence of frame sync.

Timing Specification

Unless otherwise noted, the specification applies for TA = 0 to +85 °C, DVDD = AVDD = 5 V ± 5%, DVSS = AVSS = 0 V , MCLK = 2.048 Mhz, VIH=2.0V ,VIL=0.8V,VOL=0.4V and VOH=2.4V

Parameter	Symbol	Ref fig	Min	Typ	Max	Unit
Frequency of Master Clock, MCLK 1)	1/TPM	2		2.048		MHz
Width of Master Clock High	tWMH	2	195			ns
Width of Master Clock Low	tWML	2	195			ns
Rise time of Master Clock	tRM	2			40	ns
Fall time of Master Clock	tFM	2			40	ns
Delay time to valid Data from FS or MCLK, whichever comes later, and Delay time from FS to Data Output disabled 2)	tDZF	3	20		165	ns
Delay time from MCLK Low to Data Output disabled	tDZC	2	50		165	ns
Setup time from DR Valid to MCLK Low	tSDM	3	40			ns
Hold time from MCLK Low to DR Invalid	tHMD	3	50			ns
Hold time from MCLK Low to Frame Sync	tHMF	3	0			ns
Setup time from Frame Sync to MCLK	tSFM	3	70		T_{PM} -70	ns
Hold time from 3rd period in time slot of MCLK Low to Frame Sync	tHMFI	3	90			ns
Delay time from MCLK High to Data Valid 2)	tDMD	2	0		170	ns
Setup time from FS to MCLK Low	tSF	2	80		T_{PM} -80	ns
Hold time from MCLK Low to FS Low	tHF	2	100			ns
Delay time TSX Low 3)	tXDP	2	0		140	ns

Note : 1) MCLK must be continuously present except when TST pin is low
2) Load on DX 150pF plus 2 LSTTL Loads
3) Load on TSX 150 pF

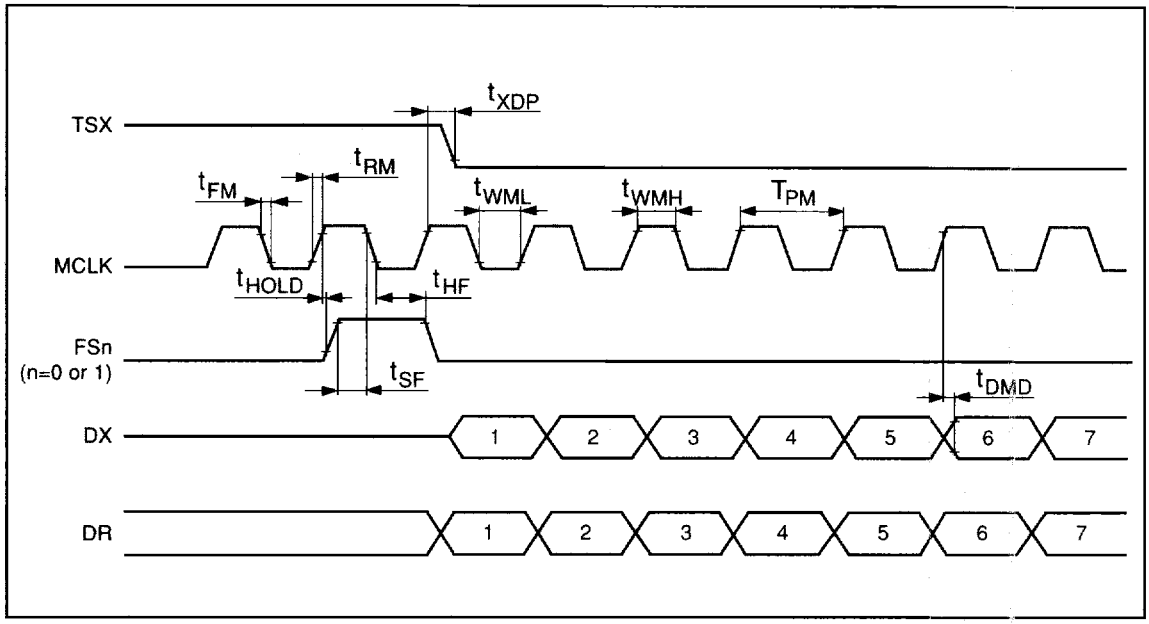

Fig. 2 Short Frame Sync Timing Diagram

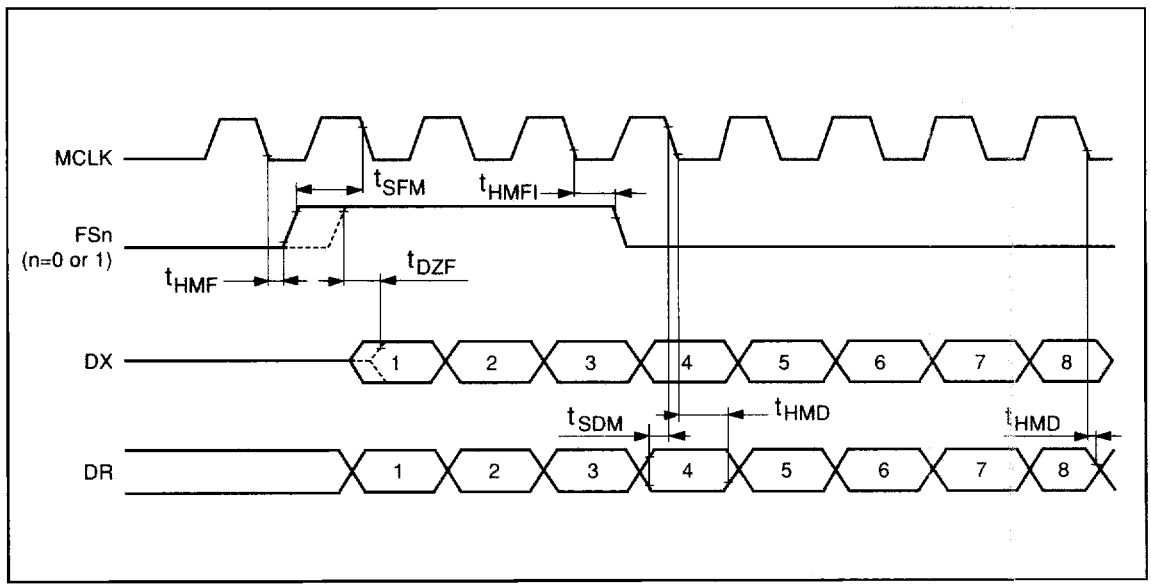

Fig. 3 Long Frame Sync Timing Diagram

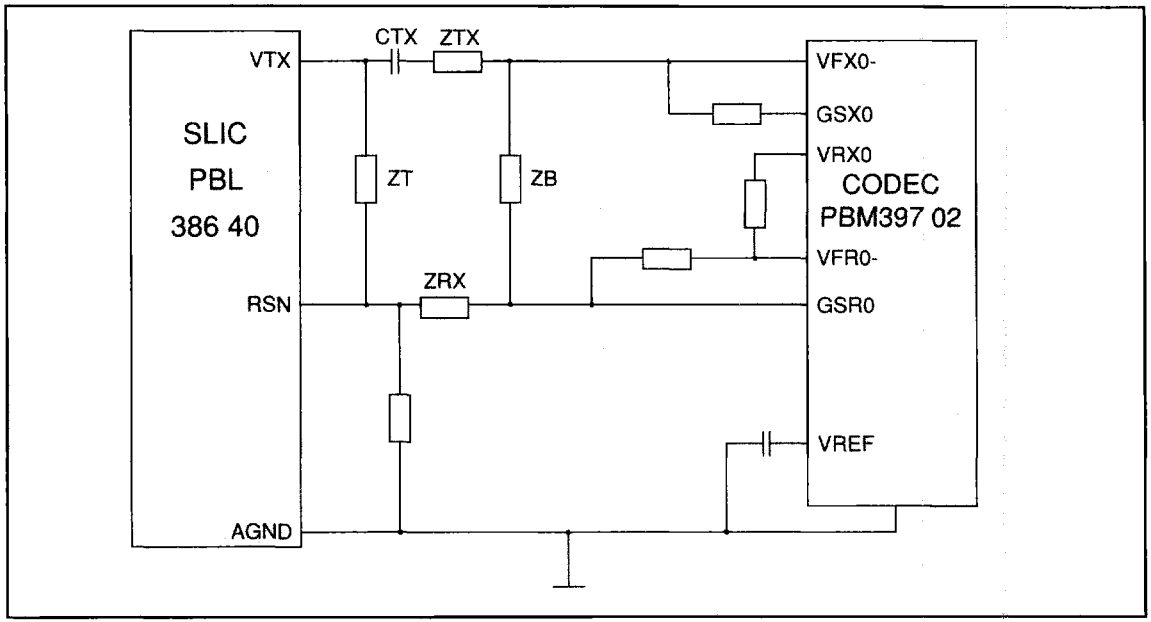

Fig 4. Typical application (one channel)