BIT Bipolar Integrated Technology, Inc.

B2018

Preliminary

TTL 16 x 16 Bit Fixed-Point Multiplier

FEATURES

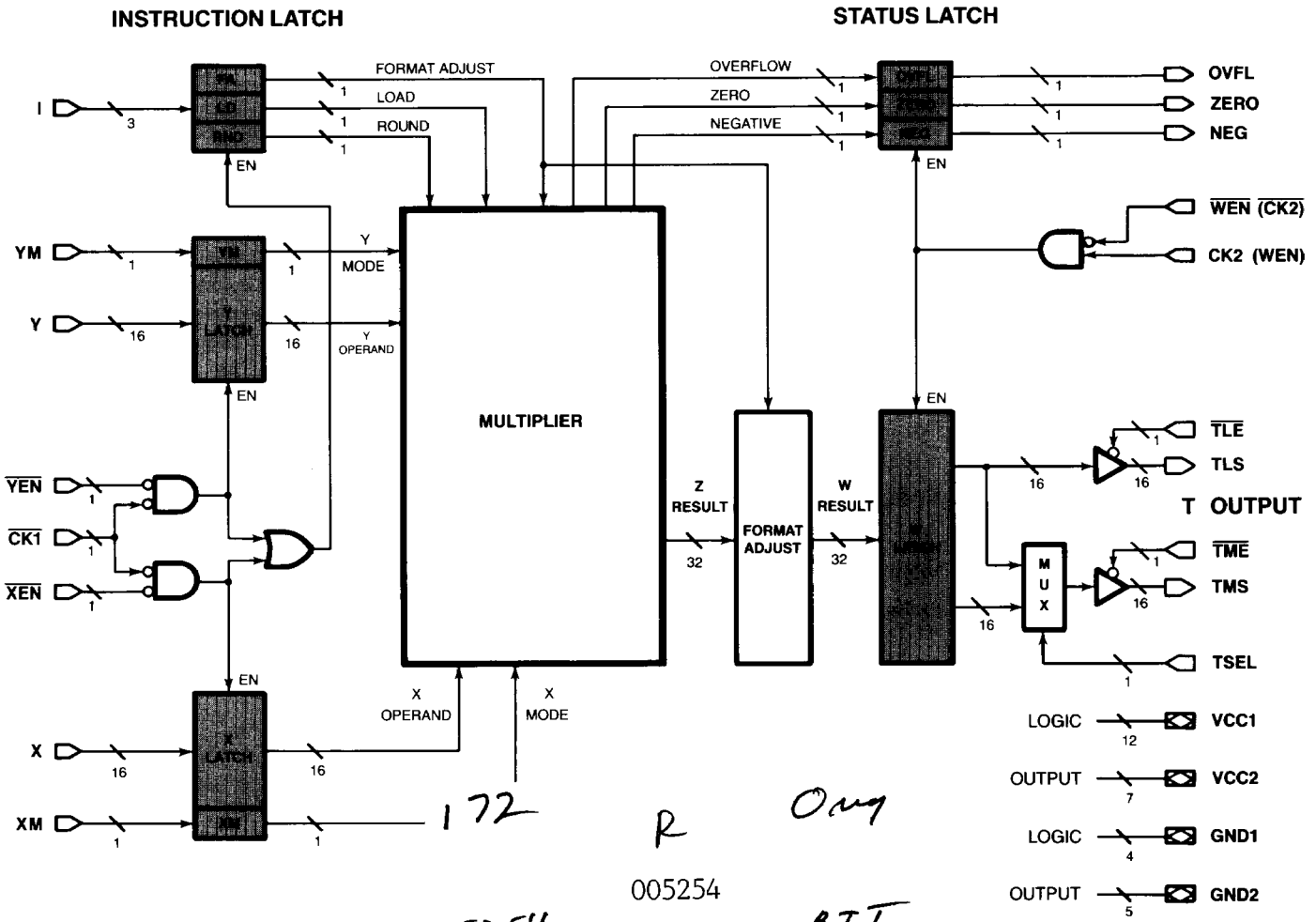
- 19ns worst case clocked multiply time
- Full 32-bit product output port
- 16-bit output multiplexer
- Transparent input and/or output latches
- Unsigned, two's complement or mixed mode operands
- Single, double or triple clock operation
- Separate negative sign, overflow and zero status flags
- Format adjust
- Rounding for both formats
- Parallel loading from input ports to output
- Separate most and least significant three-state output enables
- Individually enabled input and output latches
- Small 1.20" square 108-pin pin grid array package
- Low power, 2.2 watts typical

DESCRIPTION

The B2018 is a high-speed 16 x 16 bit fixed-point multiplier for TTL logic. Two 16-bit operands of unsigned, two's complement signed or mixed mode are multiplied to produce a 32-bit product. The full result is available in parallel, as separately enabled three-state 16-bit least and most significant portions, or multiplexed at a single 16-bit port. Input operands and output result are stored in individually enabled latches with separate clocks for input and output for pipelines. The latches can be made transparent by leaving clocks and enables active for flow-through operation. Inverted clocks may be tied together for a single-clock positive-edge-triggered-like function.

The 32-bit result may be format adjusted for a consistent signed fractional output format and for maximum precision in a 16-bit output. Rounding for a 16-bit output may be selected and is correct for either output format. Three status flags indicate the presence of a zero, negative or overflowed result. The input operands can be loaded directly to the output without multiplication but with format adjustment, rounding and setting of status flags.

BLOCK DIAGRAM



SIGNAL SUMMARY

Data		
Inputs	X0-15, Y0-15	32
Output	TLS0-15, TMS0-15	32
Control		
Latch Enables	$\overline{XEN}$, $\overline{YEN}$, $\overline{WEN}$	3
Mode	XM, YM	2
Instructions	I0-2: FA, LD, RND	3
Flags	OVFL, ZERO, NEG	3
Output Select	TSEL	1
Output Enables	$\overline{TME}$, $\overline{TLE}$	2
Clocks		
Inputs	$\overline{CK1}$	1
Outputs	CK2	1
Power		
Logic Gnd	GND 1	4
Output Gnd	GND 2	5
Logic +5.0V	VCC1	12
Output +5.0V	VCC2	7
Total		**108**

SIGNAL DESCRIPTION

Data

X0-15 — X operand input port. Bit 0 is least significant bit.

Y0-15 — Y operand input port.

TMS0-15 — Most significant 16 bits of 32-bit output port T.

TLS0-15 — Least significant 16 bits of 32-bit output port T.

Control

$\overline{XEN}$, $\overline{YEN}$, $\overline{WEN}$ — Enable input for data latches X and XM, Y and YM and W respectively.

XM, YM — Inputs to XM and YM mode latches. Determine unsigned (XM, YM = 0) or two's complement (XM, YM = 1) mode of X and Y operands. See Figure 1. Latches enabled by $\overline{XEN}$ and $\overline{YEN}$ respectively and clocked by $\overline{CK1}$.

I0-2 — Instruction input port to Format Adjust, Load and Round instruction latches respectively. Latches enabled by $\overline{XEN}$ or $\overline{YEN}$ and clocked by $\overline{CK1}$

FA — Format Adjust provides a choice of output data format in result W depending on system requirements. See Figure 3.

LD — Loads the intermediate result Z with the concatenated X and Y operands when LD = 1. XM determines the sign mode of the result. When LD = 0 the intermediate result Z is the product of the operands X and Y. Rounding and Format Adjust are always applied to the intermediate result Z and status flags are generated. See Figure 2.

RND — The full precision format-adjusted W result is rounded to the nearest most significant 16-bit portion.

ZERO, OVFL, NEG — Output status flags generated from the intermediate result Z. The ZERO latch is set when the full 32-bit result is zero, or if RND = 1, when the rounded most significant 16-bit only result is zero. ZERO will not be set if an overflow condition exists. The OVFL latch is set only on a two's complement number, when due to output format adjustment, data has exceeded what can be represented in the output format. The NEG latch is set only when the two's complement result is negative. A loaded format-adjusted negative overflow number will set NEG as well as OVFL. Flag latches are enabled by $\overline{WEN}$ and clocked by CK2.

TSEL — Input that selects the least or most significant 16-bits of result W for output through the TMS port. TSEL = 0 is the most significant portion, TSEL = 1 is the least significant portion. See Figure 4.

$\overline{TME}$, $\overline{TLE}$ — Inputs to enable the three-state outputs of the TMS and TLS ports respectively.

Clocks

$\overline{CK1}$ — Clock input to all input latches X, XM, Y, YM and I (FA, LD, RND). Data is held in the enabled latch when $\overline{CK1}$ = 1, the enabled latch follows input data when $\overline{CK1}$ = 0. The input latches are made transparent by holding $\overline{CK1}$ = 0 and their enables low.

CK2 — Clock input to all output latches W, ZERO, OVFL and NEG. Data is held in the enabled latches when CK2 = 0, the enabled latches follow data when CK2 = 1. The output latches are made transparent by holding CK2 = 1 and $\overline{WEN}$ = 0.

Power

VCC1 — Positive supply voltage to internal logic circuitry.

VCC2 — Positive supply voltage to output circuitry.

GND1 — Negative supply voltage to internal logic circuitry.

GND2 — Negative supply voltage to output circuitry.

FIGURE 1. Input Operand Formats and Sign Mode Operation

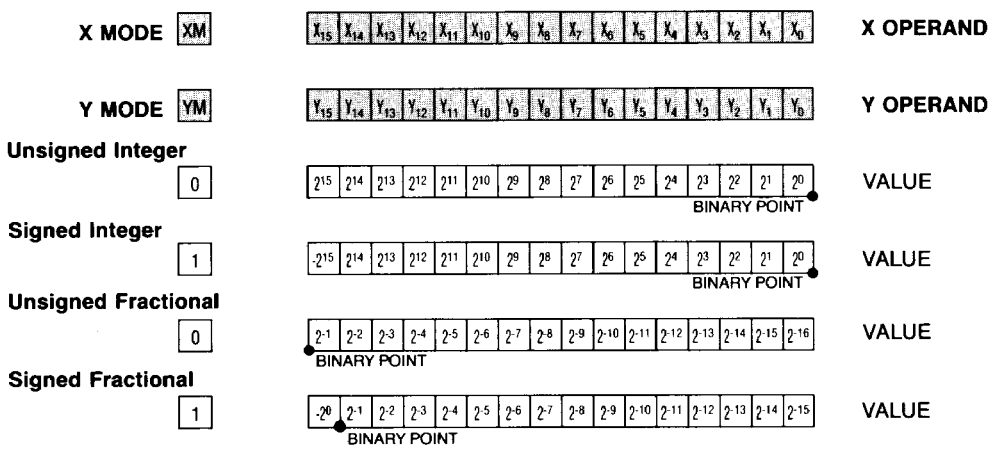
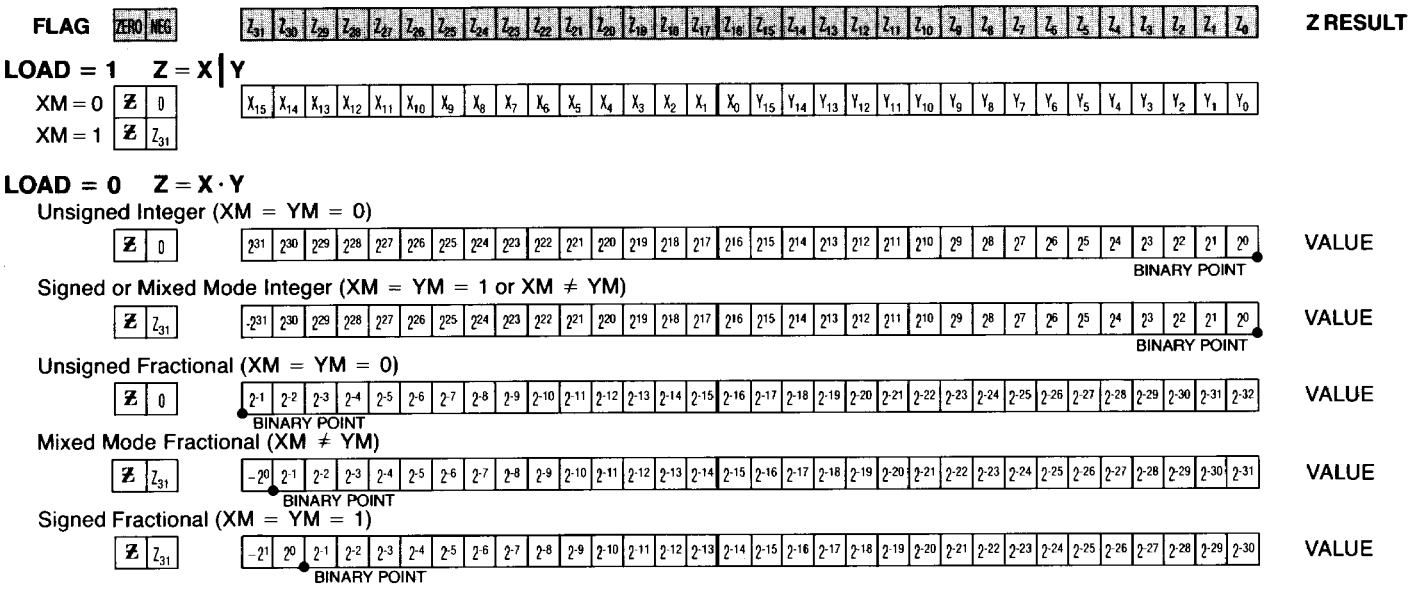


FIGURE 2. Result Z Formats, Zero and Neg Status Flags, and Load Operation

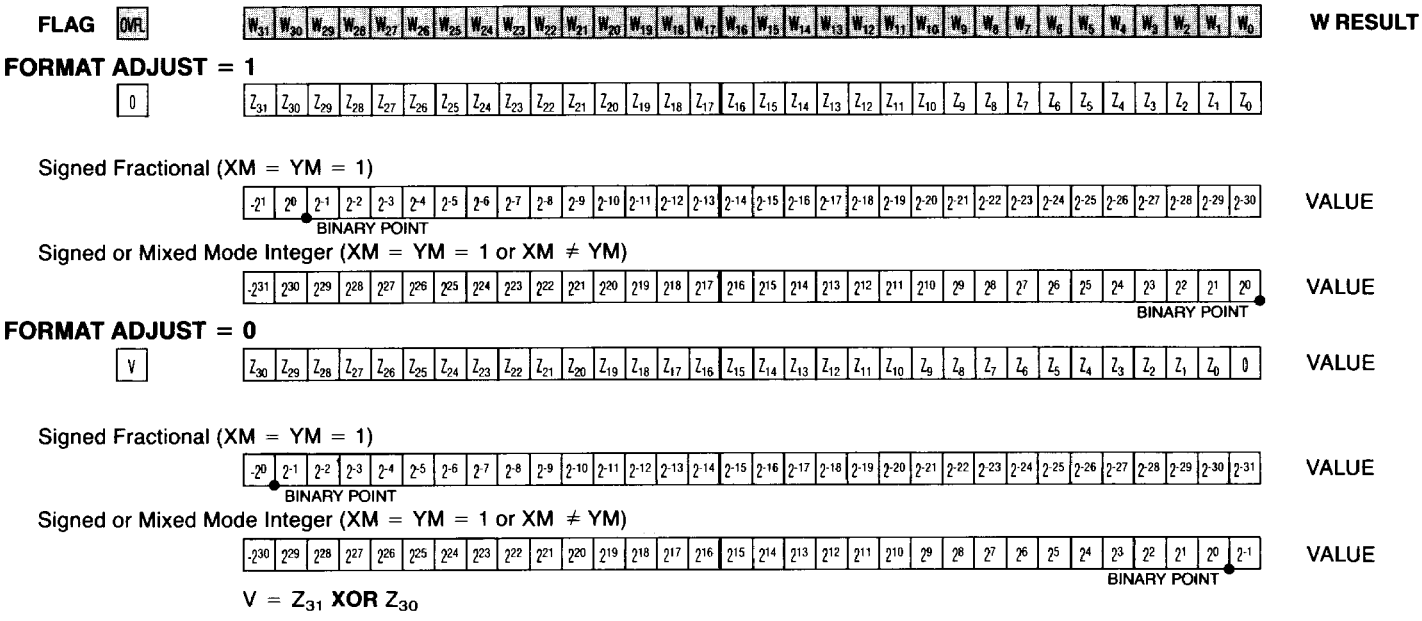


$\overline{Z}$ = **NOR** Z_0-Z_{31} when **RND** = 0

$\overline{Z}$ = **NOR** Z_{16}-Z_{31} when **RND** = 1, FA = 1

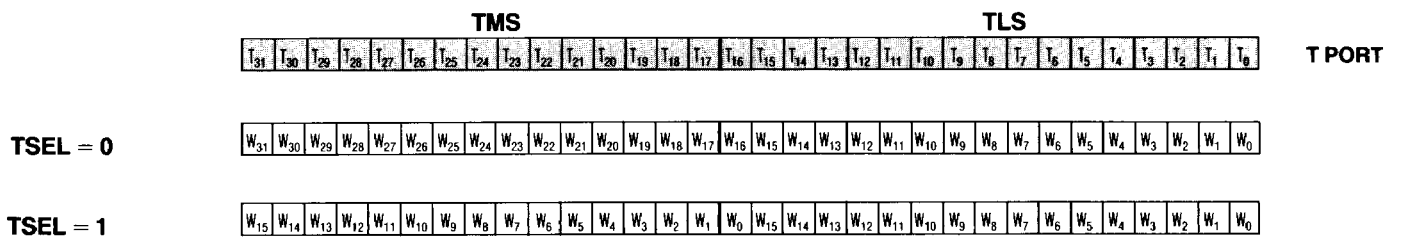
$\overline{Z}$ = **NOR** Z_{15}-Z_{31} when **RND** = 1, FA = 0

FIGURE 3. Result W Formats, Overflow Status Flag and Format Adjust Operation



V = Z_{31} **XOR** Z_{30}

FIGURE 4. Output Multiplexer



FUNCTIONAL DESCRIPTION

Format Adjust.

The Format Adjust instruction provides the system designer with a choice of output data format and status flags. This is desirable with the fractional two's complement input data format shown in figure 1.

When FA = 1 the full 32-bit intermediate result Z is available including the most significant sign and unity bits as shown in Figure 3. All possible products can be represented including $-1.0 \times -1.0 = +1.0$ without overflow. The binary point in this result does not align with the binary point in the input operands. Thus the numeric weighting of data bits within a system is not uniform. A further effect exists when only the most significant 16-bits are retained; one whole bit (the unity bit) is used to indicate the presence of one unique set of operands (-1.0 and -1.0) rather than adding an additional bit of resolution to all other results.

Setting FA = 0 provides the left shift and higher order truncation of the result Z so that the binary point of the result W aligns with that of the input operands. All data bits now have a uniform weighting. The unique $+1.0$ product is sensed and sets the OVFL flag latch so this condition does not go undetected. A zero is shifted into the least significant bit position to maintain a correct full 32-bit result. Note in comparison to when FA = 1, an additional bit of lower order resolution (2**-15) exists when only the most significant 16-bits are output.

Load.

The Load instruction concentrates the X and Y input operands into the intermediate result Z rather than multiply them. X becomes the most significant portion of Z and Y the least as shown in Figure 2. XM determines the sign mode for the complete 32-bit result. Condition codes ZERO, OVFL and NEG are set as though the concatenated operands are a full 32-bit product. For a two's complement number the format-adjust operation is the same. Round reduces the loaded 32-bit input to the rounded most significant 16-bit portion. This instruction allows any 32-bit number, including previously generated products, to be rounded, tested for zero and sign, and to have fractional binary points aligned while testing for overflow. In addition it is valuable for system testing by providing a direct path through the multiplier and greater access to the individual operations and latches within the multiplier.

Round.

The Round instruction causes a one to be added to what will be the most significant bit of the least significant 16-bits of the result W. The most significant 16-bits of result W are then correctly rounded to the nearest 16-bit value.

SPECIFICATIONS

Absolute Maximum Ratings

Permanent damage may occur if any one absolute maximum rating is exceeded. Functional operation is not implied and device reliability may be impaired by exposure to higher than recommended voltages for extended periods of time.

Parameter	Symbol	Value	Units
Supply Voltage (GND = 0)	V_{cc}	-0.5 to $+7.0$	V_{dc}
Input Voltage (GND = 0)	V_{in}	-0.5 to V_{cc} $+0.5$	V_{dc}
Output Source Current			
Continuous	I_o	30	mA_{dc}
Surge	I_o	100	mA_{dc}
Storage Temperature	T_{st}	-55 to 150	°C
Operating Junction Temperature	T_j	165	°C

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Recommended Operating and Test Conditions

Parameter	Symbol	Value			Units
		Min	Nom	Max	
Supply Voltage (GND = 0)	V_{cc}	4.75	5.00	5.25	V_{dc}
Ambient Temperature	T_a*	0		70	°C
Input Voltage High	V_{ih}	2.0			V_{dc}
Input Voltage Low	V_{il}			0.8	V_{dc}
Output Current High	I_{oh}			−0.4	mA_{dc}
Output Current Low	I_{ol}			4.0	mA_{dc}
Input Setup Time	t_s	4			ns
Input Hold Time	t_h	3			ns
Clock and Latch Enable Pulse Duration	t_c	5.5			ns

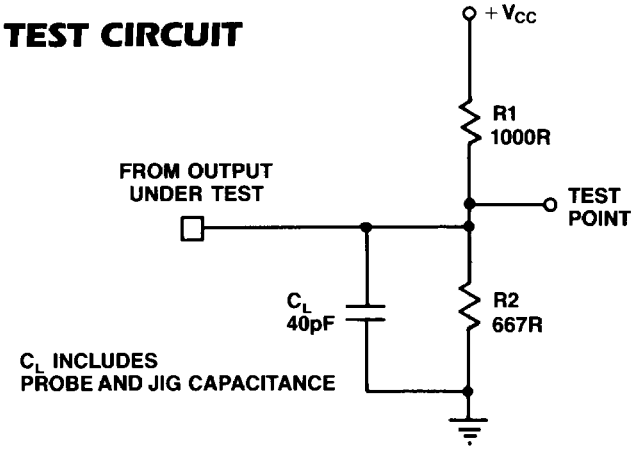
*500 Linear Feet per Minute Ambient Air Flow

Electrical Characteristics

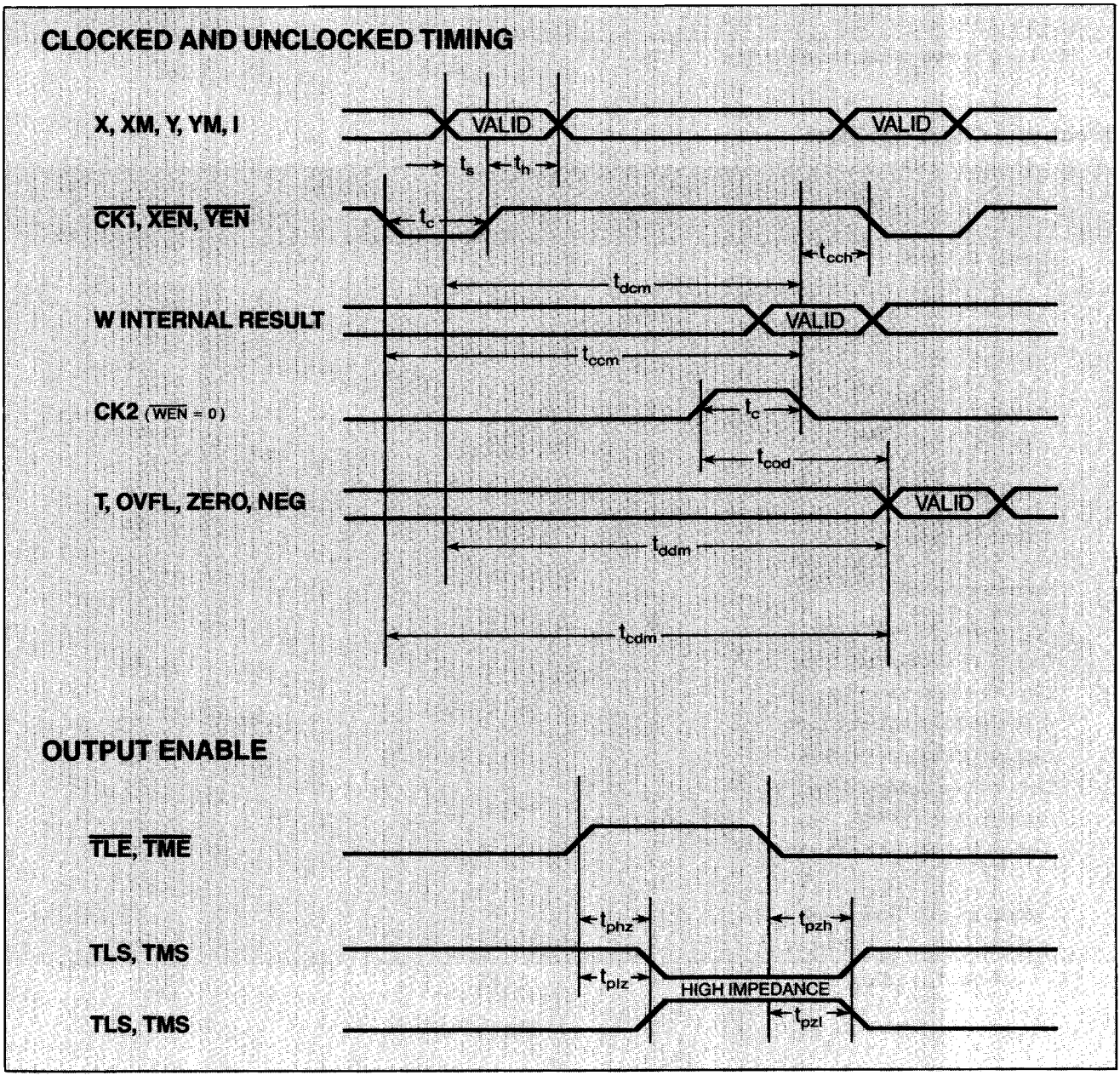
Parameter	Symbol	Value			Units
		Min	Nom*	Max	
Supply Current (V_{cc} = Max)	I_{cc}		440	800	mA_{dc}
Input Current High (V_{cc} = Max, V_{ih} = 2.4)	I_{ih}			0.2	mA_{dc}
Input Current Low (V_{cc} = Max, V_{il} = 0.4)	I_{il}			−0.2	mA_{dc}
Output Voltage High (V_{cc} = Min, I_{oh} = Max)	V_{oh}	2.4			V_{dc}
Output Voltage Low (V_{cc} = Min, I_{ol} = Max)	V_{ol}			0.4	V_{dc}
High Impedance Output Current (V_{cc} = Max, V_o = 2.4)	I_{ozh}			40	μA_{dc}
High Impedance Output Current (V_{cc} = Max, V_o = 0.4)	I_{ozl}			−40	μA_{dc}
Data to Clock Multiply Time	t_{dcm}			14	ns
Clock to Clock Hold Time	t_{cch}		−1.5		ns
Clock to Clock Multiply Time	t_{ccm}			19	ns
Clocked Output Delay Time	t_{cod}			12	ns
Data to Data Multiply Time	t_{ddm}			25	ns
Clock to Data Multiply Time	t_{cdm}			26	ns
Output Disable Time H→Z	t_{phz}			7	ns
L→Z	t_{plz}			7	ns
Output Enable Time Z→H	t_{pzh}			12	ns
Z→L	t_{pzl}			11	ns

*V_{cc} = 5.0 volts, T_a = 25°C

LOAD TEST CIRCUIT



TIMING DIAGRAMS



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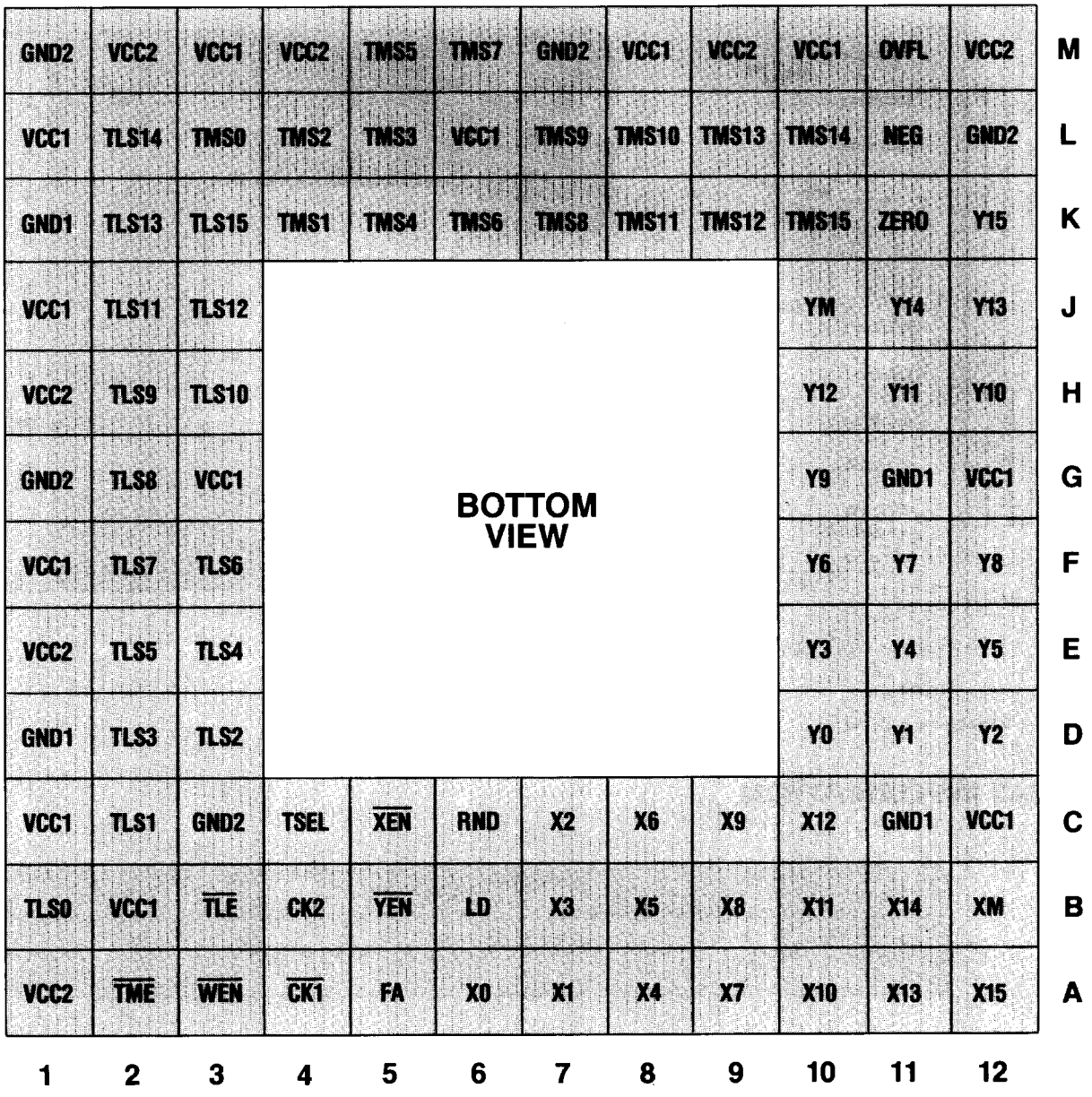
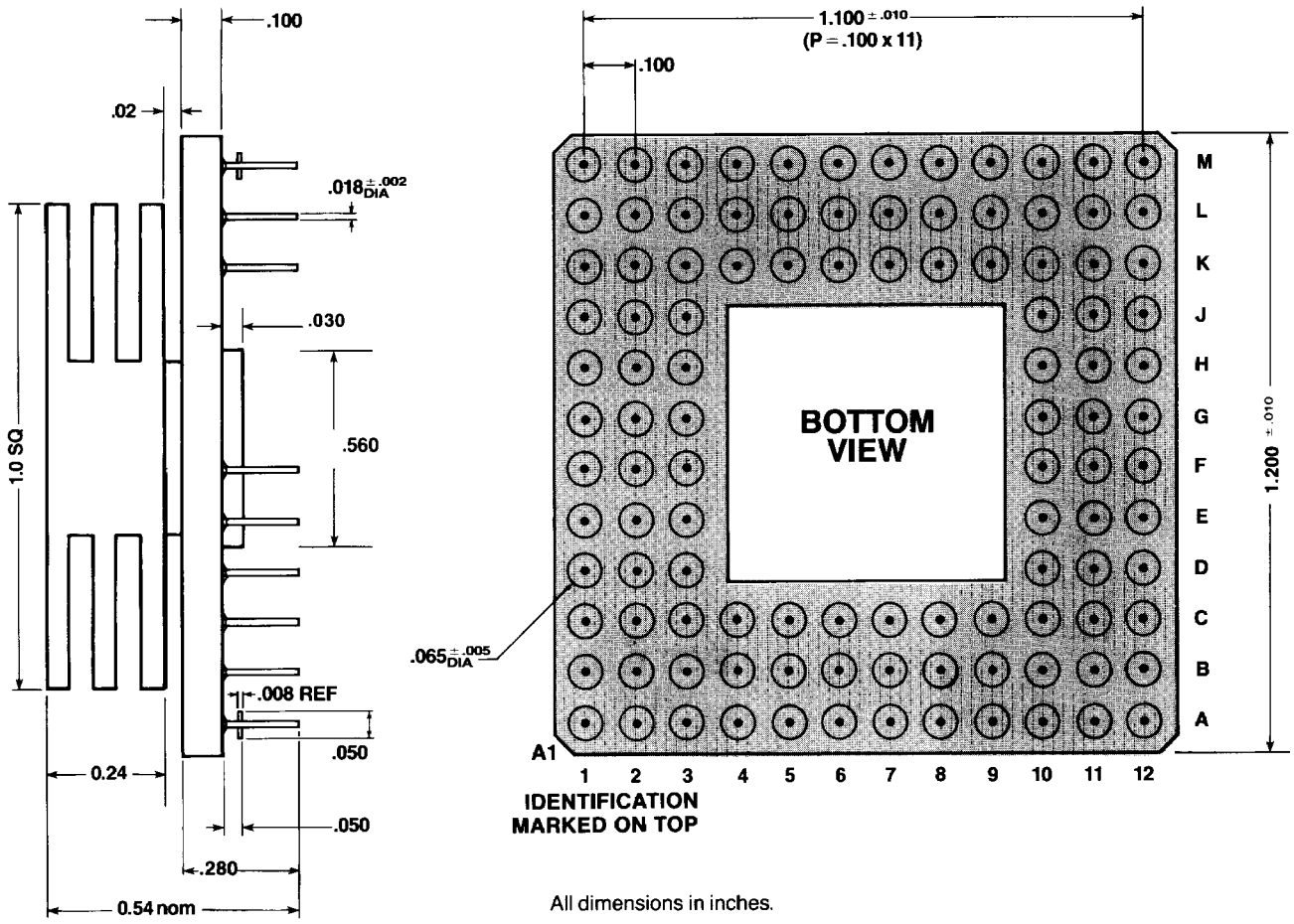
■ PINOUT



NOTES:

1) All VCC1 pins must be tied to all VCC2 pins.
2) All GND1 pins must be tied to all GND2 pins.

PACKAGING DRAWING AND DIMENSIONS



All dimensions in inches.

ORDERING INFORMATION

Order Number	Package Type	Temperature Range
B2018	108 Pin Pin Grid Array	0 - 70°C

Bipolar Integrated Technology, Inc.

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