

KS54AHCT 299
KS74AHCT
8-Bit Universal Shift/Storage Registers
with 3-State Outputs

T-46-09-05

FEATURES

- Multiplexed I/O ports provides improved bit density
- Four modes of operation: hold (store), shift right, shift left, and load data
- Operates with outputs enabled or at high impedance
- Can be cascaded for N-bit word lengths
- Direct overriding clear
- Application:
 - Stacked or push-down registers, buffer storage, and accumulator registers
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with drive current ($I_{OL} = 24 \text{ mA}$ @ $V_{OL} = 0.5\text{V}$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
 - KS74AHCT: -40°C to $+85^{\circ}\text{C}$
 - KS54AHCT: -55°C to $+125^{\circ}\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

DESCRIPTION

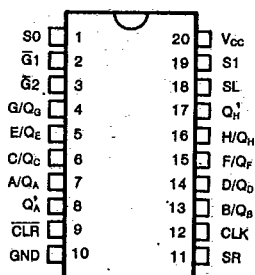
These eight-bit universal registers feature multiplexed I/O ports to achieve full eight-bit data handling. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines S0 and S1 high. This places the three-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs asynchronously when $\overline{\text{CLR}}$ is low. Pulling either of the output controls, $\overline{\text{G}}1$ or $\overline{\text{G}}2$, high disables the outputs but this has no effect on clearing, shifting, or storage of data.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATION

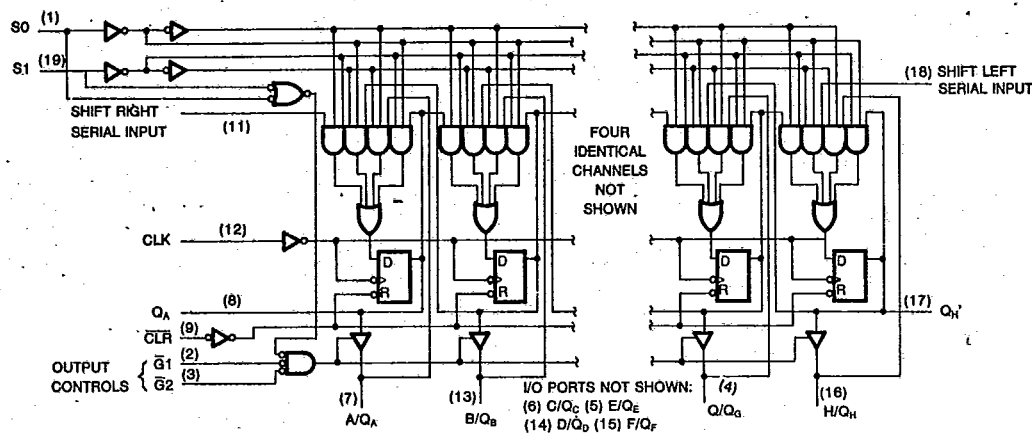


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LOGIC DIAGRAM



FUNCTION TABLE

Mode	Inputs						I/O Ports								Outputs	
	CLR	S1	S0	Output Control G1 G2	CLK	SL SR	A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA'	QH'
Clear	L	X	L	L L	X	X X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L L	X	X X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X X	X	X X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L L	X	X X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
	H	X	X	L L	L	X X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
Shift Right	H	L	H	L L	↑	X H	H	QA _n	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	H	Q _{Gn}
	H	L	H	L L	↑	X L	L	QA _n	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	L	Q _{Gn}
Shift Left	H	H	L	L L	↑	H X	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	QH _n	H	QB _n	H
	H	H	L	L L	↑	L X	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	QH _n	L	QB _n	L
Load	H	H	H	X X	↑	X X	a	b	c	d	e	f	g	h	a	h

When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

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Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , -0.5V, to +7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 70 mA
 Continuous Current Through
 V_{CC} or GND pins ± 250 mA
 Storage Temperature Range, T_{stg} -65°C to $+150^\circ\text{C}$
 Power Dissipation Per Package, P_d † 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
 Plastic Package (N): $-12\text{mW}/^\circ\text{C}$ from 65°C to 85°C
 Ceramic Package (J): $-12\text{mW}/^\circ\text{C}$ from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN} , V_{OUT} ... 0V to V_{CC}
 Operating Temperature Range
 KS74AHCT: -40°C to $+85^\circ\text{C}$
 KS54AHCT: -55°C to $+125^\circ\text{C}$
 Input Rise & Fall Times, t_r , t_f Max 500 ns
 * Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$		KS54AHCT $T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
			Typ	Guaranteed Limits					
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	2.0		V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	0.8		V
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O = -20\mu\text{A}$ Q'_A and Q'_H outputs: $I_O = -4\text{mA}$ Q_A thru Q_H outputs: $I_O = -6\text{mA}$	V_{CC}	$V_{CC} - 0.1$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	$V_{CC} - 0.1$		V
			4.2	3.98	3.84	3.7			
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O = 20\mu\text{A}$ Q'_A and Q'_H outputs: $I_O = 4\text{mA}$ $I_O = 8\text{mA}$ Q_A thru Q_H outputs: $I_O = 12\text{mA}$ $I_O = 24\text{mA}$	0	0.1	0.1	0.1	0.1		V
				0.26 0.39	0.33 0.5	0.4 0.4			
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		± 0.1	± 1.0	± 1.0	± 1.0		μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable = V_{IN} $V_{OUT}=V_{CC}$ or GND		± 0.5	± 5.0	± 5.0	± 10.0		μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	80.0	160.0		μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I = 2.4V$ other inputs: at V_{CC} or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	2.9	3.0		mA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2$ ns), AHCT299

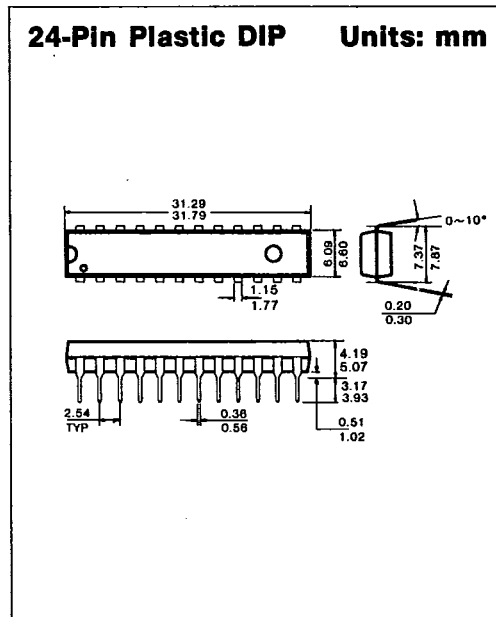
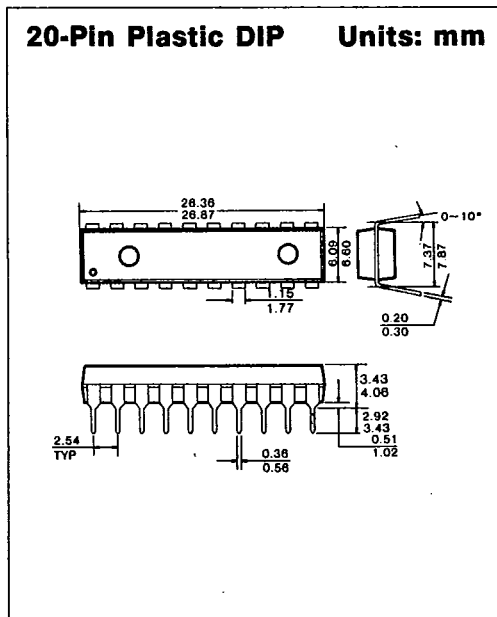
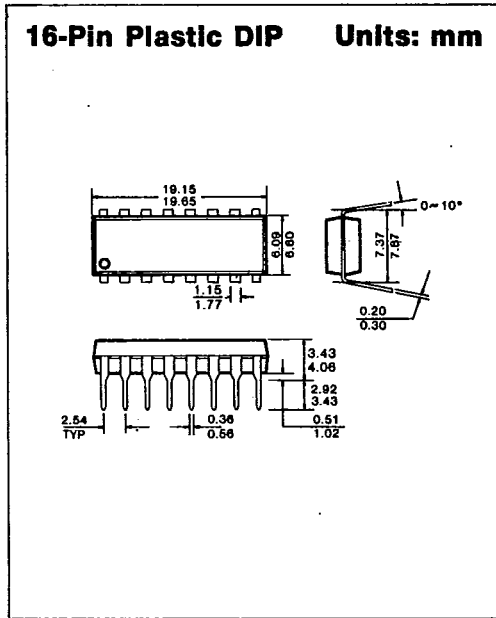
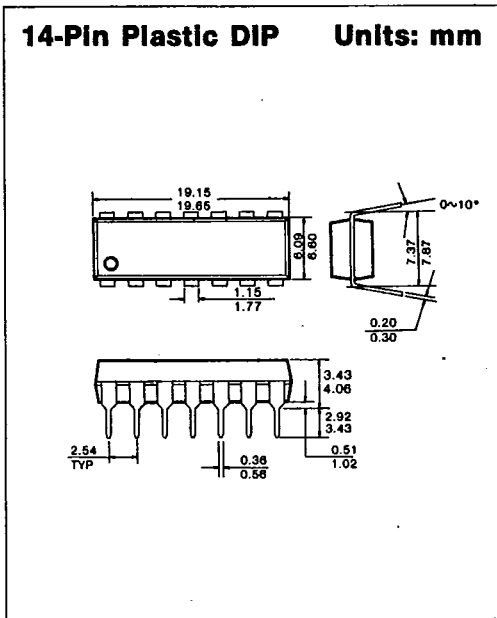
Characteristic	Symbol	Conditions†	T _a = 25°C V _{CC} = 5.0V		KS74AHCT T _a = -40°C to +85°C V _{CC} = 5.0V ± 10%		KS54AHCT T _a = -55°C to +125°C V _{CC} = 5.0V ± 10%		Unit
			Typ	Min	Max	Min	Max		
Maximum Clock Frequency	f _{max}		50	30			25		MHz
Propagation Delay, CLK to Q _A or Q _H	t _{PLH}	C _L = 50pF	10				17		ns
	t _{PHL}		10				17		
Propagation Delay, CLR to Q _A or Q _H	t _{PHL}		13				22		ns
Propagation Delay, CLK to Q _A thru Q _H	t _{PLH}	C _L = 50pF	10				16		ns
	t _{PHL}	C _L = 150pF	13				21		
Propagation Delay, CLR to Q _A thru Q _H	t _{PHL}	C _L = 50pF	10				16		ns
		C _L = 150pF	13				21		
Propagation Delay, CLR to Q _A thru Q _H	t _{PHL}	C _L = 50pF	13				22		ns
		C _L = 150pF	16				27		
Output Enable Time, G ₁ , G ₂ , to Q _A thru Q _H	t _{PZH}	R _L = 1kΩ	C _L = 50pF	11			19		ns
	t _{PZL}		C _L = 150pF	14			24		
Output Disable Time, G ₁ , G ₂ to Q _A thru Q _H	t _{PHZ}	R _L = 1kΩ C _L = 50pF		11			18		ns
	t _{PLZ}			11			18		
Pulse Width	CLK High or Low	t _w		9	15			20	ns
	CLR Low			5	8			10	
Setup time before CLK†	S ₀ and S ₁	t _{su}		12	20			10	ns
	High-Level Inputs			8	13			15	
	Low-Level Inputs			8	13			15	
	CLR Inactive			8	13			15	
Hold Time after CLK†	S ₀ and S ₁	t _h		0	0			0	ns
	All Inputs			0					
Input Capacitance	C _{IN}		5					pF	
Output Capacitance	C _{OUT}	Output Disabled	10						pF
Power Dissipation Capacitance*	C _{PD}								pF

* C_{PD} determines the no-load dynamic power dissipation: P_D = C_{PD} V_{CC}² f + I_{CC} V_{CC}.
† For AC switching test circuits and timing waveforms see section 2.

PACKAGE DIMENSIONS

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1. PLASTIC PACKAGES

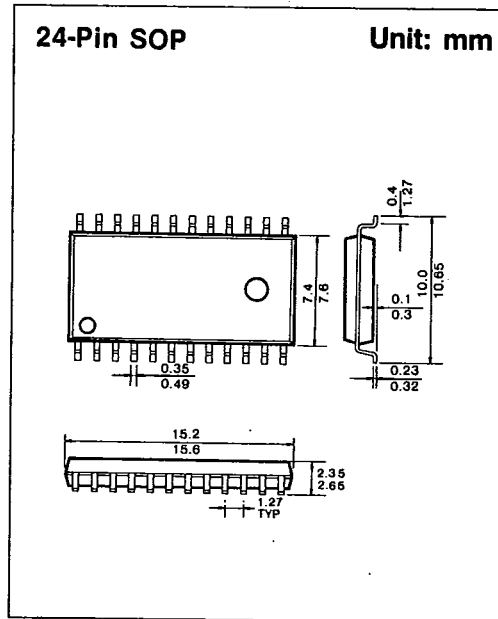
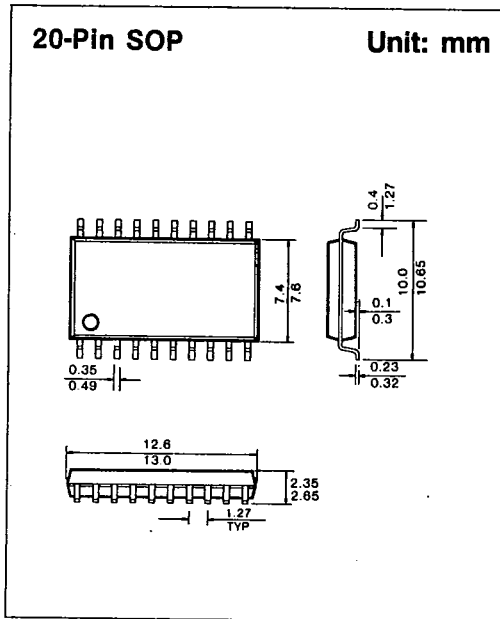
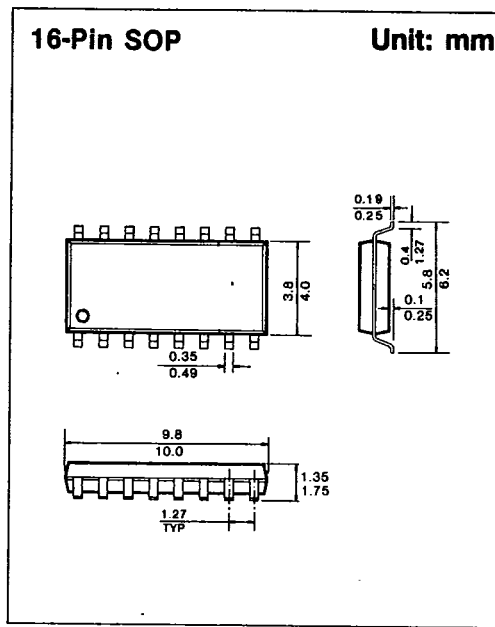
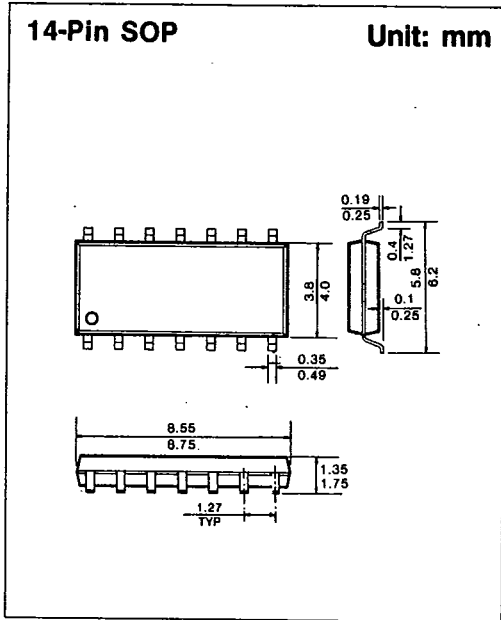


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PACKAGE DIMENSIONS

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2. CERAMIC PACKAGES

14-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	8.10	7.49
E ₁	7.82	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	8.10	7.49
E ₁	7.82	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	25.78	26.33
E	8.10	8.60
E ₁	7.77	7.95
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	31.50	32.84
E	7.24	7.75
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.776
S	1.85	1.93

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