



PAC25140, PAC25140N, PAC25141N Data Sheet

10S-20S or 10S-16S Intelligent BMS with Integrated MCU and Cell Balancing

Product Overview

The Qorvo® PAC25140 is an Intelligent Battery Monitoring System (BMS) that can monitor 10-series to 20-series Li-Ion, Li-Polymer and LiFePO4 battery packs. PAC25140N is a package spin with an offset exposed pad, supporting 10s to 20s, and PAC25141N is pin compatible to PAC25140N with a reduction on the cell count 10s to 16s.

The PAC25140 integrates a FLASH-programmable MCU, Power Management, Current/Voltage/Temperature Sense and drive circuits for charge/discharge FETs and protection fuses. It can communicate using UART, SPI I2C/SMBus or CAN 2.0B serial interfaces. The PAC25140 provides access to multiple analog and digital peripherals required to manage today's high cell count battery packs.

The PAC25140 contains an Arm® Cortex®-M4F running at 150 MHz with 128kB of FLASH and 32KB of SRAM. It has access to several different analog and digital peripherals that are intended to be used for the fuel gauging algorithm and system telemetry reporting.

The PAC25140 provides a low power hibernate mode of less than 3µA, enabling long storage time with wakeup from push button, timer, or charger detection.

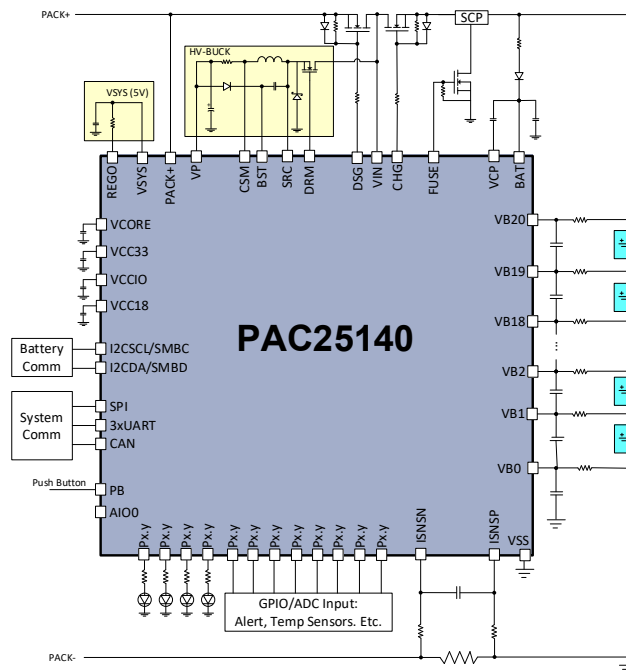
The device integrates a single-supply 145V-buck DC/DC controller reducing thermal issues and generating a system rail. The system rail supports a 5V-LDO output up to 225mA, a 3.3V-LDO output up to 90mA for running additional system peripherals. An integrated charge pump supports the charge and discharge FET drivers. Internal FETs for each cell input for cell balancing current of 50mA.

The device also integrates a programmable-gain differential amplifier and 16-bit Sigma-Delta ADC for wide range of current sensing as well as a 16-bit Sigma-Delta ADC for cell voltage sensing and an analog MUX connected to a 12-bit SAR ADC for safety checks on internal nodes and additional voltage and temperature sense inputs to ensure safe system operation.

The PAC25140 is packaged in an 10x10mm, 68-pin QFN package for compact, high cell count battery-monitoring applications. PAC25140N and PAC25141N are a package spin using a smaller, offset exposed pad and a minor pin out change from PAC25140.

APPLICATIONS

- Battery Powered Garden Tools, Lawn mowers
- Backup Power Supplies
- Renewable Energy Storage
- EBike Battery Packs, EMobility
- Warehouse Forklifts and Robots



www.qorvo.com

No portion of this document may be reproduced or reused in any form without Qorvo's prior written consent



PAC25140, PAC25140N, PAC25141N Data Sheet

10S-20S or 10S-16S Intelligent BMS with Integrated MCU and Cell Balancing

Key Features

MCU

- 150MHz Arm® Cortex®-M4F
 - 128kB FLASH
 - 32kB SRAM with SECDED ECC
 - 1kB INFO FLASH for general use
 - Floating Point Unit
 - 32-bit hardware divider
 - Single-cycle 32-bit x 32-bit hardware multiplier
 - DSP Instructions and Saturation Arithmetic Support
 - 32 interrupts, 8 priority levels
 - 8-region Memory Protection Unit (MPU)
 - Wake-up Interrupt Controller (WIC) allowing power-saving sleep modes
- Debug
 - Single Wire Debug I/F (SWD)
 - JTAG programming interface
 - Embedded Trace Macrocell (ETM) for in-system debugging at real-time without breakpoints
- Sleep/Deep Sleep & Clock-gating for low-power operation

MCU ADC

- 12-bit resolution
- 2.5MSPS
- Programmable Dynamic Triggering and Sampling Engine (DTSE)

Timing Generators

- Four 16-bit PWM timers with up to 32 PWM/CC blocks
- 24-bit SysTick count-down timer
- 2 x 24-bit General-purpose count-down timers with interrupt
- 2 x Windowed Watch-dog Timer (WWDT) running off independent clock
- Real-time Clock (RTC)
- Wake-up timer for ultra-low power hibernate mode

IO

- 3.3V Digital I/O or Analog Input for ADC
- 24 general-purpose IO with flexible interrupt controller
- Configurable weak pull-up or pull-down
- Configurable drive-strength (6mA to 25mA)
- Flexible peripheral MUX allowing each IO pin to be configured with one of up to 8 peripheral functions

Communication Peripherals

- 3 x USART (Either SPI or UART)
 - SPI Master/Slave up to 25 MHz
 - UART up to 1Mbps
- I2C/SMBus Master/Slave
- CAN 2.0B Controller

Miscellaneous

- 4-Level User-Configurable Code Protection
- CRC Engine
- 96-bit Unique ID

Power Manager

- Up to 145V supply input Buck DC/DC Controller
 - OC, OV and UV protection
- High-Voltage Charge Pump
- 5V/250mA system regulator
- Integrated LDOs for analog, IO, and core supplies
- Power and temperature monitor, warning, and fault detection
- Low-Power Operation
 - 3µA total hibernate mode
 - Push Button, PACK+/Charger Detect, and Timer wakeup modes

Configurable Analog Front-End (CAFE™)

- Programmable-Gain Differential amplifier and 16-bit Sigma-Delta ADC for battery pack current sense
- 16-bit Sigma-Delta ADC for voltage sense
- Integrated ADC references
- Programmable over-current shutdown
- Power supply monitoring via ADC
- Low-speed independent clock source

Application Specific Power Drivers (ASPD™)

- Integrated high-side gate drivers for external CHG and DSG FETs
- Integrated low-side gate driver for pack FUSE blow FET

Integrated Cell Balancing

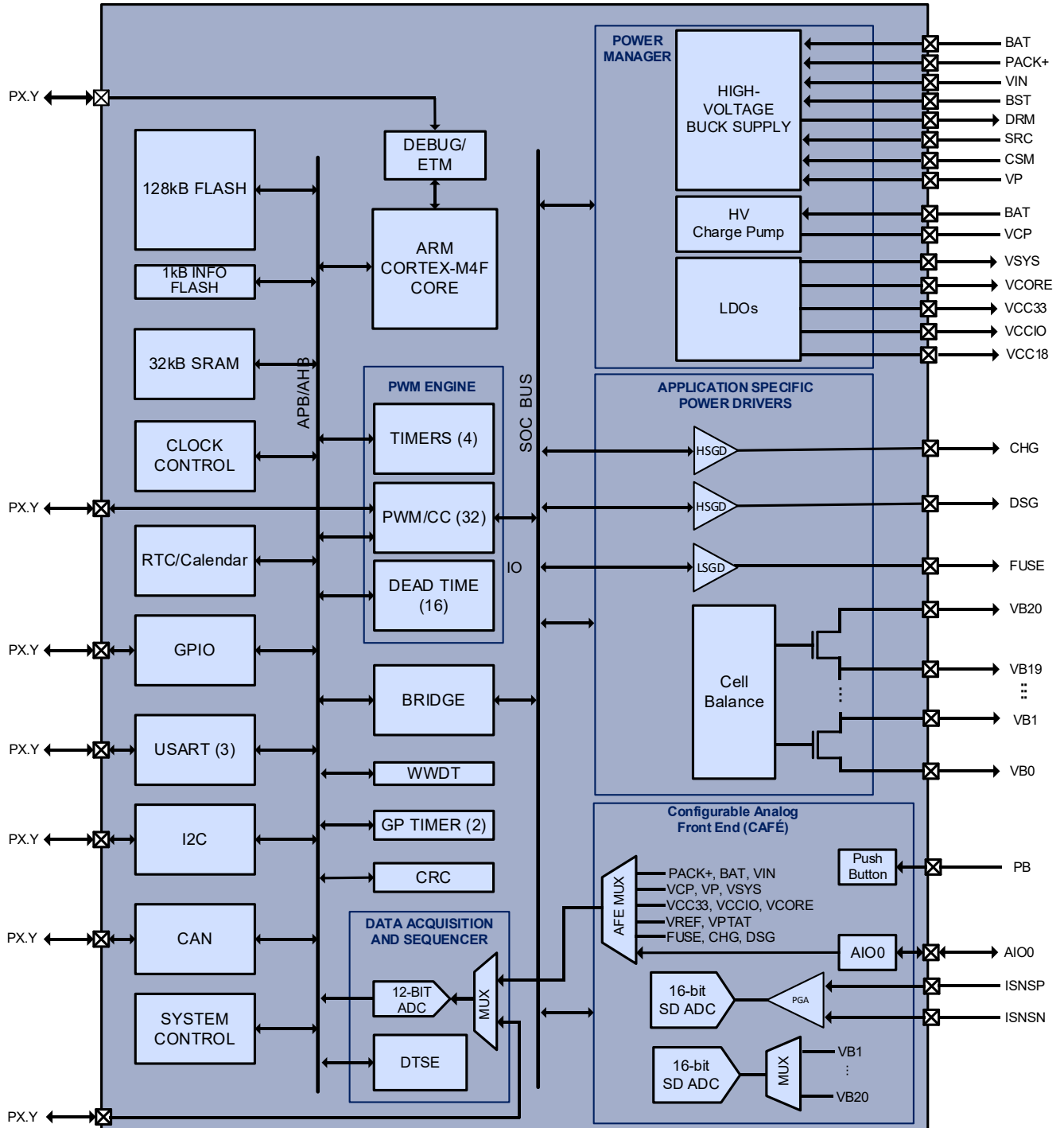
- Cell balancing for up to 20 cells

Packaging

- QFN 10x10mm 68-pin package, 0.5mm pitch
- Exposed pad for thermal management
- T_A = -40°C to 105°C

Functional Block Diagram

Figure 1 Architectural Block Diagram





PAC2514x Data Sheet

Ordering Information

| Orderable Part Number | UNIT QUANTITY | MCU | FLASH | SRAM | CELL COUNT | GPIO | PACKAGE |
|-----------------------|---------------------|-----------------------|-------|------|--------------------------------------|------|---------------------------------|
| PAC25140SR | 100-unit short reel | 150MHz ARM Cortex M4F | 128kB | 32kB | 10 to 20 | 24 | QFN 10x10mm 68-pin EP 5.6x5.6mm |
| PAC25140-T | 3000-unit reel | | | | | | |
| PAC25140NSR | 100-unit short reel | | | | QFN 10x10mm 68-pin Offset EP 4.5x5mm | | |
| PAC25140N-T | 3000-unit reel | | | | | | |
| PAC25141NSR | 100-unit short reel | | | | | | |
| PAC25141N-T | 3000-unit reel | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |
| | | | | | | | |



PAC2514x Data Sheet

Table of Contents

| | |
|--|----|
| Product Overview | 1 |
| APPLICATIONS | 1 |
| Key Features | 2 |
| Functional Block Diagram | 3 |
| Ordering Information | 4 |
| Table of Contents | 5 |
| Table of Figures | 10 |
| Table of Tables | 11 |
| Absolute Maximum Ratings | 12 |
| Recommended Operating Conditions | 13 |
| Power Manager | 13 |
| Features | 13 |
| Block Diagram | 13 |
| Functional Description | 14 |
| High-Voltage Buck (HV-BUCK) | 14 |
| High-Voltage Charge Pump (HVCP) | 14 |
| HV-BUCK Restart Handling | 14 |
| Linear Regulators | 15 |
| Power Manager Circuit Connections | 15 |
| HV-BUCK and LDO Power-up Sequence | 15 |
| HVCP Power-up Sequence | 17 |
| Hibernate Mode | 17 |
| Power Monitoring | 17 |
| Temperature Monitoring | 17 |
| Voltage References | 17 |
| Electrical Characteristics | 18 |
| HV-BUCK Electrical Characteristics | 18 |
| HVCP Electrical Characteristics | 19 |
| Linear Regulators Electrical Characteristics | 19 |
| Power Monitor Electrical Characteristics | 20 |
| Configurable Analog Front-End (CAFE) | 21 |
| Features | 21 |
| Block Diagram | 22 |
| Functional Description | 22 |
| Current Sensing | 23 |
| Over-Current Protection | 23 |
| Voltage Sensing | 23 |



PAC2514x Data Sheet

| | |
|--|----|
| AFE MUX | 24 |
| Temperature Monitoring and Protection | 24 |
| PACK+ Charger Detection | 25 |
| PACK+ Load/Short Detection | 25 |
| Push-Button (PB) Input | 26 |
| AIO0 – Analog Input Output | 27 |
| Electrical Characteristics | 28 |
| Differential Amplifier (DA) Electrical Characteristics | 28 |
| Current Sense ADC Electrical Characteristics | 28 |
| Short Circuit Protection Comparator (SCP-COMP) Electrical Characteristics | 29 |
| Over-Current Discharge Protection Comparator (OCD-COMP) Electrical Characteristics | 29 |
| Over-Current Charge Protection Comparator (OCC-COMP) Electrical Characteristics | 29 |
| Cell Voltage ADC Electrical Characteristics | 30 |
| (1) After ADC Calibration | 30 |
| TA = -40°C to 105°C unless otherwise specified | 30 |
| Push-Button Electrical Characteristics | 31 |
| Temperature Protection Electrical Characteristics | 31 |
| 12-bit ADC With Dynamic Triggering and Sampling Engine (DTSE) | 32 |
| Block Diagram | 32 |
| Functional Description | 32 |
| ADC | 32 |
| ADC Conversion Timing | 32 |
| Dynamic Triggering and Sample Engine | 34 |
| EMUX Control | 34 |
| Electrical Characteristics | 35 |
| Application Specific Power Drivers (ASPD) | 36 |
| Gate Drivers | 36 |
| Features | 36 |
| Block Diagram | 36 |
| Functional Description | 36 |
| Electrical Characteristics | 37 |
| Integrated Cell Balancing | 38 |
| Features | 38 |
| Electrical Characteristics | 39 |
| Battery AFE Windowed Watchdog Timer (WWDT) | 40 |
| Wake-up Timer | 40 |
| MCU Memory System | 41 |



PAC2514x Data Sheet

| | |
|---|----|
| Features | 41 |
| Block Diagram | 41 |
| Functional Description | 41 |
| Program FLASH | 42 |
| INFO FLASH | 42 |
| SRAM | 42 |
| Code Protection | 43 |
| Electrical Characteristics | 44 |
| MCU Clock Control System (CCS) | 45 |
| Features | 45 |
| Block Diagram | 45 |
| Functional Description | 46 |
| Clock Sources | 46 |
| Ring Oscillator | 46 |
| Reference Clock | 46 |
| External Clock Input | 46 |
| PLL | 46 |
| Clock Tree | 46 |
| FRCLK | 46 |
| SCLK | 47 |
| PCLK | 47 |
| ACLK | 47 |
| HCLK | 47 |
| Electrical Characteristics | 48 |
| MCU Core Arm® CORTEX®-M4F | 49 |
| Features | 49 |
| Block Diagram | 49 |
| Functional Description | 49 |
| Application Typical Current Consumption | 51 |
| Electrical Characteristics | 52 |
| MCU IO Controller | 53 |
| Features | 53 |
| System Block Diagram | 53 |
| Functional Description | 54 |
| IO Controller | 54 |
| GPIO Current Injection | 54 |
| Peripheral MUX | 55 |



PAC2514x Data Sheet

| | |
|---|----|
| Electrical Characteristics | 56 |
| MCU Communication Interfaces | 57 |
| Features | 57 |
| System Block Diagram | 57 |
| Functional Description | 57 |
| I ² C Controller | 58 |
| USART | 58 |
| USART SPI Mode | 58 |
| USART UART Mode | 58 |
| CAN | 59 |
| Dynamic Characteristics | 60 |
| Serial Interface | 60 |
| I2C Dynamic Characteristics | 61 |
| I2C Timing Diagram | 62 |
| MCU PWM Timers | 63 |
| Features | 63 |
| PWM Timers System Block Diagram | 64 |
| Functional Description | 65 |
| MCU General Purpose Timers | 66 |
| Features | 66 |
| System Block Diagram | 66 |
| Functional Description | 67 |
| Real-time Clock with Calendar (RTC) | 67 |
| MCU Windowed Watchdog Timer (WWDT) | 67 |
| GP Timer (GPT) | 67 |
| Cyclic Redundancy Check (CRC) | 68 |
| Features | 68 |
| System Block Diagram | 68 |
| Functional Description | 68 |
| Application Block Diagrams | 69 |
| PAC25140 Pin Configuration and Description | 72 |
| PAC25140 Mechanical Information | 75 |
| PAC25140 Package Marking | 76 |
| PAC25140N Pin Configuration and Description | 77 |
| PAC25140N Mechanical Information | 80 |
| PAC25140N Package Marking | 81 |
| PAC25141N Pin Configuration and Description | 82 |
| PAC25141N Mechanical Information | 85 |
| PAC25141N Package Marking | 86 |



PAC2514x Data Sheet

| | |
|----------------------|----|
| Handling Precautions | 87 |
| Solderability | 87 |
| REVISION HISTORY | 88 |
| Contact Information | 88 |
| Important Notice | 88 |

Table of Figures

| | |
|--|----|
| Figure 1 Architectural Block Diagram..... | 3 |
| Figure 2 Power Manager Block Diagram | 13 |
| Figure 3 Power Manager Circuit Connections..... | 15 |
| Figure 4 HV-BUCK and LDO Power-up Sequence | 15 |
| Figure 5 HVCP Power-up Sequence..... | 17 |
| Figure 6 CAFE Block Diagram | 22 |
| Figure 7 PACK+ Charger Detection | 25 |
| Figure 8 PACK+ Load/Short Detection | 25 |
| Figure 9 Push-Button (PB) Input..... | 26 |
| Figure 10 AIO0 Analog Input Output..... | 27 |
| Figure 11 12-bit MCU ADC Block Diagram | 32 |
| Figure 12 ADC Conversion Timing Diagram (standard)..... | 33 |
| Figure 13 ADC Conversion Timing Diagram (enhanced)..... | 33 |
| Figure 14 ASPD Block Diagram..... | 36 |
| Figure 15 High Side Gate Drivers | 37 |
| Figure 16 Cell Balancing | 38 |
| Figure 17 WWDT System Block Diagrams | 40 |
| Figure 18 WWDT Operation..... | 40 |
| Figure 19 Memory System Block Diagram..... | 41 |
| Figure 20 CCS Block Diagram | 45 |
| Figure 21 Arm® Cortex®-M4F Microcontroller Core Block Diagram..... | 49 |
| Figure 22 IO Controller System Block Diagram..... | 53 |
| Figure 23 Serial Interfaces System Block Diagram | 57 |
| Figure 24 I2C Timing Diagram | 62 |
| Figure 25 PWM Timers System Block Diagram | 64 |
| Figure 26 General-Purpose Timers System Block Diagrams..... | 66 |
| Figure 27 CRC System Block Diagram | 68 |
| Figure 28 Application Block Diagram for 20s | 69 |
| Figure 29 Unused Cell connection for 16s | 70 |
| Figure 30 PAC25140 Pin Diagram – Top View | 72 |
| Figure 31 PAC25140N Pin Diagram – Top View..... | 77 |
| Figure 32 PAC25141N Pin Diagram – Top View..... | 82 |



PAC2514x Data Sheet

Table of Tables

| | |
|---|----|
| Table 1 HV-BUCK Electrical Characteristics | 18 |
| Table 2 HVCP Electrical Characteristics | 19 |
| Table 3 Linear Regulators Electrical Characteristics | 19 |
| Table 4 Power Monitor Electrical Characteristics | 20 |
| Table 5 DA Electrical Characteristics | 28 |
| Table 6 Current Sense ADC Electrical Characteristics | 28 |
| Table 7 SCP-COMP Electrical Characteristics | 29 |
| Table 8 OCD-COMP Electrical Characteristics | 29 |
| Table 9 OCC-COMP Electrical Characteristics | 29 |
| Table 10 Cell Voltage ADC Electrical Characteristics | 30 |
| Table 11 Cell Voltage Measurement Accuracy Electrical Characteristics | 30 |
| Table 12 Push-Button Electrical Characteristics | 31 |
| Table 13 Temperature Protection Electrical Characteristics | 31 |
| Table 14 ADC and DTSE Electrical Characteristics | 35 |
| Table 15 ASPD Electrical Characteristics | 37 |
| Table 16 Cell Balancing Electrical Characteristics | 39 |
| Table 17 Code Protection Level Description | 43 |
| Table 18 Memory System Electrical Characteristics | 44 |
| Table 19 Clock Control System Electrical Characteristics | 48 |
| Table 20 PAC25140 Application Typical Current Consumption | 51 |
| Table 21 Microcontroller Electrical Characteristics | 52 |
| Table 22 Peripheral MUX settings | 55 |
| Table 23 IO Controller Electrical Characteristics | 56 |
| Table 24 Serial Interface Dynamic Characteristics | 60 |
| Table 25 I2C Dynamic Characteristics | 61 |
| Table 26 Thermal Characteristics | 71 |
| Table 27 PAC25140 Pin Descriptions | 73 |
| Table 28 PAC25140N Pin Descriptions | 78 |
| Table 29 PAC25140N Pin Descriptions | 83 |



PAC2514x Data Sheet

Absolute Maximum Ratings

| Symbol | Value | Unit |
|--|---------------------|------|
| Power Manager | | |
| VCP to BAT | -0.3 to 14 | V |
| VIN, BAT, PACK+ to VSS | -0.3 to 145 | V |
| BST to VSS | -0.3 to 145 | V |
| BST to SRC | -0.3 to 20 | V |
| SRC to VSS | -5 to VIN + 15 | V |
| DRM to SRC | -0.3 to 20 | V |
| VP to VSS | -0.3 to 14 | V |
| CSM to VP | -0.3 to 0.3 | V |
| VSYS to VSS | -0.3 to 6 | V |
| REGO to VSS | -0.3 to VP + 0.3 | V |
| VCC33, VCCIO to VSS | -0.3 to 4.1 | V |
| VCORE to VSS | -0.3 to 1.44 | V |
| VCC18 to VSS | -0.3 to 2.5 | V |
| Signal Manager | | |
| ISNSP, ISNSN to VSS | -0.3 to +0.3 | V |
| Cell Balancing | | |
| VB[n] to VSS | (n+1) * 6.9 | V |
| VB[n+1] to VB[n] | -0.3 to 10 | V |
| Driver Manager | | |
| CHG, DSG to VSS | -0.3 to 145 | V |
| CHG to BAT | -0.3 to 14 | V |
| DSG to PACK+ | -0.3 to 14 | V |
| FUSE to VSS | -0.3 to 14 | V |
| IO | | |
| PDx, PEx, PFx, PGx, to VSS | -0.3 to VCCIO + 0.3 | V |
| AIO0, PB to VSS | -0.3 to Vsys + 0.3 | V |
| I _{Pxy} pin injection current | 7.5 | mA |
| ∑I _{Pxy} sum of all pin injection current | 25 | mA |
| Temperature | | |
| T _A | -40 to 105 | °C |
| T _{STG} | -55 to 150 | °C |
| Electro-static Discharge (ESD) | | |
| Human Body Model (HBM) | 1 | kV |
| Charge Device Model (CDM) | 500 | V |

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Units |
|--------|-----------------------|-----|-----|-----|-------|
| PACK+ | Charger Input Voltage | 18 | | 100 | V |
| BAT | Battery Stack Voltage | 18 | | 100 | V |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

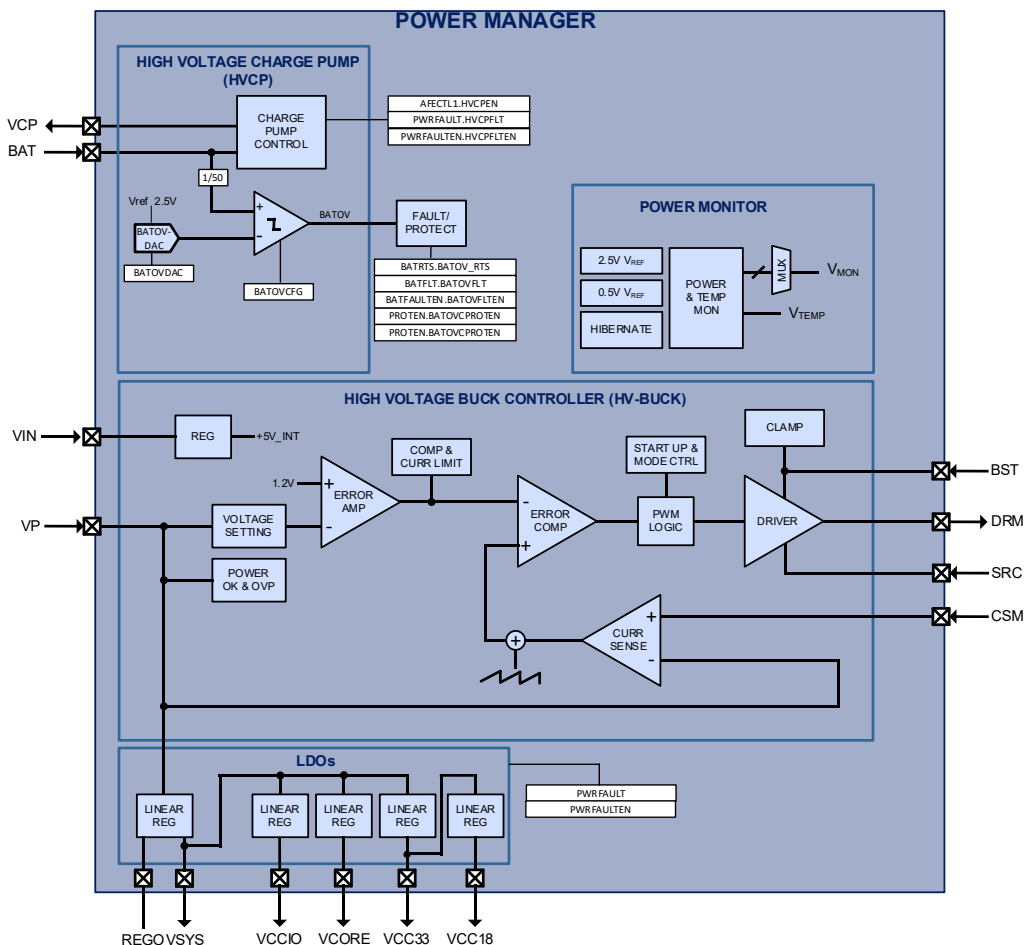
Power Manager

Features

- 145V Single Supply High-Voltage Buck (HV-BUCK) DC/DC controller
- High-Voltage Charge Pump
- 5V/250mA V_{SYS} regulator for system supply
- VCC33 LDO for 3.3V analog supply
- VCCIO LDO for 3.3V IO supply
- VCC18 LDO for 1.8V Flash internal supply
- V_{CORE} LDO for 1.2V core supply
- High-accuracy 2.5V voltage reference for MCU ADC (V_{REF})
- High-accuracy 0.5V voltage reference for Current Sense ADC
- Power and temperature monitoring, warning, and fault detection
- Extremely low hibernate mode I_Q of 3μA Typical at V_{IN}=80V

Block Diagram

Figure 2 Power Manager Block Diagram





PAC2514x Data Sheet

Functional Description

The Power Manager is optimized to efficiently provide “all-in-one” power management required by the PAC25140 and associated application circuitry. It incorporates a 145V input High-Voltage Buck DC/DC (HV-BUCK) and High-Voltage Charge Pump (HVCP) to generate the supplies for the integrated gate drivers and other sub-regulators.

The VSYS LDO generates a 5V/250mA system supply that is used to power the IC and the other LDOs. VSYS is used to supply the VCC33, VCCIO and VCORE, which are used to generate a 3.3V analog, 3.3V IO and 1.2V digital core supply. VCC18 is used for Flash memory supply and is generated from the VCC33. VCORE and VCC18 should not have any external loads.

The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

High-Voltage Buck (HV-BUCK)

The PAC25140 contains a High-Voltage Buck Controller for a Buck DC/DC (HV-BUCK). The HV-BUCK controller drives an external power MOSFET for pulse-width modulation switching of an inductor for power conversion. VIN is the HV-BUCK supply controller input. The DRM output drives the gate of the N-CH MOSFET between the VIN on state and VSS off state at proper duty cycle and switching frequency to ensure that the main supply voltage VP is regulated. The gate of the high-side power MOSFET is connected to the DRM pin and the source of the high-side power MOSFET is connected to SRC.

The VP regulation voltage is set to a fixed ~12V. When VP is lower than the target regulation voltage, the internal feedback control circuitry causes the inductor current to increase to raise VP. Conversely, when VP is higher than the regulation voltage, the feedback loop control causes the inductor current to decrease to lower VP. The feedback loop is internally stabilized. The output current capability of the switching supply is determined by the external current sense resistor. The inductor current signal is sensed differentially between the CSM pin and VP and has a peak current limit threshold of 0.2V.

High-Voltage Charge Pump (HVCP)

The High-Voltage Charge Pump (HVCP) is used as the high-side gate drive supply for the external CHG and DSG FET gate drivers. The charge pump output is VCP and charges to BAT + ~9V when enabled.

The BAT Over Voltage DAC, BATOVDAC and comparator can be used to monitor the BAT voltage, and trigger faults and protection mechanisms.

HV-BUCK Restart Handling

The HV-BUCK has a safety re-start mechanism that protects the device and external components in case of a DC/DC failure. This mechanism samples VIN and VP when the HV-BUCK is re-started and may insert a delay before it allows the power supply to be re-started, in case of some type of short or damage with the power supply components on the PCB.

If the DC/DC has been disabled due to VIN falling below $V_{UVLOF;VIN}$, VIN is sampled and as soon as $VIN > V_{UVLOR;VIN}$, then the DC/DC will immediately re-start.

If VIN is $> V_{UVLOF;VIN}$ but $VP < V_{UVLOF;VP}$ then the DC/DC is disabled and a 350ms delay is inserted. After this delay, the DC/DC is re-started.

Linear Regulators

The PAC25140 includes three linear regulators:

- VSYS
- VCC33
- VCCIO

The system supply regulator (VSYS) is a medium-voltage regulator that is supplied by VP (output of HV-BUCK) and sources up to 250mA at REGO until VSYS, externally coupled to REGO, reaches 5V. This allows a properly rated external resistor to be connected from REGO to VSYS to close the current loop and offload power dissipation between VP and VSYS. The VSYS regulator supplies the VCC33, VCCIO and VCORE sub-regulators.

The VCC33 regulator generates a 3.3V analog supply for the ADC and GPIO on the MCU. The VCORE regulator generates a dedicated 1.2V digital logic supply for the MCU. The VCCIO regulator generates a dedicated 3.3V supply for the GPIO on the MCU.

Once all LDOs are above their respective power good thresholds, then the MCU is released from reset and begins executing instructions.

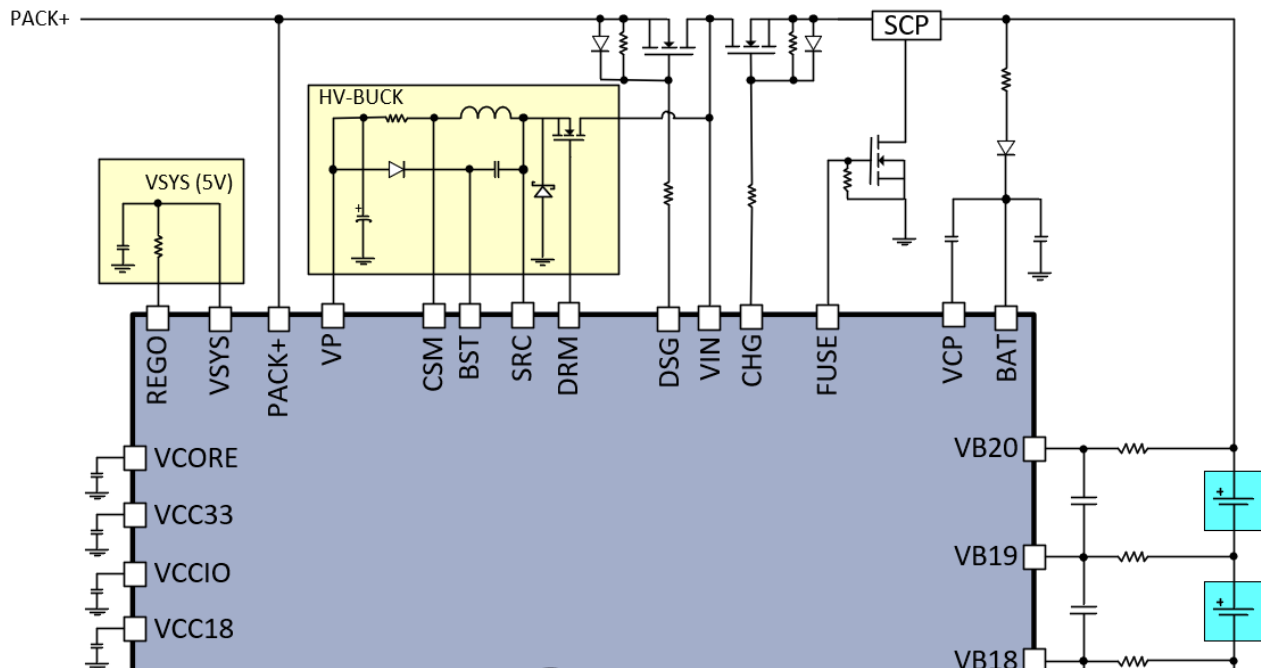
The VCC18 is generated from the VCC33 by the MCU for the flash.

Each of the LDOs must be bypassed externally to ground. See the electrical characteristics below for details on the recommended component values for each of the bypass capacitors.

Power Manager Circuit Connections

Figure 3 below shows the typical circuit connections for the HV-BUCK on the PAC25140.

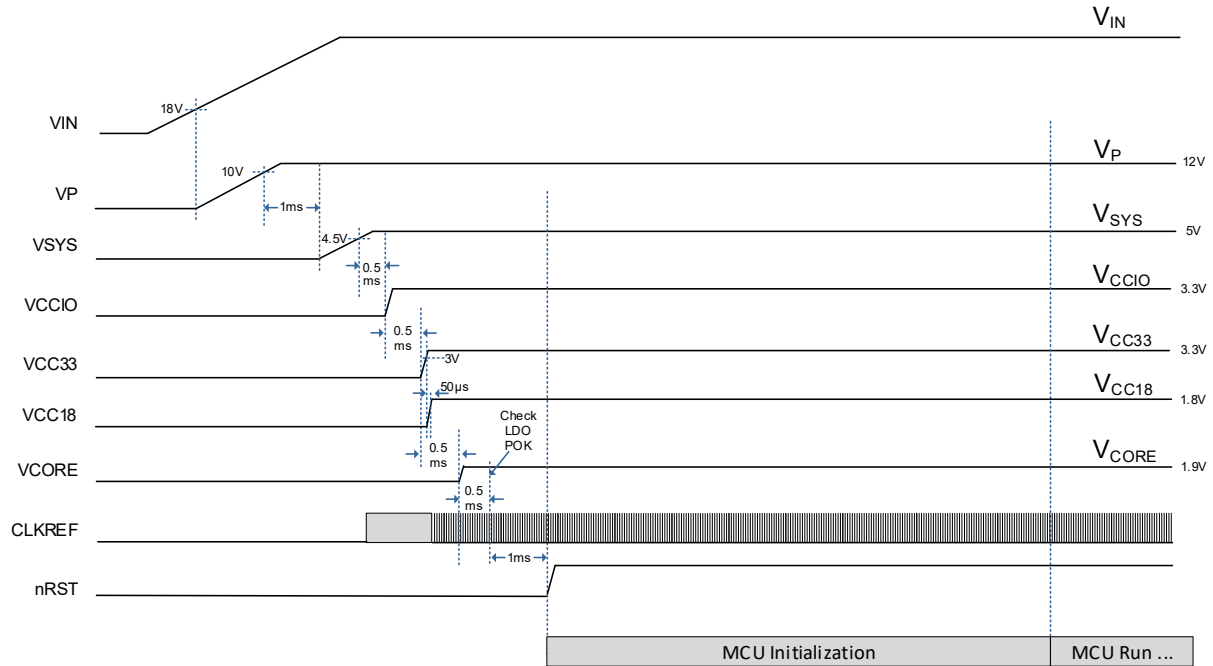
Figure 3 Power Manager Circuit Connections



HV-BUCK and LDO Power-up Sequence

The HV-BUCK and LDOs follow a typical power-up sequence as shown in Figure 4 below.

Figure 4 HV-BUCK and LDO Power-up Sequence



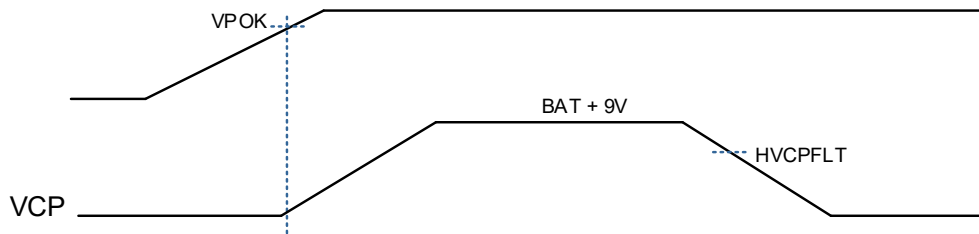
A typical sequence begins with voltage being applied on VIN. Once VIN reaches 18V, the HV-BUCK is enabled, and VP begins to rise. When VP reaches 10V, after 4ms the VSYS regulator is enabled. When VSYS reaches its power good threshold of 4.5V, after 0.5ms VCCIO begins to rise. After 0.5ms, VCC33 begins to rise and after another 1ms, and then VCC18 and VCORE begins to rise.

After VCORE rises plus 0.5ms, the power good thresholds of all LDOs are checked. If they are all OK, then there is a 1ms delay and the MCU is released from reset. At this point, the MCU will begin executing instructions.

HVCP Power-up Sequence

The HVCP follows a typical power-up sequence as shown in Figure 5 below.

Figure 5 HVCP Power-up Sequence



The HVCP is enabled and disabled under firmware control in the PAC25140 when it is needed to drive the gates on the CHG and DSG FETs.

Hibernate Mode

The PAC25140 contains a very low-power mode that may be used to minimize power consumption from the battery when the battery monitor is not operating. Hibernate mode allows the device to enter an ultra-low-power mode where only critical circuitry is enabled. In this mode, only a minimal amount of current is used by VIN, and most of the Power Manager and all internal regulators are shut down to eliminate power drain from the output supplies. The user may enter hibernate mode by writing a register in the AFE.

Hibernate mode may be exited by three user selectable options:

- 1) Push Button: by an active push-button input on the PB pin that is polarity selectable
- 2) PACK+ Charger Detect: by a PACK+ voltage selectable to 5V or 20V
- 3) Wakeup Timer: by the hibernate wakeup timer.

Power Monitoring

Whenever any of the VSYS, VCC33, VCCIO or VCORE power supplies falls below their respective power good threshold voltages, a fault event is detected and the MCU is reset. The MCU stays in the reset state until VSYS, VCC33, VCCIO, VCC18 and VCORE supply rails are all good again and the reset time has expired.

Power monitoring signals are provided onto the AFE MUX in the AFE for conversion by the 12-bit MCU ADC. The AFE MUX can select from the power monitoring signals: PACK+ * 0.02, BAT * 0.02, VIN * 0.02, VCORE, 0.4 * VCC33, 0.4 * VCCIO, 0.4 * VSYS, or VPTAT (temperature).

Temperature Monitoring

The device has monitoring for three junction temperatures. The MCU firmware can select whether to receive an interrupt when the device reaches any of the temperatures. Two temperatures, 120°C and 140°C, are warnings. A fault occurs when the junction temperature reaches 155°C and the MCU will be reset. The fault status bits are persistent during reset and can be read by the MCU upon re-initialization to determine the cause of the temperature fault reset.

Voltage References

There are two high-precision voltage references in the PAC25140: 2.5V and 0.5V.

The 2.5V high-precision reference is used by the MCU ADC (12-bit SAR), Voltage Sense ADC (16-bit Sigma-Delta) and AFE comparators. The 0.5V high-precision voltage reference is used by the Current Sense ADC (16-bit Sigma-Delta) and AFE comparators.



PAC2514x Data Sheet

Electrical Characteristics

The Electrical Characteristics for the Power Manager are shown below.

HV-BUCK Electrical Characteristics

Table 1 HV-BUCK Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|------------------|-----------------------------------|---|------|------|----------|---------|
| I_{norm} | VIN Normal mode supply current | Depending on Firmware Implementation and MCU clocking speed; No external loading. | | 7.3 | | mA |
| I_{sleep} | VIN Sleep mode supply current | CPU in deep sleep mode, systick clock disable, wait for interrupt. SCLK = CLKREF, turn off ROSC, turn off PLL, HCLK DIV = 8, all peripherals are disabled, CHG = OFF, DSG in Source Follower Mode, VCP = 0, No external loading | | 610 | | μ A |
| $I_{HIB;VIN}$ | VIN hibernate mode supply current | Hibernate mode active, VIN = 80V | | 3 | | μ A |
| $V_{UVLOR;VIN}$ | VIN UVLO rising threshold | | | 18 | | V |
| $V_{UVLOF;VIN}$ | VIN UVLO falling threshold | | | 16 | | V |
| $V_{REF;VP}$ | VP output regulation voltage | | -5% | 12 | 5% | V |
| $K_{POKR;VP}$ | VP power OK threshold | VP rising | | 91 | | % |
| $K_{POKF;VP}$ | | VP falling | | 87 | | % |
| $K_{OVPR;VP}$ | VP OV protection threshold | VP rising, blanking = 10 μ s | | 130 | | % |
| $t_{ONMIN;DRM}$ | DRM minimum on time | | 90 | 200 | 300 | ns |
| $t_{OFFMIN;DRM}$ | DRM minimum off time | | 390 | 600 | 1150 | ns |
| $V_{UVLOR;VP}$ | VP UVLO rising | | | 10 | | V |
| $V_{UVLOF;VP}$ | VP UVLO falling | | | 8 | | V |
| $V_{CSM;ILIM}$ | CSM current limit threshold | | -12% | 0.2 | 12% | V |
| $F_{S;DRM}$ | DRM switching frequency | Relative to switching frequency setting | -5 | | 5 | % |
| $I_{SOURCE;DRM}$ | DRM output high source current | | | 100 | | mA |
| $I_{SINK;DRM}$ | DRM output low sink current | | | 200 | | mA |
| | HV-BUCK inductor value | | | 100 | | μ H |
| $I_{DSG;HVBUCK}$ | Discharge current | | | 10 | | mA |
| V_{VIN} | HV-BUCK input voltage range | | 0 | | 145 | V |
| $V_{SRC;VSS}$ | SRC to ground range | | -10 | | VIN + 10 | V |
| $V_{SRC;VIN}$ | SRC to VIN range | | | | 10 | V |
| $V_{BST;VSS}$ | BST to ground range | | | | 145 | V |

VIN = 80V and TA = -40°C to 105°C unless otherwise specified



PAC2514x Data Sheet

HVCP Electrical Characteristics

Table 2 HVCP Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|----------------|------------------------------|--------------------------------|------|---------|------|---------|
| $I_{OP,VCP}$ | VCP operating output current | Steady state; No external load | | | | μA |
| $V_{OP,VCP}$ | VCP operating voltage range | $18V < BAT < 84V$ | | BAT + 9 | | V |
| C_{VCP} | VCP capacitor value | | | 0.47 | | μF |
| $V_{UVLOR,CP}$ | Charge pump UVLO rising | Blanking = 100 μs | | BAT + 6 | | V |
| $V_{UVLOF,CP}$ | Charge pump UVLO falling | | | BAT + 5 | | V |

BAT = 80V and TA = -40°C to 105°C unless otherwise specified

Linear Regulators Electrical Characteristics

Table 3 Linear Regulators Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|-----------------|-------------------------------|-------------------------------------|-------|------|-------|---------|
| V_{SYS} | VSYS output voltage | Total load up to 250mA | 4.85 | 5.0 | 5.15 | V |
| V_{CCIO} | VCCIO output voltage | Load = 10mA VCCIO from regulator | 3.152 | 3.3 | 3.398 | V |
| V_{CC33} | VCC33 output voltage | Load = 10mA | | 3.3 | | V |
| V_{CORE} | VCC18 output voltage | External Load not allowed | | 1.8 | | V |
| V_{CORE} | VCORE output voltage | | | 1.2 | | V |
| $I_{LIM,VSYS}$ | VSYS regulator current limit | | 225 | 260 | | mA |
| $I_{LIM,VCCIO}$ | VCCIO regulator current limit | | 95 | 130 | | mA |
| $I_{LIM,VCC33}$ | VCC33 regulator current limit | | 40 | 57 | | mA |
| | | | | | | |
| $I_{LIM,VCORE}$ | VCORE regulator current limit | | 40 | 57 | | mA |
| k_{SCFB} | Short-circuit fold back | | | 50 | | % |
| $V_{DO,VSYS}$ | VSYS dropout voltage | VP = 12V, I_{VSYS} = 100mA | | 350 | 680 | mV |
| $V_{UVLO,VSYS}$ | VSYS UVLO threshold | VSYS rising, hysteresis = 0.2V | 3.5 | 3.95 | 4.4 | V |
| $k_{POK,VCCIO}$ | VCCIO power OK threshold | VCCIO rising, hysteresis = 10% | 79 | 85 | 91 | % |
| $k_{POK,VCC33}$ | VCC33 power OK threshold | VCC33 rising, hysteresis = 10% | 79 | 85 | 91 | % |
| $k_{POK,VCORE}$ | VCORE power OK threshold | VCORE rising, hysteresis = 10% | 79 | 85 | 91 | % |
| C_{VSYS} | VSYS bypass capacitor value | | | 4.7 | 10 | μF |
| C_{VCC33} | VCC33 bypass capacitor value | | | 2.2 | 10 | μF |
| C_{VCC18} | VCC18 bypass capacitor value | | | 2.2 | 4.7 | μF |
| C_{VCORE} | VCORE bypass capacitor value | | | 2.2 | 10 | μF |
| C_{VCCIO} | VCCIO bypass capacitor value | | | 2.2 | 10 | μF |

VIN = 80V and TA = -40°C to 105°C unless otherwise specified



PAC2514x Data Sheet

Power Monitor Electrical Characteristics

Table 4 Power Monitor Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---------------------|---|--|------|------|------|-------|
| V _{REF;25} | Reference Voltage (2.5V) | T _A = 25°C | - | 2.5 | 0.5% | V |
| | | T _A = -40°C to 105°C | | 2.5 | | V |
| V _{REF;05} | Reference Voltage (0.5V) | T _A = 25°C | - | 0.5 | 0.5% | V |
| | | T _A = -40°C to 105°C | | 0.5 | | V |
| k _{MON} | Power Monitoring Voltage coefficient ⁽¹⁾ | PACK+, BAT, VIN, VCP, CHG, DSG | | 0.02 | | V / V |
| | | V _{CORE} | | 1 | | V / V |
| | | V _{SYS} , V _{CCIO} , V _{CC33} | 0.36 | 0.4 | 0.43 | V / V |
| | | V _P , FUSE | 0.09 | 0.1 | 0.11 | V / V |

VP = 12V and TA = -40°C to 105°C unless otherwise specified

(1) The Power Monitoring Voltage Coefficient is the scale factor used to multiply the corresponding voltage to achieve the ADC input voltage range.



PAC2514x Data Sheet

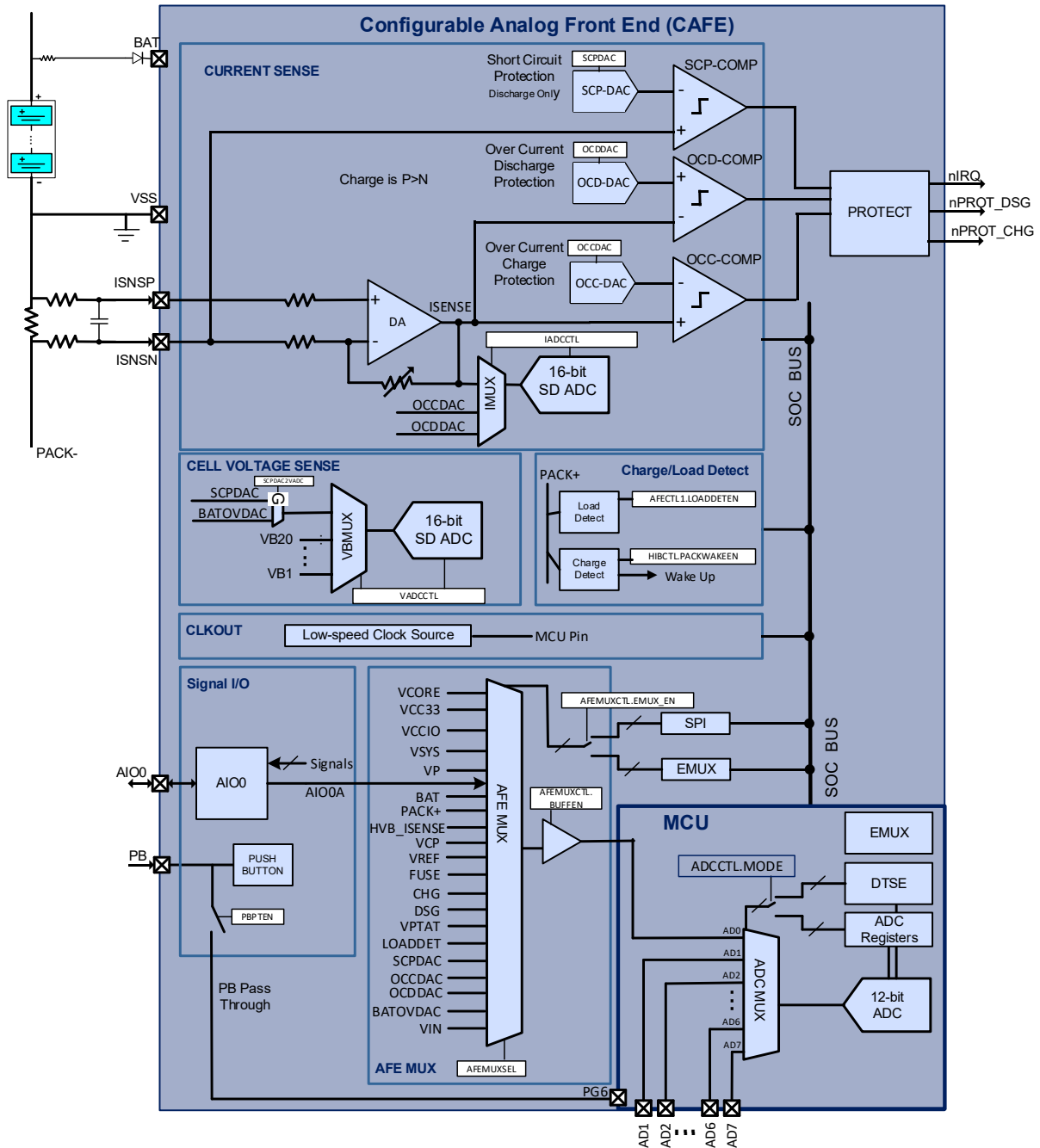
Configurable Analog Front-End (CAFE)

Features

- 16-bit Sigma-Delta ADC for current sense
- Current Sense Differential Programmable-Gain Amplifier
- Analog input/output gain amplifier with ADC Input or signal output selection
- Three comparators with DACs for programmable references for configurable OC warning or fault handling
- 16-bit Sigma-Delta ADC for Voltage Sampling of up to 20 cell voltages
- 12-bit Successive Approximation Register for Temperature sense and Pin ADC input and internal power supplies
- Internal Temperature warning and fault protection
- Push-Button (PB) input for exiting hibernate mode
- PACK+ Charge detection and Load detection
- 2kHz independent clock source

Block Diagram

Figure 6 CAFE Block Diagram



Functional Description

The PAC25140 contains a Configurable Analog Front-End (CAFE™). The CAFE can be used to sense battery pack current using an integrated Differential Amplifier and 16-bit Sigma-Delta ADC. The CAFE can configure two independent DACs to set two comparator thresholds for two levels of programmable over-current detection for the battery pack.

The CAFE can also sense voltage and temperature internally through a MUX which contains inputs for each of the cell balance channels as well as the internal power supply rails from the power manager.



PAC2514x Data Sheet

Current Sensing

The PAC25140 contains circuitry for battery pack current sense. The positive terminal (ISNSP) and negative terminal (ISNSN) are connected to each side of an external sense resistor. The ISNSP pin is connected to the positive terminal of a differential amplifier (DA) and the ISNSN pin is connected to the negative terminal of the amplifier. The differential amplifier has a programmable gain up to x128. This amplifier has a common-mode range of -0.3V to 0.5V. Using the gain stage allows a smaller current sense resistor, however, more noise will be introduced into the measurements.

The differential amplifier output is available for sampling from the 16-bit Current ADC.

To ensure accurate ADC conversion of the differential amplifier's output signal $V_{SENSE} * DA_{GAIN}$ must remain within a voltage range of +/-0.5V. The current sense voltage V_{SENSE} can be calculated using the following equation:

$$V_{SENSE} = (ADC_{RESULT} * ADC_{GAIN} + ADC_{OFFSET}) / DA_{GAIN}$$

Where:

V_{SENSE} is the voltage across the ISNSP and ISNSN pins.

ADC_{RESULT} is the 16-bit ADC result in counts

ADC_{GAIN} is $1.25V/2^{16}$ counts = 19.073 $\mu V/count$

ADC_{OFFSET} is -0.625V

DA_{GAIN} is the selected differential amplifier gain

A theoretical ADC full scale reading of 0xFFFF equals 0.625V, a half scale reading of 0x8000 equals 0V, and 0x0000 = -0.625V.

To achieve the best accuracy, a calibration step should be performed after final assembly.

Over-Current Protection

There are three analog protection comparators that may be used for over-current protection: one for short circuit protection (SCP-COMP), one for over-current discharge protection (OCD-COMP) and one for over-current charge protection (OCC-COMP). Each of the comparators has a DAC that may be used to set the comparator reference.

When one of the comparators trips, the device will send a signal to the driver manager and can be programmed in various ways to disable the CHG/DSG FETs, as well as interrupt the MCU via an IRQ signal.

Voltage Sensing

The PAC25140 also contains a 16-bit Sigma-Delta ADC that may be used for voltage sensing for the individual cells. There is a MUX that selects each of the individual cell balance nodes (VB1 to VB20) so that they may be sampled by the 16-bit ADC.

The SOC bus is used for the MUX select as well as the ADC operation and fetching of the 16-bit result from the MCU.



PAC2514x Data Sheet

AFE MUX

The CAFE also contains the AFE MUX that can be used to sample the internal power supply rails on the device, internal die temperature, and other signals. This will provide internal cross checking for references and key signals for Functional Safety (FUSA).

The AFE MUX select can be controlled from the SOC bus or via the EMUX. The output of the AFE MUX is connected to the 12-bit ADC on the MCU so it may be sampled by the auto-sequencer.

The MUX channels or scaled values (see Users Guide) that are available are:

- VCORE – 1.2V Core Logic LDO
- VCC33 – 3.3V Analog LDO
- VCCIO – 3.3V Digital I/O LDO
- VSYS – 5V System Supply
- VP – DC/DC Output
- ISENSE – Current Sense Diff Amp Output
- AIO0A – AIO0 Analog Output
- BAT – Battery Stack Input
- PACK+ - Charger Supply Input
- VCP – Charge Pump Output
- VREF – 2.5V Voltage reference
- FUSE – FUSE output
- CHG – CHG FET gate driver signal
- DSG – DSG FET gate driver signal
- VPTAT – Internal Temperature Sensor
- LOADDET – Load monitoring signal
- SCPDAC – Short Circuit Protection DAC output
- OCCDAC – Over Current Charge DAC output
- OCDDAC – Over Current Discharge DAC output
- BATOVDAC – Battery Over Voltage DAC output
- VIN – Main Input Supply Voltage

Temperature Monitoring and Protection

The PAC25140 has an integrated temperature sensor that is used for die temperature warnings and faults and can also be sampled by the MCU ADC through the AFE MUX using the VPTAT MUX channel.

This value has a compensation coefficient available in INFO FLASH that can be used to obtain an accurate temperature. The parameter VT300K will be stored in INFO FLASH and will indicate the compensation factor.

The die temperature in degrees Kelvin can then be calculated by the following formula:

$$TKELVIN = 300 * (VPTAT + 0.075) / (VT300K + 0.075)$$

The PAC25140 contains two warning thresholds and one fault threshold:

- Warn 1: 120°C
- Warn 2: 140°C
- Fault: 155°C

If the internal temperature (VPTAT) rises above the Warn 1 threshold, the device will indicate this through a latched register bit. The user may enable a mask-able interrupt to the MCU to announce this condition.

If the internal temperature (VPTAT) rises above the Warn 2 threshold, the device will indicate this through a separate latched register bit. The user may enable an interrupt to the MCU to announce this condition. This will be the same interrupt as the Warn 1 threshold.

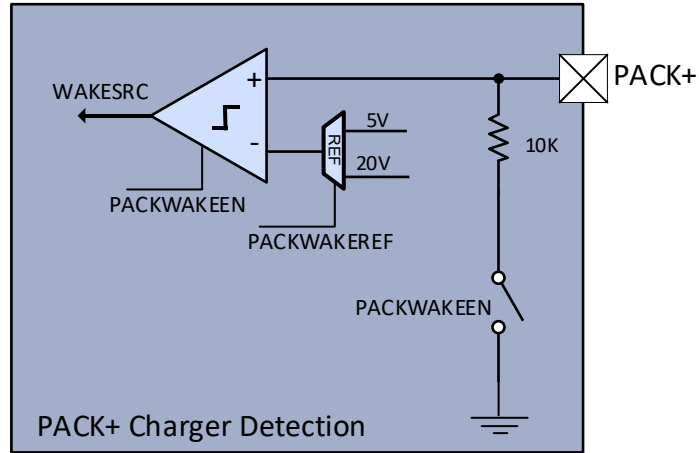
If the internal temperature (VPTAT) rises above the Fault threshold, the Charge pump, DC/DC and gate drivers will be disabled. The device will indicate this through a latched register bit. There is not interrupt for this condition. When the device falls below the hysteresis value, then the DC/DC will be re-enabled.

The temperature hysteresis level for all three thresholds is 10°C.

PACK+ Charger Detection

When properly configured the Pack+ Charger Detection can be used to exit hibernate mode. The threshold is selectable, and when PACK+ crosses it a wake up event occurs. To prevent PACK+ from floating a 10kΩ can be enabled to pull PACK+ low.

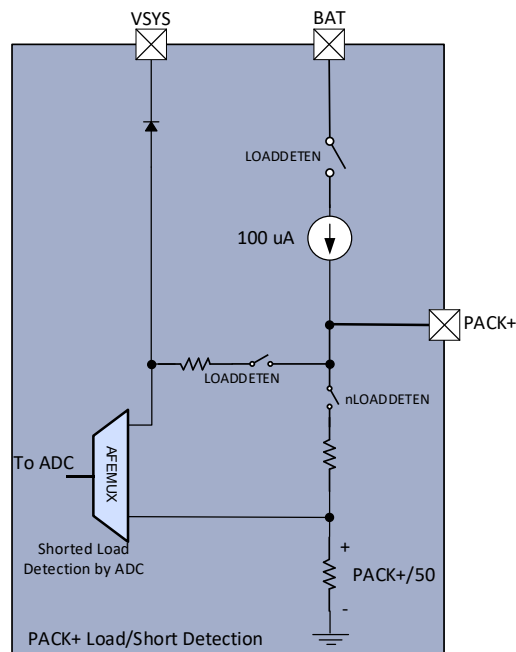
Figure 7 PACK+ Charger Detection



PACK+ Load/Short Detection

When properly configured the load detection can be used for load or shorted load event detection. This requires firmware to move the state of the system into the proper configuration. Either a load or a shorted load can be detected. This detection is disabled during hibernate mode.

Figure 8 PACK+ Load/Short Detection



Push-Button (PB) Input

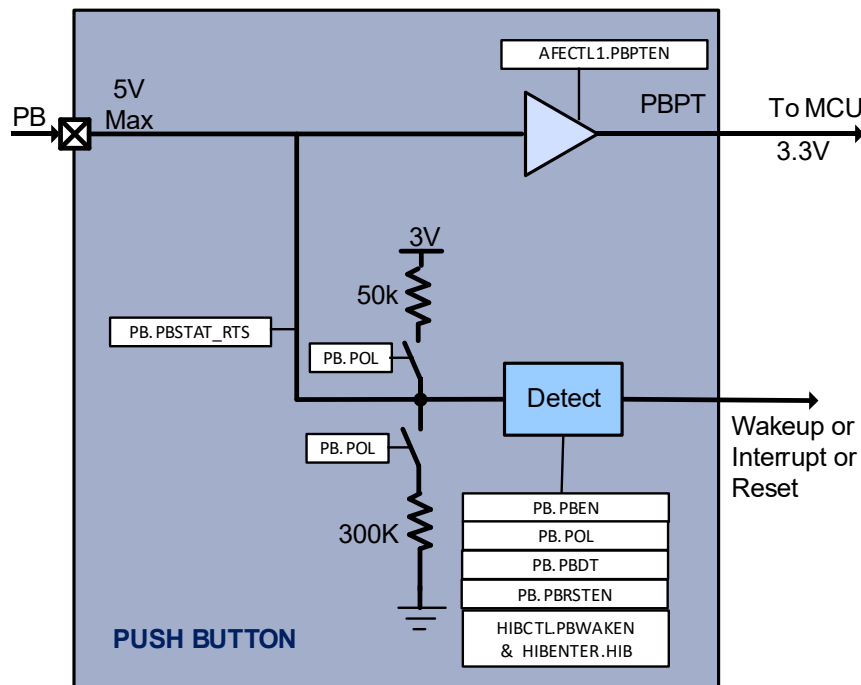
The PAC25140 contains a push-button input pin (PB) and a push-button module (see Figure 9 below). A push-button pass through to the MCU can be enabled so that the MCU can read the state of the digital PB pin directly on the PG6 GPIO. PG6 can also be configured as a UART RX input. In this case, an external UART TX signal can be used to wakeup the device, and then send UART transmissions to the MCU after the MCU comes out of reset and has been initialized.

The push-button module can be used to wake-up the device from hibernate, interrupt the MCU, or reset the device. The push-button polarity can be set to active high or active low using the polarity setting.

The push-button module can be configured so that an active PB will wake up the PAC25140 from hibernate mode.

When enabled, the push-button may also be used as a hardware reset when held active for longer than 8s during normal operation. Once the push-button is enabled, the polarity setting will determine whether the PB input will be pulled up to 3V with a 50kΩ resistor or pulled down to GND with a 300kΩ resistor. There is also a programmable de-glitch time that may be configured to 1, 4, 8, or 32ms.

Figure 9 Push-Button (PB) Input

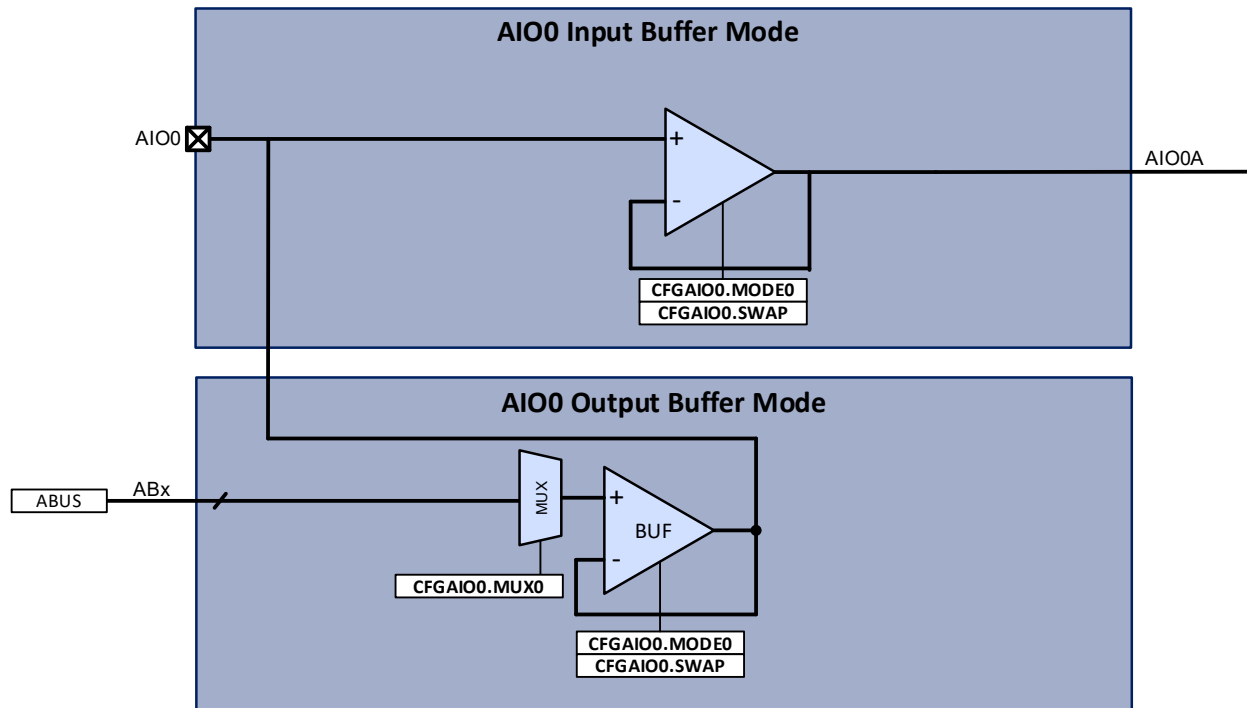


AIO0 – Analog Input Output

The PAC25140 has an AIO0 module and pin that includes a buffer for analog I/O (see Figure 10 below). The AIO0 pin can be configured as an input where the output of the buffer, AIO0A, is routed to the AFE Mux for input to the MCU ADC. Or, the AIO0 pin can be configured to output internal signals of the AFE. The following signals are available for output on the AIO0 pin:

- VREF – 2.5V Voltage Reference
- AFEMUXOUT – AFE Mux Output to the MCU ADC
- IMUXOUT – Current Mux Output to the Current ADC
- VBMUXOUT – Battery Cell Voltage Mux Output to the Voltage ADC

Figure 10 AIO0 Analog Input Output





PAC2514x Data Sheet

Electrical Characteristics

The Electrical Characteristics for the CAFE are shown below.

Differential Amplifier (DA) Electrical Characteristics

Table 5 DA Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|-----------------------|-------------------------------|--|------|------|------------------------|-------|
| V _{ICMR,DA} | Input common mode range | | -0.3 | | 0.5 | V |
| V _{OLR,DA} | Output linear range | | 0.1 | | V _{SYS} - 0.1 | V |
| I _{CC,DA} | Operating supply current | | | 150 | | μA |
| V _{OS,DA} | Input offset voltage | Gain = 8x | -8 | | 8 | mV |
| K _{CMRR,DA} | Common mode rejection ratio | | 50 | 80 | | dB |
| | Slew rate | Gain = 8x | 5 | | | V/μs |
| R _{INDIF,DA} | Differential input impedance | | | 80 | | kΩ |
| t _{ST,DA} | Settling time | To 1% of final value | | | TBD | ns |
| A _{VZ,DA} | Amplifier gain ⁽¹⁾ | Gain = 1x | | 1 | | |
| | | Gain = 2x | | 2 | | |
| | | Gain = 4x | | 4 | | |
| | | Gain = 8x, V _{DAXP} =V _{DAXN} =0V, T _A = 25°C | -2 | 8 | 2 | % |
| | | Gain = 16x | | 16 | | |
| | | Gain = 32x | | 32 | | |
| | | Gain = 64x | | 64 | | |
| | | Gain = 128x | | 128 | | |

(1) For proper ADC conversion and Over-Current protection, VISENSE * DAGAIN must be within +/- 0.5V

T_A = -40°C to 105°C unless otherwise specified

Current Sense ADC Electrical Characteristics

Table 6 Current Sense ADC Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---------------------------|--------------------------------------|--|------|---------|--------|-------|
| t _{ADCONV,ADC16} | ADC conversion time | | | 1.5 | | ms |
| | ADC resolution | | | 16 | | bits |
| | ADC effective resolution | | 15 | | | bits |
| | ADC differential non-linearity (DNL) | | | +/- 0.5 | | LSB |
| | ADC integral non-linearity (INL) | | | +/- 6 | +/- 20 | LSB |
| | ADC offset error | T _a =25°C , DiffAmp Gain =1 after calibration | | 130 | | μV |
| | ADC gain error | T _a =25°C DiffAmp Gain =1 after calibration | | 1.25 | | %FS |

T_A = -40°C to 105°C unless otherwise specified



PAC2514x Data Sheet

Short Circuit Protection Comparator (SCP-COMP) Electrical Characteristics

Table 7 SCP-COMP Electrical Characteristics

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|------------------------------|--------------------------|---------------------------------|------|------|------|-------|
| I _{CC} ; SCP-COMP | Operating supply current | | | 10 | | μA |
| V _{ICMR} ; SCP-COMP | Input range | Relative to common mode voltage | 0 | | 0.5 | V |
| V _{OS} ; SCP-COMP | Input offset voltage | T _A =25°C | -10 | | 10 | mV |
| V _{HYS} ; SCP-COMP | Hysteresis | | | 50 | | mV |
| t _{DT} ; SCP-COMP | Comparator deglitch time | 10mV difference input | | 1 | | μs |

T_A = -40°C to 105°C unless otherwise specified.

Over-Current Discharge Protection Comparator (OCD-COMP) Electrical Characteristics

Table 8 OCD-COMP Electrical Characteristics

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|------------------------------|--------------------------|---------------------------------|------|------|------|-------|
| I _{CC} ; OCD-COMP | Operating supply current | | | 10 | | μA |
| V _{ICMR} ; OCD-COMP | Input range | Relative to common mode voltage | 0 | | 0.5 | V |
| V _{OS} ; OCD-COMP | Input offset voltage | T _A =25°C | -10 | | 10 | mV |
| V _{HYS} ; OCD-COMP | Hysteresis | | | 50 | | mV |
| t _{DT} ; OCD-COMP | Comparator deglitch time | 10mV difference input | | 10 | | μs |

T_A = -40°C to 105°C unless otherwise specified.

Over-Current Charge Protection Comparator (OCC-COMP) Electrical Characteristics

Table 9 OCC-COMP Electrical Characteristics

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|------------------------------|--------------------------|---------------------------------|------|------|------|-------|
| I _{CC} ; OCC-COMP | Operating supply current | | | 10 | | μA |
| V _{ICMR} ; OCC-COMP | Input range | Relative to common mode voltage | 0 | | 0.5 | V |
| V _{OS} ; OCC-COMP | Input offset voltage | T _A =25°C | -10 | | 10 | mV |
| V _{HYS} ; OCC-COMP | Hysteresis | | | 50 | | mV |
| t _{DT} ; OCC-COMP | Comparator deglitch time | 10mV difference input | | 10 | | μs |

T_A = -40°C to 105°C unless otherwise specified.



PAC2514x Data Sheet

Voltage ADC

Each of the battery cell voltages are available for sampling from the 16-bit Voltage ADC. The ADC was designed to accurately convert voltages between 1.8V and 4.7V. The Voltage ADC equation is given by:

$$V_{CELL} = ADC_{RESULT} * ADC_{GAIN} + ADC_{OFFSET}$$

Where:

V_{CELL} is the voltage of the converted cell

ADC_{RESULT} is the ADC result in counts

ADC_{GAIN} is $12.5V/2^{16}$ counts = 190.73 μV /count

ADC_{OFFSET} is -6.25V.

A theoretical ADC full scale reading of 0xFFFF equals 6.25V and a half scale reading of 0x8000 equals 0V.

Cell Voltage ADC Electrical Characteristics

Table 10 Cell Voltage ADC Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------------------|--------------------------------------|--------------------------------------|------|---------|------|-------|
| $t_{ADCONV,ADC16}$ | ADC conversion time | $f_{ADCLK} = 16MHz$ | | 5 | | ms |
| | ADC resolution | | | 16 | | bits |
| | ADC effective resolution | | 14 | | | bits |
| | ADC differential non-linearity (DNL) | | | +/- 0.3 | | LSB |
| | ADC integral non-linearity (INL) | | | +/- 4 | | LSB |
| | ADC offset error | $T_A = 25^\circ C$ after calibration | | 3 | | LSB |
| | ADC gain error | $T_A = 25^\circ C$ after calibration | | 0.82 | | %FS |

$T_A = -40^\circ C$ to $105^\circ C$ unless otherwise specified

Cell Voltage Measurement Accuracy Electrical Characteristics

Table 11 Cell Voltage Measurement Accuracy Electrical Characteristics

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|----------------|--|---|------------|----------------|----------|-------|
| $V_{CELL,ACC}$ | Cell voltage measurement accuracy ⁽¹⁾ | 3.2V <= Vcell <= 4.2V; 1.8V <= Vcell <= 4.7V; $T_A = 25^\circ C$; ⁽¹⁾ | | +/-2.5 +/-5 | | mV |
| | | 3.2V <= Vcell <= 4.2V; 1.8V <= Vcell <= 4.7V; $T_A = 0^\circ C$ to $85^\circ C$; ⁽¹⁾ | -10 -15 | | 10 15 | mV |
| | | 3.2V <= Vcell <= 4.2V; 1.8V <= Vcell <= 4.7V; $T_A = -40^\circ C$ to $105^\circ C$; ⁽¹⁾ | -20 -30 | | 20 30 | mV |

(1) After ADC Calibration

$T_A = -40^\circ C$ to $105^\circ C$ unless otherwise specified



PAC2514x Data Sheet

Push-Button Electrical Characteristics

Table 12 Push-Button Electrical Characteristics

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|----------------------|--------------------------|---|------|------|------|-------|
| V _{I,PBTN} | Input voltage range | | 0 | | 5 | V |
| V _{IH,PBTN} | High-level input voltage | | 2.0 | | | V |
| V _{IL,PBTN} | Low-level input voltage | | | | 1.4 | V |
| R _{PU,PBTN} | Pull-up resistance | To 3V, push-button enabled PB.POL = Active Low | | 50 | | kΩ |
| R _{PD,PBTN} | Pull-down resistance | To GND, push-button enabled PB.PBPOL = Active high | | 300 | | kΩ |

TA = -40°C to 105°C unless otherwise specified

Temperature Protection Electrical Characteristics

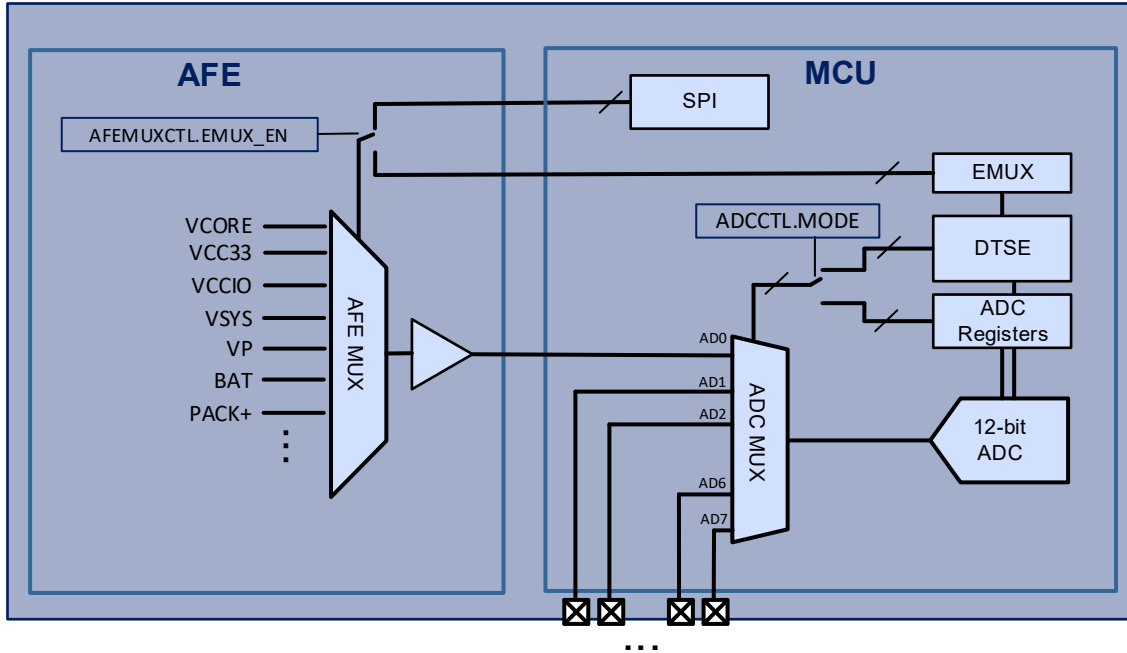
Table 13 Temperature Protection Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------------------------|----------------------------------|------------|------|------|------|-------|
| T _{WARN1} | Temperature warning 1 threshold | | | 120 | | °C |
| T _{WARN1;HYS} | Temperature warning 1 hysteresis | | | 10 | | °C |
| T _{WARN1;BLANK} | Temperature warning 1 blanking | | | 10 | | μs |
| T _{WARN2} | Temperature warning 2 threshold | | | 140 | | °C |
| T _{WARN2;HYS} | Temperature warning 2 hysteresis | | | 10 | | °C |
| T _{WARN2;BLANK} | Temperature warning 2 blanking | | | 10 | | μs |
| T _{FAULT} | Temperature fault threshold | | | 155 | | °C |
| T _{FAULT;HYS} | Temperature fault hysteresis | | | 10 | | °C |
| T _{FAULT;BLANK} | Temperature fault blanking | | | 10 | | μs |

TA = -40°C to 105°C unless otherwise specified

Block Diagram

Figure 11 12-bit MCU ADC Block Diagram



Functional Description

ADC

The analog-to-digital converter (ADC) is a 12-bit successive approximation register (SAR) ADC with 400ns conversion time and up to 2.5 MSPS capability. The integrated analog multiplexer allows selection from up to 8 direct ADx inputs, and additional analog inputs signals from the Configurable Analog Front End (CAFÉ).

The ADC contains a power down mode, and the user may configure the ADC to interrupt the MCU for the completion of a conversion when in manual mode. The ADC may be configured for either repeating or non-repeating conversions or conversion sequences.

ADC Conversion Timing

The ADC supports two modes for individual conversions: standard and enhanced. The timing diagrams for each of these modes is shown in figure 12 and 13.

Figure 12 ADC Conversion Timing Diagram (standard)

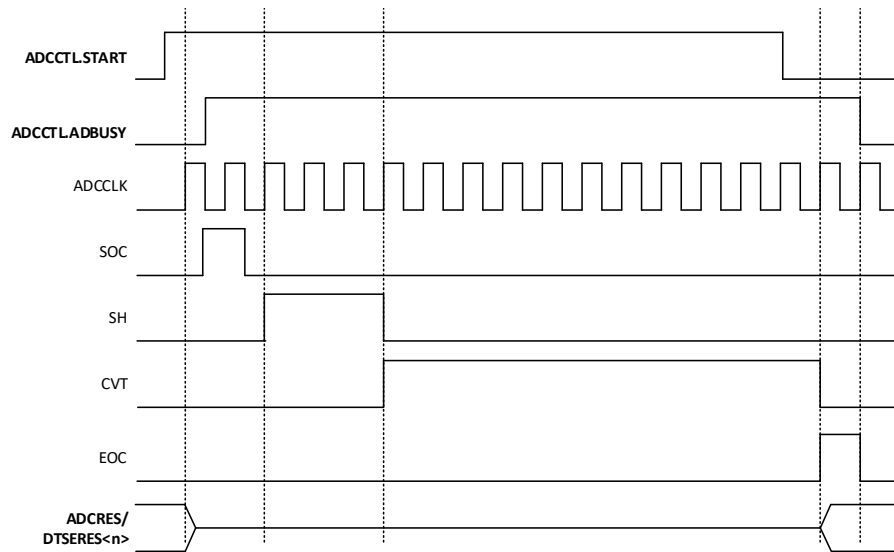
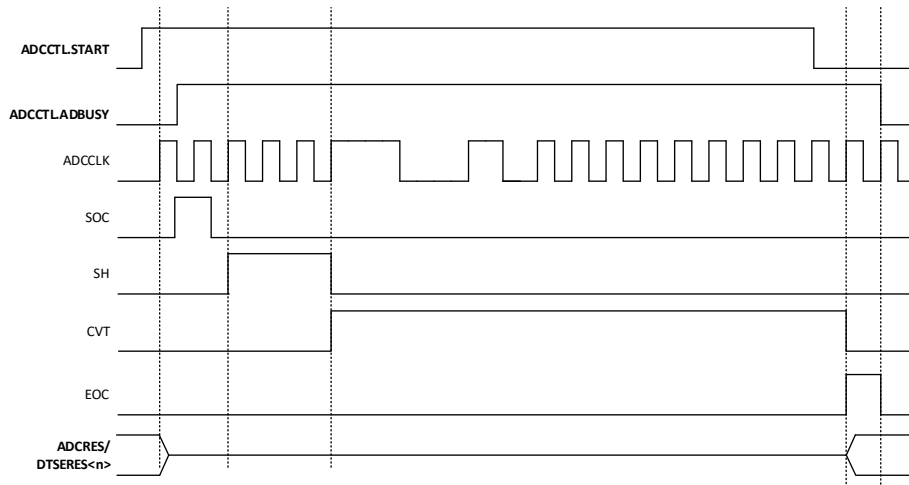


Figure 13 ADC Conversion Timing Diagram (enhanced)





PAC2514x Data Sheet

Dynamic Triggering and Sample Engine

The Dynamic Triggering and Sample Engine (DTSE) is a highly configurable automatic sequencer that allows the user to configure automatic sampling of their application-specific analog signals without any interaction from the microcontroller core. The DTSE also contains a pseudo-DMA engine that copies each of up to 24 conversion results to dedicated memory space and can interrupt the MCU when complete.

The DTSE has up to 32 input triggers, from PWM Timers A, B, C and D for either the rising, falling or rising and falling PWM edges. The user may also force any trigger sequence by writing a register via firmware. The user can configure the DTSE to chain from 1 to 24 conversions to any PWM trigger.

The DTSE has a flexible interrupt structure that allows up to 24 interrupts to be configured at the completion of any individual conversion. The user may configure one of four different IRQ signals when generating an interrupt during sequence conversions. The IRQ may be generated at the end of a conversion sequence, or at the end of a series of conversions. The user may select one of four IRQs for conversions, and each may be assigned a different interrupt priority.

Each of the 24 conversions has dedicated results registers, so that the pseudo-DMA engine has dedicated storage for each of the conversion results.

EMUX Control

A dedicated low latency interface controllable by the DTSE or register control allows changing the ADC pre-multiplexer and asserting/de-asserting the S/H circuit in the Configurable Analog Front-End (CAFE), allowing back-to-back conversions of multiple analog inputs without microcontroller interaction.

For more information on the ADC and DTSE, see the PAC55XX Family User Guide.



PAC2514x Data Sheet

Electrical Characteristics

Table 14 ADC and DTSE Electrical Characteristics

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|--------------------------|--------------------------------------|---|------|-------|------|---------|
| ADC | | | | | | |
| f _{ADCLK} | ADC conversion clock input | | | | 40 | MHz |
| t _{ADCONV} | ADC conversion time | f _{ADCLK} = 40MHz Enhanced accuracy mode disabled 16 ADC Clocks per conversion | | | 400 | ns |
| | | f _{ADCLK} = 40MHz Enhanced accuracy mode enabled 20 ADC Clocks per conversion | | | 500 | ns |
| t _{ADCSH} | ADC sample and hold time | f _{ADCCCLK} = 40MHz | | | 75 | ns |
| | | | | | 3 | ADCCLKs |
| C _{ADCIC} | ADC input capacitance | ADC Mux Input | | 1 | | pF |
| | ADC resolution | | | 12 | | bits |
| | ADC effective resolution | | 10.5 | | | bits |
| | ADC differential non-linearity (DNL) | F _{ADCCCLK} = 25MHz | | ±0.5 | | LSB |
| | | F _{ADCCCLK} = 40MHz | | ±0.75 | | LSB |
| | ADC integral non-linearity (INL) | F _{ADCCCLK} = 25MHz | | ±0.5 | | LSB |
| | | F _{ADCCCLK} = 40MHz | | ±0.75 | | LSB |
| | ADC offset error ¹ | | | 5 | | LSB |
| | ADC gain error ¹ | | | 0.5 | | % |
| Reference Voltage | | | | | | |
| V _{REFADC} | ADC reference voltage input | | | 2.5 | | V |
| EMUX Clock Speed | | | | | | |
| f _{EMUXCLK} | EMUX engine clock input | | | | 50 | MHz |

V_P = 12V, V_{SYS} = 5V and T_A = -40°C to 125°C unless otherwise specified

¹ ADC offset and gain parameters are calculated post-calibration when using the ADCOFF and AD CGAIN calibration parameters from INFO2 FLASH

Application Specific Power Drivers (ASPD)

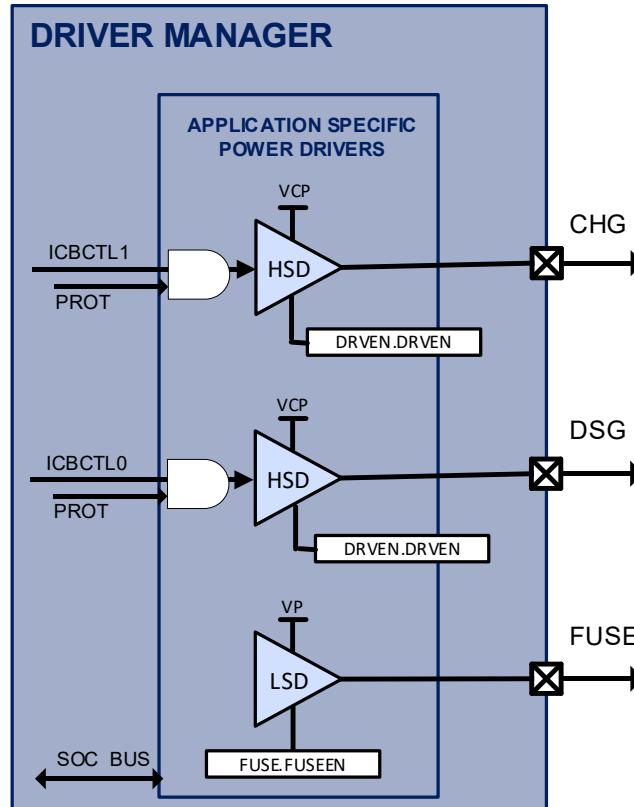
Gate Drivers

Features

- High-Side gate drivers for CHG and DSG FET
- Low-side gate driver for external FUSE

Block Diagram

Figure 14 ASPD Block Diagram



Functional Description

The Application Specific Power Drivers™ (ASPD) module drives the gate of the external CHG and DSG FETs and external protection fuse FET for the battery pack.

The CHG and DSG FET gates are driven from the CHG and DSG pins. The typical gate drive ON voltage for the CHG and DSG FETs is VCP (BAT + 9V). Source Follower Mode can be selected for lower current operations and not require enabling the charge pump. In this mode, CHG drive is off and DSG is on with a pull up to BAT. The mode is control by the DRVMODE control bits (see Users Guide). Protection mechanisms from the battery over voltage and over current comparators will also be applied as configured in the AFE protection registers. Once the CHG and DSG gate drivers enable bits are set in the analog front end (AFE), the MCU must also set the appropriate GPIOs to drive the gate driver outputs high/ON.

The FUSE output is a low-side switch supplied by VP which is intended for driving the gate on an external FET which is typically used to below an external fuse in series with PACK+ and the battery stack. The FUSE can support other low-side driver needs such as driving an LED..

Electrical Characteristics

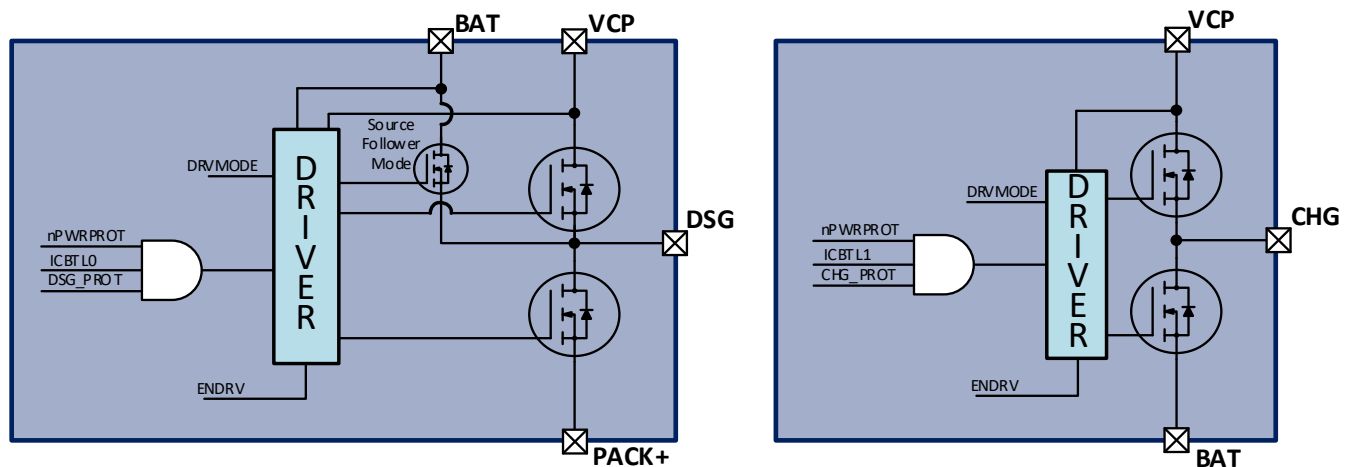
The Electrical Characteristics for the ASPD are shown below.

Table 15 ASPD Electrical Characteristics

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|------------------|---|--|------|-------|------|----------|
| V_{FETON} | CHG or DSG FET On with respect to BAT | CHG/DSG $C_L = 20$ nF | | 9 | | V |
| $V_{CHGFETOFF}$ | CHG FET Off (with respect to BAT) | CHG/DSG $C_L = 20$ nF | | | 0.3 | V |
| $V_{DSGFETOFF}$ | DSG FET Off (with respect to PACK+) | CHG/DSG $C_L = 20$ nF | | | 0.3 | V |
| $V_{SRCFLWR}$ | DSG on voltage (with respect to BAT) | CHG/DSG $C_L = 20$ nF | | 0 | | V |
| $t_{FETrise}$ | CHG or DSG rise time 0.3V to 5V (with respect to BAT) | CHG/DSG $C_L = 20$ nF, $R_{GATE} = 100$ Ω | | 25 | 50 | μ s |
| $t_{CHGFETfall}$ | CHG FET fall time to BAT + 0.3V | CHG/DSG $C_L = 20$ nF, $R_{GATE} = 100$ Ω | | 50 | 75 | μ s |
| $t_{DSGFETfall}$ | DSG FET fall time to PACK+ + 0.3V | CHG/DSG $C_L = 20$ nF, $R_{GATE} = 100$ Ω | | 5 | 25 | μ s |
| V_{FUSE} | FUSE Voltage | $C_L = 1$ nF Assumes valid VIN | | V_p | | V |
| $t_{FUSErise}$ | FUSE rise time | $C_L = 1$ nF Time to 90% of V_{FUSE} | | 0.5 | | μ s |
| $R_{FUSEdriver}$ | FUSE driver output resistance | | | 400 | | Ω |

TA = -40°C to 105°C unless otherwise specified

Figure 15 High Side Gate Drivers



Integrated Cell Balancing

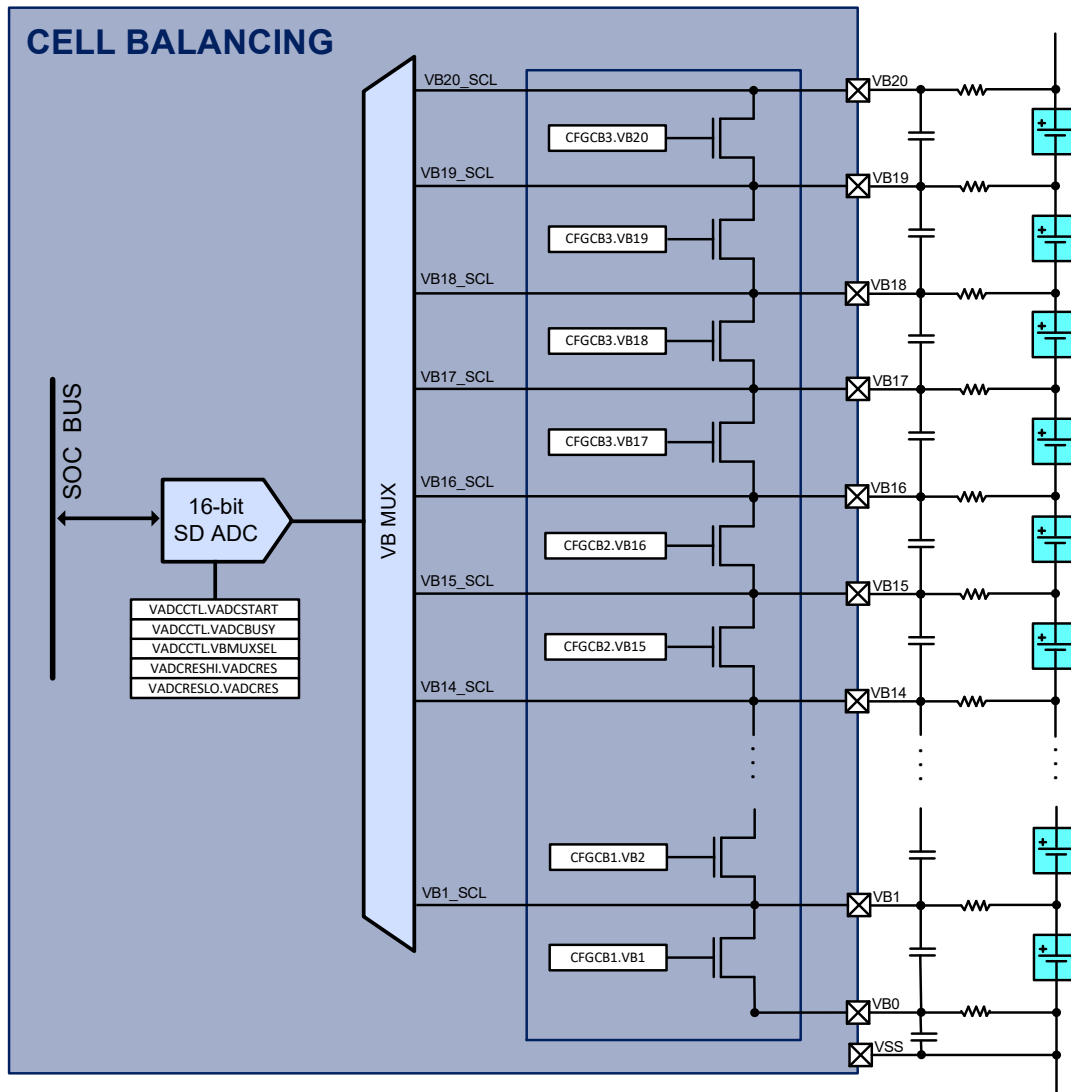
The PAC25140 contains integrated cell balancing FETs for up to 20 cells.

Features

- FETs for each cell to allow discharge of individual cells
- Voltage ADC for sensing the voltage of each cell

Block Diagram

Figure 16 Cell Balancing



The integrated cell balancing contains FETs for up to 20 battery cells. Cell balancing can be performed through firmware programming. Each of the battery cell voltages from the VB[1..20] pins are available for sampling from the 16-bit ADC.

Adjacent cells should not be balanced at the same time. In the event that too many cells are being balanced at the same time and Thermal protection occurs, then the cell balancing will be shut down first.



PAC2514x Data Sheet

Electrical Characteristics

The Electrical Characteristics for the Cell Balancing are shown below.

Table 16 Cell Balancing Electrical Characteristics

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|-----------------|---------------------------------|--------------------------------|------|------|------|----------|
| | Number of cells | | 10 | | 20 | cells |
| V_{VB} | Cell voltage range | | 1.8 | 3.6 | 4.7 | V |
| I_{VB} | Cell balance output current | $V_{VB} = 4.2V$ | | 50 | | mA |
| $R_{DS(ON);CB}$ | Cell balance FET $R_{DS(ON)}$ | $1.8V \leq V_{cell} \leq 4.7V$ | | 25 | | Ω |
| | External cell balance resistors | | 20 | 30 | | Ω |

TA = -40°C to 105°C unless otherwise specified

Battery AFE Windowed Watchdog Timer (WWDT)

This section describes the requirements for the BMS AFE Windowed Watchdog Timer (WWDT) module.

The SOC Bus Windowed Watchdog Timer must be accessed over the SOC Bridge I/F and can be used to reset the entire device if not reset at periodic intervals.

Wake-up Timer

The wake-up timer can be used for very low power hibernate and sleep modes to wake up the device periodically. It can be configured to be 125ms, 250ms, 500ms, 1s, 2s, 4, or 8s.

This AFE WWDT provides greater flexibility than previous AFE WDTs such that customers have a better chance of matching the WDT time to their system requirements. Using the AFE WWDT will provide a more complete device reset than the digital WDT.

The Windowing feature gives better robustness against rogue software that might be in a loop resetting the WDT continuously.

To comply with safety requirements, the WWDT shall be clocked from the 32 kHz Oscillator and not the 4 MHz CLKREF.

When the WWDT issues a reset, a Flag bit shall be set in the AFE reset status register indicating the WWDT caused the reset. Register bits shall be reset or retained per the Reset column in the Register Map (see Users Guide)

A key benefit of the AFE WWDT is that it will reset the MCU and also the majority of the battery AFE.

Figure 17 WWDT System Block Diagrams

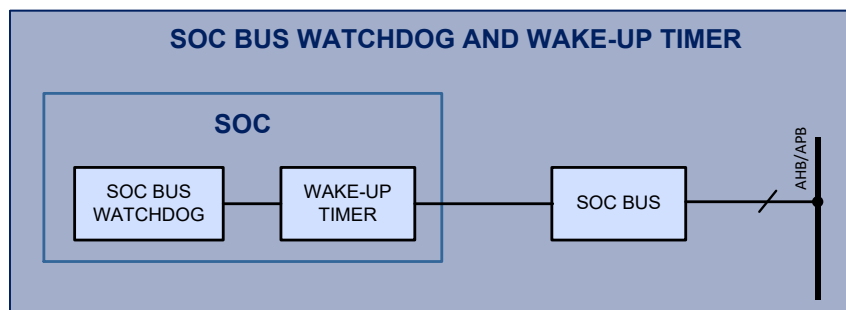
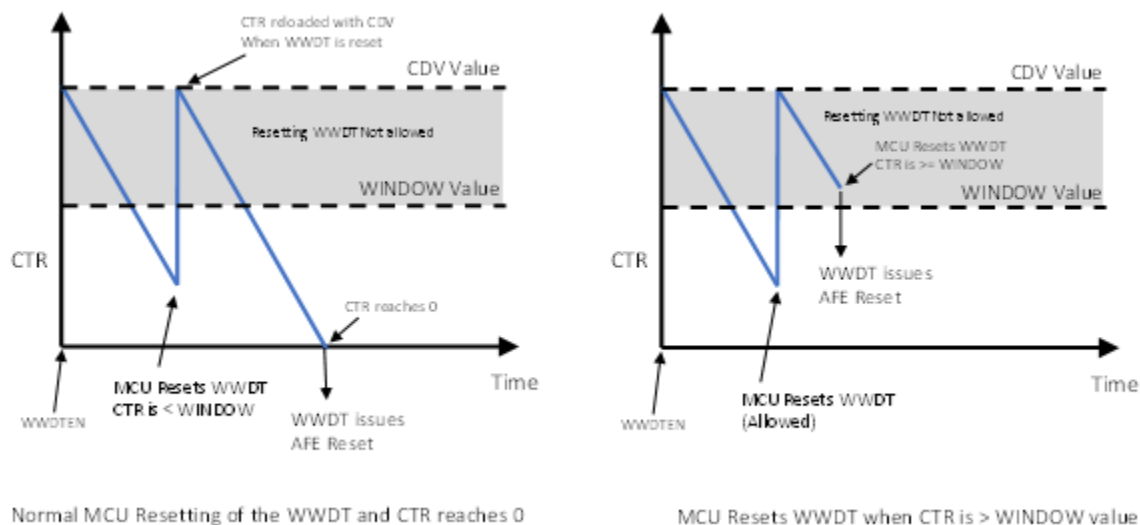


Figure 18 WWDT Operation

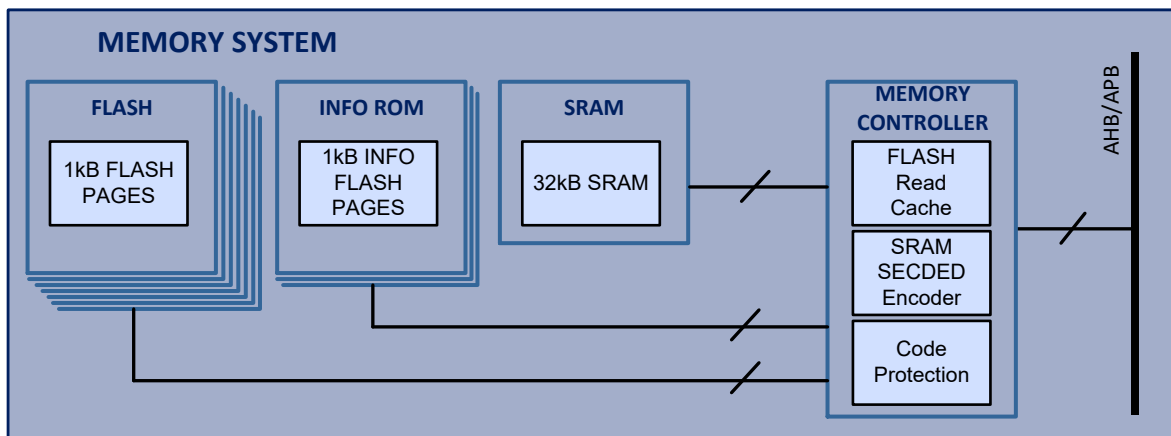


Features

- 128kB Embedded FLASH
 - ◆ 30,000 program/erase cycles
 - ◆ 10 years data retention
 - ◆ FLASH look-ahead buffer for optimizing access
- 1kB INFO-1 Embedded FLASH
- 1kB INFO-2 Embedded FLASH
 - ◆ Device ID, Unique ID, trim and manufacturing data
- 1kB INFO-3 Embedded FLASH
 - ◆ User data storage, configuration, or parameter storage
 - ◆ Data or code
- 32kB SRAM
 - ◆ 150MHz access for code or data
 - ◆ SECEDED for read/write operations
- User-configurable code protection

Block Diagram

Figure 19 Memory System Block Diagram



Functional Description

The PAC25140 has multiple banks of embedded FLASH memory, SRAM memory as well as peripheral control registers that are program-accessible in a flat memory map.



PAC2514x Data Sheet

Program FLASH

The PAC25140 Memory Controller provides access to 128 1kB pages of main program FLASH for a total of 128kB of FLASH through the system AHB bus. Each page may be individually erased or written while the MCU is executing instructions from SRAM.

The PAC25140 Memory Controller provides a FLASH read buffer that optimizes access from the MCU to the FLASH memory. This look ahead buffer monitors the program execution and fetches instructions from FLASH before they are needed to optimize access to this memory.

INFO FLASH

The PAC25140 Memory Controller provides access to the INFO-1, INFO-2 and INFO-3 FLASH memories, which are each a single 1kB page for a total of 3kB of memory.

INFO-1 and INFO-2 are read-only memories that contains device-specific information such as the device ID, a unique ID, trimming and calibration data that may be used by programs executing on the PAC25140.

INFO-3 is available to the user for data or program storage.

SRAM

The PAC25140 Memory Controller provides access to the 32kB SRAM for non-persistent data storage. The SRAM memory supports word (4B), half-word (2B) and byte addresses.

The PAC25140 Memory Controller can read or write data from RAM up to 150MHz. This can be a benefit for time-critical applications. This memory can also be used for program execution when modifying the contents of FLASH, INFO-1 or INFO-2 FLASH.

The PAC25140 Memory Controller also has an SECDDED encoder, capable of detecting and correcting single-bit errors, and detecting double-bit errors. The user may read the status of the encoder, to see if a single-bit error has occurred. The user may also enable an interrupt upon detection of single-bit errors. Dual-bit errors can be configured to generate an interrupt in the PAC25140.²

For more information on the PAC25140 Memory Controller, see the PAC55XX Family User Guide.

² Note that when writing half-word or single bytes to SRAM, the memory controller must perform a read-modify write to memory to perform the SECDDED calculation. These operations will take more than one clock cycle to perform for this reason.



PAC2514x Data Sheet

Code Protection

The PAC25140 allows user configurable code protection, to secure code from being read from the device.

There are four levels of code protection available as shown in the table below.

Table 17 Code Protection Level Description

| LEVEL | NAME | FEATURES |
|-------|-------------------------------|--|
| 0 | UNLOCKED | <ul style="list-style-type: none">● No restrictions |
| 1 | RW PROTECTION | <ul style="list-style-type: none">● SWD/JTAG enabled● Programmable protection of up to 128 regions of FLASH● User-specified Read or Write protection per region |
| 2 | SWD DISABLED | <ul style="list-style-type: none">● SWD/JTAG disabled● Programmable protection of up to 128 regions of FLASH● User-specified Read or Write protection per region |
| 3 | SWD/JTAG PERMANENTLY DISABLED | <ul style="list-style-type: none">● SWD/JTAG disabled● Programmable protection of up to 128 regions of FLASH● User-specified Read or Write protection per region● No recovery |



PAC2514x Data Sheet

Electrical Characteristics

Table 18 Memory System Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---------------------------|----------------------------|--|------|------|------|---------------|
| Embedded FLASH | | | | | | |
| $t_{\text{READ;FLASH}}$ | FLASH read time | | 40 | | | ns |
| $t_{\text{WRITE;FLASH}}$ | FLASH write time | | 30 | | | μs |
| $t_{\text{PERASE;FLASH}}$ | FLASH page erase time | | | | 2 | ms |
| $t_{\text{MERASE;FLASH}}$ | FLASH full erase time | | | | 10 | ms |
| $N_{\text{PERASE;FLASH}}$ | FLASH program/erase cycles | | 30k | | | cycles |
| $t_{\text{DR;FLASH}}$ | FLASH data retention | | 10 | | | years |
| SRAM | | | | | | |
| $t_{\text{ACC;SRAM}}$ | SRAM access cycle time | HCLK = 150MHz; Word (32-bits), aligned | 6.67 | | | ns |
| | | HCLK = 150MHz; Half-word (16-bits), byte (8-bits), aligned | 6.67 | | | ns |

TA = -40°C to 125°C unless otherwise specified.

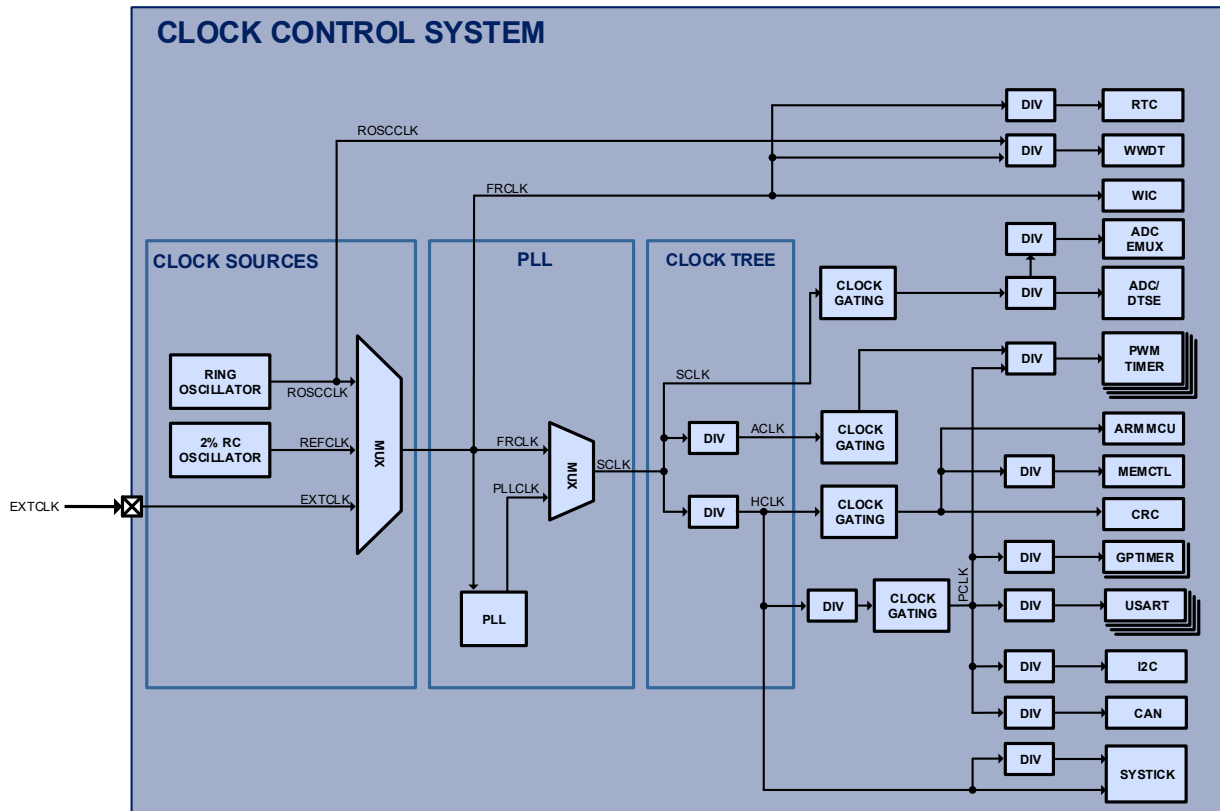
MCU Clock Control System (CCS)

Features

- 20MHz Ring Oscillator
- High accuracy 1.25% trimmed 4MHz RC oscillator
- External Clock Input for External Clocks up to 20MHz
- PLL with 1MHz to 50MHz input, 62.5MHz to 300MHz output
- Clock dividers for all system clocks
- Clock gating for power conservation during low-power operation

Block Diagram

Figure 20 CCS Block Diagram





PAC2514x Data Sheet

Functional Description

The Clock Control System (CCS) controls the clock system and clock gating for the PAC25140. There are three independent clock sources: the Ring Oscillator, Reference Clock and External Clock Input.

Clock Sources

Ring Oscillator

The Ring Oscillator (ROSC) is an integrated 20MHz clock oscillator that is the default system clock and is available by default when the PAC25140 comes out of reset. The output of the ROSC is the **ROSCCLK** clock. The **ROSCCLK** may be selected as the **FRCLK** clock and may supply the WWDT, for applications that need an independent clock source or need to continue to be clocked when the system is in a low-power mode.

The ROSC may be disabled by the user by a configuration register.

Reference Clock

The Reference Clock (**REFCLK**) is an integrated 1.25% trimmed 4MHz RC clock. This clock is suitable for many applications. This clock may be selected as the **FRCLK** and can be used as the input to the PLL and is used to derive the clock for the MPM.

External Clock Input

The External Clock Input (EXTCLK) is a clock input available through the digital peripheral MUX, and allows the drive the clock system by a 50% duty cycle clock of up to 20MHz. This clock may be selected as FRCLK and can be used as the input the PLL (as long as the accuracy is better than +/- 2%).

PLL

The PAC25140 contains a Phase Lock Loop (PLL) that can generate very high clock frequencies up to 300MHz for the peripherals and timers in the device. The input to the PLL is the **FRCLK** and must be from the **EXTCLK** or **REFCLK** clock sources

The input to the PLL must be between 1MHz – 50MHz and the output can be configured to be from 62.5MHz to 300MHz. The user can configure the PLL to generate the desired clock output based on a set of configuration registers in the CCS. The output of the PLL is the **PLLCLK** clock. The user may configure a MUX to generate the SCLK clock from **PLLCLK** or from **FRCLK**.

In addition to configuring the PLL output frequency, the PLL may be enabled, disabled and bypassed through a set of configuration registers in the CCS.

Clock Tree

The following are the system clocks available in the clock tree. See the section below to see which clocks are available for each of the digital peripherals in the system.

FRCLK

The free-running clock (**FRCLK**) is generated from one of the four clock sources (**ROSCCLK**, **EXTCLK** or **REFCLK**). This clock may be used by the WWDT and the RTC, for configurations that turn off all other system clocks during low power operation.

The **FRCLK** or **PLLCLK** is selected via a MUX and the output becomes **SCLK**.



PAC2514x Data Sheet

SCLK

The System Clock (**SCLK**) generates two system clocks: **ACLK** and **HCLK**. Each of these system clocks has their own 3b clock divider and is described below.

PCLK

The Peripheral Clock (**PCLK**) is used by most of the digital peripherals in the PAC25140. This clock has a 3b clock divider and also has clock gating support, which allows this clock output to be disabled before the system is put into the Arm® Cortex®-M4's deep sleep mode to conserve energy.

As shown above, most of the peripherals that use **PCLK** also have their own clock dividers so that this clock can be further divided down to meet the application's needs.

ACLK

The Auxiliary Clock (**ACLK**) may be optionally used by the PWM timer block in the PAC25140 in order to generate a very fast clock for PWM output to generate the best possible accuracy and edge generation.

This clock has a 3b clock divider and also has clock gating support, which disables this clock output when the system is put into the Arm® Cortex®-M4's deep sleep mode to conserve energy.

As shown above, the **ACLK** is an optional input for just the PWM timer block in the PAC25140.

HCLK

The AHB Clock (**HCLK**) is used by the Arm® Cortex®-M4 MCU and Memory Controller peripheral. This clock has a 3b divider and also has clock gating support, which allows this clock output to be disabled before the system is put into the Arm® Cortex®-M4's deep sleep mode to conserve energy.

HCLK supplies PCLK with its clock source.



PAC2514x Data Sheet

Electrical Characteristics

The Electrical Characteristics for the Clock Control System module are shown below.

Table 19 Clock Control System Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|--------|------|-------|-------|
| Clock Tree (FRCLK, FCLK, HCLK, PCLK, ACLK) | | | | | | |
| f _{FRCLK} | Free-running clock frequency | | | | 25 | MHz |
| f _{SCLK} | System clock frequency | | | | 300 | |
| f _{PCLK} | Peripheral clock frequency | After divider | | | 150 | |
| f _{ACLK} | Auxilliary clock frequency | After divider | | | 300 | |
| f _{HCLK} | High-speed clock frequency | After divider | | | 150 | |
| Internal Oscillators | | | | | | |
| f _{ROSCCLK} | Ring oscillator frequency | | | 20 | | MHz |
| f _{TRIM;REFCLK} | Trimmed RC oscillator frequency | T _A = 25°C | -1.25% | 4 | 1.25% | MHz |
| | | T _A = -40°C to 105°C | 2.25% | 4 | 2% | |
| f _{JITTER;REFCLK} | Trimmed RC oscillator clock jitter | T _A = -40°C to 85°C | | 0.5 | | % |
| PLL | | | | | | |
| f _{IN;PLL} | PLL input frequency range | | 1 | | 50 | MHz |
| f _{OUT;PLL} | PLL output frequency range | | 62.6 | | 300 | MHz |
| t _{SETTLE;PLL} | PLL settling time | T _A = 25°C, PLL settled | | | 15 | µs |
| | | T _A = 25°C, PLLLOCK = 1 | | 200 | 500 | µs |
| t _{JITTER;PLL} | PLL period jitter | RMS | | 25 | | ps |
| | | Peak to peak | | | 100 | ps |
| | PLL duty cycle | | 40 | 50 | 60 | % |
| External Clock Input | | | | | | |
| f _{EXTCLK} | External Clock Input Frequency | | | | 20 | MHz |
| | External Clock Input Duty Cycle | | 40 | | 60 | % |
| V _{IH;EXTCLK} | External Clock Input high-level input voltage | | 2.1 | | | V |
| V _{IL;EXTCLK} | External Clock Input low-level input voltage | | | | 0.825 | V |

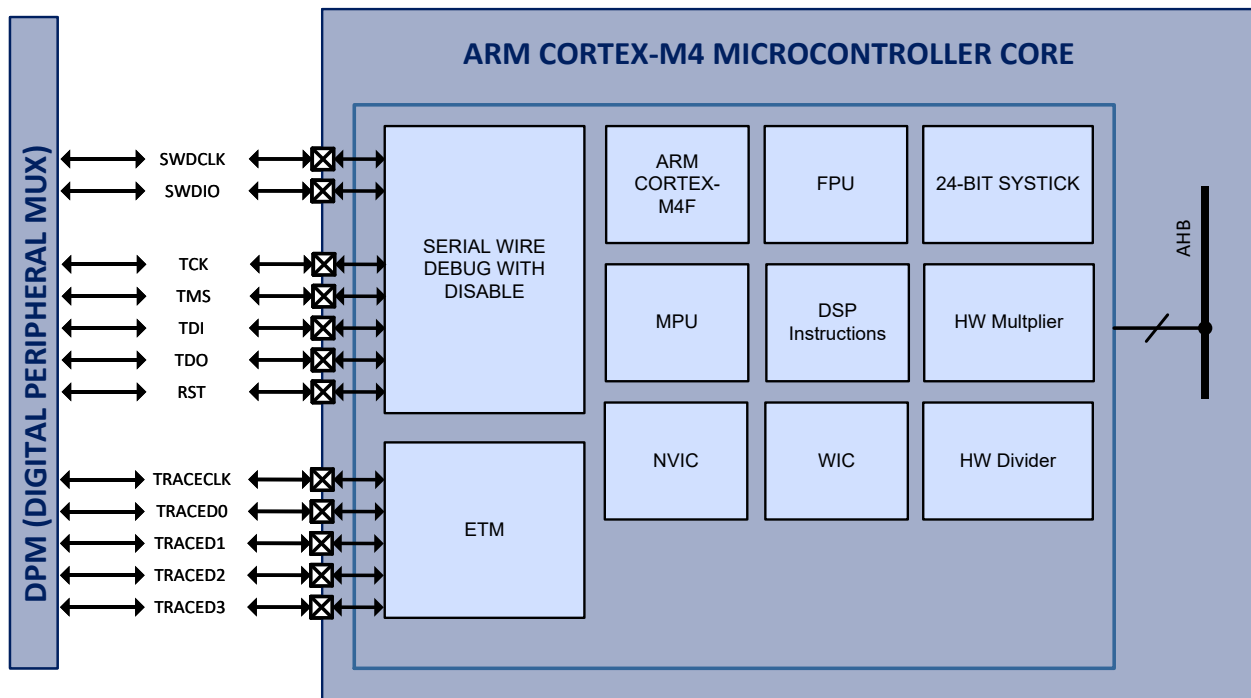
(T_A = -40°C to 125°C unless otherwise specified.)

Features

- Arm® Cortex®-M4F core
- SWD or JTAG Debug
- SWD/JTAG code security
- Embedded Trace Module (ETM) for instruction tracing
- Memory Protection Unit (MPU)
- Nested Vectored Interrupt Controller (NVIC) with 29 user interrupts and 8 levels of priority
- Floating Point Unit (FPU)
- Wakeup Interrupt Controller (WIC)
- 24-bit SysTick Count-down Timer
- Hardware Multiply and Divide Instructions

Block Diagram

Figure 21 Arm® Cortex®-M4F Microcontroller Core Block Diagram



Functional Description

The Arm® Cortex®-M4F microcontroller core is configured for little endian operation and includes hardware support for multiplication and division, DSP instructions as well as an IEEE754 single-precision Floating Point Unit (FPU).



PAC2514x Data Sheet

The MCU also contains an 8-region Memory Protection Unit (MPU), as well as a Nested Vector Interrupt Controller (NVIC) that supports 29 user interrupts with 8 levels of priority. There is a 24-bit SysTick count-down timer.

The Arm® Cortex®-M4F supports sleep and deep sleep modes for low power operation. In sleep mode, the Arm® Cortex®-M4F is disabled. In deep sleep mode, the MCU as well as many peripherals are disabled. The Wakeup Interrupt Controller (WIC) can wake up the MCU when in deep sleep mode by using any GPIO interrupt, the Real-Time Clock (RTC) or Windowed Watchdog Timer (WWDT). The PAC25140 also supports clock gating to reduce power during deep sleep operation.

The debugger supports 4 breakpoint and 2 watch-point unit comparators using the SWD or JTAG protocols. The debug serial interfaces may be disabled to prevent memory access to the firmware during customer production.

For more information on the detailed operation of the Microcontroller Core in the PAC25140, see the PAC55XX Family User Guide.



PAC2514x Data Sheet

Application Typical Current Consumption

The MCU clock configuration and peripheral configuration have a large influence on the amount of load that the power supplies in the PAC25140 will have.

The table below shows a few popular configurations and what the typical power consumption will be on the VSYS and VCORE power supplies in the PAC25140.

Table 20 PAC25140 Application Typical Current Consumption

| CLOCK CONFIGURATION | MCU PERIPHERALS | MCU STATE | I _{vsys} | I _{vcore} | I _{vcc33} | I _{vcc10} |
|--|--|-----------|-------------------|--------------------|--------------------|--------------------|
| CLKREF = 4MHz PLL Disabled ACLK=HCLK=PCLK=SCLK=MCLK = 16MHz ROSCCLK Enabled FRCLK MUX = ROSCCLK | All peripherals disabled | Halted | 9.5mA | 2.3mA | n/a | 0.5mA |
| CLKREF = 4MHz PLLCLK = 30MHz ACLK=HCLK=PCLK=SCLK= 16MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF | All peripherals disabled | Halted | 10.5mA | 3.5mA | n/a | 3mA |
| CLKREF = 4MHz PLLCLK = 150MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF | All peripherals disabled | Halted | 20mA | 13.5mA | n/a | 3mA |
| CLKREF = 4MHz PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF | All peripherals disabled | Halted | 22mA | 15mA | n/a | 3mA |
| CLKREF = 4MHz PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF ADCCLK = 40MHz | ADC enabled (repeated conversions) | Halted | 36mA | 16mA | 13.5mA | 3.5mA |
| CLKREF = 4MHz PLLCLK = 300MHz ACLK=HCLK=PCLK=SCLK= 150MHz MCLK = 30MHz ROSCCLK Enabled FRCLK MUX = CLKREF | Timer A enabled; TAPWM[7:0] enabled; Fs = 100kHz; 50% duty cycle | Halted | 22mA | 15mA | n/a | 3.5mA |



PAC2514x Data Sheet

Electrical Characteristics

Table 21 Microcontroller Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---------------------------------|--------------------------------------|---|------|------|------|-------|
| f _{HCLK} | MCU Clock | | | | 50 | MHz |
| I _{Q;V_{CO}RE} | V _{CO} RE quiescent current | Arm® Cortex®-M4F Sleep/Deep Sleep Modes | | | 2 | mA |
| | | Device Hibernate Mode | | | 0 | mA |
| I _{Q;V_SYS} | V _S YS quiescent current | Arm® Cortex®-M4F Sleep/Deep Sleep Modes | | | 8 | mA |
| | | Device Hibernate Mode | | | 15 | µA |
| I _{Q;V_{CC}IO} | V _{CC} IO quiescent current | Arm® Cortex®-M4F Sleep/Deep Sleep Modes | | | 0.15 | mA |
| | | Device Hibernate Mode | | | 0 | mA |
| I _{Q;V_{CC}33} | V _{CC} 33 quiescent current | Arm® Cortex®-M4F Sleep/Deep Sleep Modes | | | 0.4 | mA |
| | | Device Hibernate Mode | | | 0 | mA |

(T_A = -40°C to 125°C unless otherwise specified)

MCU IO Controller

Features

- 3.3V Input/Output, 4.6V input tolerant
- Push-Pull Output, Open-Drain Output or High-Impedance Input for each IO
- Configurable Pull-up and Pull-down for each IO (60k)
- Configurable Drive Strength for each IO (up to 24mA)
- Analog Input for some IOs
- Edge-sensitive or level-sensitive interrupts
- Rising edge, falling edge or both edge interrupts
- Peripheral MUX allowing up to 8 peripheral selections for each IO
- Configurable De-bouncing Circuit for each IO

System Block Diagram

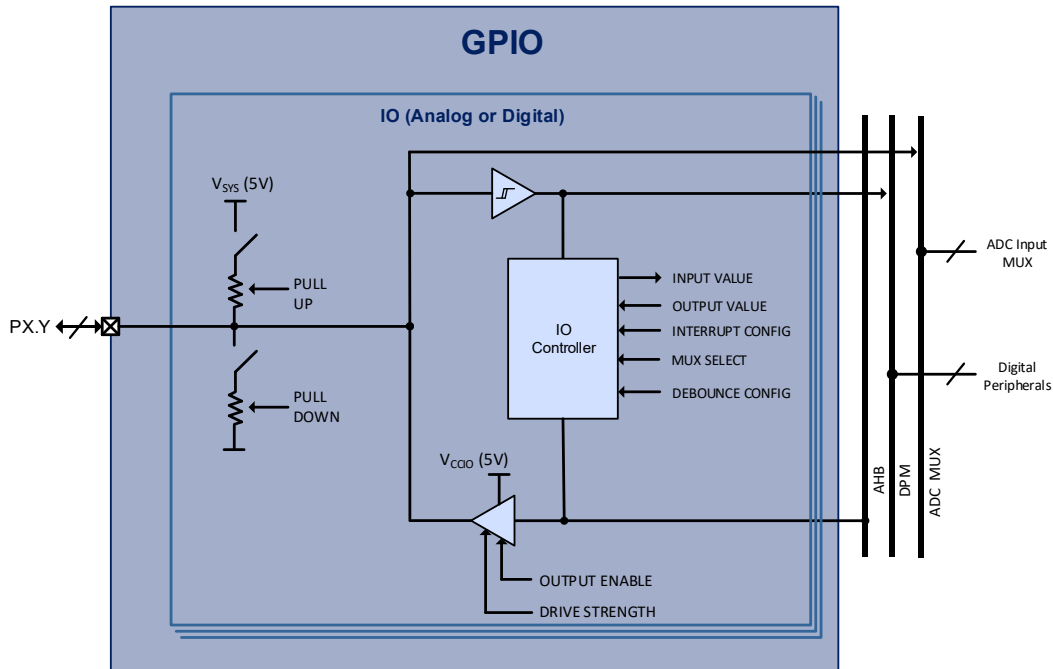


Figure 22 IO Controller System Block Diagram



PAC2514x Data Sheet

Functional Description

IO Controller

The PAC25140 IO cells can be used for digital input/output and analog input for the ADC. All IOs are supplied by the V_{CCIO} (3.3V) power supply.

Each IO can be configured for digital push-pull output, open-drain output or high-impedance input. Each IO also has a configurable 60k weak pull-up or weak pull-down that can be enabled.

NOTE: Configuring both pull-up and pull-down at the same time may cause device damage and should be avoided.

Each IO has a configurable de-bouncing filter that can be enabled or disabled, to help filter out noise.

All IO have interrupt capability. Each pin can be configured for either level or edge sensitive interrupts, and can select between rising edge, falling edge and both edges for interrupts. Each pin has a separate interrupt enable and interrupt flag.

Some of the IO on the PAC25140 can be configured as an analog input to the ADC.

GPIO Current Injection

Under normal operation, there should not be current injected into the GPIOs on the device due to the GPIO voltage below ground or above the GPIO supply (V_{CCIO}). Current will be injected into the GPIO when the GPIO pin voltage is less than $-0.3V$ or when greater than GPIO supply $+ 0.3V$.

In order provide a robust solution when this situation occurs, the PAC25140 family of products allows a small amount of injected current into the GPIO pins, to avoid excessive leakage or device damage.

For information on the GPIO current injection thresholds, see the absolute maximum parameters for this device.

Sustained operation with the GPIO pin voltage greater than the GPIO supply or when the GPIO pin voltage is less than $-0.3V$ may result in reduced lifetime of the device. GPIO current injection should only be a temporary condition.



PAC2514x Data Sheet

Peripheral MUX

The Peripheral MUX (DPM) allows the IO controller to select one of up to four peripheral functions for each IO pin. Note that if the pin is configured for analog input, the peripheral MUX is bypassed.

The Peripheral MUX for the PAC25140 is shown below.

Table 22 Peripheral MUX settings

| PIN | PERIPHERAL MUX SETTINGS | | | | | | | | ADC CH |
|-----|-------------------------|--------|--------|-----------|----------|---------|----------|----------|--------|
| | S0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | |
| PD0 | GPIOD0 | TBPWM0 | TCPWM0 | TDQEPIDX | | USCSCLK | CANTXD | EMUXD | AD4 |
| PD1 | GPIOD1 | TBPWM1 | TCPWM1 | TDQEPPHA | | USCSS | CANRXD | EMUXC | AD3 |
| PD2 | GPIOD2 | TBPWM2 | TCPWM2 | TDQEPPHB | | USCMOSI | | | AD2 |
| PD3 | GPIOD3 | TBPWM3 | TCPWM3 | | | USCMISO | FRCLK | TRACED3 | AD1 |
| PD4 | GPIOD4 | TBPWM4 | TCPWM4 | TDQEPIDX | TBQEPIDX | USDSCLK | TRACED3 | USDMOSI | |
| PD5 | GPIOD5 | TBPWM5 | TCPWM5 | TDQEPPHA | TBQEPPHA | USDSS | CANRXD | USDMISO | |
| PE0 | GPIOE0 | TCPWM4 | TDPWM0 | TAQEPIDX | TBQEPIDX | USCCLK | I2CSCL | EMUXC | |
| PE1 | GPIOE1 | TCPWM5 | TDPWM1 | TAQEPPHA | TBQEPPHA | USCSS | I2CSDA | EMUXD | |
| PE2 | GPIOE2 | TCPWM6 | TDPWM2 | TAQEPPHB | TBQEPPHB | USCMOSI | CANRXD | EXTCLK | |
| PE3 | GPIOE3 | TCPWM7 | TDPWM3 | FRCLK | | USCMISO | CANTXD | | |
| PF0 | GPIOF0 | TCPWM0 | TDPWM0 | TCK/SWDCL | TBQEPIDX | USBSCLK | TRACED2 | TRACECLK | |
| PF1 | GPIOF1 | TCPWM1 | TDPWM1 | TMS/SWDIO | TBQEPPHA | USBSS | TRACED1 | TRACED0 | |
| PF2 | GPIOF2 | TCPWM2 | TDPWM2 | TDI | TBQEPPHB | USBMOSI | TRACED0 | TRACED1 | |
| PF3 | GPIOF3 | TCPWM3 | TDPWM3 | TDO | FRCLK | USBMISO | TRACECLK | TRACED2 | |
| PF4 | GPIOF4 | TCPWM4 | TDPWM4 | | TCQEPIDX | USDSCLK | TRACED3 | EMUXC | AD4 |
| PF5 | GPIOF5 | TCPWM5 | TDPWM5 | | TCQEPPHA | USDSS | | EMUXD | AD5 |
| PF6 | GPIOF6 | TCPWM6 | TDPWM6 | | TCQEPPHB | USDMOSI | CANRXD | I2CSCL | AD6 |
| PF7 | GPIOF7 | TCPWM7 | TDPWM7 | | | USDMISO | CANTXD | I2CSDA | AD7 |
| PG0 | GPIOG0 | TCPWM0 | TDPWM0 | EMUXC | | USDSCLK | TRACECLK | TCQEPIDX | |
| PG1 | GPIOG1 | TCPWM1 | TDPWM1 | EMUXD | | USDSS | TRACED0 | TCQEPPHA | |
| PG2 | GPIOG2 | TCPWM2 | TDPWM2 | FRCLK | | USDMOSI | TRACED1 | TCQEPPHB | |
| PG3 | GPIOG3 | TCPWM3 | TDPWM3 | | | USDMISO | TRACED2 | | |



PAC2514x Data Sheet

Electrical Characteristics

The Electrical Characteristics for the IO Controller are shown below.

Table 23 IO Controller Electrical Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units | |
|-----------------------|---|--|-----------|------|-------|------------|----|
| V_{IH} | High-level input voltage | | 2.1 | | | V | |
| V_{IL} | Low-level input voltage | | | | 0.825 | V | |
| I_{OL} | Low-level output sink current (Limited by $I_{V_{SYS}}$ and $I_{V_{CCIO}}$) | $V_{OL} = 0.4V$ | DS = 6mA | 6 | | | mA |
| | | | DS = 8mA | 8 | | | |
| | | | DS = 11mA | 11 | | | |
| | | | DS = 14mA | 14 | | | |
| | | | DS = 17mA | 17 | | | |
| | | | DS = 20mA | 20 | | | |
| | | | DS = 22mA | 22 | | | |
| | | | DS = 25mA | 25 | | | |
| I_{OH} | High-level output source current (Limited by $I_{V_{SYS}}$ and $I_{V_{CCIO}}$) | $V_{OH} = 2.4V$ | DS = 6mA | | | -6 | mA |
| | | | DS = 8mA | | | -8 | |
| | | | DS = 11mA | | | -11 | |
| | | | DS = 14mA | | | -14 | |
| | | | DS = 17mA | | | -17 | |
| | | | DS = 20mA | | | -20 | |
| | | | DS = 22mA | | | -22 | |
| | | | DS = 25mA | | | -25 | |
| I_{IL} | Input leakage current | | -2 | | 0.95 | μA | |
| R_{PU} | Weak pull-up resistance | When pull-up enabled | 45 | 60 | 100 | k Ω | |
| R_{PD} | Weak pull-down resistance | When pull-down enabled | 45 | 60 | 115 | k Ω | |
| $I_{INJ;GPIO}$ | GPIO pin current injection | $V_{GPIO} < -0.3V$ or $V_{GPIO} > V_{CCIO} + 0.3V$ | -15 | | 15 | mA | |
| $\Sigma I_{INJ;GPIO}$ | Sum of all GPIO pin current injection | $V_{GPIO} < -0.3V$ or $V_{GPIO} > V_{CCIO} + 0.3V$ | -40 | | 40 | mA | |

TA = -40°C to 105°C unless otherwise specified

MCU Communication Interfaces

Features

- USART (UART or SPI master/slave)
- I2C master/slave
- CAN 2.0B controller

System Block Diagram

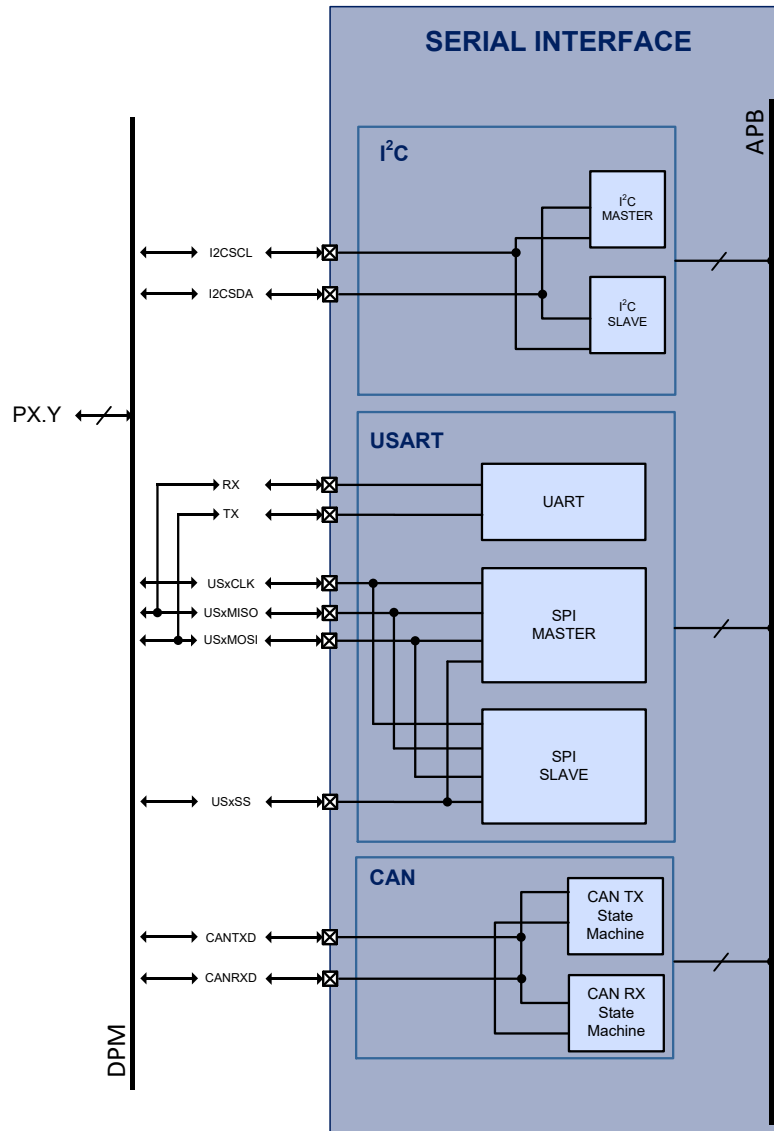


Figure 23 Serial Interfaces System Block Diagram

Functional Description

The PAC25140 has three types of serial interfaces: I²C, USART (SPI/UART) and CAN. The PAC25140 has one I²C controller, one CAN controller and up to 3 USARTs.



PAC2514x Data Sheet

I²C Controller

The PAC25140 contains one I²C controller. This is a configurable APB peripheral and the clock input is PCLK. This peripheral has an input clock divider that can be used to generate various master clock frequencies. The I²C controller can support various modes of operation:

- I²C master operation
 - Standard (100kHz), full-speed (400kHz), fast (1MHz) or high-speed modes (3.4MHz)
 - Single and multi-master
 - Synchronization (multi-master)
 - Arbitration (multi-master)
 - 7-bit or 10-bit slave addressing
- I²C slave operation
 - Standard (100kHz), full-speed (400kHz), fast (1MHz) or high-speed modes (3.4MHz)
 - Clock stretching
 - 7-bit or 10-bit slave addressing

The I²C peripheral may operate either by polling or can be configured to be interrupt driven for both receive and transmit operations.

USART

The PAC25140 contains up to 3 Universal Synchronous Receive Transmit (USART) peripherals. Each USART is a configurable APB bus client and input clock is PCLK. These peripherals have a configurable clock divider that can be used to produce various frequencies for the UART or SPI master peripheral.

The number of these peripherals depends on the peripheral MUX configuration. See the IO Controller section on information on how to configure the peripheral MUX with the USART peripheral.

The USART peripheral supports two main modes: SPI mode and UART mode.

USART SPI Mode

- Master or slave mode operation
- 8-bit, 16-bit or 32-bit word transfers
- Configurable clock polarity (active high or active low)
- Configurable data phase (setup/sample or sample/setup)
- Interrupts and status flags for RX and TX operations
- Support for up to 25MHz SPI clock

USART UART Mode

- 8-bit data
- Programmable data bit rate
- Maximum baud rate of 1Mbaud
- RX and TX FIFOs
- Configurable stop bits (1 or 2)
- Configurable parity: even, odd, none
 - Mark/space support for 9-bit addressing protocols
- Interrupt and status flags for RX and TX operations



PAC2514x Data Sheet

CAN

The PAC25140 contains one Controller Area Network (CAN) peripheral. The CAN peripheral is a configurable APB bus client and input clock is PCLK. This peripheral has a configurable clock divider that can be used to produce various frequencies for the CAN peripheral.

- CAN 2.0B support
- 1Mb/s data rate
- 64-byte receive FIFO
- 16-byte transmit buffer
- Standard and extended frame support
- Arbitration
- Overload frame generated on FIFO overflow
- Normal and Listen Only modes supported
- Interrupt and status flags for RX and TX operations



PAC2514x Data Sheet

Dynamic Characteristics

The Dynamic Characteristics for the Serial Interfaces on the PAC25140 are shown below.

Serial Interface

Table 24 Serial Interface Dynamic Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|--------------------------|--|-----------------------------------|-------|------|---------------|-------|
| I2C | | | | | | |
| f_{I2CCLK} | I ² C input clock frequency | Standard mode (100kHz) | 2.8 | | | MHz |
| | | Full-speed mode (400kHz) | 2.8 | | | MHz |
| | | Fast mode (1MHz) | 6.14 | | | MHz |
| | | High-speed mode (3.4MHz) | 20.88 | | | MHz |
| USART (UART mode) | | | | | | |
| $f_{UARTCLK}$ | USART input clock frequency | | | | $f_{PCLK}/16$ | MHz |
| $f_{UARTBAUD}$ | USART baud rate | $f_{USARTCLK} = 7.1825\text{MHz}$ | | | 1 | Mbps |
| USART (SPI mode) | | | | | | |
| f_{SPICLK} | USART input clock frequency | Master mode | | | 50 | MHz |
| | | Slave mode | | | 50 | MHz |
| $f_{USARTSPICLK}$ | USART SPI clock frequency | Master mode | | | 25 | MHz |
| | | Slave mode | | | 25 | MHz |
| CAN | | | | | | |
| f_{CANCLK} | CAN input clock frequency | | | | 50 | MHz |
| f_{CANTX} | CAN transmit clock frequency | | | | 1 | Mbps |
| f_{CANRX} | CAN receive clock frequency | | | | 1 | Mbps |



PAC2514x Data Sheet

I2C Dynamic Characteristics

Table 25 I2C Dynamic Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---------------------|--|--------------------------------|------|------|------|-------|
| f _{SCL} | SCL clock frequency | Standard mode | 0 | | 100 | kHz |
| | | Full-speed mode | 0 | | 400 | kHz |
| | | Fast mode | 0 | | 1 | MHz |
| t _{LOW} | SCL clock low | Standard mode | 4.7 | | | μs |
| | | Full-speed mode | 1.3 | | | μs |
| | | Fast mode | 0.5 | | | μs |
| t _{HIGH} | SCL clock high | Standard mode | 4.0 | | | μs |
| | | Full-speed mode | 0.6 | | | μs |
| | | Fast mode | 0.26 | | | μs |
| t _{HD;STA} | Hold time for a repeated START condition | Standard mode | 4.0 | | | μs |
| | | Full-speed mode | 0.6 | | | μs |
| | | Fast mode | 0.26 | | | μs |
| t _{SU;STA} | Set-up time for a repeated START condition | Standard mode | 4.7 | | | μs |
| | | Full-speed mode | 0.6 | | | μs |
| | | Fast mode | 0.26 | | | μs |
| t _{HD;DAT} | Data hold time | Standard mode | 0 | | 3.45 | μs |
| | | Full-speed mode | 0 | | 0.9 | μs |
| | | Fast mode | 0 | | | μs |
| t _{SU;DAT} | Data setup time | Standard mode | 250 | | | ns |
| | | Full-speed mode | 100 | | | ns |
| | | Fast mode | 50 | | | ns |
| t _{SU;STO} | Set-up time for STOP condition | Standard mode | 4.0 | | | μs |
| | | Full-speed mode | 0.6 | | | μs |
| | | Fast mode | 0.26 | | | μs |
| t _{BUF} | Bus free time between a STOP and START condition | Standard mode | 4.7 | | | μs |
| | | Full-speed mode | 1.3 | | | μs |
| | | Fast mode | 0.5 | | | μs |
| t _r | Rise time for SDA and SCL | Standard mode | | | 1000 | ns |
| | | Full-speed mode | 20 | | 300 | ns |
| | | Fast mode | | | 120 | ns |
| t _f | Fall time for SDA and SCL | Standard mode | | | 300 | ns |
| | | Full-speed mode | | | 300 | ns |
| | | Fast mode | | | 120 | ns |
| C _b | Capacitive load for each bus line | Standard mode, full-speed mode | | | 400 | pF |
| | | Fast mode | | | 550 | pF |

I2C Timing Diagram

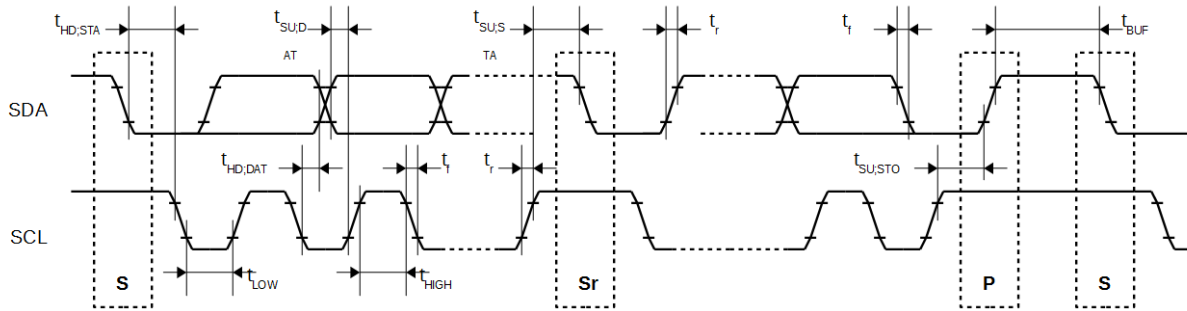


Figure 24 I2C Timing Diagram

MCU PWM Timers

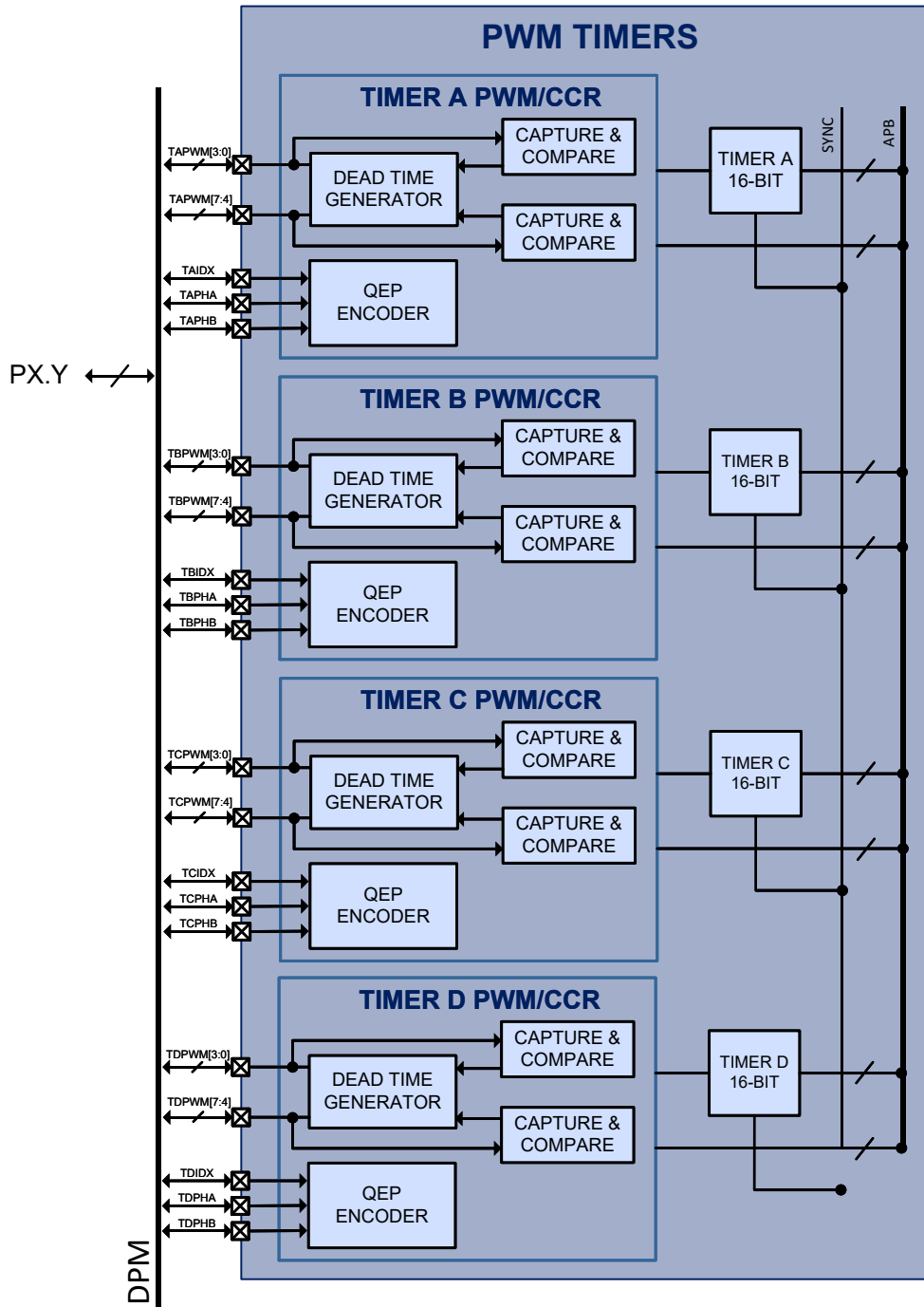
Features

- Base timer features:
 - Configurable input clock source: PCLK or ACLK
 - Up to 300MHz input clock
 - 3-bit Input clock divider
 - Timer counting modes
 - Up, up/down and asymmetric
 - Timer latch modes
 - Latch when counter = 0
 - Latch when counter = period
 - Latch when CCR value written
 - Latch all CCR values at same time
 - Base timer interrupts
 - Single shot or auto-reload
- CCR/PWM Timer
 - PWM output or capture input
 - CCR interrupt enable
 - CCR interrupt skips
 - SW force CCR interrupt
 - CCR interrupt type
 - Rising, falling or both
 - CCR compare latch modes
 - Latch when counter = 0
 - Latch when counter = period
 - Latch immediate
 - CCR capture latch modes
 - Latch on rising edge
 - Latch on falling edge
 - Latch on both rising and falling edges
 - Invert CCR output
 - CCR phase delay for phase shifted drive topologies
 - ADC trigger outputs
 - PWM rising edge or falling edge
- Dead-time Generators (DTG)
 - DTG enabled
 - 12-bit rising edge delay
 - 12-bit falling edge delay
- QEP Decoder
 - QEP encoder enabled
 - Direction status
 - Configurable Interrupts:
 - Phase A rising edge
 - Phase B rising edge
 - Index event
 - Counter wrap

- 4 different counting modes for best resolution, range and speed performance

PWM Timers System Block Diagram

Figure 25 PWM Timers System Block Diagram





PAC2514x Data Sheet

Functional Description

The PAC25140 contains four 16-bit timer units that may be used for PWM output and capture input. Each timer has a 16-bit time-base that may configure the counting style to up, up/down and up/down asymmetric modes. These modes can be used to support different drive topologies such as 120° trapezoidal and 180° sinusoidal.

Each base timer block may be clocked by either PCLK or ACLK. Configuring the timer to clock using ACLK allows higher PWM edge resolution by offering a clock that is up to 2X higher than the system clock. The base timer supports interrupts as well as single shot or auto-reload modes for maximum flexibility.

Each base timer has up to 8 CCR units that may be used for PWM output or capture input. When configured for PWM output, the user may configure a delay in order to support phase delay drive topologies. The CCR output may also be inverted in order to support full-bridge topologies.

The user may configure each CCR output rising or falling edge to interrupt the DTSE to begin a sequence of conversions.

MCU General Purpose Timers

Features

- SOC Bus Windowed Watchdog Timer
- Hibernate Wake-up Timer
- Real-Time Clock with Calendar and Alarm
- MCU Windowed Watchdog Timer (WWDT)
- 24-Bit General-purpose Timers

System Block Diagram

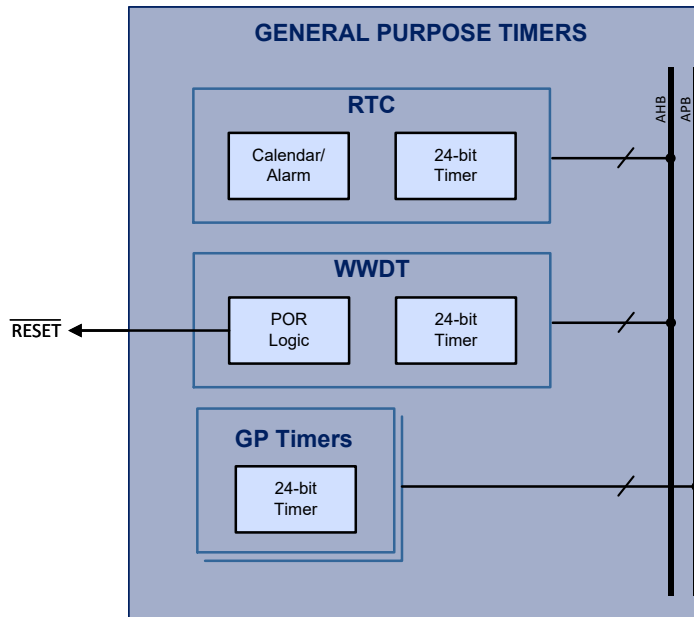


Figure 26 General-Purpose Timers System Block Diagrams



PAC2514x Data Sheet

Functional Description

Real-time Clock with Calendar (RTC)

The 24-bit real-time clock with calendar (RTC) is an AHB bus client and may also be used to measure long time periods and periodic wake up from sleep mode. It is reset if power is lost or hibernate mode.

The RTC uses FRCLK as its clock source and has a divider that can be configured up to a /65536 input clock divider. In order to count accurately, the input clock divider must be configured to generate a 1MHz clock to the RTC.

The RTC counts the time (seconds, minutes, hours, days) since enabled. It also allows the user to set a calendar date to set an alarm function that can be configured to generate an interrupt to the NVIC when it counts to that value.

MCU Windowed Watchdog Timer (WWDT)

The 16-bit windowed watchdog timer (WWDT) is an AHB bus client and can be used for long time period measurements or periodic wake up from sleep mode. Its primary use is to reset the MCU if it is not reset at a certain periodic interval.

The WWDT can be configured to use FRCLK or ROSCCLK as its clock source and has a divider that be configured up to a /65536 input clock divider.

The WWDT can be configured to allow only a small window when it is valid to reset the timer, to maximize application security and catch any stray code operating on the MCU.

The WWDT may be configured to enable an interrupt for the MCU, and the timer can be disabled when unused to save energy for low power operations.

GP Timer (GPT)

The PAC25140 contains two General Purpose (GP) Timers.

These timers are 24-bit timers and are both APB bus clients. These count-down timers use PCLK as their input clock and have a configurable divider of up to /32768. Each of the GPT can be configured to interrupt the MCU when they count down to 0.

Cyclic Redundancy Check (CRC)

Features

- 8-bit or 16-bit CRC
- User may select the polynomial through configuration:
 - CCITT CRC-16
 - IBM/ANSI CRC-16
 - Dallas/Maxim CRC-8
- Input data width: 8b or 32b
- Reflect input
- Reflect output
- Specify seed value

System Block Diagram

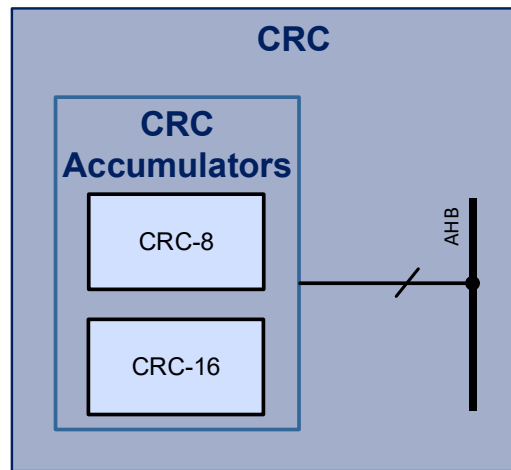


Figure 27 CRC System Block Diagram

Functional Description

The CRC peripheral can perform CRC calculation on data through registers from the MCU to accelerate the calculation or validation of a CRC for communications protocols or data integrity checks.

The CRC peripheral allows the calculation of both CRC-8 and CRC-16 on data. The CRC peripheral also allows the user to specify a seed value, select the data input to be 8b or 32b and to reflect the final output for firmware efficiency.

Application Block Diagrams

Figure 28 Application Block Diagram for 20s

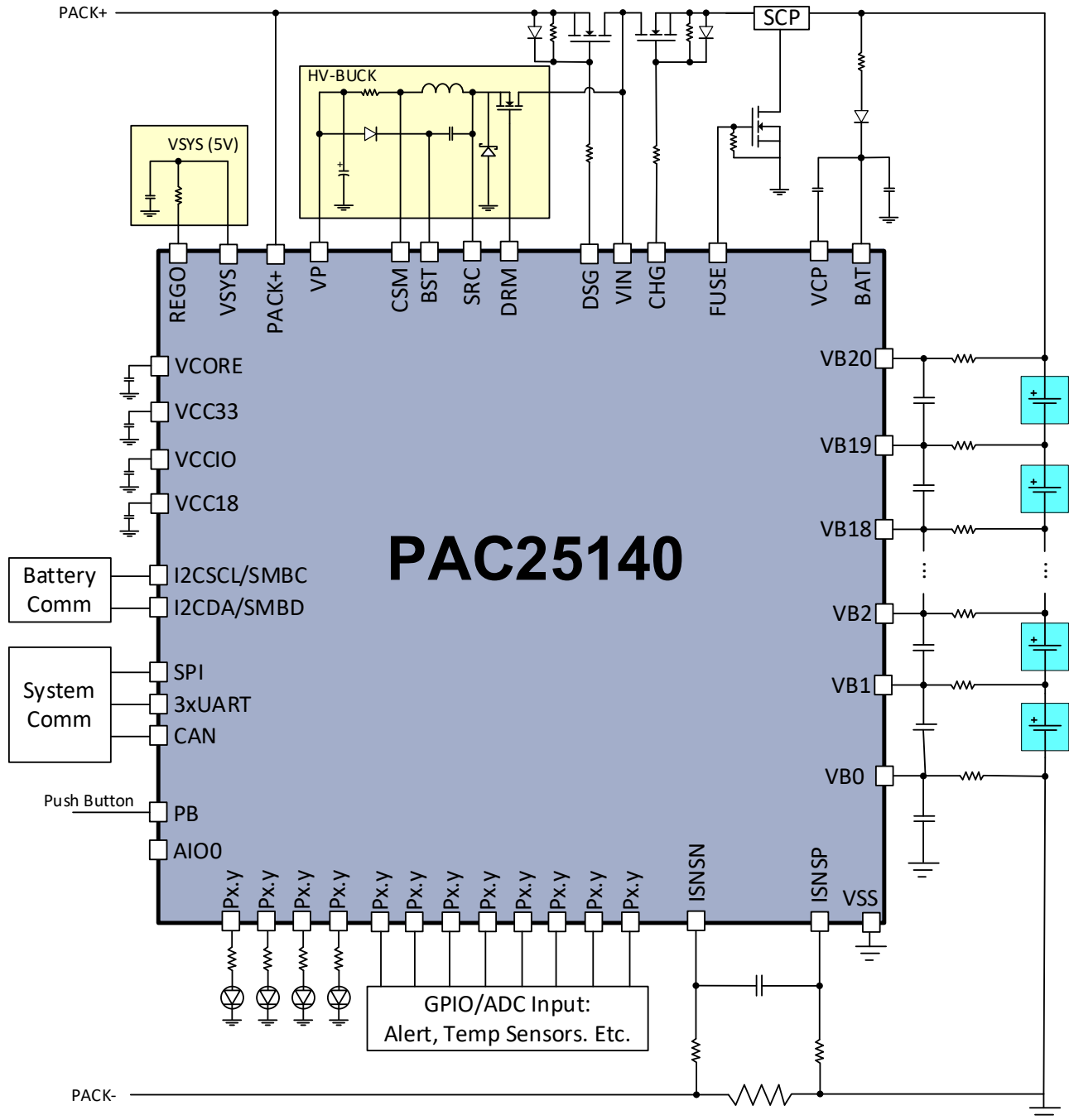
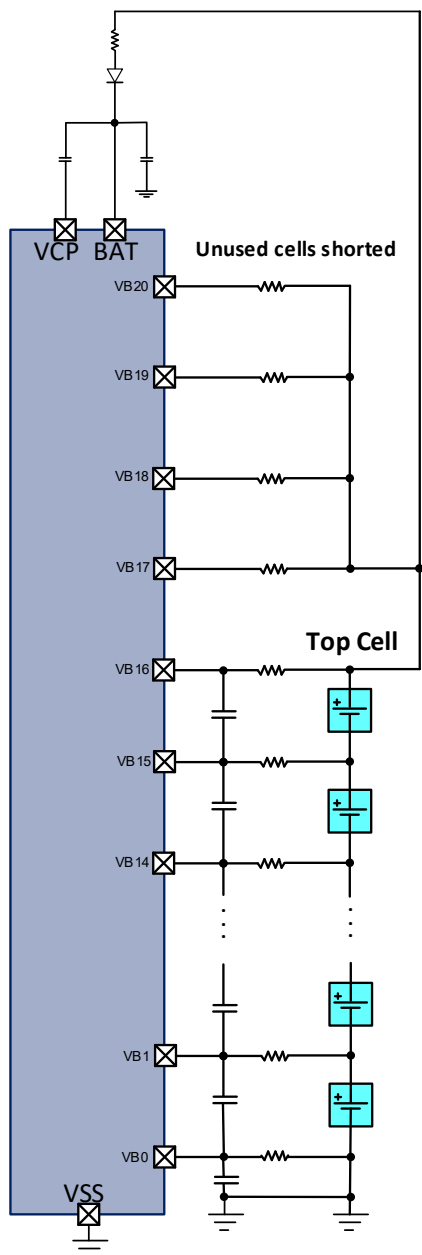


Figure 29 Unused Cell connection for 16s



The PAC25140 can monitor a 10-series to 20 series battery pack. In the actual application, the number of used cells may be less than 20 cells, in the figure above is a 16s example. When using less than 20 cells, the unused cells and corresponding VBx pins should be shorted together. The Top of the highest cell should be tied to the VBAT connection as shown.



PAC2514x Data Sheet

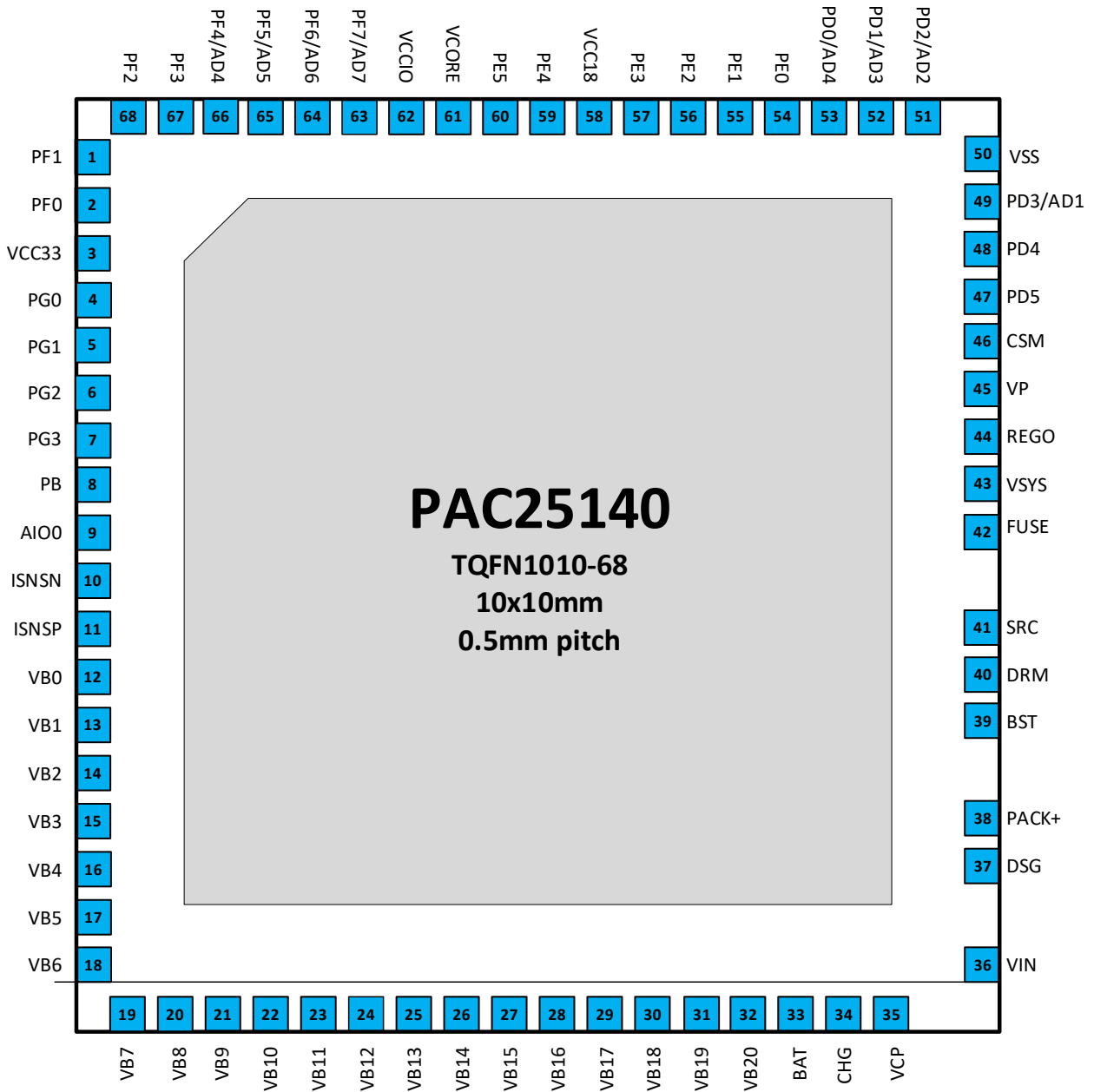
Thermal Characteristics

Table 26 Thermal Characteristics

| SYMBOL | PARAMETER | VALUE | UNIT |
|---------------|--|------------|------|
| T_A | Operating ambient temperature range | -40 to 125 | °C |
| T_J | Operating junction temperature range | -40 to 150 | °C |
| T_{STG} | Storage temperature range | -55 to 150 | °C |
| | Lead temperature (Soldering, 10 seconds) | 300 | °C |
| Θ_{JC} | Junction-to-case thermal resistance | 2.897 | °C/W |
| Θ_{JA} | Junction-to-ambient thermal resistance | 23.36 | °C/W |

PAC25140 Pin Configuration and Description

Figure 30 PAC25140 Pin Diagram – Top View





PAC2514x Data Sheet

Table 27 PAC25140 Pin Descriptions

| Pin Number | Label | Description |
|------------|-------|---|
| 1 | PF1 | IO port PF1 |
| 2 | PF0 | IO port PF0 |
| 3 | VCC33 | Internally generated 3.3V power supply. Connect to a 2.2 μ F or higher value ceramic capacitor from VCC33 to VSS |
| 4 | PG0 | IO port PG0 |
| 5 | PG1 | IO port PG1 |
| 6 | PG2 | IO port PG2 |
| 7 | PG3 | IO port PG3 |
| 8 | PB | Push Button Sense Input |
| 9 | AIO0 | Analog I/O |
| 10 | ISNSN | Current sense, negative terminal |
| 11 | ISNSP | Current sense, positive terminal |
| 12 | VB0 | Sense voltage input for the bottom of the battery stack |
| 13 | VB1 | Sense voltage input for the 1 st cell in the battery stack |
| 14 | VB2 | Sense voltage input for the 2 nd cell in the battery stack |
| 15 | VB3 | Sense voltage input for the 3 rd cell in the battery stack |
| 16 | VB4 | Sense voltage input for the 4 th cell in the battery stack |
| 17 | VB5 | Sense voltage input for the 5 th cell in the battery stack |
| 18 | VB6 | Sense voltage input for the 6 th cell in the battery stack |
| 19 | VB7 | Sense voltage input for the 7 th cell in the battery stack |
| 20 | VB8 | Sense voltage input for the 8 th cell in the battery stack |
| 21 | VB9 | Sense voltage input for the 9 th cell in the battery stack |
| 22 | VB10 | Sense voltage input for the 10 th cell in the battery stack |
| 23 | VB11 | Sense voltage input for the 11 th cell in the battery stack |
| 24 | VB12 | Sense voltage input for the 12 th cell in the battery stack |
| 25 | VB13 | Sense voltage input for the 13 th cell in the battery stack |
| 26 | VB14 | Sense voltage input for the 14 th cell in the battery stack |
| 27 | VB15 | Sense voltage input for the 15 th cell in the battery stack |
| 28 | VB16 | Sense voltage input for the 16 th cell in the battery stack |
| 29 | VB17 | Sense voltage input for the 17 th cell in the battery stack |
| 30 | VB18 | Sense voltage input for the 18 th cell in the battery stack |
| 31 | VB19 | Sense voltage input for the 19 th cell in the battery stack |
| 32 | VB20 | Sense voltage input for the 20 th cell in the battery stack |
| 33 | BAT | Battery Stack Voltage, Connect to the top of the battery stack. |
| 34 | CHG | Charge FET gate drive output |
| 35 | VCP | High-Voltage Charge Pump output. Connect a 0.47 μ F VP rated capacitor between VCP and VIN close to the device. |
| 36 | VIN | High-Voltage Buck Regulator supply controller input. Connect a 1 μ F 200V or higher value ceramic capacitor, and a 0.1 μ F 200V ceramic capacitor and in parallel with a 22 μ F 200V or higher electrolytic capacitor from VIN to VSS. This pin requires good capacitive bypass to VSS, so the ceramic capacitor must have a trace less than 10mm from the pin. |
| 37 | DSG | Discharge FET gate drive output |



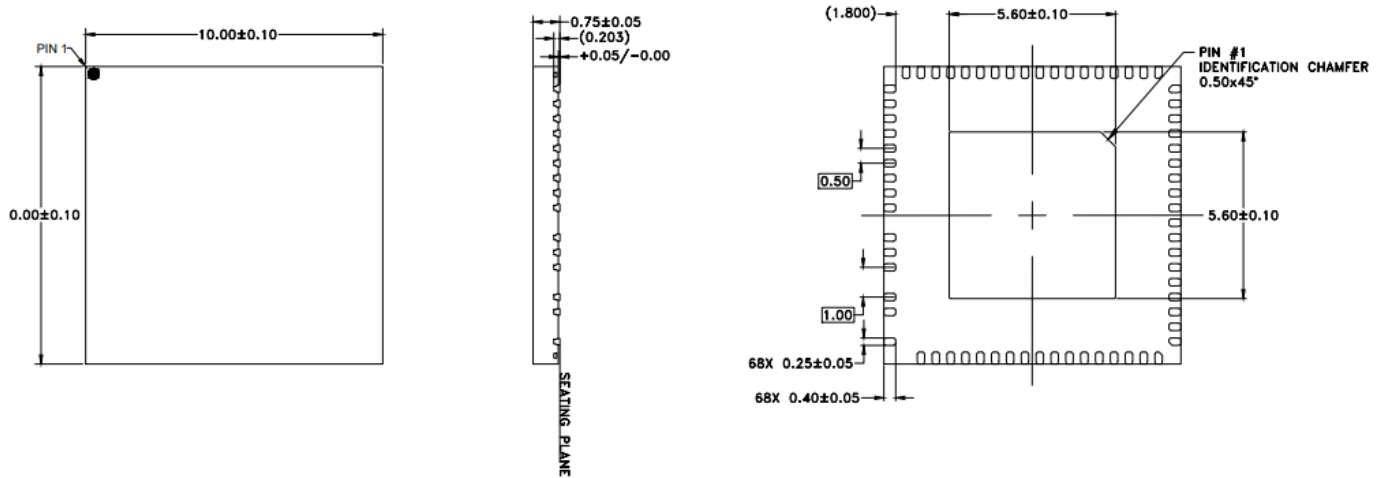
PAC2514x Data Sheet

| Pin Number | Label | Description |
|------------|---------|---|
| 38 | PACK+ | Battery Pack Positive Output. Connect to the positive terminal of the battery charger supply or load. |
| 39 | BST | High-Voltage Buck Regulator bootstrap input, Connect a 2.2 μ F or higher value ceramic capacitor from BST to SRC with a shorter than 10mm trace from the pin. |
| 40 | DRM | High-Voltage Buck Regulator Switching supply driver output, Connect to the base or gate of the external N-channel MOSFET. |
| 41 | SRC | High-Voltage Buck Regulator Source, Connect to the source of the high-side power MOSFET of the high-voltage buck regulator. |
| 42 | FUSE | FUSE/Low Side FET gate drive output |
| 43 | VSYS | Internally generated 5V power supply. Connect to a 10V/4.7 μ F ceramic capacitor from VSYS to VSS close to the device |
| 44 | REGO | VSYS regulator output |
| 45 | VP | Main power supply. Provides power to the power drivers as well as voltage feedback path for the switching supply. Connect a properly sized supply bypass capacitor in parallel with a 10 μ F ceramic capacitor in parallel with a 100 μ F aluminum capacitor from VP to VSS for voltage loop stabilization. If the switching frequency of the HV-BUCK is \geq 200kHz, then the 100 μ F aluminum capacitor can be replaced with 47 μ F, but the efficiency will be worse. This pin requires good capacitive bypass to VSS, so the ceramic capacitor must have a trace less than 10mm from the pin. |
| 46 | CSM | High-Voltage Buck Regulator Switching supply current sense input, Connect to the positive side of the current sense resistor |
| 47 | PD5 | IO port PD5 |
| 48 | PD4 | IO port PD4 |
| 49 | PD3/AD1 | IO port PD3 or ADC channel AD1 |
| 50 | VSS | Ground, shorted to Exposed Pad |
| 51 | PD2/AD2 | IO port PD2 or ADC channel AD2 |
| 52 | PD1/AD3 | IO port PD1 or ADC channel AD3 |
| 53 | PD0/AD4 | IO port PD0 or ADC channel AD4 |
| 54 | PE0 | IO port PE0 |
| 55 | PE1 | IO port PE1 |
| 56 | PE2 | IO port PE2 |
| 57 | PE3 | IO port PE3 |
| 58 | VCC18 | Internally generated 1.8V power supply. Connect a 2.2 μ F value ceramic capacitor from VCC18 to VSS. No external load allowed. |
| 59 | PE4 | IO port PE4 |
| 60 | PE5 | IO port PE5 |
| 61 | VCORE | Internally generated 1.2V core power supply. Connect a 2.2 μ F or higher value ceramic capacitor from VCORE to VSS |
| 62 | VCCIO | Internally generated digital I/O 3.3V power supply. Connect a 2.2 μ F or higher value ceramic capacitor from VCCIO to VSS |
| 63 | PF7/AD7 | IO port PF7 or ADC channel AD7 |
| 64 | PF6/AD6 | IO port PF6 or ADC channel AD6 |
| 65 | PF5/AD5 | IO port PF5 or ADC channel AD5 |
| 66 | PF4/AD4 | IO port PF4 or ADC channel AD4 |
| 67 | PF3 | IO port PF3 |
| 68 | PF2 | IO port PF2 |



PAC2514x Data Sheet

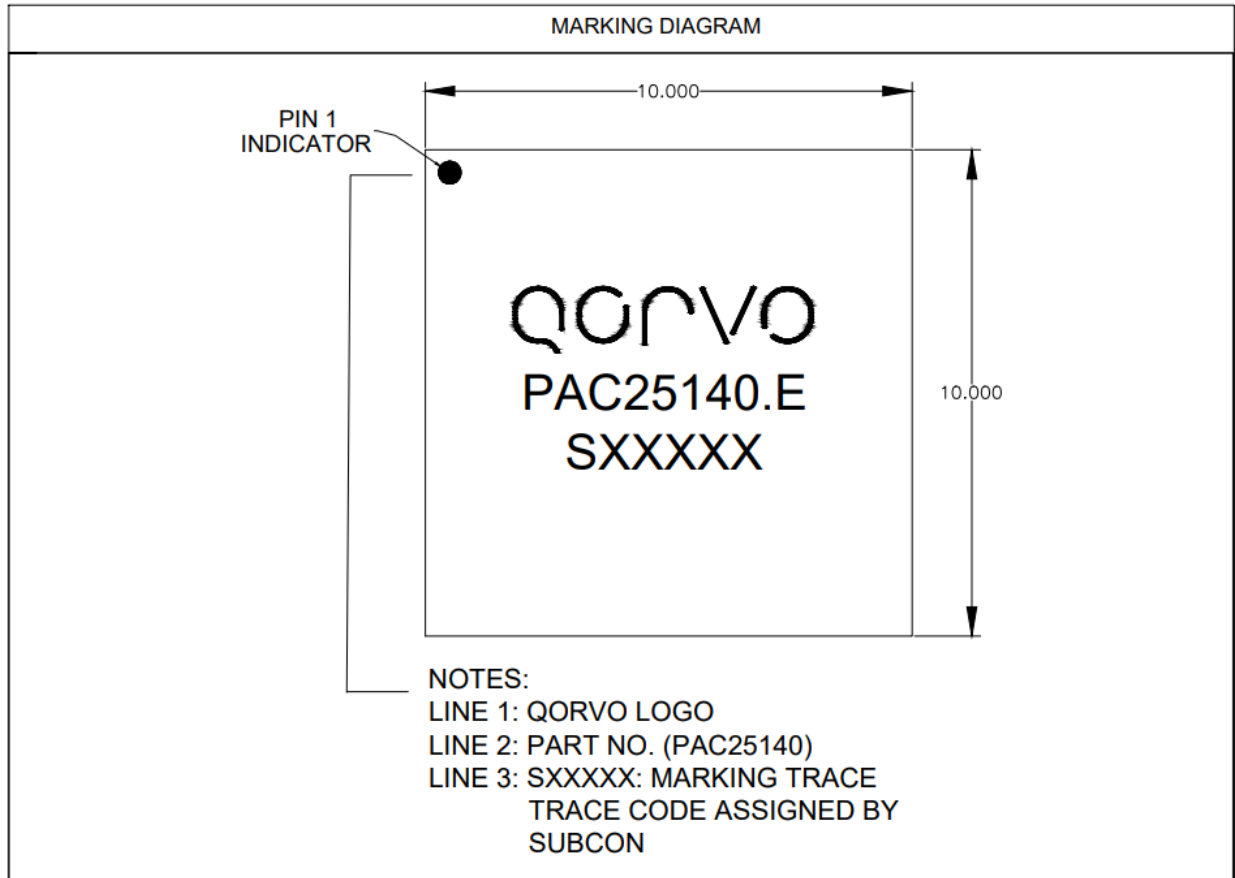
PAC25140 Mechanical Information



Notes:

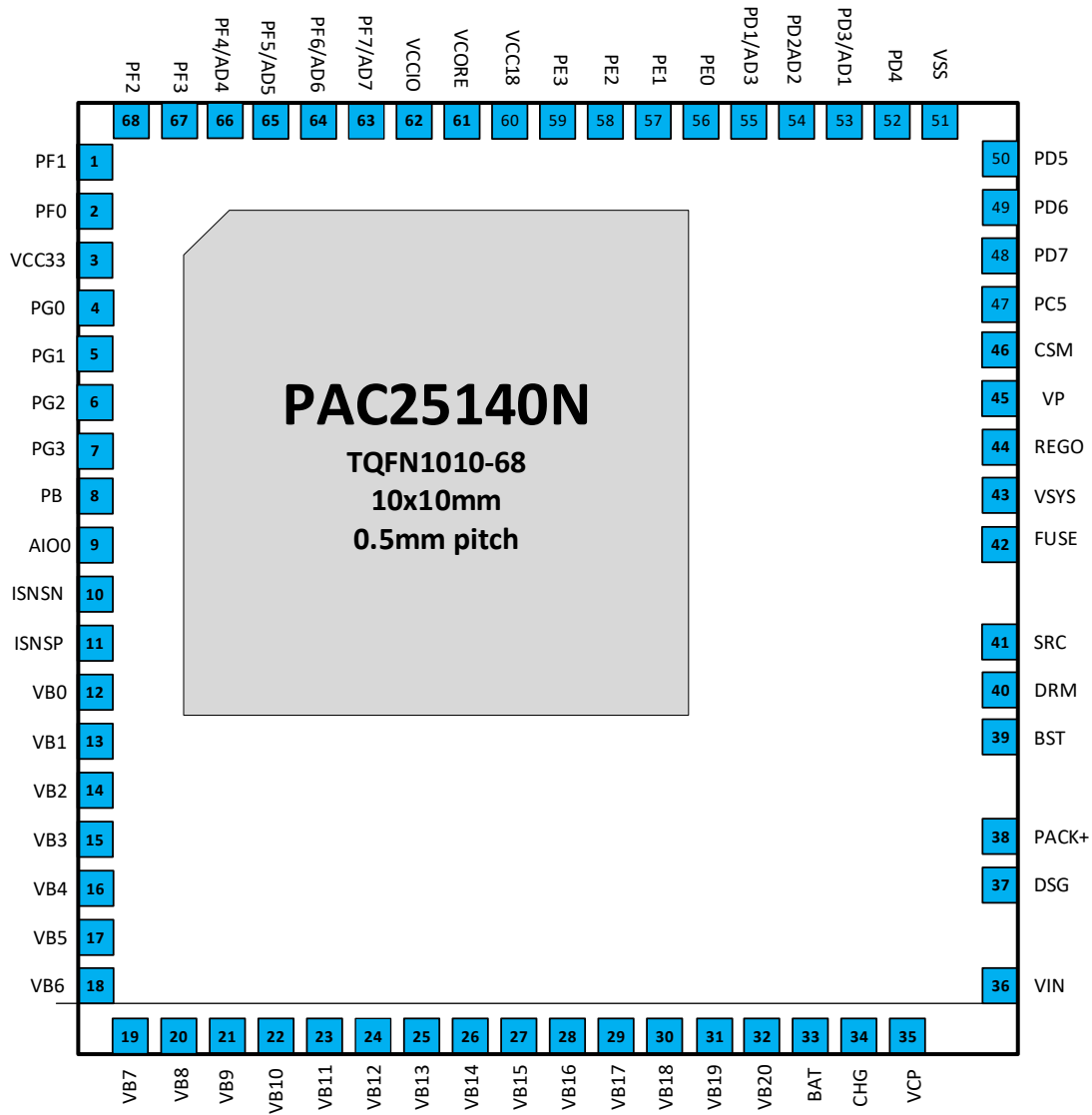
1. All dimensions are in mm. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PAC25140 Package Marking



PAC25140N Pin Configuration and Description

Figure 31 PAC25140N Pin Diagram – Top View





PAC2514x Data Sheet

Table 28 PAC25140N Pin Descriptions

| PIN NUMBER | LABEL | DESCRIPTION |
|------------|-------|---|
| 1 | PF1 | IO port PF1 |
| 2 | PF0 | IO port PF0 |
| 3 | VCC33 | Internally generated 3.3V power supply. Connect to a 2.2 μ F or higher value ceramic capacitor from VCC33 to VSS |
| 4 | PG0 | IO port PG0 |
| 5 | PG1 | IO port PG1 |
| 6 | PG2 | IO port PG2 |
| 7 | PG3 | IO port PG3 |
| 8 | PB | Push Button Sense Input |
| 9 | AIO0 | Analog I/O |
| 10 | ISNSN | Current sense, negative terminal |
| 11 | ISNSP | Current sense, positive terminal |
| 12 | VB0 | Sense voltage input for the bottom of the battery stack |
| 13 | VB1 | Sense voltage input for the 1 st cell in the battery stack |
| 14 | VB2 | Sense voltage input for the 2 nd cell in the battery stack |
| 15 | VB3 | Sense voltage input for the 3 rd cell in the battery stack |
| 16 | VB4 | Sense voltage input for the 4 th cell in the battery stack |
| 17 | VB5 | Sense voltage input for the 5 th cell in the battery stack |
| 18 | VB6 | Sense voltage input for the 6 th cell in the battery stack |
| 19 | VB7 | Sense voltage input for the 7 th cell in the battery stack |
| 20 | VB8 | Sense voltage input for the 8 th cell in the battery stack |
| 21 | VB9 | Sense voltage input for the 9 th cell in the battery stack |
| 22 | VB10 | Sense voltage input for the 10 th cell in the battery stack |
| 23 | VB11 | Sense voltage input for the 11 th cell in the battery stack |
| 24 | VB12 | Sense voltage input for the 12 th cell in the battery stack |
| 25 | VB13 | Sense voltage input for the 13 th cell in the battery stack |
| 26 | VB14 | Sense voltage input for the 14 th cell in the battery stack |
| 27 | VB15 | Sense voltage input for the 15 th cell in the battery stack |
| 28 | VB16 | Sense voltage input for the 16 th cell in the battery stack |
| 29 | VB17 | Sense voltage input for the 17 th cell in the battery stack |
| 30 | VB18 | Sense voltage input for the 18 th cell in the battery stack |
| 31 | VB19 | Sense voltage input for the 19 th cell in the battery stack |
| 32 | VB20 | Sense voltage input for the 20 th cell in the battery stack |
| 33 | BAT | Battery Stack Voltage, Connect to the top of the battery stack. |
| 34 | CHG | Charge FET gate drive output |
| 35 | VCP | High-Voltage Charge Pump output. Connect a 0.47 μ F VP rated capacitor between VCP and VIN close to the device. |
| 36 | VIN | High-Voltage Buck Regulator supply controller input. Connect a 1 μ F 200V or higher value ceramic capacitor, and a 0.1 μ F 200V ceramic capacitor and in parallel with a 22 μ F 200V or higher electrolytic capacitor from VIN to VSS. This pin requires good capacitive bypass to VSS, so the ceramic capacitor must have a trace less than 10mm from the pin. |
| 37 | DSG | Discharge FET gate drive output |
| 38 | PACK+ | Battery Pack Positive Output. Connect to the positive terminal of the battery charger supply or load. |



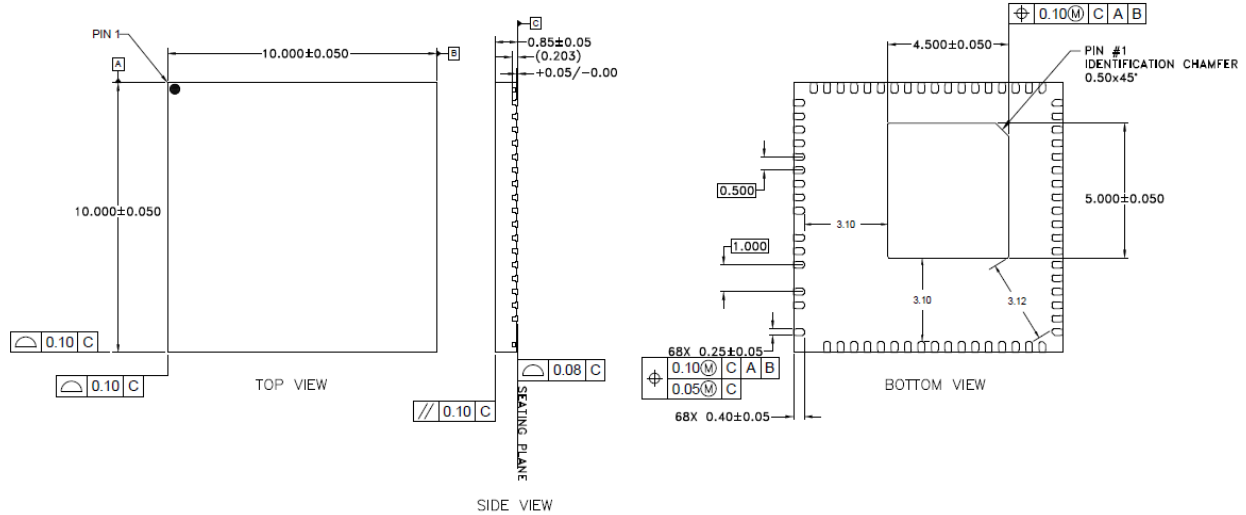
PAC2514x Data Sheet

| PIN NUMBER | LABEL | DESCRIPTION |
|------------|---------|---|
| 39 | BST | High-Voltage Buck Regulator bootstrap input. Connect a 2.2 μ F or higher value ceramic capacitor from BST to SRC with a shorter than 10mm trace from the pin. |
| 40 | DRM | High-Voltage Buck Regulator Switching supply driver output. Connect to the base or gate of the external N-channel MOSFET. |
| 41 | SRC | High-Voltage Buck Regulator Source. Connect to the source of the high-side power MOSFET of the high-voltage buck regulator. |
| 42 | FUSE | FUSE/Low Side FET gate drive output |
| 43 | VSYS | Internally generated 5V power supply. Connect to a 10V/4.7 μ F ceramic capacitor from VSYS to VSS close to the device |
| 44 | REGO | VSYS regulator output |
| 45 | VP | Main power supply. Provides power to the power drivers as well as voltage feedback path for the switching supply. Connect a properly sized supply bypass capacitor in parallel with a 10 μ F ceramic capacitor in parallel with a 100 μ F aluminum capacitor from VP to VSS for voltage loop stabilization. If the switching frequency of the HV-BUCK is \geq 200kHz, then the 100 μ F aluminum capacitor can be replaced with 47 μ F, but the efficiency will be worse. This pin requires good capacitive bypass to VSS, so the ceramic capacitor must have a trace less than 10mm from the pin. |
| 46 | CSM | High-Voltage Buck Regulator Switching supply current sense input, Connect to the positive side of the current sense resistor |
| 47 | PC5 | IO port PC5 |
| 48 | PD7 | IO port PD7 |
| 49 | PD6 | IO port PD6 |
| 50 | PD5 | IO port PD5 |
| 51 | VSS | Ground, shorted to Exposed Pad |
| 52 | PD4 | IO port PD4 |
| 53 | PD3/AD1 | IO port PD3 or ADC channel AD1 |
| 54 | PD2/AD2 | IO port PD2 or ADC channel AD2 |
| 55 | PD1/AD3 | IO port PD1 or ADC channel AD3 |
| 56 | PE0 | IO port PE0 |
| 57 | PE1 | IO port PE1 |
| 58 | PE2 | IO port PE2 |
| 59 | PE3 | IO port PE3 |
| 60 | VCC18 | Internally generated 1.8V power supply. Connect a 2.2 μ F value ceramic capacitor from VCC18 to VSS. No external load allowed. |
| 61 | VCORE | Internally generated 1.2V core power supply. Connect a 2.2 μ F or higher value ceramic capacitor from VCORE to VSS |
| 62 | VCCIO | Internally generated digital I/O 3.3V power supply. Connect a 2.2 μ F or higher value ceramic capacitor from VCCIO to VSS |
| 63 | PF7/AD7 | IO port PF7 or ADC channel AD7 |
| 64 | PF6/AD6 | IO port PF6 or ADC channel AD6. |
| 65 | PF5/AD5 | IO port PF5 or ADC channel AD5. |
| 66 | PF4/AD4 | IO port PF4 or ADC channel AD4. |
| 67 | PF3 | IO port PF3 |
| 68 | PF2 | IO port PF2 |



PAC2514x Data Sheet

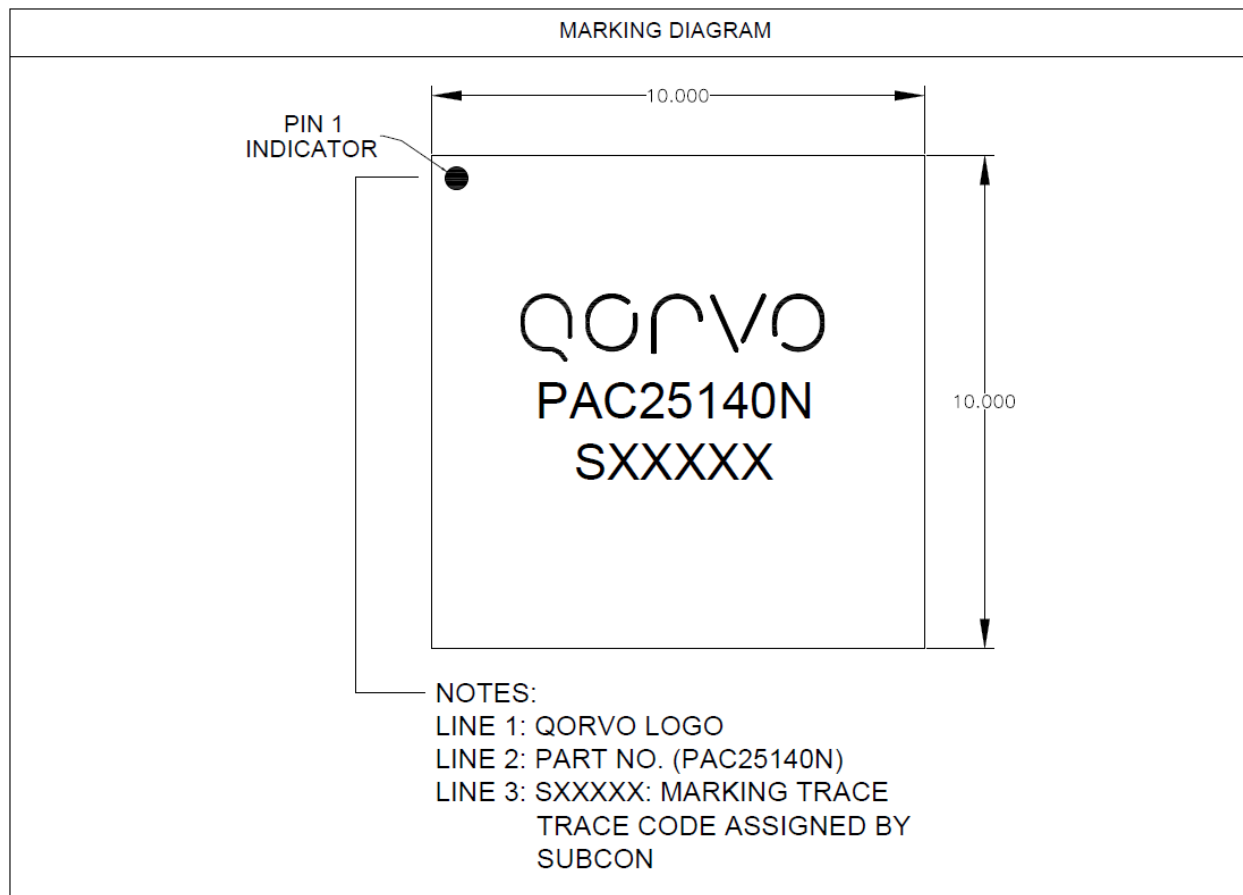
PAC25140N Mechanical Information



Notes:

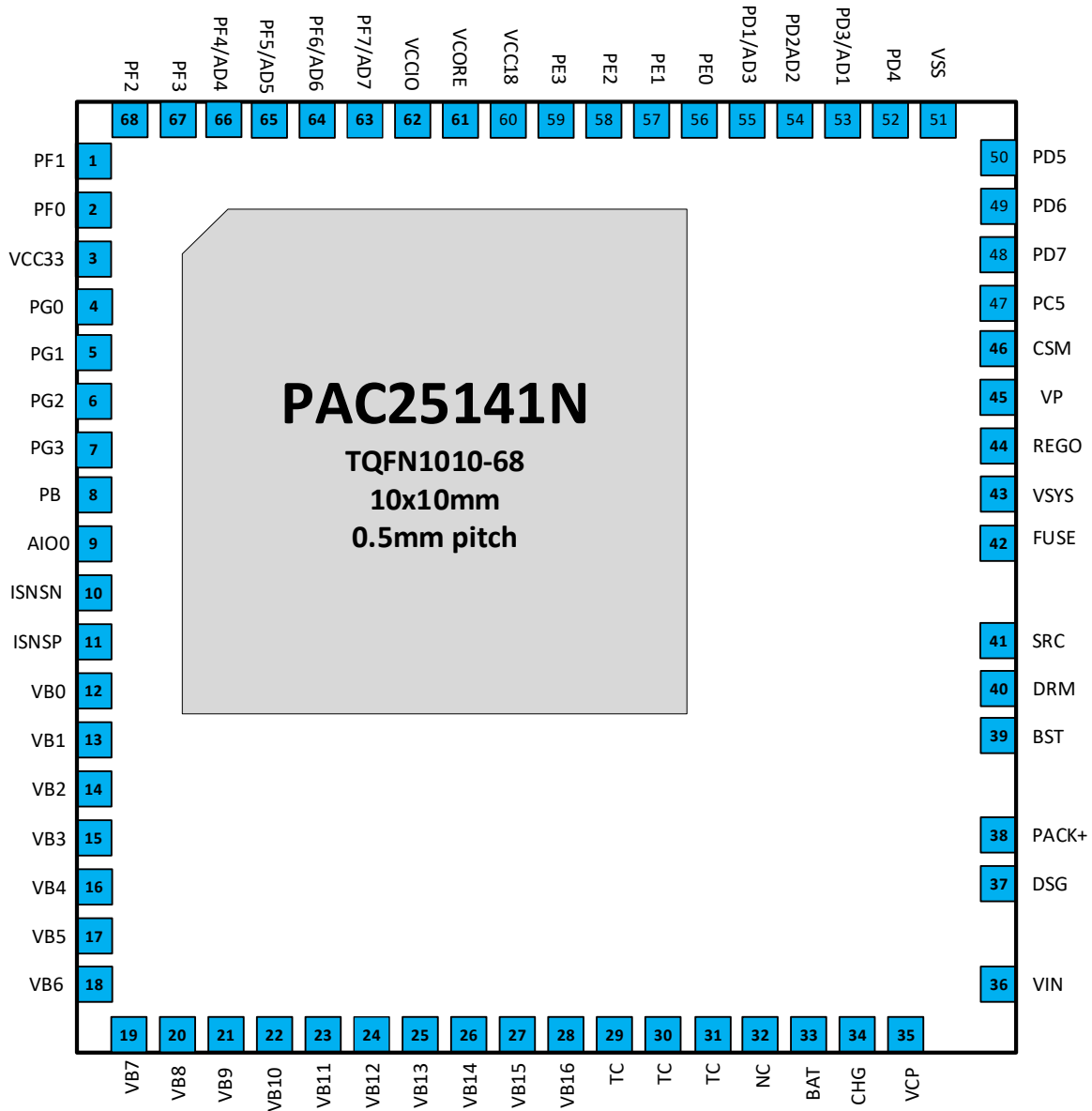
1. All dimensions are in mm. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PAC25140N Package Marking



PAC25141N Pin Configuration and Description

Figure 32 PAC25141N Pin Diagram – Top View





PAC2514x Data Sheet

Table 29 PAC25140N Pin Descriptions

| PIN NUMBER | LABEL | DESCRIPTION |
|------------|-------|---|
| 1 | PF1 | IO port PF1 |
| 2 | PF0 | IO port PF0 |
| 3 | VCC33 | Internally generated 3.3V power supply. Connect to a 2.2 μ F or higher value ceramic capacitor from VCC33 to VSS |
| 4 | PG0 | IO port PG0 |
| 5 | PG1 | IO port PG1 |
| 6 | PG2 | IO port PG2 |
| 7 | PG3 | IO port PG3 |
| 8 | PB | Push Button Sense Input |
| 9 | AIO0 | Analog I/O |
| 10 | ISNSN | Current sense, negative terminal |
| 11 | ISNSP | Current sense, positive terminal |
| 12 | VB0 | Sense voltage input for the bottom of the battery stack |
| 13 | VB1 | Sense voltage input for the 1 st cell in the battery stack |
| 14 | VB2 | Sense voltage input for the 2 nd cell in the battery stack |
| 15 | VB3 | Sense voltage input for the 3 rd cell in the battery stack |
| 16 | VB4 | Sense voltage input for the 4 th cell in the battery stack |
| 17 | VB5 | Sense voltage input for the 5 th cell in the battery stack |
| 18 | VB6 | Sense voltage input for the 6 th cell in the battery stack |
| 19 | VB7 | Sense voltage input for the 7 th cell in the battery stack |
| 20 | VB8 | Sense voltage input for the 8 th cell in the battery stack |
| 21 | VB9 | Sense voltage input for the 9 th cell in the battery stack |
| 22 | VB10 | Sense voltage input for the 10 th cell in the battery stack |
| 23 | VB11 | Sense voltage input for the 11 th cell in the battery stack |
| 24 | VB12 | Sense voltage input for the 12 th cell in the battery stack |
| 25 | VB13 | Sense voltage input for the 13 th cell in the battery stack |
| 26 | VB14 | Sense voltage input for the 14 th cell in the battery stack |
| 27 | VB15 | Sense voltage input for the 15 th cell in the battery stack |
| 28 | VB16 | Sense voltage input for the 16 th cell in the battery stack |
| 29 | TC | Top Cell connection, short to the top cell of the battery stack or to BAT pin |
| 30 | TC | Top Cell connection, short to the top cell of the battery stack or to BAT pin |
| 31 | TC | Top Cell connection, short to the top cell of the battery stack or to BAT pin |
| 32 | NC | No Connect, leave this pin floating, or short to BAT |
| 33 | BAT | Battery Stack Voltage, Connect to the top of the battery stack. |
| 34 | CHG | Charge FET gate drive output |
| 35 | VCP | High-Voltage Charge Pump output. Connect a 0.47 μ F VP rated capacitor between VCP and VIN close to the device. |
| 36 | VIN | High-Voltage Buck Regulator supply controller input. Connect a 1 μ F 200V or higher value ceramic capacitor, and a 0.1 μ F 200V ceramic capacitor and in parallel with a 22 μ F 200V or higher electrolytic capacitor from VIN to VSS. This pin requires good capacitive bypass to VSS, so the ceramic capacitor must have a trace less than 10mm from the pin. |
| 37 | DSG | Discharge FET gate drive output |
| 38 | PACK+ | Battery Pack Positive Output. Connect to the positive terminal of the battery charger supply or load. |



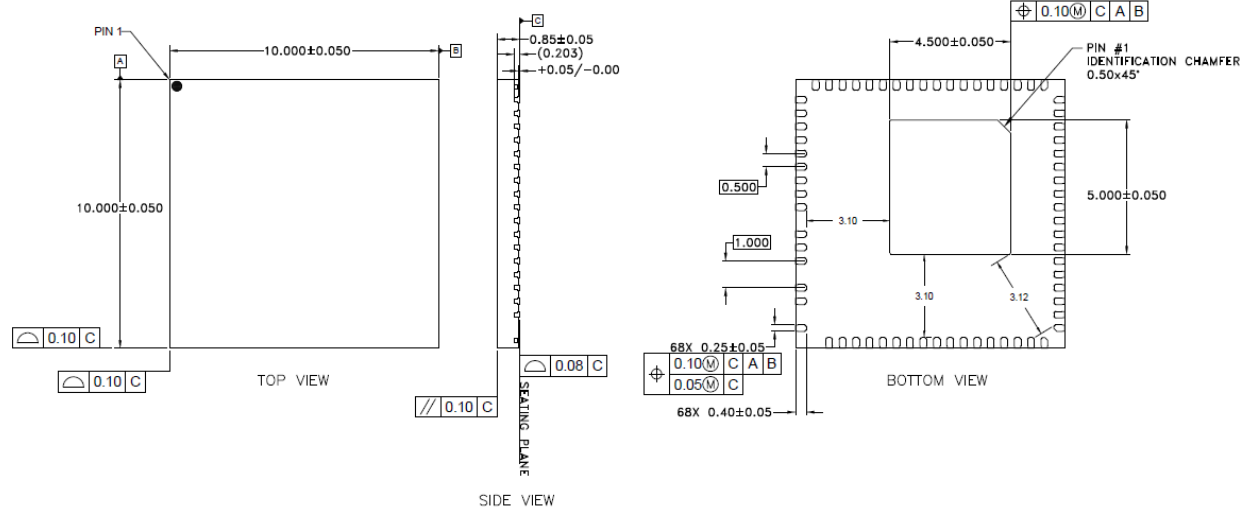
PAC2514x Data Sheet

| PIN NUMBER | LABEL | DESCRIPTION |
|------------|---------|---|
| 39 | BST | High-Voltage Buck Regulator bootstrap input. Connect a 2.2 μ F or higher value ceramic capacitor from BST to SRC with a shorter than 10mm trace from the pin. |
| 40 | DRM | High-Voltage Buck Regulator Switching supply driver output. Connect to the base or gate of the external N-channel MOSFET. |
| 41 | SRC | High-Voltage Buck Regulator Source. Connect to the source of the high-side power MOSFET of the high-voltage buck regulator. |
| 42 | FUSE | FUSE/Low Side FET gate drive output |
| 43 | VSYS | Internally generated 5V power supply. Connect to a 10V/4.7 μ F ceramic capacitor from VSYS to VSS close to the device |
| 44 | REGO | VSYS regulator output |
| 45 | VP | Main power supply. Provides power to the power drivers as well as voltage feedback path for the switching supply. Connect a properly sized supply bypass capacitor in parallel with a 10 μ F ceramic capacitor in parallel with a 100 μ F aluminum capacitor from VP to VSS for voltage loop stabilization. If the switching frequency of the HV-BUCK is \geq 200kHz, then the 100 μ F aluminum capacitor can be replaced with 47 μ F, but the efficiency will be worse. This pin requires good capacitive bypass to VSS, so the ceramic capacitor must have a trace less than 10mm from the pin. |
| 46 | CSM | High-Voltage Buck Regulator Switching supply current sense input. Connect to the positive side of the current sense resistor |
| 47 | PC5 | IO port PC5 |
| 48 | PD7 | IO port PD8 |
| 49 | PD6 | IO port PD6 |
| 50 | PD5 | IO port PD5 |
| 51 | VSS | Ground, shorted to Exposed Pad |
| 52 | PD4 | IO port PD4 |
| 53 | PD3/AD1 | IO port PD3 or ADC channel AD1 |
| 54 | PD2/AD2 | IO port PD2 or ADC channel AD2 |
| 55 | PD1/AD3 | IO port PD1 or ADC channel AD3 |
| 56 | PE0 | IO port PE0 |
| 57 | PE1 | IO port PE1 |
| 58 | PE2 | IO port PE2 |
| 59 | PE3 | IO port PE3 |
| 60 | VCC18 | Internally generated 1.8V power supply. Connect a 2.2 μ F value ceramic capacitor from VCC18 to VSS. No external load allowed. |
| 61 | VCORE | Internally generated 1.2V core power supply. Connect a 2.2 μ F or higher value ceramic capacitor from VCORE to VSS |
| 62 | VCCIO | Internally generated digital I/O 3.3V power supply. Connect a 2.2 μ F or higher value ceramic capacitor from VCCIO to VSS |
| 63 | PF7/AD7 | IO port PF7 or ADC channel AD7 |
| 64 | PF6/AD6 | IO port PF6 or ADC channel AD6. |
| 65 | PF5/AD5 | IO port PF5 or ADC channel AD5. |
| 66 | PF4/AD4 | IO port PF4 or ADC channel AD4. |
| 67 | PF3 | IO port PF3 |
| 68 | PF2 | IO port PF2 |



PAC2514x Data Sheet

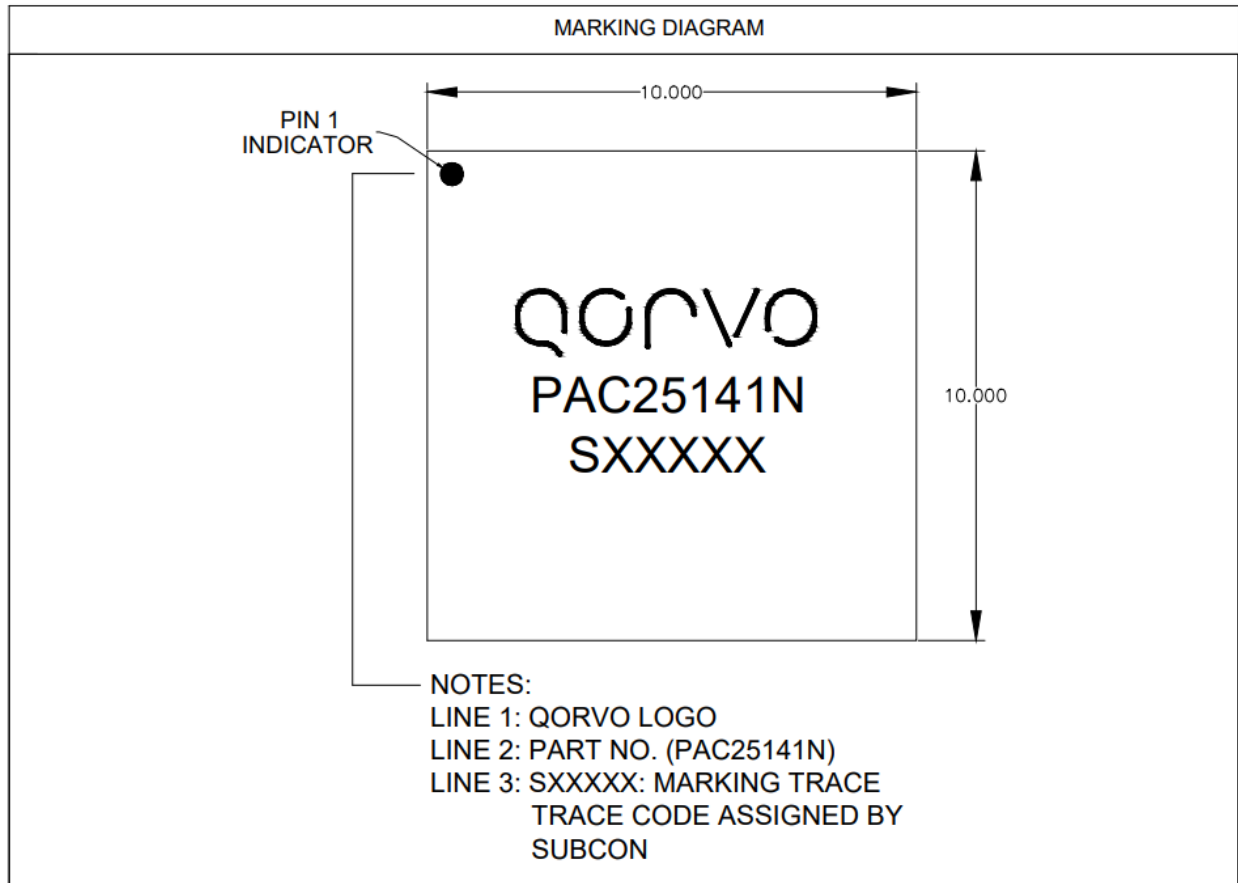
PAC25141N Mechanical Information



Notes:

1. All dimensions are in mm. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PAC25141N Package Marking



Handling Precautions

| Parameter | Rating | Standard |
|----------------------------------|----------|------------------------|
| ESD – Human Body Model (HBM) | Class 1A | ESDA/JEDEC JS-001-2012 |
| ESD – Charged Device Model (CDM) | Class C3 | JEDEC JESD22-C101F |
| MSL – Moisture Sensitivity Level | Level 3 | IPC/JEDEC J-STD-020 |



Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

REVISION HISTORY

| Revision | Description |
|----------|--|
| 1.0 | <ul style="list-style-type: none"> PAC25140 Preview Release |
| 1.1 | <ul style="list-style-type: none"> Align format to PAC22140, remove preview status |
| 1.2 | <ul style="list-style-type: none"> Cell error tolerance tightened, added Sleep power state current, VIN pin cap description |
| 1.3 | <ul style="list-style-type: none"> Updated CAFÉ figure,; Sleep mode typo fixed |
| C.0 | <ul style="list-style-type: none"> Aligned rev number to PDE; Added PAC25140N package spin |
| D.0 | <ul style="list-style-type: none"> Added PAC25141N package spin |
| D.1 | <ul style="list-style-type: none"> Fixed pin out drawing and label |
| | <ul style="list-style-type: none"> |

Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- PFOS Free
- SVHC Free



Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

Important Notice

The information contained herein, and any associated documents is considered to be reliable; however, Qorvo makes no warranties regarding the information contained herein and assumes no responsibility or liability whatsoever for the use of said information. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for Qorvo® products. Information contained herein or any use of such information does not grant, explicitly, implicitly, or otherwise any rights or licenses to any third party with respect to patents or any other intellectual property whether with regard to such information itself or anything described by such information.

THIS INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Without limiting the generality of the foregoing, Qorvo® products are not warranted or authorized for use as critical components in medical, lifesaving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.

Arm® and Cortex® are registered trademarks of Arm Limited. All referenced brands and trademarks are the property of their respective owners.

© 2024 Qorvo US, Inc. All rights reserved. This document is subject to copyright laws in various jurisdictions worldwide and may not be reproduced or distributed, in whole or in part, without the express written consent of Qorvo US, Inc. QORVO® is a registered trademark of Qorvo US, Inc.