

4M x 4 Bit CMOS Dynamic RAM with Extended Data Out

FEATURES

• Performance range:

	trAC	tcAC	trc	thPC
KM44V4004A/AL/ALL/ASL-6	60ns	15ns	110ns	24ns
KM44V4004A/AL/ALL/ASL-7	70ns	20ns	130ns	29ns
KM44V4004A/AL/ALL/ASL-8	80ns	20ns	150ns	34ns

- Fast Page Mode with Extended data out
- Self Refresh Operation (LL-ver. only)
- CAS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- Fast parallel test mode Capability
- LVTTTL compatible inputs and outputs
- Early write or output enable controlled write
- Single+3.3V ± 0.3V power supply
- 4096 cycles/64ms refresh (Normal)
- 4096 cycles/128ms refresh (Low power & Self Ref.)
- 4096 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

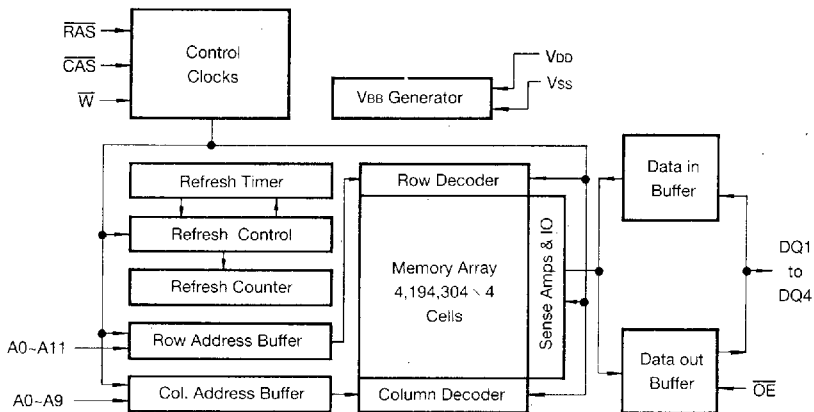
The Samsung KM44V4004A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit x 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44V4004A/AL/ALL/ASL features EDO Mode operation which allows high speed random access of memory cells within the same row.

CAS-before-RAS refresh capability provides on-chip auto refresh as an alternative to RAS-only refresh. All inputs and outputs are fully TTL compatible.

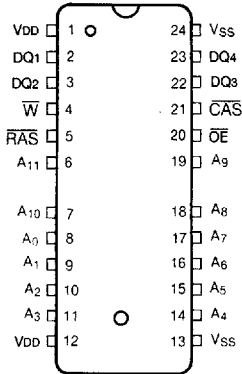
The KM44V4004A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



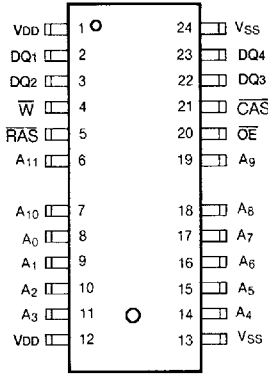
PIN CONFIGURATION (Top Views)

• KM44V4004 AJ/ALJ/ALLJ/ASLJ
AK/ALK/ALLK/ASLK



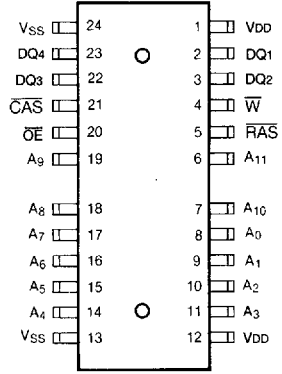
J : 400MIL
K : 300MIL

• KM44V4004 AT/ALT/ALLT/ASLT
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)
S : 300MIL(Forward)

• KM44V4004 ATR/ALTR/ALLTR/ASLTR
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)
SR : 300MIL(Reverse)

Pin Name	Pin Function
A ₀ -A ₁₁	Address Inputs
DQ ₁ -DQ ₄	Data In/Out
V _{SS}	Ground
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{OE}}$	Data Output Enable
V _{DD}	Power(+3.3V)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5~ 4.6	V
Voltage on V _{DD} Supply Relative to Vss	V _{DD}	-0.5~ 4.6	V
Storage Temperature	T _{stg}	-55 to + 150	°C
Power Dissipation	P _D	1	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{DD}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	—	V _{DD} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Operating Current* (RAS and CAS Cycling @trc=min.)	KM44V4004A/AL/ALL/ASL-6 KM44V4004A/AL/ALL/ASL-7 KM44V4004A/AL/ALL/ASL-8 I _{CC1}	-	80 70 60	mA mA mA
Standby Current (RAS=CAS=W=V _{IH})	KM44V4004A KM44V4004AL KM44V4004ALL KM44V4004ASL I _{CC2}	-	2 1 1 1	mA mA mA mA
RAS-Only Refresh Current* (CAS=V _{IH} , RAS Cycling @trc=min.)	KM44V4004A/AL/ALL/ASL-6 KM44V4004A/AL/ALL/ASL-7 KM44V4004A/AL/ALL/ASL-8 I _{CC3}	-	80 70 60	mA mA mA
Hyper Page Mode Current* (RAS=V _{IL} , CAS, Address Cycling @tpc=min.)	KM44V4004A/AL/ALL/ASL-6 KM44V4004A/AL/ALL/ASL-7 KM44V4004A/AL/ALL/ASL-8 I _{CC4}	-	90 80 70	mA mA mA
Standby Current (RAS=CAS=W=V _{DD} -0.2V)	KM44V4004A KM44V4004AL KM44V4004ALL KM44V4004ASL I _{CC5}	-	1 300 200 200	mA μA μA μA
CAS-Before-RAS Refresh Current* (RAS and CAS Cycling @trc=min.)	KM44V4004A/AL/ALL/ASL-6 KM44V4004A/AL/ALL/ASL-7 KM44V4004A/AL/ALL/ASL-8 I _{CC6}	-	80 70 60	mA mA mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage (V _{IH})=V _{DD} -0.2V Input Low Voltage (V _{IL})=0.2V CAS=CAS-Before-RAS Cycling or 0.2V DQ1~DQ4=Don't Care trc=31.25μs(L-Ver.) 62.5μs(SL-Ver.), tras=tras min. ~300ns	KM44V4004AL KM44V4004ASL I _{CC7}	-	450 350	μA μA
Self Refresh Current RAS=CAS=0.2V W=OE=A0-A11=V _{DD} -0.2V or 0.2V DQ1~DQ4=V _{DD} -0.2V, 0.2V or Open	KM44V4004ALL I _{CC8}	-	250	μA



DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{DD} + 0.3V$, all other pins not under test=0 volts.)	IIL	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{DD}$)	IOL	-10	10	μA
Output High Voltage Level (I _{OH} =-2mA)	V _{OH}	2.4	-	V
Output Low Voltage Level (I _{OL} =2mA)	V _{OL}	-	0.4	V

*NOTE: I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. In I_{CC4}, Address can be changed maximum once within one Hyper Page cycle.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A ₀ -A ₁₁)	C _{IN1}	-	5	pF
Input Capacitance (\overline{RAS} , \overline{CAS} , \overline{W} , \overline{OE})	C _{IN2}	-	7	pF
Output Capacitance (DQ ₁ -DQ ₄)	C _{DQ}	-	7	pF

AC CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{DD}=3.3V ± 0.3V, See notes 1,2)

Test condition: V_{ih}/V_{il}=2.0V/0.8V, V_{oh}/V_{ol}=2.0V/0.8V, Output Loading C_L=100pF

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	110		130		150		ns	
Read-modify-write cycle time	t _{RWC}	155		185		205		ns	
Access time from \overline{RAS}	t _{RAC}		60		70		80	ns	3,4,11
Access time from \overline{CAS}	t _{CAC}		15		20		20	ns	3,4,5
Access time from column address	t _{AAC}		30		35		40	ns	3,11
\overline{CAS} to output in Low-Z	t _{CLZ}	3		3		3		ns	3
\overline{OE} to output in Low-Z	t _{OLZ}	3		3		3		ns	3
Output buffer turn-off delay from \overline{CAS}	t _{CEZ}	3	15	3	20	3	20	ns	7,14,16
Transition time (rise and fall)	t _t	2	50	2	50	2	50	ns	2
\overline{RAS} precharge time	t _{RP}	40		50		60		ns	
\overline{RAS} pulse width	t _{RAS}	60	10,000	70	10,000	80	10,000	ns	
\overline{RAS} hold time	t _{RSH}	15		20		20		ns	
\overline{CAS} hold time	t _{CASH}	45		50		60		ns	
\overline{CAS} pulse width	t _{CAS}	10	10,000	15	10,000	20	10,000	ns	
\overline{RAS} to \overline{CAS} delay time	t _{RCD}	20	45	20	50	20	60	ns	4
\overline{RAS} to column address delay time	t _{RAD}	15	30	15	35	15	40	ns	11
\overline{CAS} to \overline{RAS} precharge time	t _{CRP}	5		5		5		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Row address set-up time	tASR	0		0		0		ns	
Row address hold time	tRAH	10		10		10		ns	
Column address set-up time	tASC	0		0		0		ns	
Column address hold time	tCAH	10		10		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	45		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	tRAL	30		35		40		ns	
Read command set-up time	tRCS	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		0		ns	9
Write command hold time	tWCH	10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	tWCR	45		55		60		ns	6
Write command pulse width	tWP	10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	15		20		20		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	10		15		20		ns	
Data set-up time	tDS	0		0		0		ns	10
Data hold time	tDH	10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	45		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256	ms	
Write command set-up time	tWCS	0		0		0		ns	8
$\overline{\text{CAS}}$ to $\overline{\text{W}}$ delay time	tCWD	40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	tRWD	85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	55		65		70		ns	8
$\overline{\text{CAS}}$ precharge to $\overline{\text{W}}$ delay time	tCPWD	60		70		75		ns	8
$\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		ns	
$\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		5		ns	
$\overline{\text{CAS}}$ precharge time ($\overline{\text{C}}$ -B- $\overline{\text{F}}$ counter test cycle)	tCPT	20		30		30		ns	
Access time from $\overline{\text{CAS}}$ precharge	tCPA		35		40		45	ns	3
Hyper Page cycle time	tHPC	24		29		34		ns	17
Hyper Page read-modify-write cycle time	tHPRWC	71		86		96		ns	17
$\overline{\text{CAS}}$ precharge time (Hyper Page cycle)	tCP	10		10		10		ns	
$\overline{\text{RAS}}$ pulse width (Hyper Page cycle)	tRASP	60	200,000	70	200,000	80	200,000	ns	
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	tRHCP	35		40		45		ns	
$\overline{\text{OE}}$ access time	tOEA		15		20		20	ns	
$\overline{\text{OE}}$ to data delay	tOED	15		20		20		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Output buffer turn off delay time from \overline{OE}	toEZ	3	15	3	20	3	20	ns	7,14
\overline{OE} commend hold time	toEH	15		20		20		ns	
Write command set-up time (Test mode in)	twTS	10		10		10		ns	
Write command hold time (Test mode in)	twTH	10		10		10		ns	
\overline{W} to \overline{RAS} precharge time (\overline{C} -B- \overline{R} refresh)	tWRP	10		10		10		ns	
\overline{W} to \overline{RAS} hold time (\overline{C} -B- \overline{R} refresh)	tWRH	10		10		10		ns	
Output data hold time	tDOH	5		5		5		ns	7,16
\overline{OE} to \overline{CAS} hold time	toCH	5		5		5		ns	
\overline{CAS} hold time to \overline{OE}	tCHO	5		5		5		ns	
\overline{OE} precharge time	toEP	5		5		5		ns	
\overline{W} pulse width(Hyper Page cycle)	twPE	5		5		5		ns	
Output buffer turn off delay from \overline{RAS}	trEZ	3	15	3	20	3	20	ns	7,14,16
Output buffer turn off delay from \overline{W}	twEZ	3	15	3	20	3	20	ns	7,14
\overline{W} to data delay	twED	15		20		20		ns	
\overline{RAS} pulse width (LL-Ver)	trASS	100		100		100		μ s	15
\overline{RAS} precharge time (LL-Ver)	trPS	110		130		150		ns	15
\overline{CAS} hold time (LL-Ver)	tCHS	-50		-50		-50		ns	15

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TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trC	115		135		155		ns	
Read-modify-write cycle time	trWC	160		190		210		ns	
Access time from \overline{RAS}	trAC		65		75		85	ns	3,4,11
Access time from \overline{CAS}	tcAC		20		20		25	ns	3,4,5
Access time from column address	tAA		35		40		45	ns	3,11
\overline{RAS} pulse width	trAS	65	10,000	75	10,000	85	10,000	ns	
\overline{CAS} pulse width	tcAS	15	10,000	20	10,000	25	10,000	ns	
\overline{RAS} hold time	trSH	20		25		25		ns	
\overline{CAS} hold time	tcSH	20		55		65		ns	
Column address to \overline{RAS} lead time	trAL	35		40		45		ns	
\overline{CAS} to \overline{W} delay time	tcWD	45		55		55		ns	8
\overline{RAS} to \overline{W} delay time	trWD	90		105		115		ns	8
Column address to \overline{W} delay time	tAWD	60		70		75		ns	8
Hyper Page mode cycle time	thPC	29		34		39		ns	
Hyper Page mode read-modify-write cycle time	thPRWC	76		91		101		ns	
\overline{RAS} pulse width (Hyper Page Mode)	trASP	65	200,000	75	200,000	85	200,000	ns	



TEST MODE CYCLE(Continued)

Parameter	Symbol	-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{CAS}}$ precharge	tCPA		40		45		50	ns	
$\overline{\text{OE}}$ access time	tOEA		20		25		25	ns	3
$\overline{\text{OE}}$ to data delay	tOED	20		25		25		ns	
$\overline{\text{OE}}$ command hold time	tOEH	20		25		25		ns	

TEST MODE DESCRIPTION

The KM44V4004A/AL/ALL/ASL is the CMOS DRAM organized 4,194,304 words by 4 bit internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit Ao is not used. If upon reading, two bits on one I/O pin are equal (all "1" or "0"s) the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 4Mx4 DRAM can be tested as if it were a 1Mx4 DRAM.

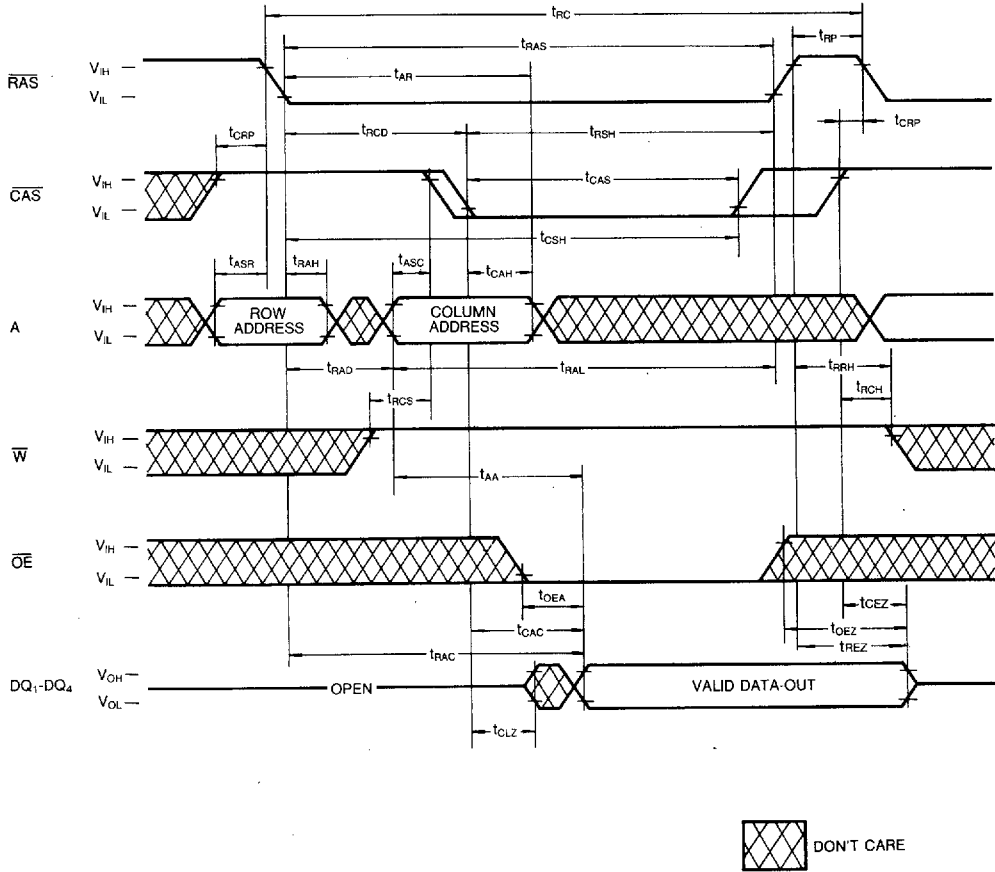
$\overline{\text{W}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Cycle (WCBR, Test Mode In Cycle) puts the device into "Test Mode", And " $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle" or " $\overline{\text{RAS}}$ Only Refresh Cycle" puts it back into "Normal Mode". In the Test Mode, " $\overline{\text{W}}$ and $\overline{\text{RAS}}$ Refresh Cycle" performs the refresh operation with internal CBR refresh address counter. The "Test Mode" function reduces test time (1/4 in cases of N test pattern)

NOTES

- An initial pause of 200µs is required after power-up followed by any 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved.
- V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) are assumed to be 5ns for all inputs, without tHPC and tHPRWC.
- Measured with a load equivalent to 100pF and V_{oh}=2.0V(I_{out}=2mA), V_{ol}=0.8V(I_{out}=2mA)
- Operation within the t_{RC}(max) limit insures that t_{RC}(max) can be met. t_{RC}(max) is specified as a reference point only. If t_{RC} is greater than the specified t_{RC}(max) limit, then access time is controlled exclusively by t_{CAC}.
- Assumes that t_{RC} ≥ t_{RC}(max).
- t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{TRAD}(max).
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
- t_{WCS}, t_{TRWD}, t_{ICWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If t_{WCS} ≥ t_{WCS}(min) the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If t_{ICWD} ≥ t_{ICWD}(min), t_{TRWD} ≥ t_{TRWD}(min) and t_{AWD} ≥ t_{AWD}(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
- Either t_{TRCH} or t_{TRRH} must be satisfied for a read cycle.
- These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and to the $\overline{\text{W}}$ leading edge in read-write cycles.
- Operation within the t_{TRAD}(max) limit insures that t_{TRAC}(max) can be met. t_{TRAD}(max) is specified as a reference point only. If t_{TRAD} is greater than the specified t_{TRAD}(max) limit, then access time is controlled by t_{AA}.
- These specifications are applied in the test mode.
- In test mode read cycle, the value of t_{TRAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
- t_{TRWZ}(max), t_{CEZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
- 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.
- If $\overline{\text{RAS}}$ goes high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going
- t_{ASC} ≥ t_{CP}(min), Assumn t_T=2.0ns



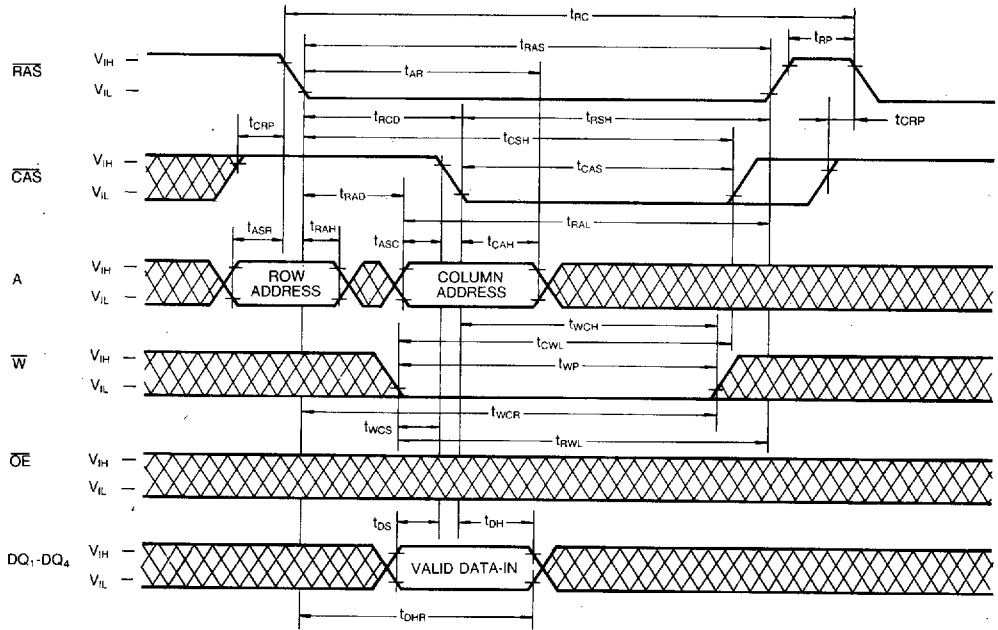
TIMING DIAGRAMS
READ CYCLE



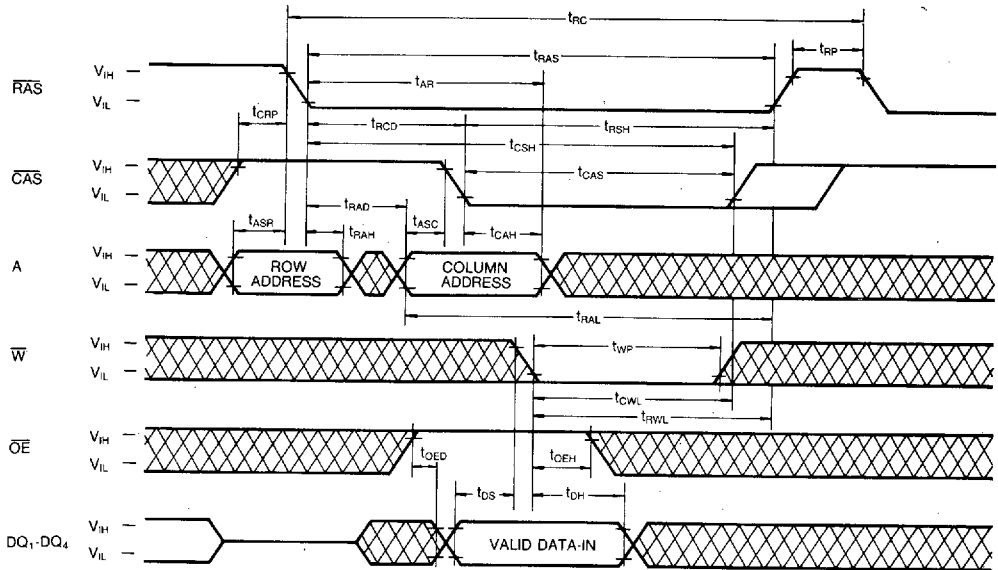
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TIMING DIAGRAMS (Continued)

WRITE CYCLE (EARLY CYCLE)



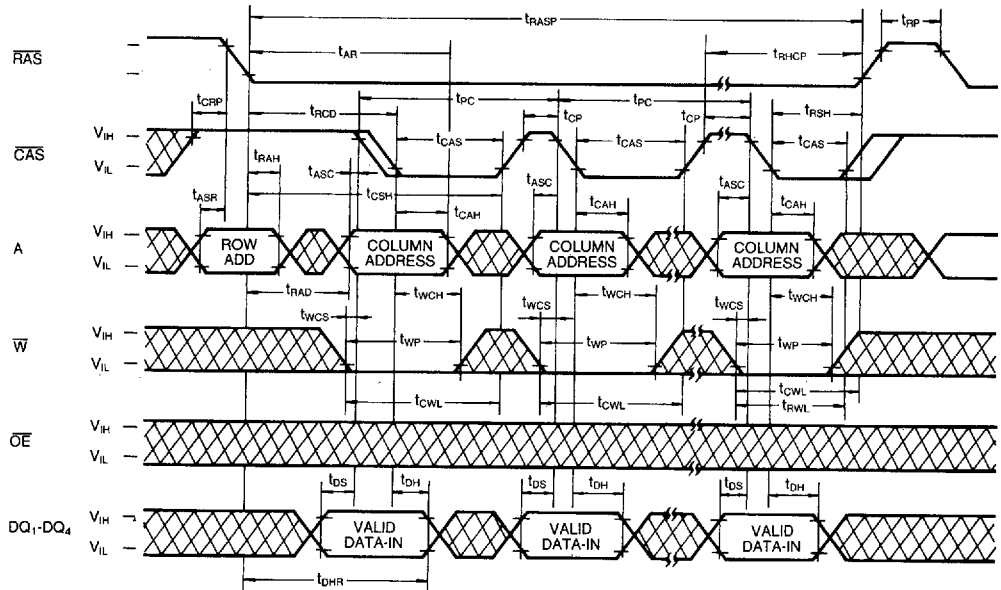
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)



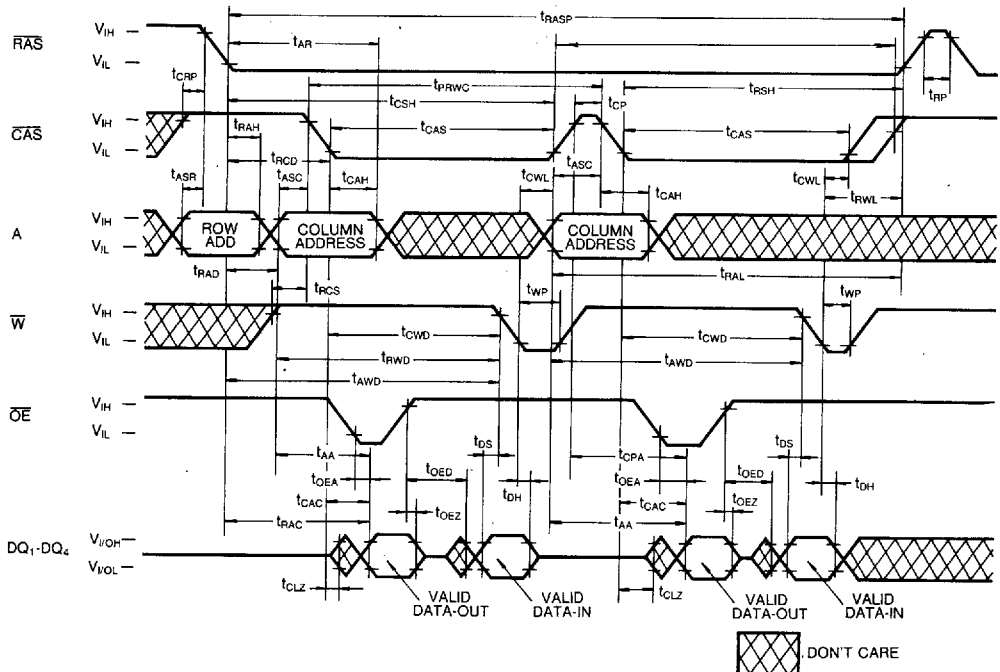
 DONT CARE

TIMING DIAGRAMS (Continued)

HYPER PAGE WRITE CYCLE (EARLY WRITE)

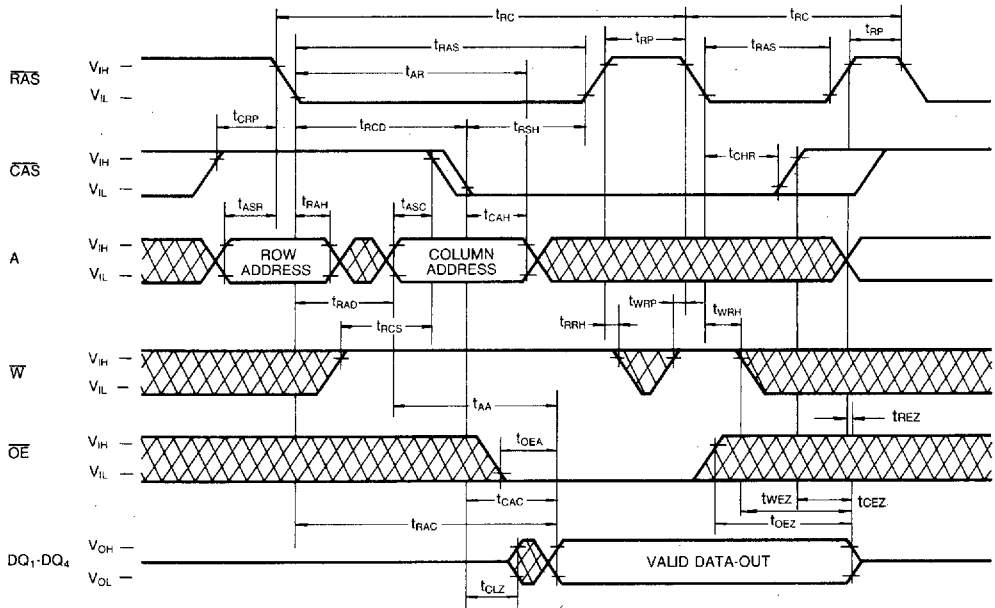


HYPER PAGE READ-MODIFY-WRITE CYCLE

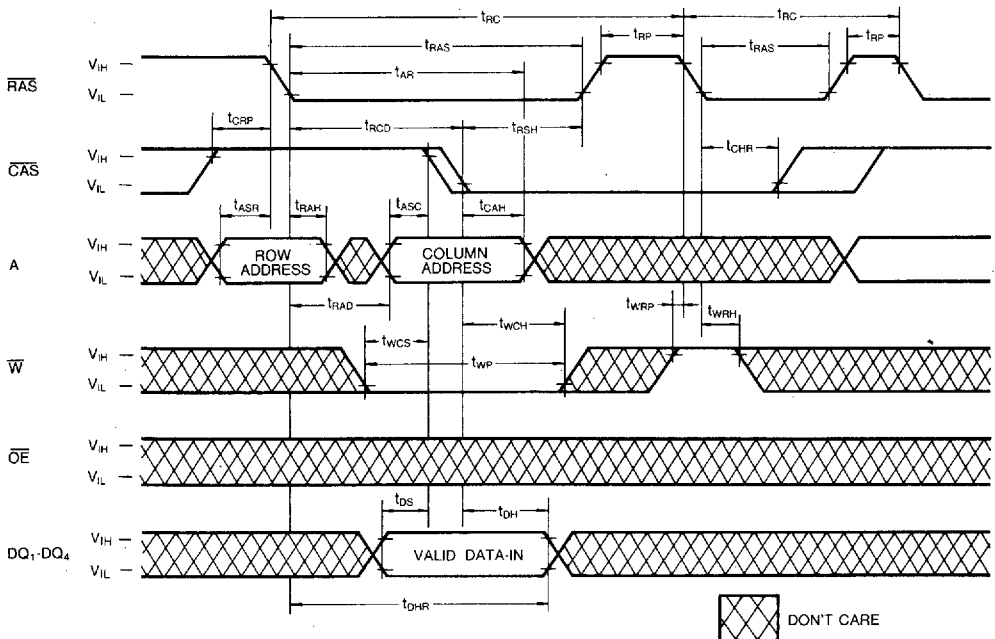


TIMING DIAGRAMS (Continued)

HIDDEN REFRESH CYCLE (READ)



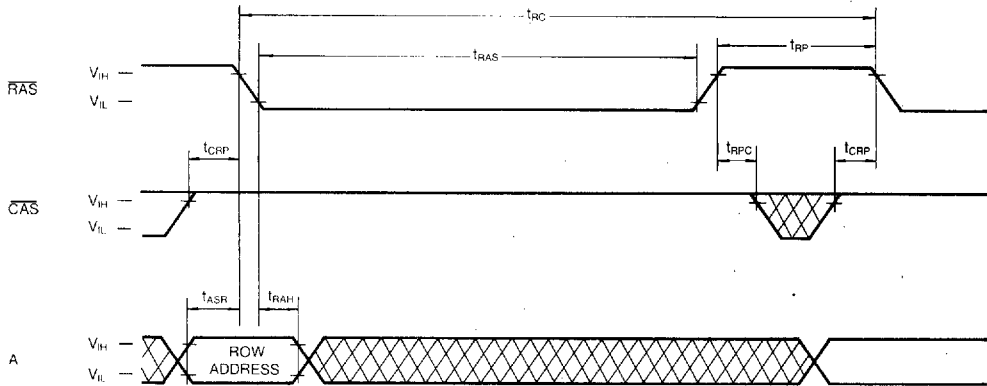
HIDDEN REFRESH CYCLE (WRITE)



TIMING DIAGRAMS (Continued)

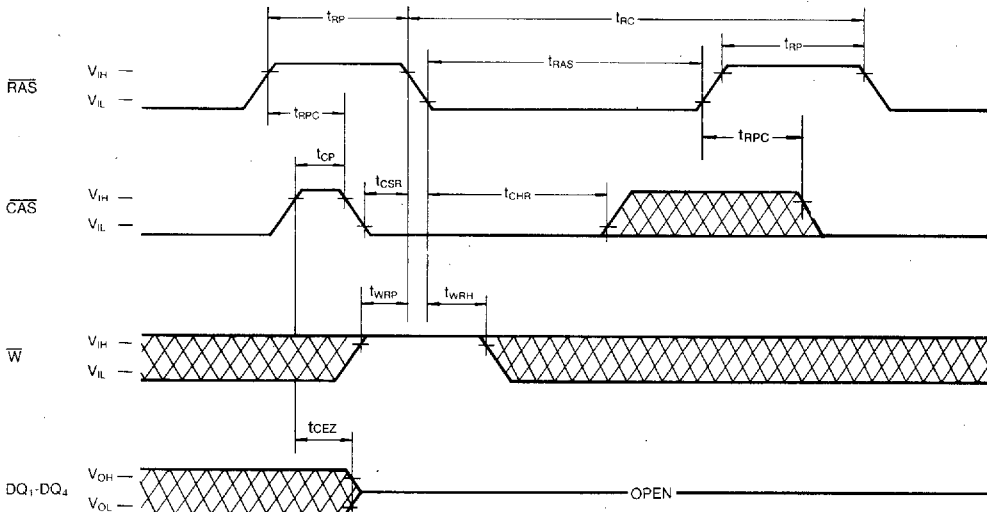
RAS-ONLY REFRESH CYCLE

Note: \bar{W} , \bar{OE} =Don't Care



CAS-BEFORE-RAS REFRESH CYCLE

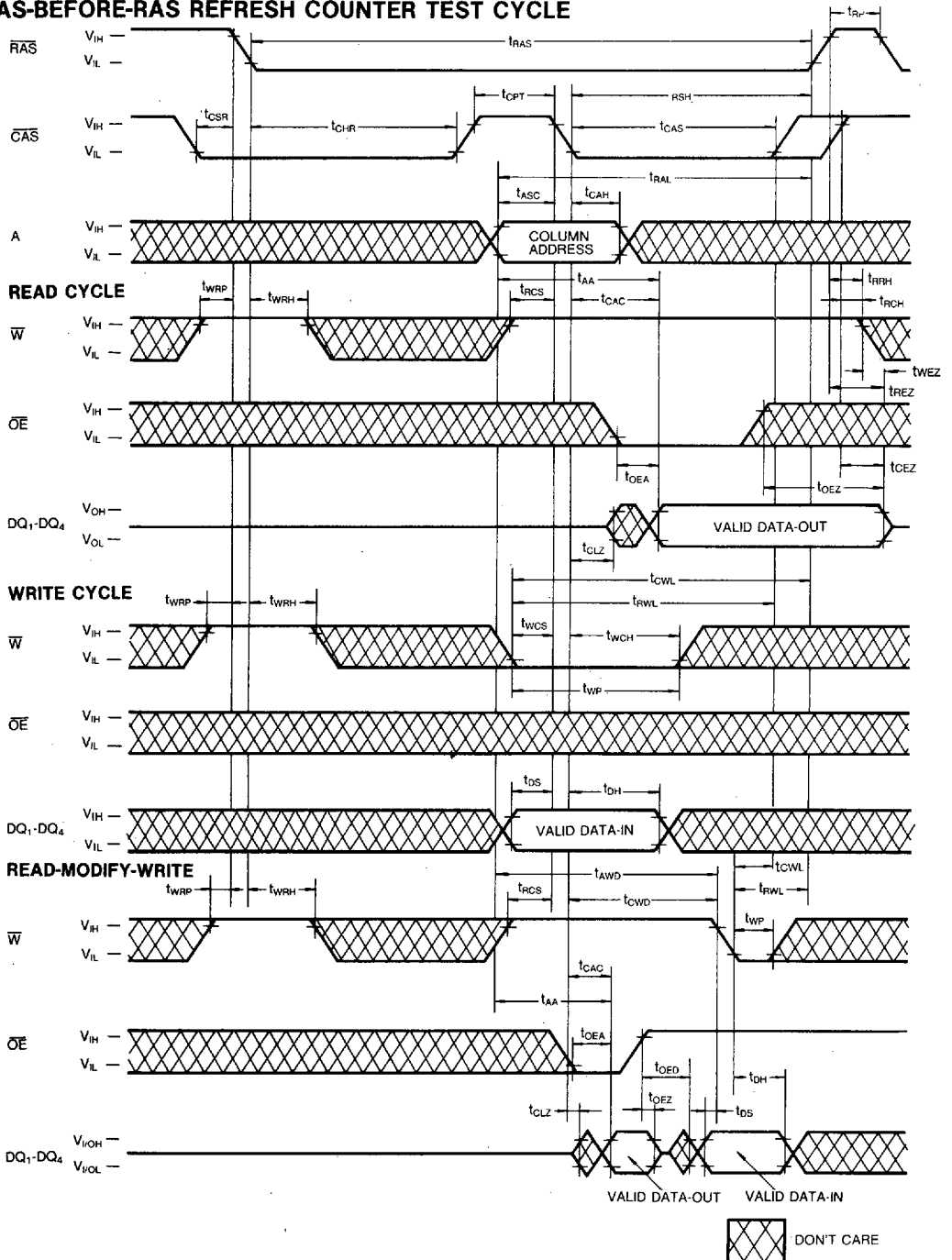
Note: \bar{OE} , Address=Don't Care



 DON'T CARE

TIMING DIAGRAMS (Continued)

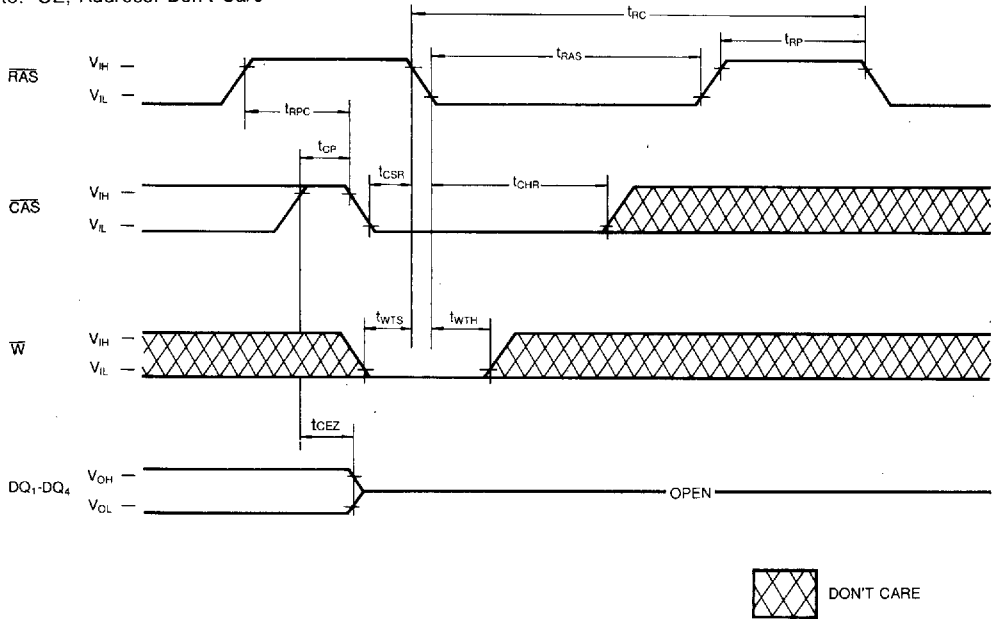
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

TEST MODE IN CYCLE

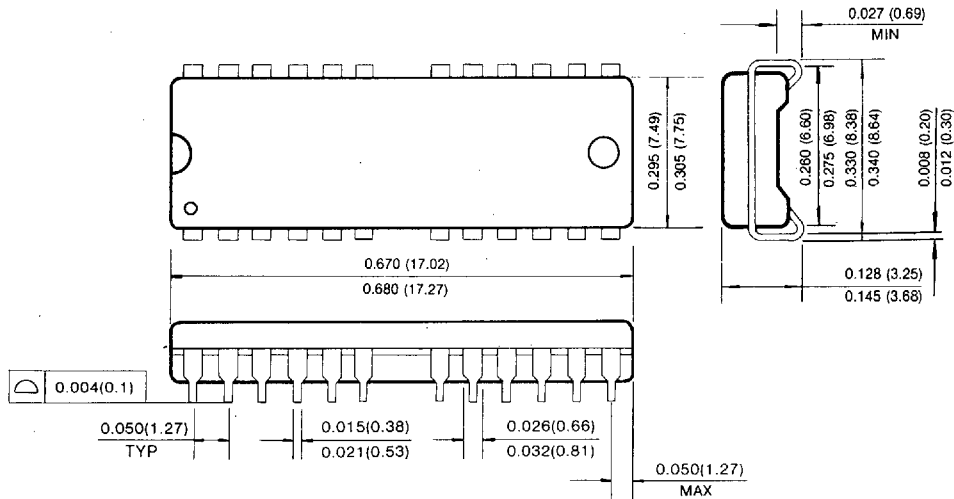
Note: OE, Address: Don't Care



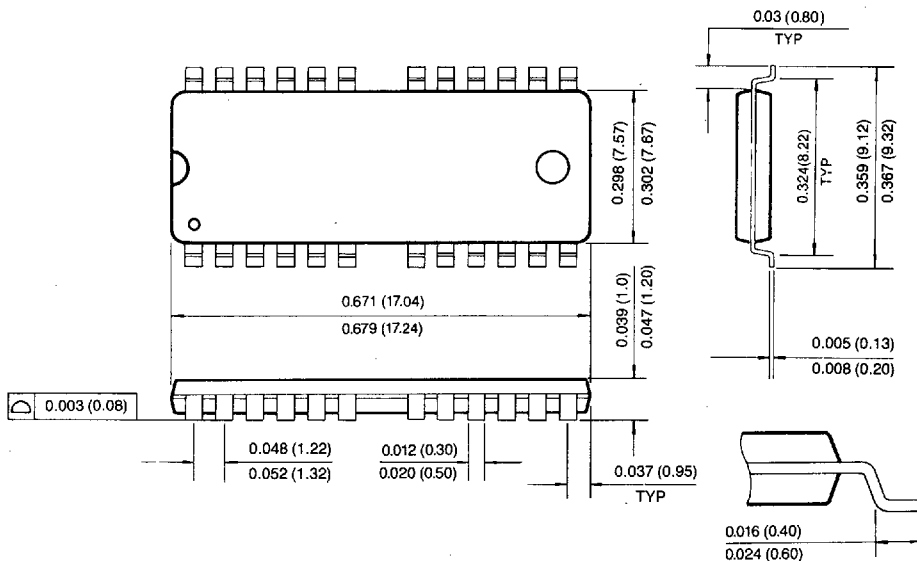
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



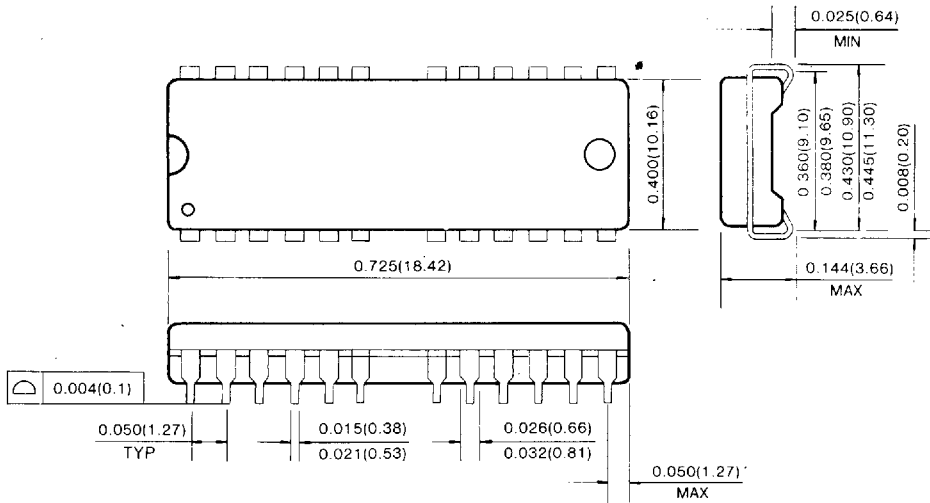
24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)



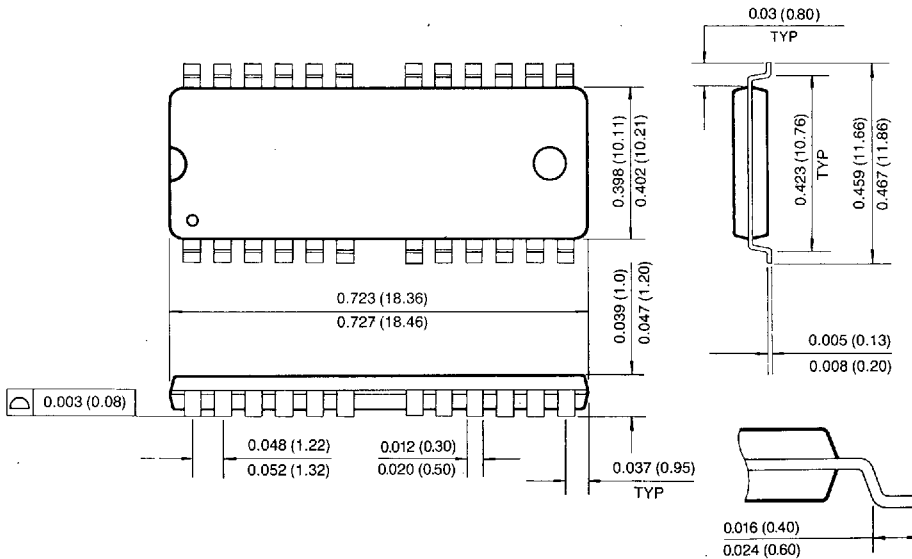
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE
(400MIL, Forward and Reverse Type)



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