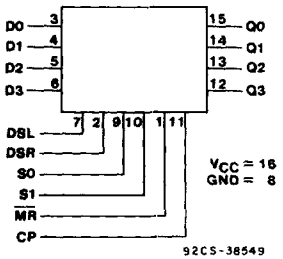
File Number **1668**

CD54/74HC194
CD54/74HCT194

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

4-Bit Bidirectional Universal Shift Register

Type Features:

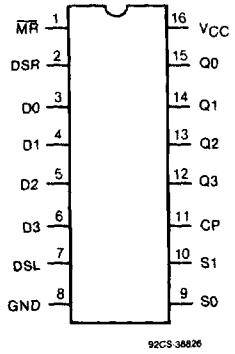
- *Four Operating Modes: Shift Right, Shift Left, Hold and Reset*
- *Synchronous parallel or serial operation*
- *Typical f_{MAX} = 60 MHz @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*
- *Asynchronous Master Reset*

The RCA-CD54/74HC194 and CD54/74HCT194 are 4-bit shift registers with Asynchronous Master Reset ($\overline{MR}$). In the parallel mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the clock input (CP). During parallel loading serial data flow is inhibited. Shift left and shift right are accomplished synchronously on the positive clock edge with serial data entered at the shift left (DSL) serial input for the shift right mode, and at the shift right (DSR) serial input for the shift left mode. Clearing the register is accomplished by a Low applied to the Master Reset ($\overline{MR}$) pin.

The CD54HC/HCT194 devices are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT194 devices are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC194
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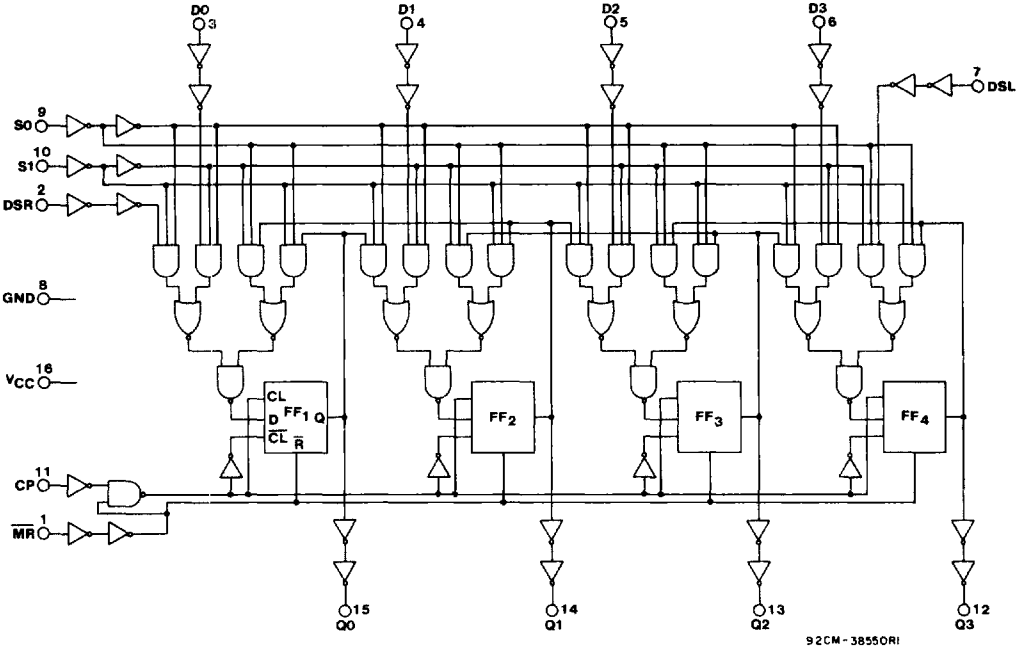

Fig. 1 - Logic diagram for the CD54/74HC194 and CD54/74HCT194.

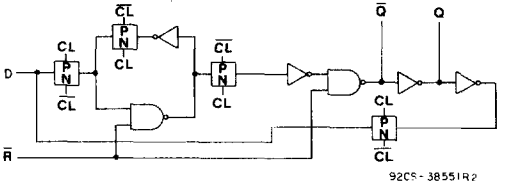

Fig. 2 - Detail of single Flip-Flop for the CD54/74HC194 and CD54/74HCT194.

TRUTH TABLE

Operating Mode	Inputs							Outputs			
	CP	$\overline{MR}$	S_1	S_0	DSR	DSL	D_n	Q0	Q1	Q2	Q3
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l(b)	l(b)	X	X	X	q0	q1	q2	q3
Shift Left	↑	H	h	l(b)	X	l	X	q1	q2	q3	L
	↑	H	h	l(b)	X	h	X	q1	q2	q3	H
Shift Right	↑	H	l(b)	h	l	X	X	L	q0	q1	q2
	↑	H	l(b)	h	h	X	X	H	q0	q1	q2
Parallel Load	↑	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

NOTE: b. The HIGH-to-LOW transition of the S_0, and S_1 inputs on the 54/74194 should only take place while CP is HIGH for conventional operation.

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) ..... ± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ OR $V_O > V_{CC}$ +0.5 V) ..... ± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < V_O < V_{CC} +0.5 V) ..... ± 25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}): ..... ± 50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING -TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 +150°C
LEAD TEMPERATUARE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC/54HC194										CD74HCT/54HCT194									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
	V_I V	Io mA	Vcc V	+ 25°C			-40/ + 85°C		-55/ + 125°C		V_I V	Vcc V	+ 25°C			-40/ + 85°C		-55/ + 125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—		4.5								
			4.5	3.15	—	—	3.15	—	3.15	—		to	2	—	—	2	—	2	—	
			6	4.2	—	—	4.2	—	4.2	—	—	5.5								V
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5		4.5								
			4.5	—	—	1.35	—	1.35	—	1.35		to	—	—	0.8	—	0.8	—	0.8	
			6	—	—	1.8	—	1.8	—	1.8		5.5								V
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										V
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	
			4.5	—	—	0.1	—	0.1	—	0.1										V
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	Vcc or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between Vcc & Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	Vcc or Gnd	0	6	—	—	8	—	80	—	160	Vcc or Gnd	5.5	—	—	8	—	80	—	160	µA
Additional quiescent Device Current ΔI_{CC}* per input pin: 1 unit load											Vcc-2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
CP	0.6
$\overline{MR}$	0.55
DSL, DSR, Dn	0.25
Sn	1.10

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 µA max. @ 25°C.

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L pF	TYPICAL		UNIT
			HC	HCT	
Propagation Delay, Clock to Q	t_{PLH}, t_{PHL}	15	14	15	ns
Maximum Clock Frequency	f_{MAX}	15	60	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	55	60	pF

*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where:
f_i = input frequency.
f_o = output frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS												UNITS
			25°C				-40°C to + 85°C				-55°C to + 125°C				
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Max. Clock Frequency Fig. 3	f_{MAX}	2	6		—		5		—		4		—		MHz
		4.5	30		27		24		22		20		18		
		6	35		—		28		—		23		—		
$\overline{MR}$ Pulse Width Fig. 4	t_W	2	80		—		100		—		120		—		ns
		4.5	16		16		20		20		24		24		
		6	14		—		17		—		20		—		
Clock Pulse Width Fig. 3	t_W	2	80		—		100		—		120		—		ns
		4.5	16		16		20		20		24		24		
		6	14		—		17		—		20		—		
Set-up time Data to Clock Fig. 5	t_{SU}	2	70		—		90		—		105		—		ns
		4.5	14		14		18		18		21		21		
		6	12		—		15		—		19		—		
Removal Time $\overline{MR}$ to Clock Fig. 4	t_{REM}	2	60		—		75		—		90		—		ns
		4.5	12		12		15		15		18		18		
		6	10		—		13		—		15		—		
Set-up Time S1, S0 to Clock Fig. 6	t_{SU}	2	80		—		100		—		120		—		ns
		4.5	16		20		20		25		24		30		
		6	14		—		17		—		20		—		
Set-up Time DSL, DSR to Clock Fig. 6	t_{SU}	2	70		—		90		—		105		—		ns
		4.5	14		14		18		18		21		21		
		6	12		—		15		—		18		—		
Hold Time S1, S0 to Clock Fig. 6	t_H	2	0		—		0		—		0		—		ns
		4.5	0		0		0		0		0		0		
		6	0		—		0		—		0		—		
Hold Time Data to Clock Fig. 5	t_H	2	0		—		0		—		0		—		ns
		4.5	0		0		0		0		0		0		
		6	0		—		0		—		0		—		

CD54/74HC194
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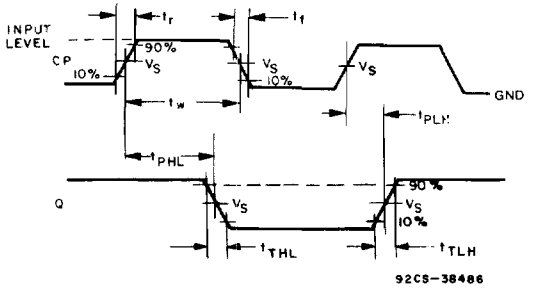
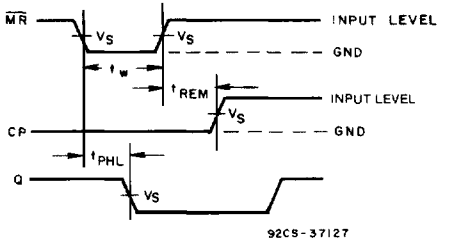
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation Delay	t_{PLH}	2		175		—		220		—		265		—	
Clock to Output	t_{PHL}	4.5		35		37		44		46		53		56	ns
Fig. 3		6		30		—		37		—		45		—	
Output Transition	t_{TLH}	2		75		—		95		—		110		—	
Time	t_{THL}	4.5		15		15		19		19		22		22	ns
Fig. 3		6		13		—		16		—		19		—	
Propagation Delay	t_{PHL}	2		140		—		175		—		210		—	
$\overline{MR}$ to Output		4.5		28		40		35		50		42		60	ns
Fig. 4		6		24		—		30		—		36		—	
Input Capacitance	C_I	—		10		10		10		10		10		10	pF



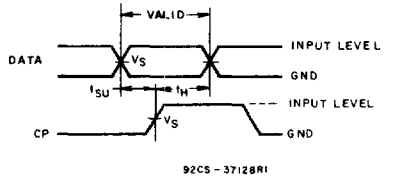
	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50% V_{CC}	1.3 V

Fig. 3 - Clock pre-requisite times and propagation and output transition times.



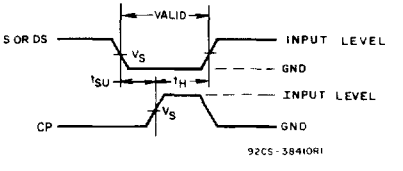
	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50% V_{CC}	1.3 V

Fig. 4 - Master reset pre-requisite times and propagation delays.



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE V_S	50% V_{CC}	1.3 V

Fig. 5 - Data pre-requisite times.



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3 V
SWITCHING VOLTAGE, V_S	50% V_{CC}	1.3 V

Fig. 6 Parallel load or shift-left/shift-right pre-requisite times.