FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16308-1E

32-Bit RISC Microcontroller

CMOS

FR30 Series

MB91133/MB91F133

■ DESCRIPTION

The MB91133/MB91F133, a standard single-chip microcontroller featuring various I/O resources and bus control mechanisms to incorporate the control required for high-performance high-speed CPU processes, is the core unit in the 32-bit RISC CPU (FR family) .

This unit has the optimal specifications for incorporating applications that require high-performance CPU processing power by featuring peripheral I/O resources suitable for single-lens reflex cameras, digital video cameras, etc.

■ FEATURES

1. CPU

- 32-bit RISC (FR30) , load/store architecture, 5-level pipeline
- Multi-purpose register : 32 bits × 16
- 16-bit fixed length instructions (basic instructions) , 1 instruction per cycle
- Instructions for barrel shift, bit processing and inter-memory transfers : Instructions suited to loading purposes
- Function entry / exit instruction, multi load / store instruction of register details : High-level language handling instruction
- Register interlock function : Simplification of assembler description
- Branch instruction with delay slot : Reduction in overheads in case of branching
- Multiplier is built-in / supported at instruction level.
- Signed 32-bit multiplication : 5 cycles
- Signed 16-bit multiplication : 3 cycles
- Interruption (saving PC and PS) : 6 cycles, 16 priority levels

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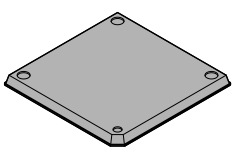
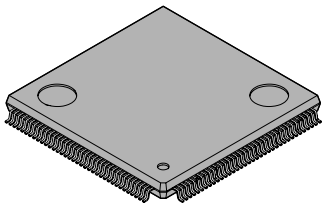
■ PACKAGES

144-pin plastic FBGA	144-pin plastic LQFP
	
(BGA-144P-M01)	(FPT-144P-M08)

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2. Bus Interface

- 24-bit address output, 8/16-bit data input/output
- Basic bus cycle : 2 clock cycles
- Interface support for various memories
- Unused data and address pins can be used as input/output ports.
- Supports “little endian” mode

3. Built-in ROM

Mask device : 254 KB; FLASH device : 254 KB; EVA-FLASH device : 254 KB

4. Built-in RAM

Mask device : 8 KB; FLASH device : 8 KB; EVA-FLASH device : 8 KB

5. DMA Controller

This is a descriptor-type MA controller whose transfer parameters are arranged in the main memory.

A maximum of 8 factors in total (internal and external) can be transferred.

External factors are 3 channels.

6. Bit Search Module

Searches the first “1” / “0” change bit positions within 1 cycle from MSB in 1 word

7. Timer

- 16-bit reload timer × 5 channels
- 16-bit OCU × 8 channels, ICU × 4 channels, free-run timer × 1 channel
  Output waveform adjusting function for AC motor waveforms is included in the above timer.
- 8/16-bit up/down timer/counter (8-bit × 2 channels or 16-bit × 1 channel)
  External interruption and pin are shared for AIN and BIN.
- 16-bit down count timer × 5 channels; can also be used as the UART baud rate timer
- 16-bit PPG timer × 6 channels; out-pulse cycle / duty can be changed at random

8. D/A Converter

- 8-bit × 3 channels

9. A/D Converter (Sequential comparison type)

- 10-bit × 8 channels
- Sequential conversion method (conversion time 5.0 μs at 33 MHz)
- Setting for single conversion, scan conversion and repeat conversion is possible.
- Conversion starting function using hardware or software

10. Serial I/O

- UART × 5 channels; clock synchronous serial transfer with LSB / MSB switching function is possible for both.
- Serial data output or serial lock output can be selected using push-pull / open-drain software.

11. Level Comparator Input

- 1 channel; shared input and pins of A/D converter.

12. Clock Switching Function

- Base clock : Software can be used to select from two types of clock sources, namely 32 kHz and high-speed.
- Gear function : Four types of settings (1 : 1, 1 : 2, 1 : 4, 1 : 8) can be set individually as the operating clock ratio to the basic clock per CPU and peripheral equipment.

13. Interruption Controller

- **External interruption input (total 24 channels)**
- With pull up pin control / standby return function : 4 channels
  (rising / falling / H level / L level settings are possible)
- With pull up pin control / standby return function; AIN / BIN pins of the up/down counter are shared : 4 channels
  (rising / falling / H level / L level settings are possible)
- With pull up pin controln : 16 channels
  (rising / falling / H level / L level settings are possible)
- **Internal interruption factor**
- Interruption / delay interruption by resource

14. Others

- **Reset factors**
  Power on reset, watchdog timer, software reset, external reset
- **Low power consumption mode**
  Sleep/stop mode
- **Packages**
  FBGA-144, LQFP-144
- **CMOS technology (0.35 μm)**
- **Power**
  Two power sources (5 V / 3 V)
  1) 5 V system : 5 V ± 10% (A/D, D/A and level comparator included)
  2) 3 V system : A) 3.0 V to 3.6 V : All functions guaranteed
  B) 2.7 V to 3.0 V : All functions guaranteed for single-chip mode of mask devices only

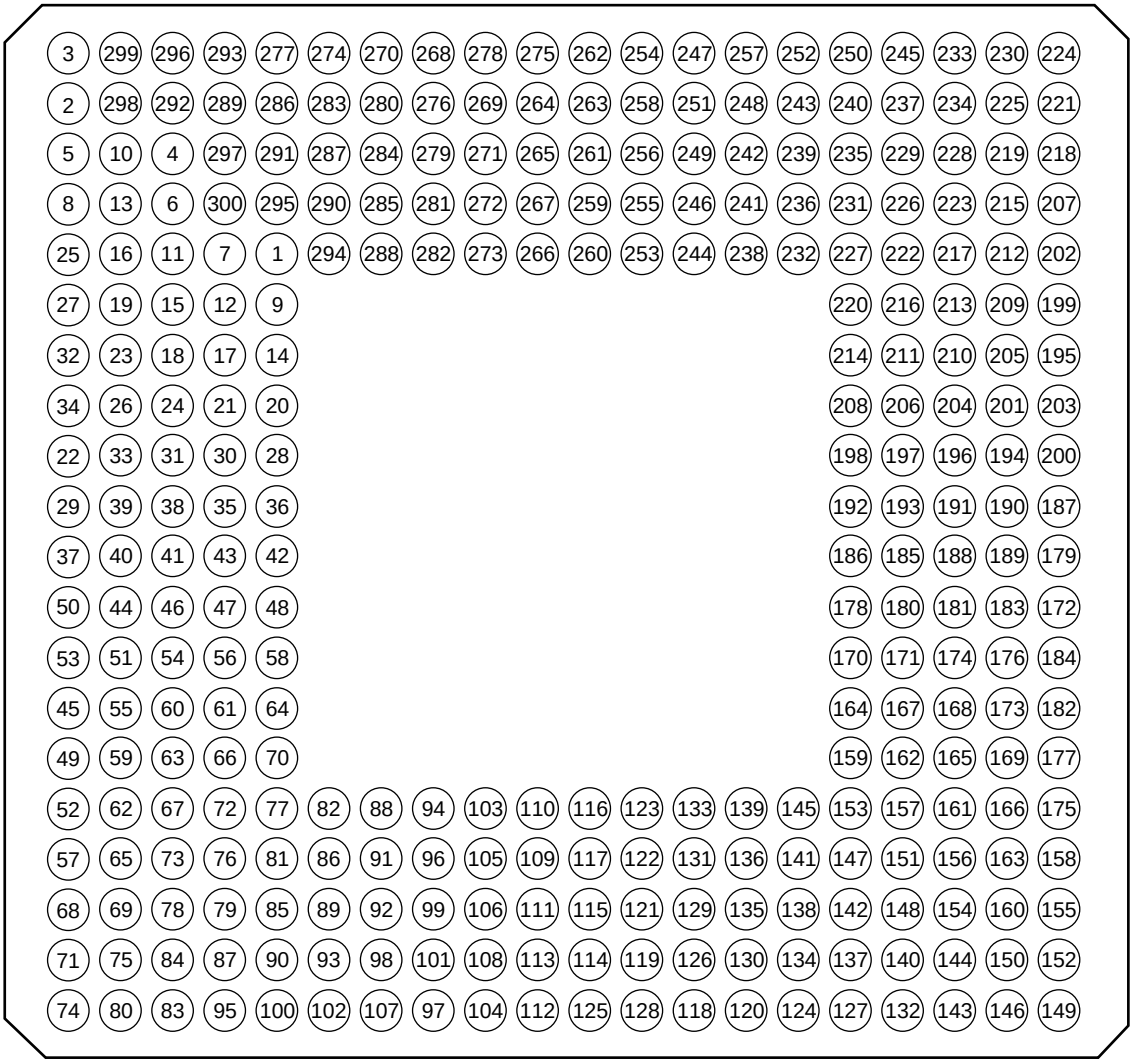
■ PRODUCT LINEUP

	MB91133	MB91F133	MB91FV130
CLASSIFICATION	MASK ROM device (mass production item)	FLASH ROM device (for evaluation)	Piggy/EVA device (for evaluation / development)
RAM capacity	6 KB	6 KB	6 KB
CROM capacity	254 KB	—	—
FLASH capacity	—	254 KB	254 KB
CRAM capacity	2 KB	2 KB	2 KB
Others	Mass production	Trial production	Provided

■ PIN ASSIGNMENTS

- **MB91FV130**

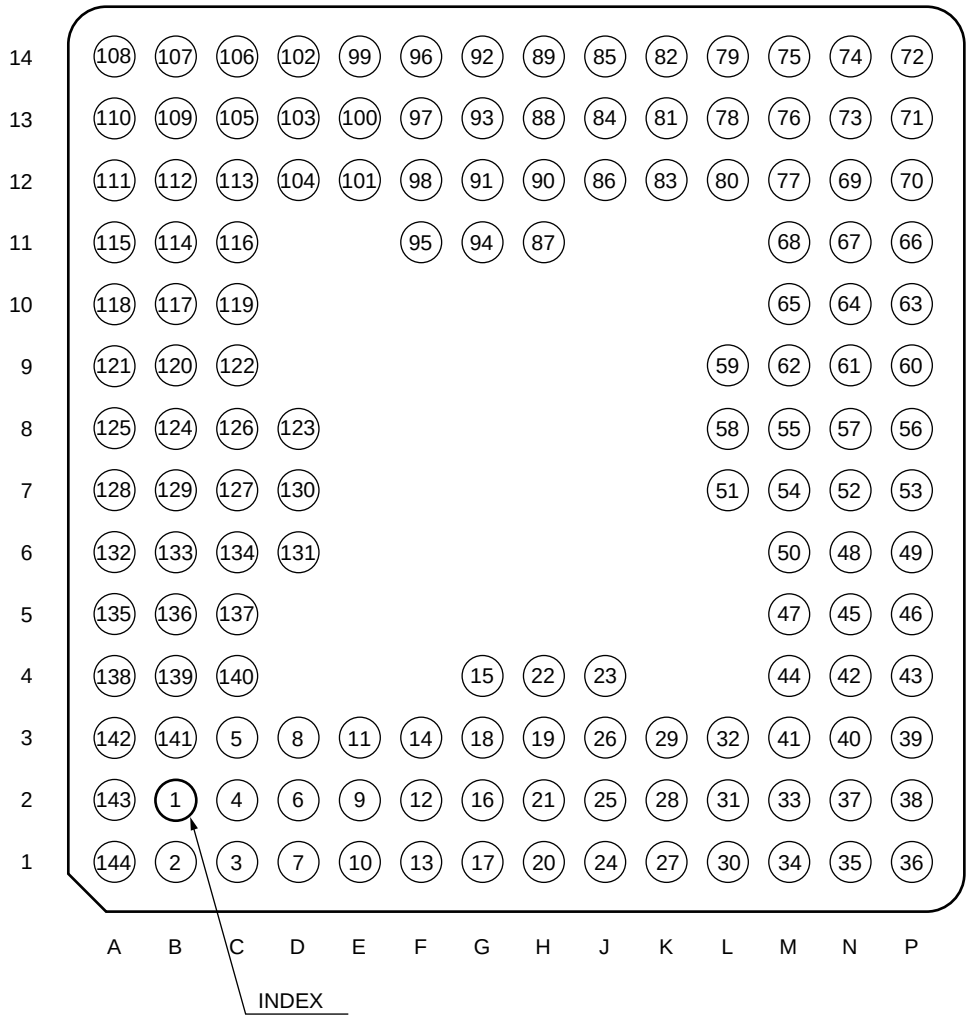
(BOTTOM VIEW)



(PGA-299C-A01)

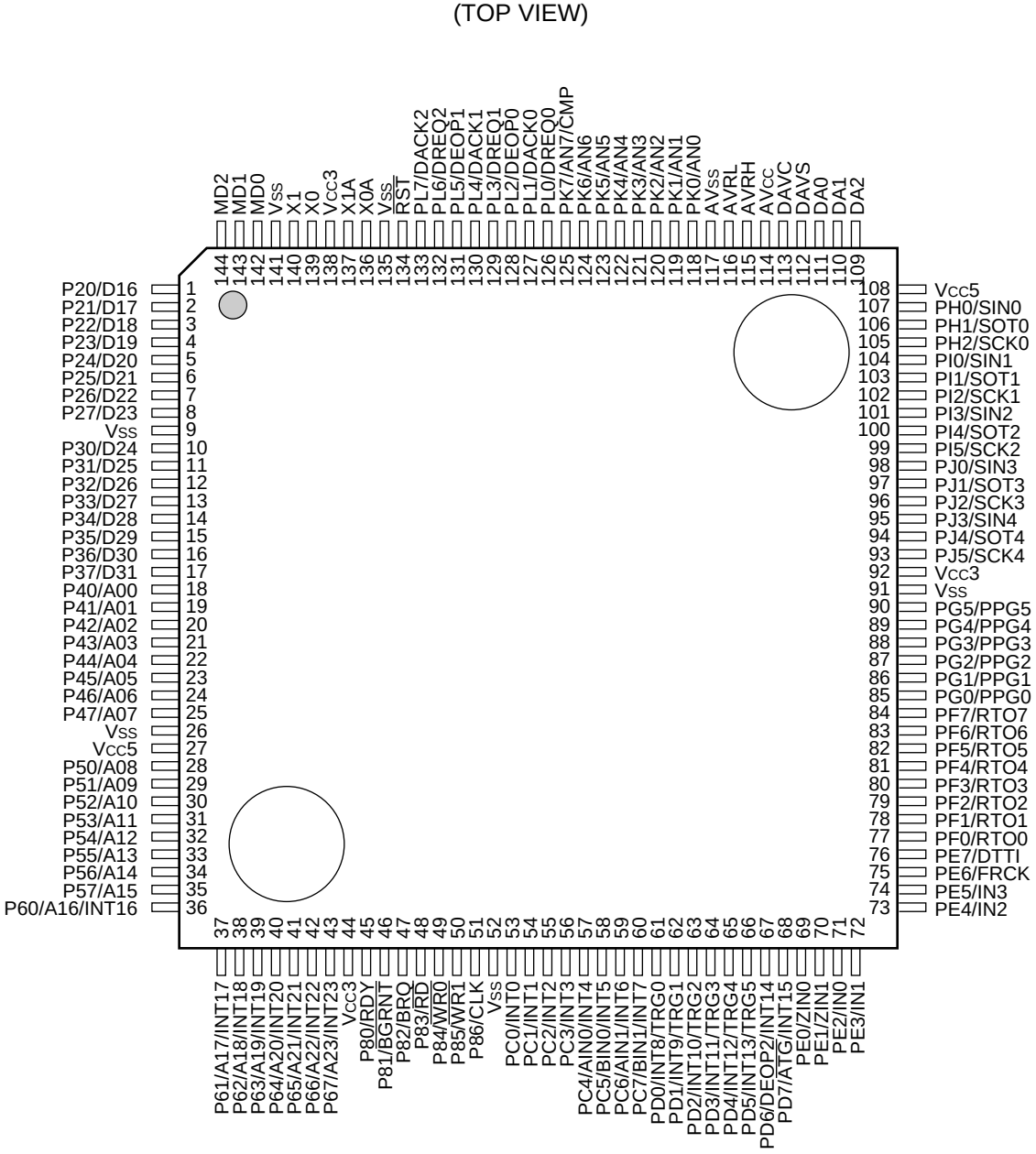
- **MB91F133/MB91133**

(TOP VIEW)



(BGA-144P-M01)

- **MB91F133/MB91133**



■ PIN NUMBERS LIST

• **Device : MB91FV130 Package : PGA-299C-A01**

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
1	P20/D16	35	P54/A12	69	N.C.	103	PK3/AN3
2	V_{SS}	36	P55/A13	70	N.C.	104	$V_{CC}5$
3	OPEN	37	$V_{CC}5$	71	V_{SS}	105	PK4/AN4
4	P21/D17	38	P56/A14	72	N.C.	106	PK5/AN5
5	$V_{CC}5$	39	P57/A15	73	N.C.	107	PK6/AN6
6	P22/D18	40	P60/A16/INT16	74	$V_{CC}5$	108	PK7/AN7/CMP
7	P23/D19	41	P61/A17/INT17	75	N.C.	109	DAVC
8	V_{SS}	42	P62/A18/INT18	76	MD0	110	DAVS
9	P24/D20	43	P63/A19/INT19	77	MD1	111	DA0
10	P25/D21	44	P64/A20/INT20	78	MD2	112	V_{SS}
11	P26/D22	45	P65/A21/INT21	79	$V_{CC}3$	113	DA1
12	P27/D23	46	P66/A22/INT22	80	V_{SS}	114	DA2
13	P30/D24	47	P67/A23/INT23	81	X0	115	PH0/SIN0
14	P31/D25	48	P80/RDY	82	X1	116	PH1/SOT0
15	P32/D26	49	$V_{CC}3$	83	$V_{CC}5$	117	PH2/SCK0
16	P33/D27	50	V_{SS}	84	$\overline{RST}$	118	PI0/SIN1
17	P34/D28	51	P81/$\overline{BGRNT}$	85	N.C.	119	PI1/SOT1
18	P35/D29	52	P82/BRQ	86	ICLK	120	PI2/SCK1
19	P36/D30	53	$V_{CC}5$	87	ICS0	121	PI3/SIN2
20	P37/D31	54	P83/$\overline{RD}$	88	ICS1	122	PI4/SOT2
21	P40/A00	55	P84/$\overline{WR0}$	89	ICS2	123	PI5/SCK2
22	$V_{CC}5$	56	P85/$\overline{WR1}$	90	ICD0	124	PJ0/SIN3
23	P41/A01	57	P86/CLK	91	ICD1	125	$V_{CC}5$
24	P42/A02	58	PL0/DREQ0	92	ICD2	126	PJ1/SOT3
25	P43/A03	59	PL1/DACK0	93	ICD3	127	PJ2/SCK3
26	P44/A04	60	PL2/DEOP0	94	BREAK	128	V_{SS}
27	P45/A05	61	PL3/DREQ1	95	AV_{CC}	129	$V_{CC}3$
28	P46/A06	62	PL4/DACK1	96	AVRH	130	X0A
29	V_{SS}	63	PL5/DEOP1	97	V_{SS}	131	X1A
30	P47/A07	64	PL6/DREQ2	98	AVRL	132	V_{SS}
31	P50/A08	65	PL7/DACK2	99	AV_{SS}	133	PJ3/SIN4
32	P51/A09	66	N.C.	100	PK0/AN0	134	PJ4/SOT4
33	P52/A10	67	N.C.	101	PK1/AN1	135	PJ5/SCK4
34	P53/A11	68	$V_{CC}5$	102	PK2/AN2	136	PC0/INT0

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No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
137	PC1/INT1	173	PF5/RTO5	209	$\overline{\text{TAD14}}$	245	TDT23	281	TDT53
138	PC2/INT2	174	PF6/RTO6	210	$\overline{\text{TAD15}}$	246	TDT24	282	TDT54
139	PC3/INT3	175	PF7/RTO7	211	$V_{CC}3$	247	V_{SS}	283	TDT55
140	PC4/INT4/AIN0	176	PG0/PPG0	212	$\overline{\text{TOE}}$	248	TDT25	284	TDT56
141	PC5/INT5/BIN0	177	PG1/PPG1	213	$\overline{\text{TCE1}}$	249	TDT26	285	TDT57
142	PC6/INT6/AIN1	178	PG2/PPG2	214	$\overline{\text{TADSC}}$	250	TDT27	286	$V_{CC}3$
143	$V_{CC}5$	179	V_{SS}	215	$\overline{\text{TWR}}$	251	TDT28	287	TDT58
144	PC7/INT7/BIN1	180	PG3/PPG3	216	TDT00	252	TDT29	288	TDT59
145	PD0/INT8/TRG0	181	PG4/PPG4	217	TDT01	253	TDT30	289	TDT60
146	V_{SS}	182	PG5/PPG5	218	V_{SS}	254	$V_{CC}5$	290	TDT61
147	PD1/INT9/TRG1	183	N.C.	219	TDT02	255	TDT31	291	TDT62
148	PD2/INT10/TRG2	184	N.C.	220	TDT03	256	TDT32	292	TDT63
149	$V_{CC}5$	185	N.C.	221	$V_{CC}5$	257	TDT33	293	$V_{CC}5$
150	PD3/INT11/TRG3	186	N.C.	222	TDT04	258	TDT34	294	TDT64
151	PD4/INT12/TRG4	187	$V_{CC}5$	223	TDT05	259	TDT35	295	TDT65
152	V_{SS}	188	EXRAM	224	V_{SS}	260	TDT36	296	V_{SS}
153	PD5/INT13/TRG5	189	TAD00	225	TDT06	261	TDT37	297	TDT66
154	PD6/INT14/DEOP2	190	TAD01	226	TDT07	262	V_{SS}	298	TDT67
155	$V_{CC}5$	191	TAD02	227	TDT08	263	TDT38	299	$V_{CC}5$
156	PD7/INT15/$\overline{\text{ATG}}$	192	TAD03	228	TDT09	264	TDT39	300	TDT68
157	PE0/ZIN0	193	$V_{CC}3$	229	TDT10	265	TDT40		
158	V_{SS}	194	TAD04	230	$V_{CC}5$	266	TDT41		
159	PE1/ZIN1	195	TAD05	231	TDT11	267	TDT42		
160	PE2/IN0	196	TAD06	232	TDT12	268	TDT43		
161	PE3/IN1	197	TAD07	233	V_{SS}	269	$V_{CC}3$		
162	PE4/IN2	198	TAD08	234	TDT13	270	TDT44		
163	PE5/IN3	199	TAD09	235	TDT14	271	TDT45		
164	PE6/FRCK	200	V_{SS}	236	TDT15	272	TDT46		
165	PE7/DTTI	201	TAD10	237	TDT16	273	TDT47		
166	$V_{CC}3$	202	TAD11	238	TDT17	274	TDT48		
167	PF0/RTO0	203	$V_{CC}5$	239	TDT18	275	$V_{CC}5$		
168	PF1/RTO1	204	TAD12	240	$V_{CC}3$	276	TDT49		
169	PF2/RTO2	205	TAD13	241	TDT19	277	TDT50		
170	PF3/RTO3	206	TAD14	242	TDT20	278	V_{SS}		
171	PF4/RTO4	207	TAD15	243	TDT21	279	TDT51		
172	$V_{CC}5$	208	TCLK	244	TDT22	280	TDT52		

- **Device : MB91F133/MB91133 Package : BGA-144P-M01/FPT-144P-M08**

LQFP	FBGA	Pin Name	LQFP	FBGA	Pin Name	LQFP	FBGA	Pin Name
1	B2	P20/D16	36	P1	P60/A16/INT16	71	P13	PE2/IN0
2	B1	P21/D17	37	N2	P61/A17/INT17	72	P14	PE3/IN1
3	C1	P22/D18	38	P2	P62/A18/INT18	73	N13	PE4/IN2
4	C2	P23/D19	39	P3	P63/A19/INT19	74	N14	PE5/IN3
5	C3	P24/D20	40	N3	P64/A20/INT20	75	M14	PE6/FRCK
6	D2	P25/D21	41	M3	P65/A21/INT21	76	M13	PE7/DTTI
7	D1	P26/D22	42	N4	P66/A22/INT22	77	M12	PF0/RTO0
8	D3	P27/D23	43	P4	P67/A23/INT23	78	L13	PF1/RTO1
9	E2	V_{SS}	44	M4	$V_{CC}3$	79	L14	PF2/RTO2
10	E1	P30/D24	45	N5	P80/RDY	80	L12	PF3/RTO3
11	E3	P31/D25	46	P5	P81/$\overline{\text{BGRNT}}$	81	K13	PF4/RTO4
12	F2	P32/D26	47	M5	P82/BRQ	82	K14	PF5/RTO5
13	F1	P33/D27	48	N6	P83/$\overline{\text{RD}}$	83	K12	PF6/RTO6
14	F3	P34/D28	49	P6	P84/$\overline{\text{WR0}}$	84	J13	PF7/RTO7
15	G4	P35/D29	50	M6	P85/$\overline{\text{WR1}}$	85	J14	PG0/PPG0
16	G2	P36/D30	51	L7	P86/CLK	86	J12	PG1/PPG1
17	G1	P37/D31	52	N7	V_{SS}	87	H11	PG2/PPG2
18	G3	P40/A00	53	P7	PC0/INT0	88	H13	PG3/PPG3
19	H3	P41/A01	54	M7	PC1/INT1	89	H14	PG4/PPG4
20	H1	P42/A02	55	M8	PC2/INT2	90	H12	PG5/PPG5
21	H2	P43/A03	56	P8	PC3/INT3	91	G12	V_{SS}
22	H4	P44/A04	57	N8	PC4/AIN0/INT4	92	G14	$V_{CC}3$
23	J4	P45/A05	58	L8	PC5/BIN0/INT5	93	G13	PJ5/SCK4
24	J1	P46/A06	59	L9	PC6/AIN1/INT6	94	G11	PJ4/SOT4
25	J2	P47/A07	60	P9	PC7/BIN1/INT7	95	F11	PJ3/SIN4
26	J3	V_{SS}	61	N9	PD0/INT8/TRG0	96	F14	PJ2/SCK3
27	K1	$V_{CC}5$	62	M9	PD1/INT9/TRG1	97	F13	PJ1/SOT3
28	K2	P50/A08	63	P10	PD2/INT10/TRG2	98	F12	PJ0/SIN3
29	K3	P51/A09	64	N10	PD3/INT11/TRG3	99	E14	PI5/SCK2
30	L1	P52/A10	65	M10	PD4/INT12/TRG4	100	E13	PI4/SOT2
31	L2	P53/A11	66	P11	PD5/INT13/TRG5	101	E12	PI3/SIN2
32	L3	P54/A12	67	N11	PD6/DEOP2/INT14	102	D14	PI2/SCK1
33	M2	P55/A13	68	M11	PD7/$\overline{\text{ATG}}$/INT15	103	D13	PI1/SOT1
34	M1	P56/A14	69	N12	PE0/ZIN0	104	D12	PI0/SIN1
35	N1	P57/A15	70	P12	PE1/ZIN1	105	C13	PH2/SCK0

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LQFP	FBGA	Pin Name	LQFP	FBGA	Pin Name
106	C14	PH1/SOT0	126	C8	PL0/DREQ0
107	B14	PH0/SIN0	127	C7	PL1/DACK0
108	A14	$V_{CC}5$	128	A7	PL2/DEOP0
109	B13	DA2	129	B7	PL3/DREQ1
110	A13	DA1	130	D7	PL4/DACK1
111	B12	DA0	131	D6	PL5/DEOP1
112	A12	DAVS	132	A6	PL6/DREQ2
113	C12	DAVC	133	B6	PL7/DACK2
114	B11	AV_{CC}	134	C6	$\overline{RST}$
115	A11	AVRH	135	A5	V_{SS}
116	C11	AVRL	136	B5	X0A
117	B10	AV_{SS}	137	C5	X1A
118	A10	PK0/AN0	138	A4	$V_{CC}3$
119	C10	PK1/AN1	139	B4	X0
120	B9	PK2/AN2	140	C4	X1
121	A9	PK3/AN3	141	B3	V_{SS}
122	C9	PK4/AN4	142	A3	MD0
123	D8	PK5/AN5	143	A2	MD1
124	B8	PK6/AN6	144	A1	MD2
125	A8	PK7/AN7/CMP			

■ PIN DESCRIPTIONS

Pin No.	Pin name	Circuit type	Function
1 2 3 4 5 6 7 8	D16/P20 D17/P21 D18/P22 D19/P23 D20/P24 D21/P25 D22/P26 D23/P27	C	**External data bus bits 16 to 23** Only valid for external bus 16-bit mode. Can be used as ports in single-chip and external bus 8-bit modes.
10 11 12 13 14 15 16 17	D24/P30 D25/P31 D26/P32 D27/P33 D28P34 D29/P35 D30/P36 D31/P37	C	**External data bus bits 24 to 31** Can be used as ports in single-chip mode.
18 19 20 21 22 23 24 25 28 29 30 31 32 33 34 35	A00/P40 A01/P41 A02/P42 A03/P43 A04/P44 A05/P45 A06/P46 A07/P47 A08/P50 A09/P51 A10/P52 A11/P53 A12/P54 A13/P55 A14/P56 A15/P57	F	**External address bus bits 0 to 15** Valid for external bus mode. Can be used as ports in single-chip mode.
36 37 38 39 40 41 42 43	A16/INT16/P60 A17/INT17/P61 A18/INT18/P62 A19/INT19/P63 A20/INT20/P64 A21/INT21/P65 A22/INT22/P66 A23/INT23/P67	O	**External address bus bits 16 to 23** [INT16 to 23] are external interruption request inputs 16 to 23. These inputs are always used when dealing with external interruptions is permitted, so output by ports should be stopped except when carried out intentionally. Can be used as ports when address bus and external interruption request input are not used.
45	RDY/P80	C	**External RDY input** This function is valid when external RDY input is permitted. “0” is input if the bus cycle being executed is not completed. Can be used as a port when the external RDY input is not used.

(Continued)

Pin No.	Pin name	Circuit type	Function
46	$\overline{\text{BGRNT}}$/P81	F	**External bus open reception output** This function is valid when external bus open reception output is permitted. “L” is output if the external bus is opened. Can be used as a port when the external bus open reception output is prohibited.
47	BRQ/P82	C	**External bus open request input** This function is valid when external bus open request input is permitted. “1” is input if the external bus requests to be opened. Can be used as a port when the external bus open request input is not used.
48	$\overline{\text{RD}}$/P83	F	**External bus read strobe output** This function is valid when external bus read strobe output is permitted. Can be used as a port when the external bus read strobe output is prohibited.
49	$\overline{\text{WR0}}$/P84	F	**External bus write strobe output** This function is valid in external bus mode. Can be used as a port in single-chip mode.
50	$\overline{\text{WR1}}$/P85	F	**External bus write strobe output** This function is valid in external bus mode and with 16-bit buses. Can be used as a port in single-chip mode or with external 8-bit bus.
51	CLK/P86	F	**System clock output** Outputs the same clock frequency as the external bus operation. Can be used as a port when it is not otherwise used.
53 54 55 56	INT0/PC0 INT1/PC1 INT2/PC2 INT3/PC3	H	**External interruption request inputs 0 to 3** These inputs are always used when dealing with external interruptions is permitted, so output by ports should be stopped except when carried out intentionally. Can be used to reset standby as input is permitted in this port under standby status.Can be used as ports when external interruption request input is not used.
57 58 59 60	AIN0/INT4/PC4 BIN0/INT5/PC5 AIN1/INT6/PC6 BIN1/INT7/PC7	H	**External interruption request inputs 4 to 7** These inputs are always used when dealing with external interruptions is permitted, so output by ports should be stopped except when carried out intentionally. Can be used to reset standby as input is permitted in these ports under standby status. **[AIN, BIN] Up/down timer input** This input is always used when input is permitted, so output by ports should be stopped except when carried out intentionally. Can be used as a port when external interruption request input and up/down timer input are not used.

(Continued)

Pin No.	Pin name	Circuit type	Function
61 62 63 64 65 66 67 68	TRG0/INT8/PD0 TRG1/INT9/PD1 TRG2/INT10/PD2 TRG3/INT11/PD3 TRG4/INT12/PD4 TRG5/INT13/PD5 DEOP2/INT14/PD6 $\overline{ATG}$/INT15/PD7	O	**External interruption request inputs 8 to 15** These inputs are always used when dealing with external interruptions is permitted, so output by ports should be stopped except when carried out intentionally. **[TRG0 to 5] These are external trigger inputs for PPG timers.** **[DEOP2] DMA external transfer termination output** This function is valid when external transfer termination output specification of the DMA controller is permitted. **[$\overline{ATG}$] A/D converter external trigger input** These inputs are always used when they are selected as A/D initiation factors, so output by ports should be stopped except when carried out intentionally. Can be used as ports when not otherwise used.
69 70	ZIN0/PE0 ZIN1/PE1	O	**Up/down timer input** These inputs are always used when input is permitted, so output by ports should be stopped except when carried out intentionally. Can be used as ports when up/down timer input is not used.
71 72 73 74	IN0/PE2 IN1/PE3 IN2/PE4 IN3/PE5	F	**Input capture input** This function is valid when input capture activates input. Can be used as ports when input capture input is not used.
75	FRCK/PE6	F	**External clock input pin of free-run timer** Can be used as a port when external clock input of free-run timer is not used.
76	DTTI/PE7	F	**RTOn pin level fixed input** Invalid when input is permitted in the waveform generation area. Can be used as a port when RTOn pin level fixed input is not used.
77 78 79 80 81 82 83 84	RTO0/PF0 RTO1/PF1 RTO2/PF2 RTO3/PF3 RTO4/PF4 RTO5/PF5 RTO6/PF6 RTO7/PF7	F	**Output compare event pins/waveform output pins in the waveform generation area** Can be used as ports when specification of the output compare event pin/waveform output pin of the waveform generation area is prohibited.
85 86 87 88 89 90	PPG0/PG0 PPG1/PG1 PPG2/PG2 PPG3/PG3 PPG4/PG4 PPG5/PG5	F	**PPG timer output** This function is valid when output specification of the PPG timer is permitted. Can be used as ports when output specification of the PPG timer is prohibited.
111 110 109	DA0 DA1 DA2	—	**D/A converter output** This function is valid when output specification of the D/A converter is permitted.

(Continued)

Pin No.	Pin name	Circuit type	Function
107	SIN0/PH0	P	**UART0 data input** This input is always used when UART0 activates input, so output by ports should be stopped except when carried out intentionally. Can be used as a port when UART0 data input is not used.
106	SOT0/PH1	P	**UART0 data output** This function is valid when UART0 data output specification is permitted. Can be used as a port when UART0 data output specification is prohibited.
105	SCK0/PH2	P	**UART0 clock input/output** This function is valid when UART0 clock output specification is permitted. Can be used as a port when UART0 clock output specification is prohibited.
104	SIN1/PI0	P	**UART1 data input** This input is always used when UART1 activates input, so output by ports should be stopped except when carried out intentionally. Can be used as a port when UART1 data input is not used.
103	SOT1/PI1	P	**UART1 data output** This function is valid when UART1 data output specification is permitted. Can be used as a port when UART1 data output specification is prohibited.
102	SCK1/PI2	P	**UART1 clock input/output** This function is valid when UART1 clock output specification is permitted. Can be used as a port when UART1 clock output specification is prohibited.
101	SIN2/PI3	P	**UART2 data input** This input is always used when UART2 activates input, so output by ports should be stopped except when carried out intentionally. Can be used as a port when UART2 data input is not used.
100	SOT2/PI4	P	**UART2 data output** This function is valid when UART2 data output specification is permitted. Can be used as a port when UART2 data output specification is prohibited.
99	SCK2/PI5	P	**UART2 clock input/output** This function is valid when UART2 clock output specification is permitted. Can be used as a port when UART2 clock output specification is prohibited.
98	SIN3/PJ0	P	**UART3 data input** This input is always used when UART3 activates input, so output by ports should be stopped except when carried out intentionally. Can be used as a port when UART3 data input is not used.
97	SOT3/PJ1	P	**UART3 data output** This function is valid when UART3 data output specification is permitted. Can be used as a port when UART3 data output specification is prohibited.

(Continued)

Pin No.	Pin name	Circuit type	Function
96	SCK3/PJ2	P	**UART3 clock input/output** This function is valid when UART3 clock output specification is permitted. Can be used as a port when UART3 clock output specification is prohibited.
95	SIN4/PJ3	P	**UART4 data input** This input is always used when UART4 activates input, so output by ports should be stopped except when carried out intentionally. Can be used as a port when UART4 data input is not used.
94	SOT4/PJ4	P	**UART4 data output** This function is valid when UART4 data output specification is permitted. Can be used as a port when UART4 data output specification is prohibited.
93	SCK4/PJ5	P	**UART4 clock input/output** This function is valid when UART4 clock output specification is permitted. Can be used as a port when UART4 clock output specification is prohibited.
118 119 120 121 122 123 124 125	AN0/PK0 AN1/PK1 AN2/PK2 AN3/PK3 AN4/PK4 AN5/PK5 AN6/PK6 CMP/AN7/PK7	N	**A/D converter analog input** This is valid when the AICK register specification is analog input. **[CMP] level comparator input** Can be used as ports when A/D converter analog input is not used.
126	DREQ0/PL0	F	**DMA external transfer request input** This input is always used if selected as the transfer factor for the DMA controller, so output by ports should be stopped except when carried out intentionally. Can be used as a port when DMA external transfer request input is not used.
127	DACK0/PL1	F	**DMA external transfer request reception output** This function is valid when external transfer request reception output specification of the DMA controller is permitted. Can be used as a port when transfer request reception output specification of the DMA controller is prohibited.
128	DEOP0/PL2	F	**DMA external transfer termination output** This function is valid when external transfer termination output specification of the DMA controller is permitted.
129	DREQ1/PL3	F	**DMA external transfer request input** This input is always used if selected as the transfer factor for the DMA controller, so output by ports should be stopped except when carried out intentionally. Can be used as a port when DMA external transfer request input is not used.

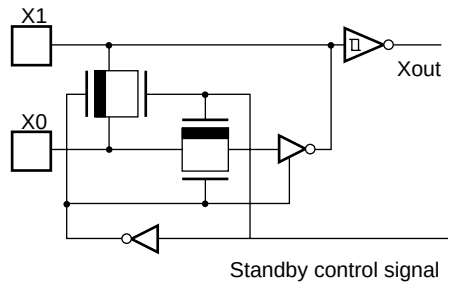
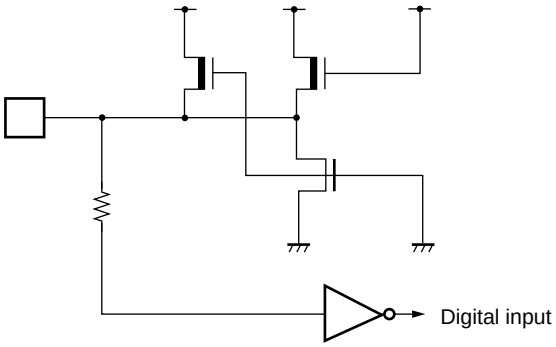
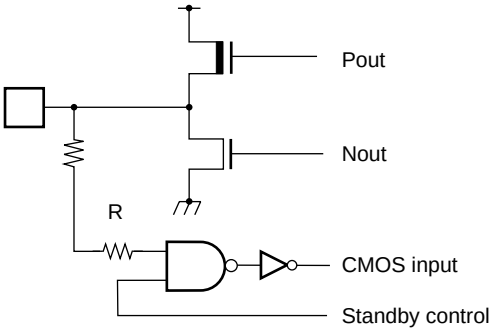
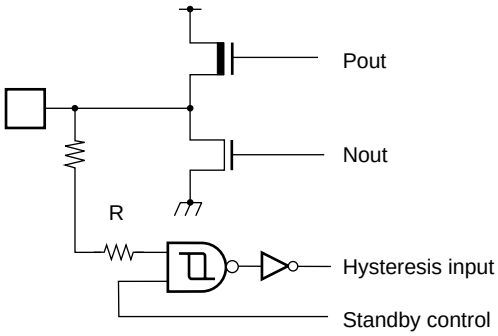
(Continued)

(Continued)

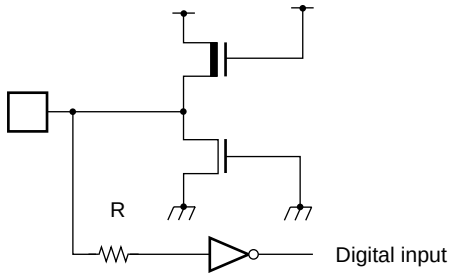
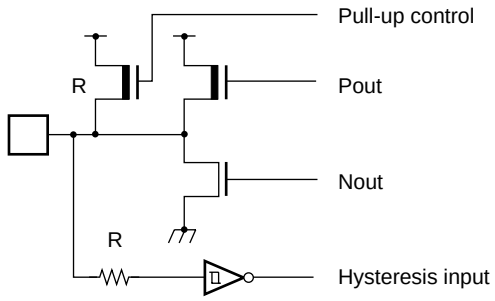
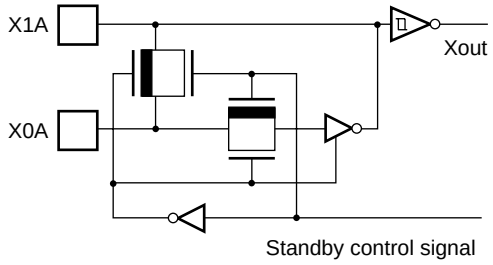
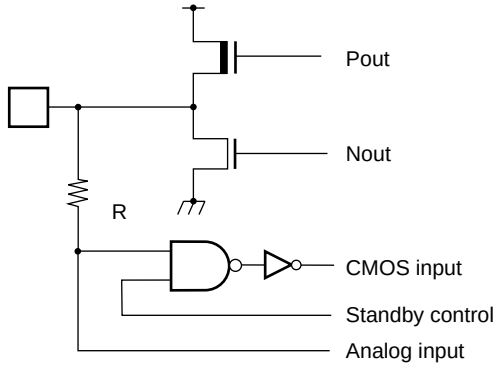
Pin No.	Pin name	Circuit type	Function
130	DACK1/PL4	F	**DMA external transfer request reception output** This function is valid when external transfer request reception output specification of the DMA controller is permitted. Can be used as a port when transfer request reception output specification of the DMA controller is prohibited.
131	DEOP1/PL5	F	**DMA external transfer termination output** This function is valid when external transfer termination output specification of the DMA controller is permitted.
132	DREQ2/PL6	F	**DMA external transfer request input** This input is always used if selected as the transfer factor for the DMA controller, so output by ports should be stopped except when carried out intentionally. Can be used as a port when DMA external transfer request input is not used.
133	DACK2/PL7	F	**DMA external transfer request reception output** This function is valid when external transfer request reception output specification of the DMA controller is permitted. Can be used as a port when transfer request reception output specification of the DMA controller is prohibited.
134	$\overline{\text{RST}}$	B	**External reset input**
136 137	X0A X1A	K	**Oscillation pin for low-speed clock (32 kHz)**
139 140	X0 X1	A	**Oscillation pin for high-speed clock (16.5 MHz)**
142 143 144	MD0 MD1 MD2	G	**Mode pins** Basic MCU operation mode is set by these pins. They should be directly connected to V_{CC} or V_{SS} for use.
112	DAVS	—	**Ground pin of D/A converter (connected to analog ground)**
113	DAVC	—	**Power pin of D/A converter**
114	AV_{CC}	—	**Power pin for A/D converter**
115	AVRH	—	**Reference voltage pin for A/D converter (high electric potential side)** When this pin is turned on/off, AVRH or more electric potential must be supplied to V_{CC}.
116	AVRL	—	**Reference voltage pin for A/D converter (low electric potential side)**
117	AV_{SS}	—	**Ground pin for A/D converter (connected to analog ground)**
27, 108	$V_{CC}5$	—	**5 V power of digital circuit** Power must be connected to all $V_{CC}5$ pins for use.
44, 92 138	$V_{CC}3$	—	**3 V power of digital circuit** Power must be connected to all $V_{CC}3$ pins for use.
9, 26, 52, 91, 135, 141	V_{SS}	—	**Ground level of digital circuit**

Note : In most of the above pins, the input/output of the I/O ports and resources are multiplexed, such as xxxx/Pxx. If the output from ports and resources of those pins compete with each other, the resource is given priority.

■ INPUT/OUTPUT CIRCUIT TYPES

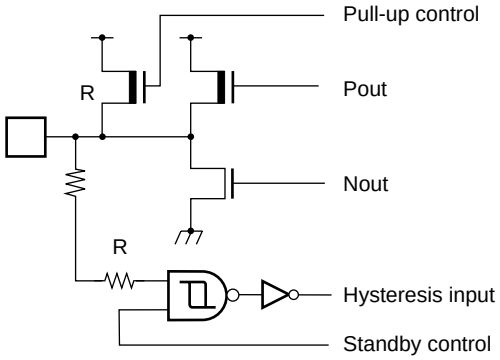
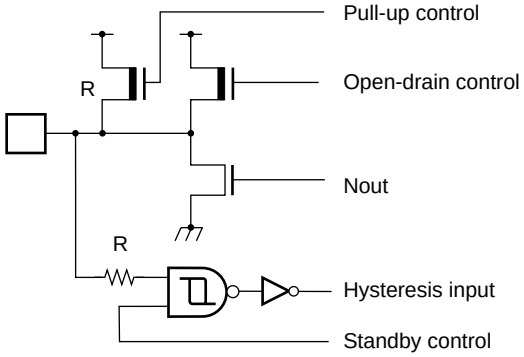
Type	Circuit	Remarks
A		• High-speed oscillation circuit (16.5 MHz) Oscillation feedback resistance = approximately 1 MΩ 3 V CMOS level input
B		• With pull up resistance CMOS level input Pull-up resistance value = approximately 25 kΩ (Typ.)
C		• CMOS level input/output pin CMOS level output CMOS level input (with standby control) I_{OL} = 4 mA
F		• CMOS hysteresis input/output pin CMOS level output CMOS hysteresis input (with standby control) I_{OL} = 4 mA

(Continued)

Type	Circuit	Remarks
G		• CMOS level input pin CMOS level input (without standby control) I_{OL} = 4 mA
H		• CMOS hysteresis input/output pin with pull- up control CMOS level output CMOS hysteresis input (without standby control) Pull-up resistance value = approximately 50 kΩ (Typ.) I_{OL} = 4 mA
K		• Clock oscillation circuit (32 kHz) Oscillation feedback resistance = approximately 4.5 MΩ/3 V 3 V CMOS level input
N		• Analog/CMOS level input/output pin CMOS level output CMOS level input (with standby control) Analog input (Analog input is valid when bit dealt by AIC is “1”.) I_{OL} = 4 mA

(Continued)

(Continued)

Type	Circuit	Remarks
O		• CMOS hysteresis input/output pin with pull-up control CMOS level output CMOS hysteresis input (with standby control) Pull-up resistance value = approximately 50 kΩ (Typ.) I_{OL} = 4 mA
P		• CMOS hysteresis input/output pin with pull-up control CMOS level output (with open-drain control) CMOS hysteresis input (with standby control) Pull-up resistance value = approximately 50 kΩ (Typ) I_{OL} = 4 mA

■ HANDLING DEVICES

1. Points to Note on Handling Devices

(1) Latch-up prevention

Latch-up may occur by CMOS IC if a voltage in excess of $V_{CC}5$ or lower than V_{SS} is applied to the input/output pins, or if the voltage exceeds the rating between $V_{CC}5$ and V_{SS}. If latch-up occurs, the electrical current increases significantly and may destroy certain components due to excessive heat, so great care must be taken to ensure that the maximum rating is not exceeded during use.

(2) Handling Pins

- **Handling unused pins**
  Input pins that are not used should be pulled up or down as they may cause erroneous operations if left open.

- **Handling N.C. pins**
  N.C. pins must be opened for use.

- **Handling output pins**
  Excessive electric current may flow if the output pin is shorted by the power source or other output pins, or connected to large loads. If such status is prolonged, the device is liable to be damaged, so great care must be taken to ensure that the usage volume does not exceed the maximum rating.

- **Mode pins (MD0 to MD2)**
  Those pins must be directly connected to $V_{CC}5$ or V_{SS} for use.
  Pattern lengths between $V_{CC}5$ or V_{SS} and each mode pin on the printed-circuit board should be arranged to be as short as possible to prevent the test mode from being erroneously turned on due to noise, and they should be connected with low impedance.

- **Power pins**
  When there are a number of $V_{CC}5/V_{CC}3/V_{SS}$, those whose electrical potential must be the same within the device are connected to prevent erroneous operation such as latch-up for device design purposes, but those must be externally connected to a power source and earthed to follow the general output current standard and prevent erroneous operation of strobe signals due to increased ground level and reduction in unnecessary radiation.
  Care must also be taken to ensure that they are connected to the $V_{CC}5/V_{SS}$ or $V_{CC}3/V_{SS}$ of this device at the lowest possible impedance from the source of the electrical current supply.
  Furthermore, it is recommended that a ceramic capacitor of around 0.1 μF be used to connect the $V_{CC}5$ and V_{SS}, or $V_{CC}3$ and V_{SS} near the device as a bypass capacitor.

- **Crystal oscillation circuits**
  Noise near the X0, X1, X0A or X1A pins can cause erroneous operation. The printed-circuit board must be designed so that the X0, X1, X0A and X1A pins, crystal oscillator (or ceramic oscillator) and bypass capacitor to the ground can be arranged as close as possible.
  Also, a printed-circuit board with grounded artwork enclosing the X0, X1, X0A and X1A pins is strongly recommended to ensure stable operation.

(3) Points to note on usage

- **External reset input**
  "L" level should be input to the $\overline{RST}$ pin, which is required for at least five machine cycles to ensure that the internal status is reset.

- **Oscillation pin**
  Oscillation pin is 3 V CMOS input level.

- **External clock**
  Use with an external clock is prohibited. A crystal (or ceramic) oscillator should be used.

- **Analog Power**
  The AV_{CC} should always be used at the same electric potential as $V_{CC}5$. If the $V_{CC}5$ is larger than the AV_{CC}, electricity may flow through pins AN 0 to AN 7.

- **Points to note for using level comparator**
  When the level comparator is used, a reference current (IR) flows even though it is stopped. The stop mode must be turned on after prohibiting action of the level comparator.

2. Points to Note on Turning On Power

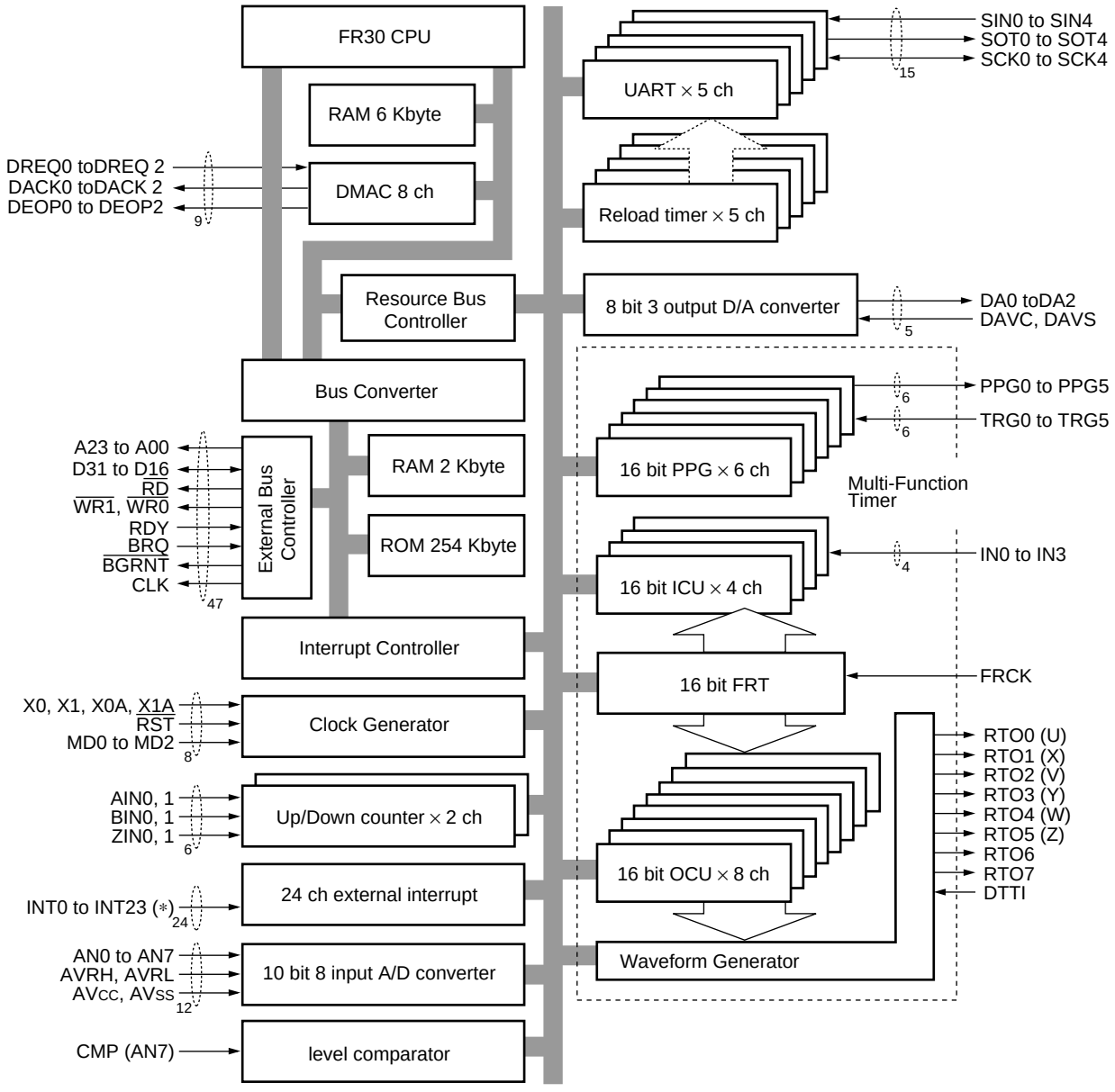
- **$\overline{RST}$ pin handling**
  The $\overline{RST}$ pin must be started from "L" level when the power is turned on, and when the power is adjusted to the V_{DD} level, it should be changed to the "H" level after being left on for at least 5 cycles of the internal operation clock.

- **Original oscillation input**
  The clock must be input until the waiting status for oscillation stability is reset in the event that power is turned on.

- **Power on reset**
  "Power on reset" must be executed if power is turned on, but the power voltage falls below the guaranteed operating temperature and power is turned on again.

- **Order for turning on power**
  Power should be turned on in the following order.
  $V_{CC}3 \rightarrow V_{CC}5 \rightarrow AV_{CC} \rightarrow$ AVRH
  The opposite order should be used when turning off.

■ BLOCK DIAGRAM



* : INT23 to INT16 share pins with A23 to A16
* : INT15 shares pins with $\overline{ATG}$
* : INT14 shares pins with DEOP2
* : INT13 to INT8 share pins with TRG5 to TRG0
* : INT7 to INT4 share pins with AIN0, BIN0, AIN1 and BIN1

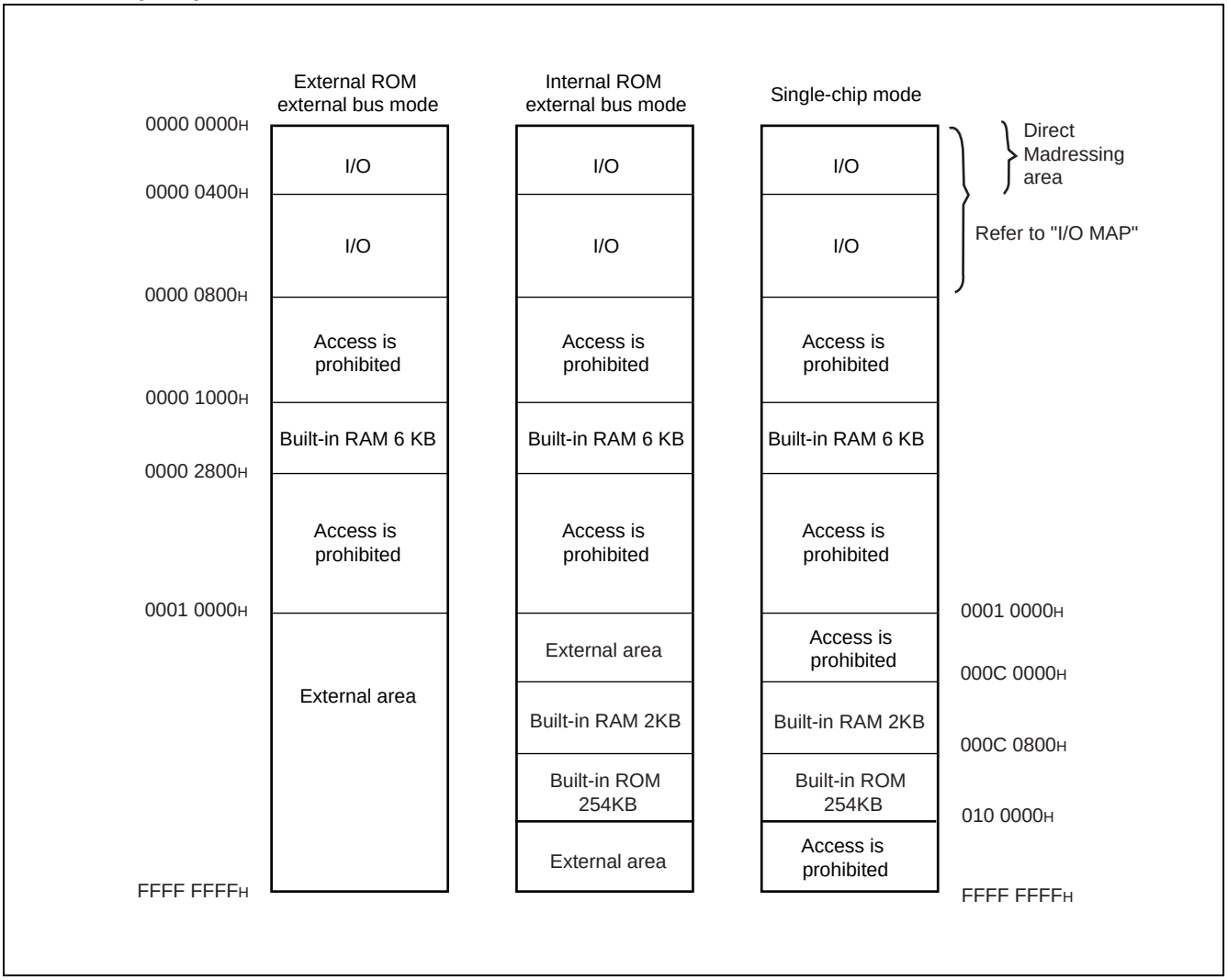
The total number of above pins is 133. The remainder (144 – 133 = 11 pins) are $V_{CC}5$, $V_{CC}3$ and V_{SS}.

■ CPU

1. Memory Space

The FR series has 4 Gbytes (2^{32} addresses) of logic address space which the CPU accesses linearly.

- **Memory Map**



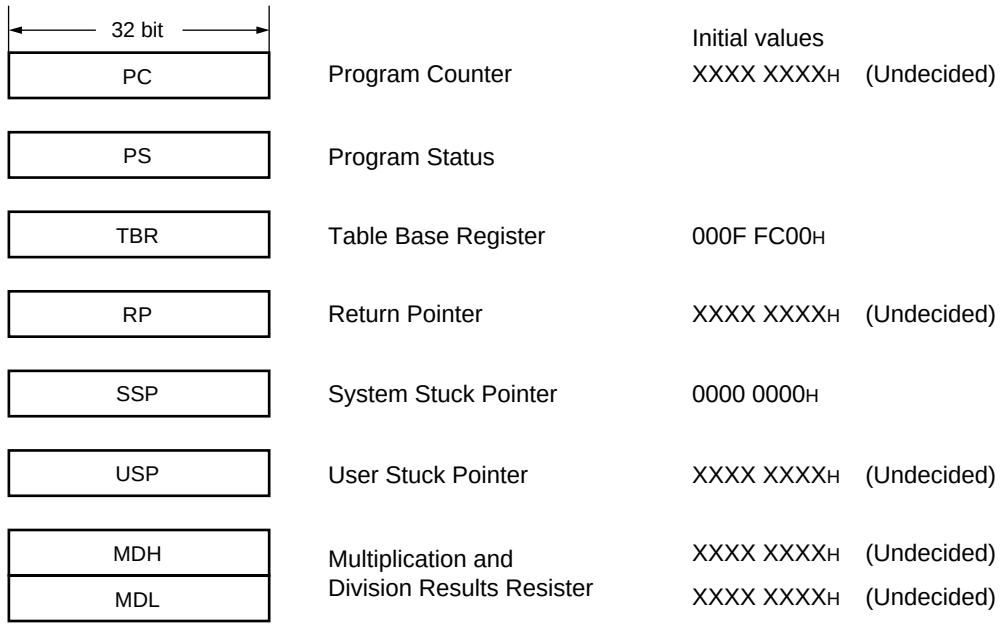
* : It is impossible to access the external area on single-chip mode. When accessing the external area, select the internal ROM external bus mode.

2. Registers

There are two types of multi-purpose registers in the FR family. One is a dedicated purpose register that exists within the CPU and the other is a multi-purpose register that exists in the memory.

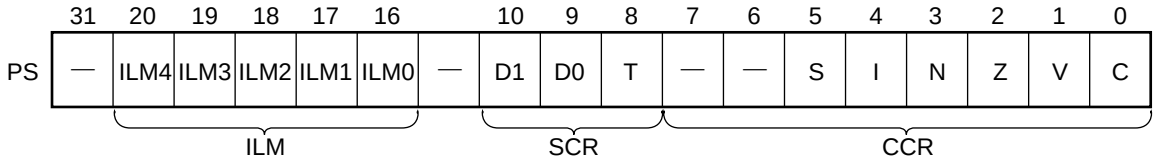
- **Dedicated Registers**

Program Counter (PC)	:	32-bit length; indicates instruction storage position.
Program Status (PS)	:	32-bit length; stores register pointers and condition codes.
Table Base Register (TBR)	:	Holds the starting address of the vector table to be used for Exception, Interruption and Trapping (EIT) .
Return Pointer (RP)	:	Holds the address to return to from the sub-routine.
System Stuck Pointer (SSP)	:	Indicates the system stuck position.
User Stuck Pointer (USP)	:	Indicates the user's stuck position.
Multiplication and Division Results Resister (MDH/MDL)	:	32-bit length; act as registers for multiplication and division.



- **Program Status (PS)**

PS is the register that holds the program status and is classified into three categories, namely, Condition Code Register (CCR) , System Condition Code Register (SCR) and Interruption Level Master Register (ILM) .



- **Condition Code Register (CCR)**
  - S flag : Specifies the stuck pointer to be used as R15.
  - I flag : Controls permission and prohibition of user interruption requests.
  - N flag : Indicates codes when computation results are defined as integers that are expressed in complements of 2.
  - Z flag : Indicates whether or not a result of the computation is “0” .
  - V flag : Operands used for computation are defined as integers expressed in complements of 2, and indicate whether or not an overflow is generated as a result of the computation.
  - C flag : Indicates whether carrying or borrowing is generated from the highest bit as a result of the computation.

- **System Condition Code Register (SCR)**
  - T flag : Specifies whether or not the step trace trap will be valid.

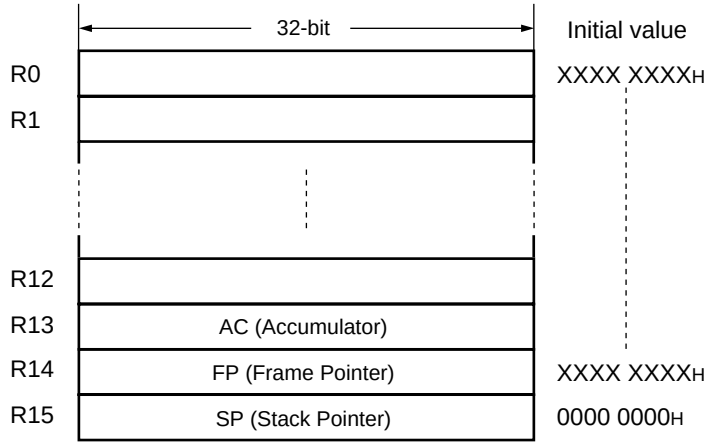
- **Interruption Level Mask Register** (**ILM**)
  - ILM4 to ILM0 : Holds the interruption level mask values, and those values that are held by the ILM are used for the level mask. Interruption requests can be accepted only when the interruption levels handled within the interruption requests to be input into the CPU are stronger than the levels shown by the ILM.

ILM4	ILM3	ILM2	ILM1	ILM0	Interruption level	Strength
0	0	0	0	0	0	Strong
		⋮			⋮	↕
0	1	0	0	0	15	
		⋮			⋮	
1	1	1	1	1	31	Weak

■ MULTI-PURPOSE REGISTERS

The multi-purpose registers are CPU registers R0 to R15 which are used as accumulators for various computations and memory access pointers (fields that indicate the address) .

- **Register bank configuration**



Special purposes are assumed for the following 3 of the 16 registers. Thus, some instructions are emphasized.

R13 : Virtual accumulator (AC)
R14 : Frame Pointer (FP)
R15 : Stack Pointer (SP)

Initial values for R0 to R14 on resetting are unspecified. The initial value of R15 will be 0000 0000H (SSP value) .

■ MODE SETTING

1. Pins

• **Mode pins and set mode**

Mode pins			Mode name	Reset vector access areas	External data bus width	Bus modes
MD2	MD1	MD0				
0	0	0	External vector mode 0	External	8-bit	External ROM external bus mode
0	0	1	External vector mode 1	External	16-bit	
0	1	0	—	—	—	Setting is prohibited
0	1	1	Internal vector mode	Internal	(Mode register)	Single chip mode
1	—	—	—	—	—	Usage is prohibited

2. Register

Mode register (MODR) and set mode

Address
0000 07FF$_H$

M1	M0	*	*	*	*	*	*

Bus mode set bit

Initial value XXXX XXXX$_B$ Access W

W : Write only
X : Undecided
* : “0” should always be written for bits other than M1 and M0.

• **Bus mode set bit and its functions**

M1	M0	Functions	Remarks
0	0	Single chip mode	
0	1	Internal ROM external bus mode	
1	0	External ROM external bus mode	
1	1	—	Setting is prohibited

■ I/O MAP

Address	Register				Block
	+0	+1	+2	+3	
000000H	PDR3 (R/W) XXXXXXXX	PDR2 (R/W) XXXXXXXX	—		Port Data Register
000004H	—	PDR6 (R/W) XXXXXXXX	PDR5 (R/W) XXXXXXXX	PDR4 (R/W) XXXXXXXX	
000008H	—	—	—	PDR8 (R/W) -XXXXXXX	
00000CH	—				
000010H	PDRF (R/W) XXXXXXXX	PDRE (R/W) XXXXXXXX	PDRD (R/W) XXXXXXXX	PDRC (R/W) XXXXXXXX	
000014H	PDRJ (R/W) --XXXXXX	PDRI (R/W) --XXXXXX	PDRH (R/W) -----XXX	PDRG (R/W) --XXXXXX	
000018H	LVLC (R/W) XXXX0000	—	PDRL (R/W) XXXXXXXX	PDRK (R/W) XXXXXXXX	Level Comparator
00001CH	SSR0 (R/W) 00001-00	SIDR0/SODR0 (R/W) XXXXXXXX	SCR0 (R/W) 00000100	SMR0 (R/W) 00000-00	UART0
000020H	SSR1 (R/W) 00001-00	SIDR1/SODR1 (R/W) XXXXXXXX	SCR1 (R/W) 00000100	SMR1 (R/W) 00000-00	UART1
000024H	SSR2 (R/W) 00001-00	SIDR2/SODR2 (R/W) XXXXXXXX	SCR2 (R/W) 00000100	SMR2 (R/W) 00000-00	UART2
000028H	TMRLR (W) XXXXXXXX XXXXXXXX		TMR (R) XXXXXXXX XXXXXXXX		Reload Timer 0
00002CH	—		TMCSR (R/W) ----0000 00000000		
000030H	TMRLR (W) XXXXXXXX XXXXXXXX		TMR (R) XXXXXXXX XXXXXXXX		Reload Timer 1
000034H	—		TMCSR (R/W) ----0000 00000000		
000038H	ADCR (R/W) 00101-XX XXXXXXXX		ADCS1 (R/W) 00000000	ADCS0 (R/W) 00000000	A/D Converter (Sequential type)
00003CH	TMRLR (W) XXXXXXXX XXXXXXXX		TMR (R) XXXXXXXX XXXXXXXX		Reload Timer 2
000040H	—		TMCSR (R/W) ----0000 00000000		

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000044H	IPCP1 (R) XXXXXXXX XXXXXXXX		IPCP0 (R) XXXXXXXX XXXXXXXX		16-bit ICU
000048H	IPCP3 (R) XXXXXXXX XXXXXXXX		IPCP2 (R) XXXXXXXX XXXXXXXX		
00004CH	—	ICS23 (R/W) 0 0 0 0 0 0 0 0	—	ICS01 (R/W) 0 0 0 0 0 0 0 0	
000050H	—				Reserved
000054H	OCCP1 (R/W) XXXXXXXX XXXXXXXX		OCCP0 (R/W) XXXXXXXX XXXXXXXX		16-bit OCU
000058H	OCCP3 (R/W) XXXXXXXX XXXXXXXX		OCCP2 (R/W) XXXXXXXX XXXXXXXX		
00005CH	OCCP5 (R/W) XXXXXXXX XXXXXXXX		OCCP4 (R/W) XXXXXXXX XXXXXXXX		
000060H	OCCP7 (R/W) XXXXXXXX XXXXXXXX		OCCP6 (R/W) XXXXXXXX XXXXXXXX		
000064H	OCS32 (R/W) XXX 0 0 0 0 0 0 0 0 0 0 XX 0 0		OCS10 (R/W) XXX 0 0 0 0 0 0 0 0 0 0 XX 0 0		
000068H	OCS76 (R/W) XXX 0 0 0 0 0 0 0 0 0 0 XX 0 0		OCS54 (R/W) XXX 0 0 0 0 0 0 0 0 0 0 XX 0 0		
00006CH	TCDT (R/W) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		TCCS (R/W) 0------- 0 0 0 0 0 0 0 0		16-bit Free-run Timer
000070H	SSR3 (R/W) 0 0 0 0 1 0 0 0	SIDR3/SODR3 (R/W) XXXXXXXX	SCR3 (R/W) 0 0 0 0 0 1 0 0	SMR3 (R/W) 0 0 0 0 0-0 0	UART3
000074H	SSR4 (R/W) 0 0 0 0 1 0 0 0	SIDR4/SODR4 (R/W) XXXXXXXX	SCR4 (R/W) 0 0 0 0 0 1 0 0	SMR4 (R/W) 0 0 0 0 0-0 0	UART4
000078H	CDCR1 (R/W) 0 - - - 0 0 0 0	—	CDCR0 (R/W) 0 - - - 0 0 0 0	—	Communication Pre-scalar
00007CH	CDCR3 (R/W) 0 - - - 0 0 0 0	—	CDCR2 (R/W) 0 - - - 0 0 0 0	—	
000080H	—		CDCR4 (R/W) 0 - - - 0 0 0 0	—	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000084H	RCR1 (W) 0 0 0 0 0 0 0 0	RCR0 (W) 0 0 0 0 0 0 0 0	UDCR1 (R) 0 0 0 0 0 0 0 0	UDCR0 (R) 0 0 0 0 0 0 0 0	8-/16-bit U/D Counter
000088H	CCRH0 (R/W) 0 0 0 0 0 0 0 0	CCRL0 (R/W) -0 0 0 1 0 0 0	—	CSR0 (R/W) 0 0 0 0 0 0 0 0	
00008CH	CCRH1 (R/W) -0 0 0 0 0 0 0	CCRL1 (R/W) -0 0 0 1 0 0 0	—	CSR1 (R/W) 0 0 0 0 0 0 0 0	
000090H	—				Reserved
000094H	EIRR0 (R/W) 0 0 0 0 0 0 0 0	ENIR0 (R/W) 0 0 0 0 0 0 0 0	EIRR1 (R/W) 0 0 0 0 0 0 0 0	ENIR1 (R/W) 0 0 0 0 0 0 0 0	Ext Int
000098H	ELVR0 (R/W) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		ELVR1 (R/W) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
00009CH	EIRR2 (R/W) 0 0 0 0 0 0 0 0	ENIR2 (R/W) 0 0 0 0 0 0 0 0	—		
0000A0H	ELVR2 (R/W) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		—		
0000A4H	—	DACR2 (R/W) -------0	DACR1 (R/W) -------0	DACR0 (R/W) -------0	D/A Converter
0000A8H	—	DADR2 (R/W) XXXXXXXX	DADR1 (R/W) XXXXXXXX	DADR0 (R/W) XXXXXXXX	
0000ACH	DTCR1 (R/W) 0 0 0 0 0 0 0 0	TMRR1 (R/W) XXXXXXXX	DTCR0 (R/W) 0 0 0 0 0 0 0 0	TMRR0 (R/W) XXXXXXXX	Waveform Generator
0000B0H	—	SIGCR (R/W) 0 0 0 0 0 0 0 0	DTCR2 (R/W) 0 0 0 0 0 0 0 0	TMRR2 (R/W) XXXXXXXX	
0000B4H to 0000BCH	—				Reserved
0000C0H	—	PCRE (R/W) ------0 0	PCRD (R/W) 0 0 0 0 0 0 0 0	PCRC (R/W) 0 0 0 0 0 0 0 0	Pull-up Control
0000C4H	PCRJ (R/W) --0 0 0 0 0 0	PCRI (R/W) --0 0 0 0 0 0	PCRH (R/W) -----0 0 0	—	
0000C8H	OCRJ (R/W) --0 0 0 0 0 0	OCRI (R/W) --0 0 0 0 0 0	OCRH (R/W) -----0 0 0	—	Open-drain Control
0000CCH	—	—	—	AICK (R/W) 0 0 0 0 0 0 0 0	Analog Input Control

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0000D0H	DDRF (R/W) 0 0 0 0 0 0 0 0	DDRE (R/W) 0 0 0 0 0 0 0 0	DDRD (R/W) 0 0 0 0 0 0 0 0	DDRC (R/W) 0 0 0 0 0 0 0 0	Data Direction Register
0000D4H	DDRJ (R/W) - - 0 0 0 0 0 0	DDRI (R/W) - - 0 0 0 0 0 0	DDRH (R/W) - - - - - 0 0 0	DDRG (R/W) - - 0 0 0 0 0 0	
0000D8H	—	—	DDRL (R/W) 0 0 0 0 0 0 0 0	DDRK (R/W) 0 0 0 0 0 0 0 0	
0000DCH	GCN1 (R/W) 0 0 1 1 0 0 1 0 0 0 0 1 0 0 0 0		—	GCN2 (R/W) 0 0 0 0 0 0 0 0	PPG ctl
0000E0H	PTMR0 (R) 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		PCSR0 (W) XXXXXXXX XXXXXXXX		PPG0
0000E4H	PDUT0 (W) XXXXXXXX XXXXXXXX		PCNH0 (R/W) 0 0 0 0 0 0 0 -	PCNL0 (R/W) 0 0 0 0 0 0 0 0	
0000E8H	PTMR1 (R) 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		PCSR1 (W) XXXXXXXX XXXXXXXX		PPG1
0000ECH	PDUT1 (W) XXXXXXXX XXXXXXXX		PCNH1 (R/W) 0 0 0 0 0 0 0 -	PCNL1 (R/W) 0 0 0 0 0 0 0 0	
0000F0H	PTMR2 (R) 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		PCSR2 (W) XXXXXXXX XXXXXXXX		PPG2
0000F4H	PDUT2 (W) XXXXXXXX XXXXXXXX		PCNH2 (R/W) 0 0 0 0 0 0 0 -	PCNL2 (R/W) 0 0 0 0 0 0 0 0	
0000F8H	PTMR3 (R) 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		PCSR3 (W) XXXXXXXX XXXXXXXX		PPG3
0000FCH	PDUT3 (W) XXXXXXXX XXXXXXXX		PCNH3 (R/W) 0 0 0 0 0 0 0 -	PCNL3 (R/W) 0 0 0 0 0 0 0 0	
000100H	PTMR4 (R) 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		PCSR4 (W) XXXXXXXX XXXXXXXX		PPG4
000104H	PDUT4 (W) XXXXXXXX XXXXXXXX		PCNH4 (R/W) 0 0 0 0 0 0 0 -	PCNL4 (R/W) 0 0 0 0 0 0 0 0	
000108H	PTMR5 (R) 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		PCSR5 (W) XXXXXXXX XXXXXXXX		PPG5
00010CH	PDUT5 (W) XXXXXXXX XXXXXXXX		PCNH5 (R/W) 0 0 0 0 0 0 0 -	PCNL5 (R/W) 0 0 0 0 0 0 0 0	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000110H	TMRLR (W) XXXXXXXX XXXXXXXX		TMR (R) XXXXXXXX XXXXXXXX		Reload Timer 3
000114H	—		TMCSR (R/W) ----0000 00000000		
000118H	TMRLR (W) XXXXXXXX XXXXXXXX		TMR (R) XXXXXXXX XXXXXXXX		Reload Timer 4
00011CH	—		TMCSR (R/W) ----0000 00000000		
000120H to 0001FCH	—				Reserved
000200H	DPDP (R/W) -------- -------- -------- -0000000				DMAC
000204H	DACSR (R/W) 00000000 00000000 00000000 00000000				
000208H	DATCR (R/W) XXXXXXXX XXXX0000 XXXX0000 XXXX0000				
00020CH	—				
000210H to 0003ECH	—				Reserved
0003F0H	BSD0 (W) XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003E4H	BSD1 (R/W) XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC (W) XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR (R) XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H	ICR00 (R/W) ----1111	ICR01 (R/W) ----1111	ICR02 (R/W) ----1111	ICR03 (R/W) ----1111	Interrupt Control Unit
000404H	ICR04 (R/W) ----1111	ICR05 (R/W) ----1111	ICR06 (R/W) ----1111	ICR07 (R/W) ----1111	
000408H	ICR08 (R/W) ----1111	ICR09 (R/W) ----1111	ICR10 (R/W) ----1111	ICR11 (R/W) ----1111	

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
00040C$_H$	ICR12 (R/W) ----1111	ICR13 (R/W) ----1111	ICR14 (R/W) ----1111	ICR15 (R/W) ----1111	Interrupt Control Unit
000410$_H$	ICR16 (R/W) ----1111	ICR17 (R/W) ----1111	ICR18 (R/W) ----1111	ICR19 (R/W) ----1111	
000414$_H$	ICR20 (R/W) ----1111	ICR21 (R/W) ----1111	ICR22 (R/W) ----1111	ICR23 (R/W) ----1111	
000418$_H$	ICR24 (R/W) ----1111	ICR25 (R/W) ----1111	ICR26 (R/W) ----1111	ICR27 (R/W) ----1111	
00041C$_H$	ICR28 (R/W) ----1111	ICR29 (R/W) ----1111	ICR30 (R/W) ----1111	ICR31 (R/W) ----1111	
000420$_H$	ICR32 (R/W) ----1111	ICR33 (R/W) ----1111	ICR34 (R/W) ----1111	ICR35 (R/W) ----1111	
000424$_H$	ICR36 (R/W) ----1111	ICR37 (R/W) ----1111	ICR38 (R/W) ----1111	ICR39 (R/W) ----1111	
000428$_H$	ICR40 (R/W) ----1111	ICR41 (R/W) ----1111	ICR42 (R/W) ----1111	ICR43 (R/W) ----1111	
00042C$_H$	ICR44 (R/W) ----1111	ICR45 (R/W) ----1111	ICR46 (R/W) ----1111	ICR47 (R/W) ----1111	
000430$_H$	DICR (R/W) -------0	HRCL (R/W) ---11111	—		Delay Int
000434$_H$ to 00047C$_H$	—				Reserved
000480$_H$	RSRR/WTCR (R/W) 1XXXX-00	STCR (R/W) 000111--	PDRR (R/W) ----0000	CTBR (W) XXXXXXXX	Clock Control Unit
000484$_H$	GCR (R/W) 110011-1	WPR (W) XXXXXXXX	—		
000488$_H$	CT (R/W) 00--0-00	—			PLL Control
00048C$_H$ to 0005FC$_H$	—				Reserved

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
000600H	DDR3 (W) 0 0 0 0 0 0 0 0	DDR2 (W) 0 0 0 0 0 0 0 0	—	—	Data Direction Register
000604H	—	DDR6 (W) 0 0 0 0 0 0 0 0	DDR5 (W) 0 0 0 0 0 0 0 0	DDR4 (W) 0 0 0 0 0 0 0 0	
000608H	—	—	—	DDR8 (W) -0 0 0 0 0 0 0	
00060CH	ASR1 (W) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1		AMR1 (W) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		T-unit
000610H	ASR2 (W) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0		AMR2 (W) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
000614H	ASR3 (W) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1		AMR3 (W) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
000618H	ASR4 (W) 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0		AMR4 (W) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
00061CH	ASR5 (W) 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 1		AMR5 (W) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0		
000620H	AMD0 (R/W) ---0 0 1 1 1	AMD1 (R/W) 0--0 0 0 0 0	AMD32 (R/W) 0 0 0 0 0 0 0 0	AMD4 (R/W) 0--0 0 0 0 0	
000624H	AMD5 (R/W) 0--0 0 0 0 0	—			
000628H	EPCR0 (W) ----1 1 0 0 -1------		EPCR1 (W) -------- 1 1 1 1 1 1 1 1		
00062CH	—				
000630H	—	PCR6 (R/W) 0 0 0 0 0 0 0 0	—		Pull-up Control
000634H to 0007BCH	—				Reserved
0007C0H	FLCR (R/W) 0 0 0 X 0 0 0 0	—			FLASH Control
0007C4H	FWTC (R/W) -----0 0 0	—			
0007C8H to 0007F8H	—				Reserved

(Continued)

(Continued)

Address	Register				Block
	+0	+1	+2	+3	
0007FC$_H$	—		LER (W) -----000	MODR (W) XXXXXXXX	Little Endian Register Mode Register

*1 : Do not execute RMW instructions to registers with write-only bits.

*2 : Do not execute write access to read-only or reserved registers except for particular requests.

*3 : Data in areas with “-” or reserved ones are unspecified.

*4 : RMW instructions (RMW : Read / Modify / Write)

AND	Rj, @Ri	OR	Rj, @Ri	EOR	Rj, @Ri
ANDH	Rj, @Ri	ORH	Rj, @Ri	EORH	Rj, @Ri
ANDB	Rj, @Ri	ORB	Rj, @Ri	EORB	Rj, @Ri
BANDL	#u4, @Ri	BORL	#u4, @Ri	BEORL	#u4, @Ri
BANDH	#u4, @Ri	BORH	#u4, @Ri	BEORH	#u4, @Ri

■ INTERRUPTION VECTOR

Causes of MB91130 interruptions and allocation of interruption vectors and interruption control registers are described in the interruption vector table.

Interruption sauce	Interruption number		Interruption level *1	Offset	Address *2 of TBR default
	Decimal	Hexadecimal			
Reset	0	00	—	3FC$_H$	000FFFFC$_H$
System reservation	1	01	—	3F8$_H$	000FFFF8$_H$
System reservation	2	02	—	3F4$_H$	000FFFF4$_H$
System reservation	3	03	—	3F0$_H$	000FFFF0$_H$
System reservation	4	04	—	3EC$_H$	000FFFEC$_H$
System reservation	5	05	—	3E8$_H$	000FFFE8$_H$
System reservation	6	06	—	3E4$_H$	000FFFE4$_H$
System reservation	7	07	—	3E0$_H$	000FFFE0$_H$
System reservation	8	08	—	3DC$_H$	000FFFDC$_H$
System reservation	9	09	—	3D8$_H$	000FFFD8$_H$
System reservation	10	0A	—	3D4$_H$	000FFFD4$_H$
System reservation	11	0B	—	3D0$_H$	000FFFD0$_H$
System reservation	12	0C	—	3CC$_H$	000FFFCC$_H$
System reservation	13	0D	—	3C8$_H$	000FFFC8$_H$
Exceptions to undefined instructions	14	0E	—	3C4$_H$	000FFFC4$_H$
System reservation	15	0F	—	3C0$_H$	000FFFC0$_H$
External interruption 0	16	10	ICR00	3BC$_H$	000FFFBC$_H$
External interruption 1	17	11	ICR01	3B8$_H$	000FFFB8$_H$
External interruption 2	18	12	ICR02	3B4$_H$	000FFFB4$_H$
External interruption 3	19	13	ICR03	3B0$_H$	000FFFB0$_H$
External interruption 4	20	14	ICR04	3AC$_H$	000FFFAC$_H$
External interruption 5	21	15	ICR05	3A8$_H$	000FFFA8$_H$
External interruption 6	22	16	ICR06	3A4$_H$	000FFFA4$_H$
External interruption 7	23	17	ICR07	3A0$_H$	000FFFA0$_H$
External interruption 8 to 15	24	18	ICR08	39C$_H$	000FFF9C$_H$
External interruption 16 to 23	25	19	ICR09	398$_H$	000FFF98$_H$
UART0 (Reception completion)	26	1A	ICR10	394$_H$	000FFF94$_H$
UART1 (Reception completion)	27	1B	ICR11	390$_H$	000FFF90$_H$
UART2 (Reception completion)	28	1C	ICR12	38C$_H$	000FFF8C$_H$
UART3 (Reception completion)	29	1D	ICR13	388$_H$	000FFF88$_H$
UART4 (Reception completion)	30	1E	ICR14	384$_H$	000FFF84$_H$

(Continued)

Interruption sauce	Interruption number		Interruption level *1	Offset	Address *2 of TBR default
	Decimal	Hexadecimal			
UART0 (Transmission completion)	31	1F	ICR15	380H	000FFF80H
UART1 (Transmission completion)	32	20	ICR16	37CH	000FFF7CH
UART2 (Transmission completion)	33	21	ICR17	378H	000FFF78H
UART3 (Transmission completion)	34	22	ICR18	374H	000FFF74H
UART4 (Transmission completion)	35	23	ICR19	370H	000FFF70H
DMAC (end, error)	36	24	ICR20	36CH	000FFF6CH
Reload timer 0	37	25	ICR21	368H	000FFF68H
Reload timer 1	38	26	ICR22	364H	000FFF64H
Reload timer 2	39	27	ICR23	360H	000FFF60H
Reload timer 3	40	28	ICR24	35CH	000FFF5CH
Reload timer 4	41	29	ICR25	358H	000FFF58H
A/D (sequential type)	42	2A	ICR26	354H	000FFF54H
PPG0	43	2B	ICR27	350H	000FFF50H
PPG1	44	2C	ICR28	34CH	000FFF4CH
PPG2	45	2D	ICR29	348H	000FFF48H
PPG3	46	2E	ICR30	344H	000FFF44H
PPG4/5	47	2F	ICR31	340H	000FFF40H
Waveform generator	48	30	ICR32	33CH	000FFF3CH
U/D counter 0 (compare/ underflow-overflow, up/down invert)	49	31	ICR33	338H	000FFF38H
U/D counter 1 (compare/ underflow-overflow, up/down invert)	50	32	ICR34	334H	000FFF34H
ICU0 (load)	51	33	ICR35	330H	000FFF30H
ICU1 (load)	52	34	ICR36	32CH	000FFF2CH
ICU2 (load)	53	35	ICR37	328H	000FFF28H
ICU3 (load)	54	36	ICR38	324H	000FFF24H
OCU0 (matched)	55	37	ICR39	320H	000FFF20H
OCU1 (matched)	56	38	ICR40	31CH	000FFF1CH
OCU2 (matched)	57	39	ICR41	318H	000FFF18H
OCU3 (matched)	58	3A	ICR42	314H	000FFF14
OCU4/5 (matched)	59	3B	ICR43	310H	000FFF10H
OCU6/7 (matched)	60	3C	ICR44	30CH	000FFF0CH
Level comparator	61	3D	ICR45	308H	000FFF08H
16-bit freerun timer	62	3E	ICR46	304H	000FFF04H
Delay interruption factor bit	63	3F	ICR47	300H	000FFF00H

(Continued)

(Continued)

Interruption sauce	Interruption number		Interruption level *1	Offset	Address *2 of TBR default
	Decimal	Hexadecimal			
System reservation (used under REALOS *3)	64	40	—	$2FC_H$	$000FFEFC_H$
System reservation (used under REALOS *3)	65	41	—	$2F8_H$	$000FFEF8_H$
Used under INT instruction	66	42	—	$2F4_H$	$000FFEF4_H$
Used under INT instruction	67	43	—	$2F0_H$	$000FFEF0_H$
Used under INT instruction	68	44	—	$2EC_H$	$000FFEEC_H$
Used under INT instruction	69	45	—	$2E8_H$	$000FFEE8_H$
Used under INT instruction	70	46	—	$2E4_H$	$000FFEE4_H$
Used under INT instruction	71	47	—	$2E0_H$	$000FFEE0_H$
Used under INT instruction	72	48	—	$2DC_H$	$000FFEDC_H$
Used under INT instruction	73	49	—	$2D8_H$	$000FFED8_H$
Used under INT instruction	74	4A	—	$2D4_H$	$000FFED4_H$
Used under INT instruction	75	4B	—	$2D0_H$	$000FFED0_H$
Used under INT instruction	76	4C	—	$2CC_H$	$000FFECC_H$
Used under INT instruction	77	4D	—	$2C8_H$	$000FFEC8_H$
Used under INT instruction	78	4E	—	$2C4_H$	$000FFEC4_H$
Used under INT instruction	79	4F	—	$2C0_H$	$000FFEC0_H$
Used under INT instruction	80 to 255	50 to FF	—	$2BC_H$ to 000_H	$000FFEBC_H$ to $000FFC00_H$

*1 : ICR sets the interruption level for each interruption request using the register built into the interruption controller. ICR is prepared in accordance with each interruption request.

*2 : TBR is the register that indicates the starting address of the vector table for EIT. Addresses with added offset values that are specified per TBR and EIT factor will be the vector addresses.

*3 : 0X40, 0X41 interruptions for system codes are used in the event that REALOS/FR is used.

■ PERIPHERAL RESOURCES

1. Bus Interface

The bus interface controls the interface with external memory and external I/O.

- **Bus Interface Characteristics**
- 24-bit (16 MB) address output
- 16/8-bit bus width can be set.
- Insertion of programmable “automatic memory wait” (maximum of 7 cycles)
- Supports “little endian” mode
- Unused addresses / data pins can be used as I/O ports.
- Clock doubled should be used if the external bus exceeds 25 MHz. Bus speed is 1/2 of the CPU speed.

- **Areas**

A total of six types of chip selection areas are prepared for the bus interface. The position of each area can be randomly arranged per 64 KB at least using area selection registers (ASR1 to ASR 5) and area mask registers (AMR1 to AMR 5) in an area of 4 GB. The area 0 is allocated to space outside the area specified by ASR1 to ASR5. External areas other than 00010000_H to $0005FFFF_H$ are deemed area 0 on resetting.

There is no chip selection output pin so no setting is required. Setting it has no effect on usage.

Figure 4.1-1 shows an example in which areas 1 to 5 are arranged from 00100000_H to $0014FFFF_H$ in 64 KB units. Also, Figure 4.1-2 shows an example in which area 1 is arranged as 00000000_H to $0007FFFF_H$ in 512 KB and areas 2 to 5 are arranged as 00100000_H to $004FFFFF_H$ in 1-MB units.

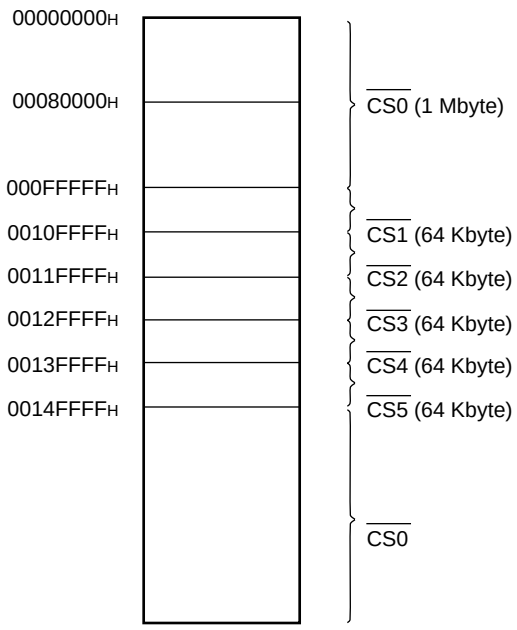


Figure 4.1-1
Area Arrangement Example 1

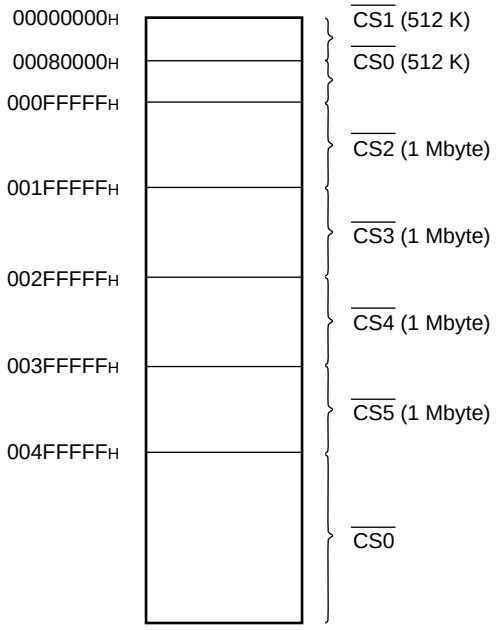
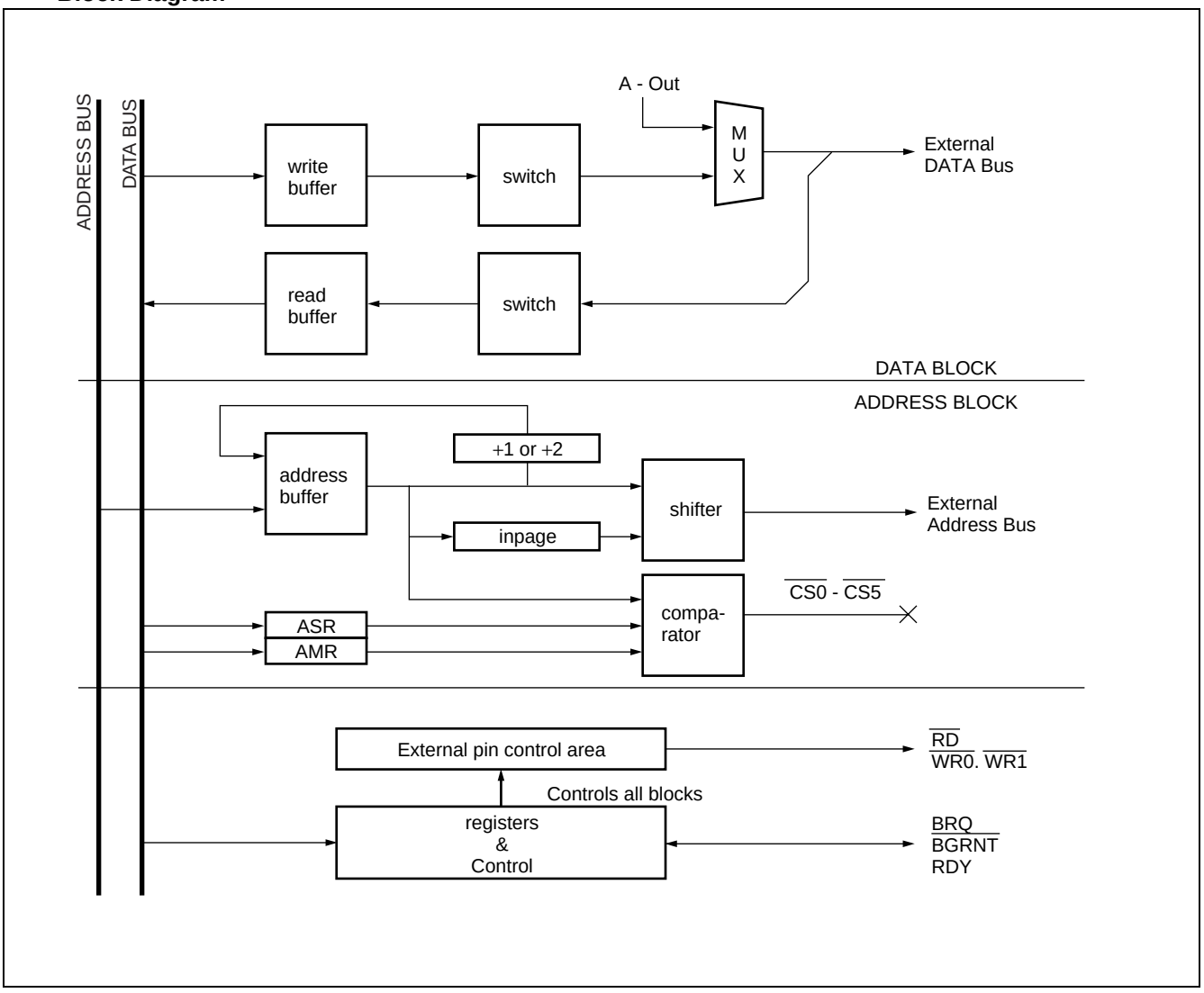


Figure 4.1-2
Area Arrangement Example 2

- **Block Diagram**



- **Register List**

Address	15 8	7 0	
0000060CH	ASR1		Area Select Register 1
0000060EH	AMR1		Area Mask Register 1
00000610H	ASR2		Area Select Register 2
00000612H	AMR2		Area Mask Register 2
00000614H	ASR3		Area Select Register 3
00000616H	AMR3		Area Mask Register 3
00000618H	ASR4		Area Select Register 4
0000061AH	AMR4		Area Mask Register 4
0000061CH	ASR5		Area Select Register 5
0000061EH	AMR5		Area Mask Register 5
00000620H	AMD0	AMD1	Area Mode Register 0 / Area Mode Register 1
00000622H	AMD32	AMD4	Area Mode Register 32 / Area Mode Register 4
00000624H	AMD5	—	Area Mode Register 5
00000626H	RFCR		ReFresh Control Register
0000062CH	DMCR4		DRAM Control Register 4
0000062EH	DMCR5		DRAM Control Register 4
00000688H	EPCR0	EPCR1	External Pin Control Register
000007FEH	LER	MODR	Little Endian Register / MODe Register

Note : Functional pins have not been prepared in the shaded area for MB91133/MB91F133, so these registers should not be accessed.

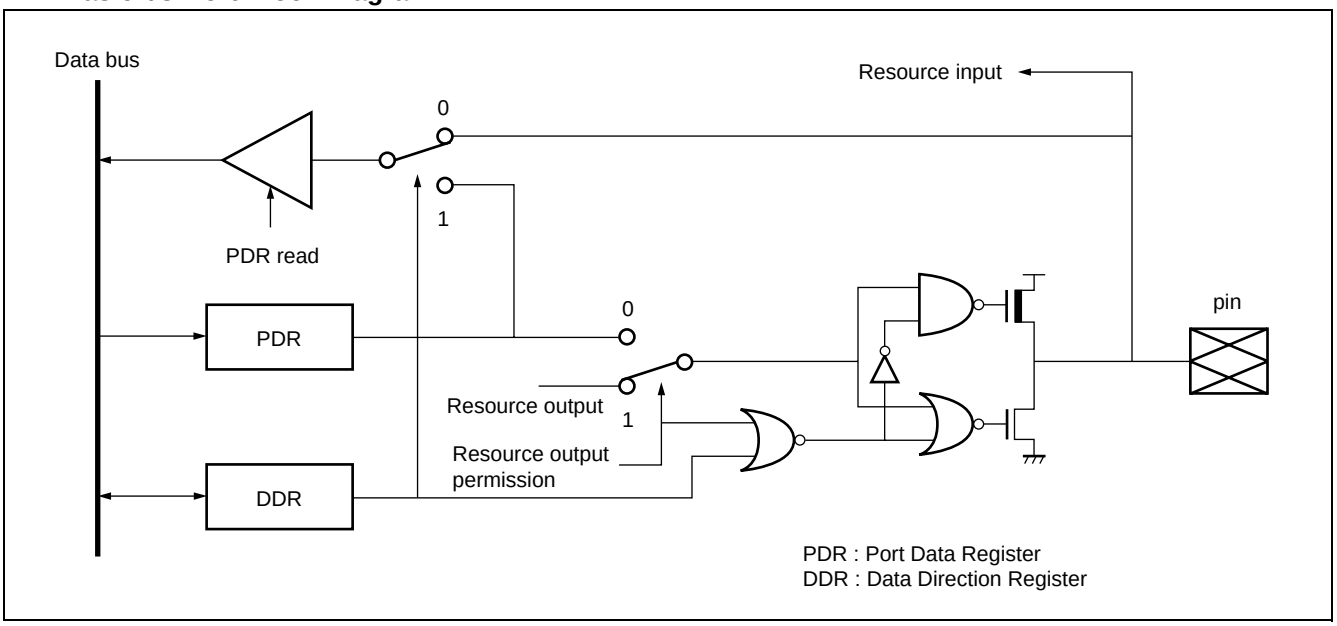
2. I/O Port

MB91133/MB91F133 can be used as an I/O port when the setting for resources dealing with each pin does not use the pin for input/output.

As regards the read value of the port (PDR) , the pin level is read out when input is set for the port. If output is set, the data register value is read out. This is the same for reading under Read Modify Write.

If the input setting is changed to output setting, output data should be set first. If Read Modify Write instructions (i.e. bit set) are used in this case, the data that is read out is the input data from the pin and is not the latch value of the data register, so care must be taken.

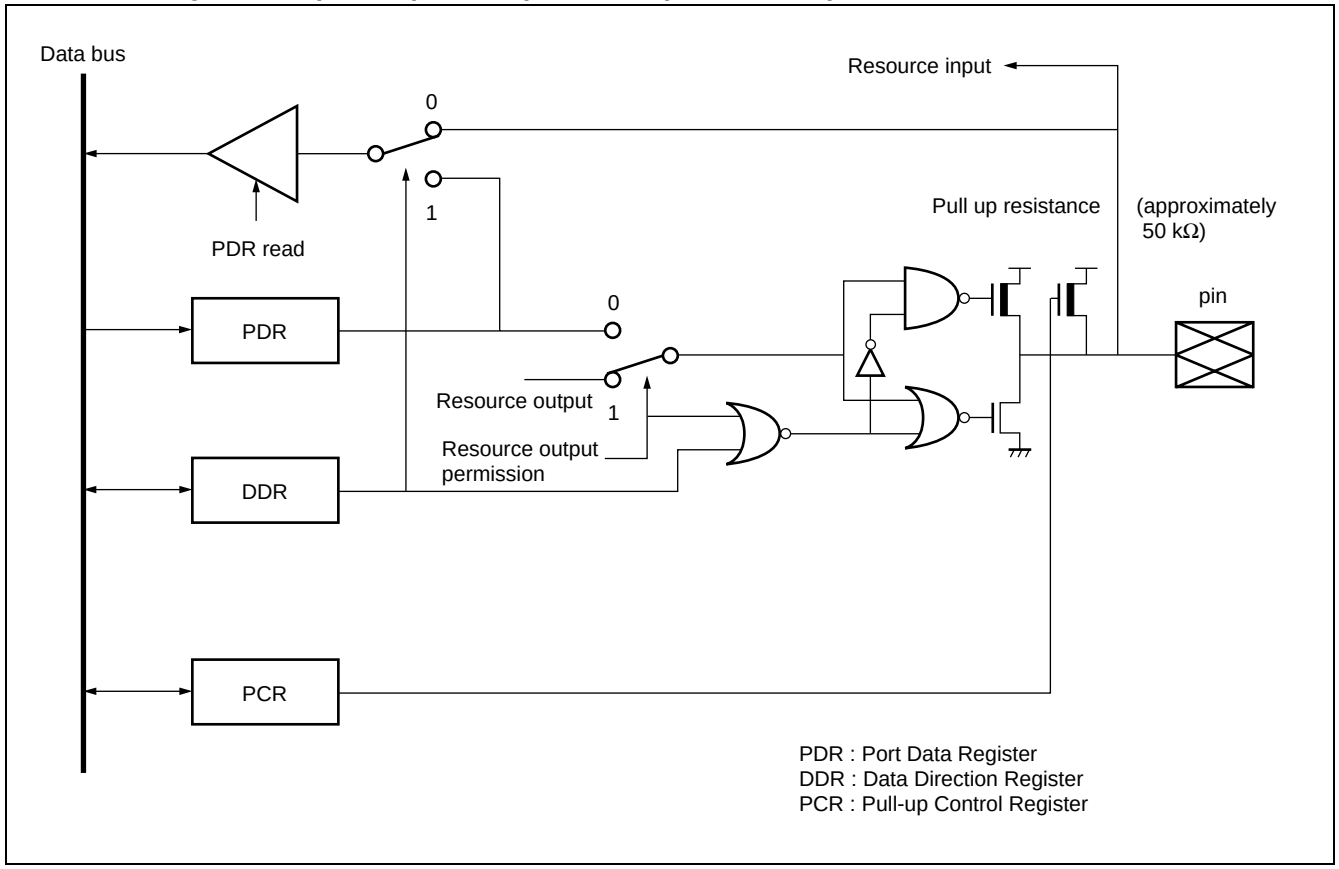
- **Basic I/O Port Block Diagram**



- **I/O Port Register**
  The I/O port consists of the Port Data Register (PDR) and Port Direction Register (DDR) .
- In case of input mode (DDR = “0”)
  When PDR reads : Level of external pins handled is read out.
  When PDR writes : Set value is written in PDR.
- In case of output mode (DDR = “1”)
  When PDR reads : PDR values are read out.
  When PDR writes : PDR values are output to the external pin handled.

- **Switching control for resources and ports of the analog pin (A/D)**
- Resources and ports of the analog pin (A/D) are switched using the Analog Input Control register on Port K (AICK) .
  This controls whether Port K is used as an analog or general-purpose port.
  0 : General-purpose port
  1 : Analog input (A/D)

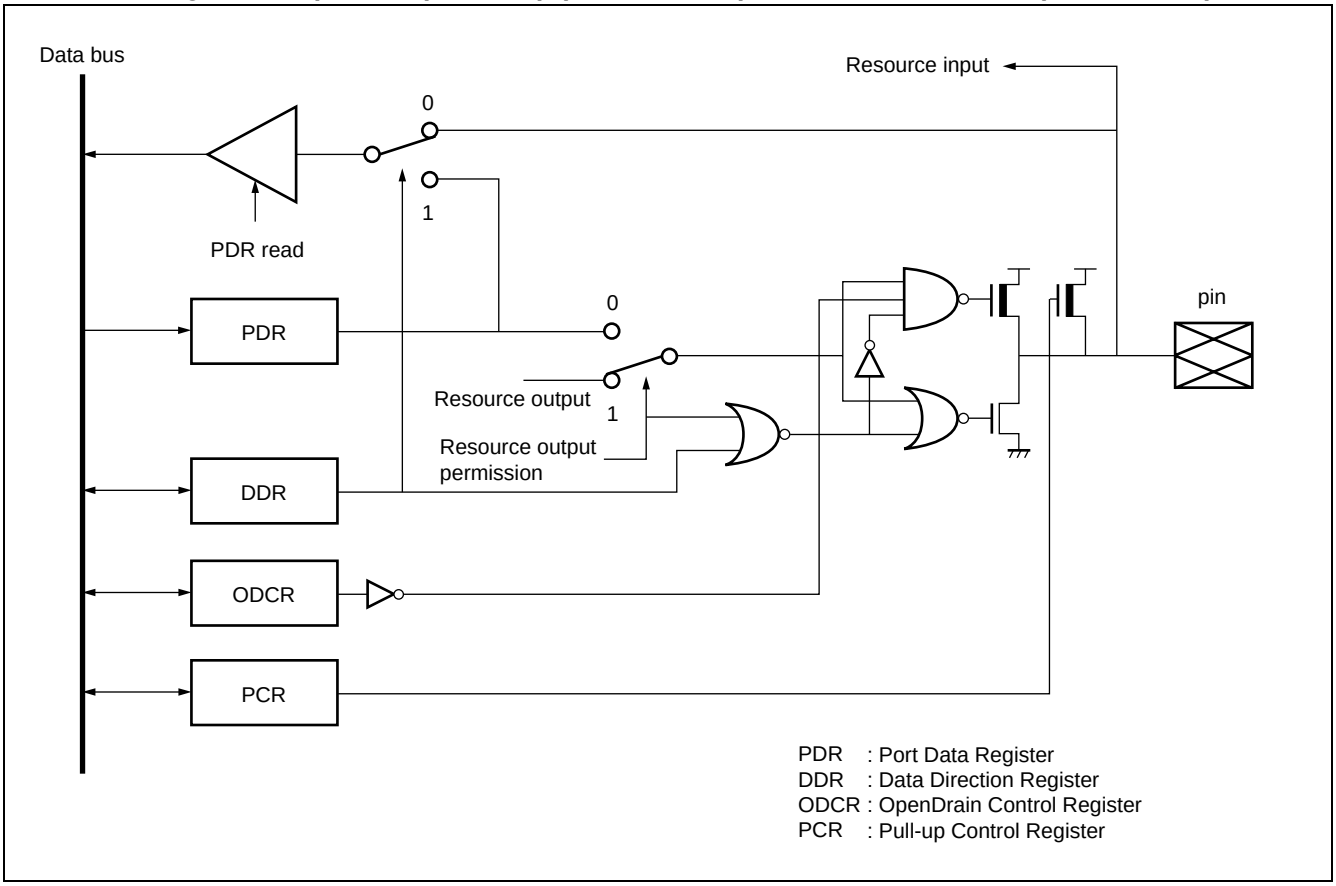
- **Block Diagram of Input/Output Port (with Pull-up Resistance)**



- **Pull-up resistance control register (PCR) R/W**
  Turns pull-up resistance ON/OFF.
  0 : Pull-up resistance turned off
  1 : Pull-up resistance turned on

Notes : • The pull-up resistance control register setting is handled as a priority in stop mode ($\overline{HIZ}$ = 1) as well.
• Use of the pull-up resistance control function is prohibited when the pin concerned is used as the external bus pin. “1” should not be written in this register.

- **Block Diagram of Input / Output Port (Open-drain Output Function with Pull-up Resistance)**



- **Pull-up resistance control register (PCR) R/W**
  Controls pull up resistance ON/OFF.
  0 : Without pull-up resistance
  1 : With pull-up resistance
- **Open-drain control register (ODCR) R/W**
  Controls open-drain in output mode.
  0 : Standard output port in output mode
  1 : Open-drain output port in output mode

Notes :
- This has no meaning in input mode (output Hi-Z) . Input/output mode is decided by the Direction Register (DDR) .
- Pull-up resistance control register setting is handled as the priority in stop mode ($\overline{HIZ}$ = 1) as well.
- Use of both the pull-up resistance control function and open-drain control function are prohibited when the pin concerned is used as an external bus pin. “1” should not be written in both registers.

- **Port Data Register (PDR)**

	7	6	5	4	3	2	1	0	Initial value	Access
PDR2 Address : 000001H	P27	P26	P25	P24	P23	P22	P21	P20	XXXXXXXXB	R/W
PDR3 Address : 000000H	P37	P36	P35	P34	P33	P32	P31	P30	XXXXXXXXB	R/W
PDR4 Address : 000007H	P47	P46	P45	P44	P43	P42	P41	P40	XXXXXXXXB	R/W
PDR5 Address : 000006H	P57	P56	P55	P54	P53	P52	P51	P50	XXXXXXXXB	R/W
PDR6 Address : 000005H	P67	P66	P65	P64	P63	P62	P61	P60	XXXXXXXXB	R/W
PDR8 Address : 00000BH	—	P86	P85	P84	P83	P82	P81	P80	- XXXXXXXB	R/W
PDRC Address : 000013H	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	XXXXXXXXB	R/W
PDRD Address : 000012H	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	XXXXXXXXB	R/W
PDRE Address : 000011H	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	XXXXXXXXB	R/W
PDRF Address : 000010H	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	XXXXXXXXB	R/W
PDRG Address : 000017H	—	—	PG5	PG4	PG3	PG2	PG1	PG0	- - XXXXXXB	R/W
PDRH Address : 000016H	—	—	—	—	—	PH2	PH1	PH0	- - - - - XXXB	R/W
PDRI Address : 000015H	—	—	PI5	PI4	PI3	PI2	PI1	PI0	- - XXXXXXB	R/W
PDRJ Address : 000014H	—	—	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	- - XXXXXXB	R/W
PDRK Address : 00001BH	PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0	XXXXXXXXB	R/W
PDRL Address : 00001AH	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	XXXXXXXXB	R/W

PDR2 to L are input/output data registers of the I/O port.
Input/output control is carried out by DDR2 to L that are handled.

- **Data Direction Register (DDR)**

DDR2
Address : 000601H

7	6	5	4	3	2	1	0	Initial value	Access
P27	P26	P25	P24	P23	P22	P21	P20	00000000B	W

DDR3
Address : 000600H

7	6	5	4	3	2	1	0	Initial value	Access
P37	P36	P35	P34	P33	P32	P31	P30	00000000B	W

DDR4
Address : 000607H

7	6	5	4	3	2	1	0	Initial value	Access
P47	P46	P45	P44	P43	P42	P41	P40	00000000B	W

DDR5
Address : 000606H

7	6	5	4	3	2	1	0	Initial value	Access
P57	P56	P55	P54	P53	P52	P51	P50	00000000B	W

DDR6
Address : 000605H

7	6	5	4	3	2	1	0	Initial value	Access
P67	P66	P65	P64	P63	P62	P61	P60	00000000B	W

DDR8
Address : 00060BH

7	6	5	4	3	2	1	0	Initial value	Access
—	P86	P85	P84	P83	P82	P81	P80	- 0000000B	W

DDRC
Address : 0000D3H

7	6	5	4	3	2	1	0	Initial value	Access
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	00000000B	R/W

DDRD
Address : 0000D2H

7	6	5	4	3	2	1	0	Initial value	Access
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	00000000B	R/W

DDRE
Address : 0000D1H

7	6	5	4	3	2	1	0	Initial value	Access
PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0	00000000B	R/W

DDRF
Address : 0000D0H

7	6	5	4	3	2	1	0	Initial value	Access
PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	00000000B	R/W

DDRG
Address : 0000D7H

7	6	5	4	3	2	1	0	Initial value	Access
—	—	PG5	PG4	PG3	PG2	PG1	PG0	- - 000000B	R/W

DDRH
Address : 0000D6H

7	6	5	4	3	2	1	0	Initial value	Access
—	—	—	—	—	PH2	PH1	PH0	- - - - - 000B	R/W

DDRI
Address : 0000D5H

7	6	5	4	3	2	1	0	Initial value	Access
—	—	PI5	PI4	PI3	PI2	PI1	PI0	- - 000000B	R/W

DDRJ
Address : 0000D4H

7	6	5	4	3	2	1	0	Initial value	Access
—	—	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	- - 000000B	R/W

DDRK
Address : 0000DBH

7	6	5	4	3	2	1	0	Initial value	Access
PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0	00000000B	R/W

DDRL
Address : 0000DAH

7	6	5	4	3	2	1	0	Initial value	Access
PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000B	R/W

DDR0 to L control input/output direction of the I/O ports handled per bit.
DDR = 0 : Port input DDR = 1 : Port output "0" must be written into the empty bit.

- **Pull up Control Register (PCR)**

	7	6	5	4	3	2	1	0	Initial value	Access
PCR6 Address : 000631H	P67	P66	P65	P64	P63	P62	P61	P60	00000000B	R/W
PCRC Address : 0000C3H	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	00000000B	R/W
PCRD Address : 0000C2H	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	00000000B	R/W
PCRE Address : 0000C1H	—	—	—	—	—	—	PE1	PE0	- - - - - - 00B	R/W
PCRH Address : 0000C6H	—	—	—	—	—	PH2	PH1	PH0	- - - - - 000B	R/W
PCRI Address : 0000C5H	—	—	PI5	PI4	PI3	PI2	PI1	PI0	- - 000000B	R/W
PCRJ Address : 0000C4H	—	—	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	- - 000000B	R/W

PCR6 to J carry out pull-up resistance control of the I/O ports handled.
PCR = 0 : Pull-up resistance turned off
PCR = 1 : Pull-up resistance turned on

- **Open-drain Control Register (ODCR)**

	7	6	5	4	3	2	1	0	Initial value	Access
OCRH Address : 0000CAH	—	—	—	—	—	PH2	PH1	PH0	- - - - - 000B	R/W
OCRI Address : 0000C9H	—	—	PI5	PI4	PI3	PI2	PI1	PI0	- - 000000B	R/W
OCRJ Address : 0000C8H	—	—	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	- - 000000B	R/W

OCRH to J carry out open-drain control in output mode of the I/O ports handled.
OCR = 0 : Standard output port in output mode
OCR = 1 : Open-drain output port in output mode
This has no meaning in input mode (output Hi-z) .

- **Analog Input Control Register (AICR)**

AICK

Address : 0000CF$_H$

7	6	5	4	3	2	1	0
PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0

Initial value: 00000000$_B$

Access: R/W

AICK controls each pin of the I/O ports handled as follows.
AIC = 0 : Analog input mode
AIC = 1 : Port input mode
Set to “0” when reset.

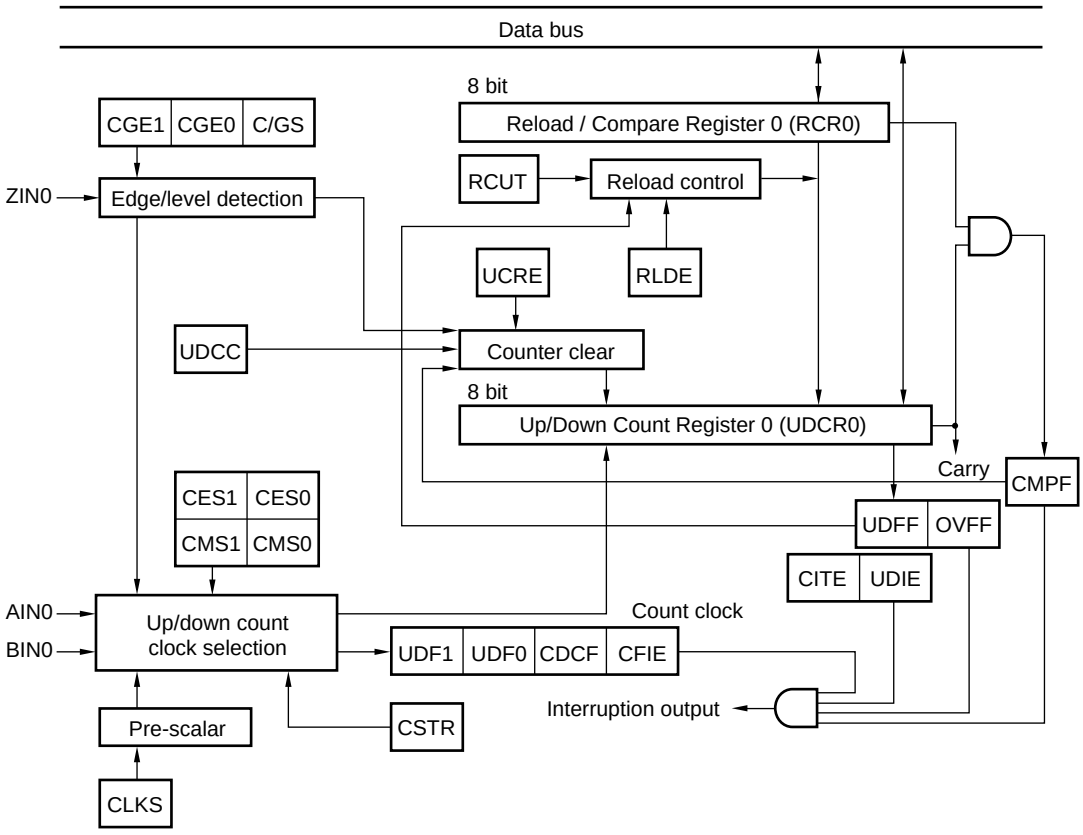
3. 8/16-bit Up/Down Counter / Timer

8/16-bit up/down counter / timer is configured of event input pins × 6, 8-bit up/down counters × 2, 8-bit reload / compare registers × 2 and their control circuits.

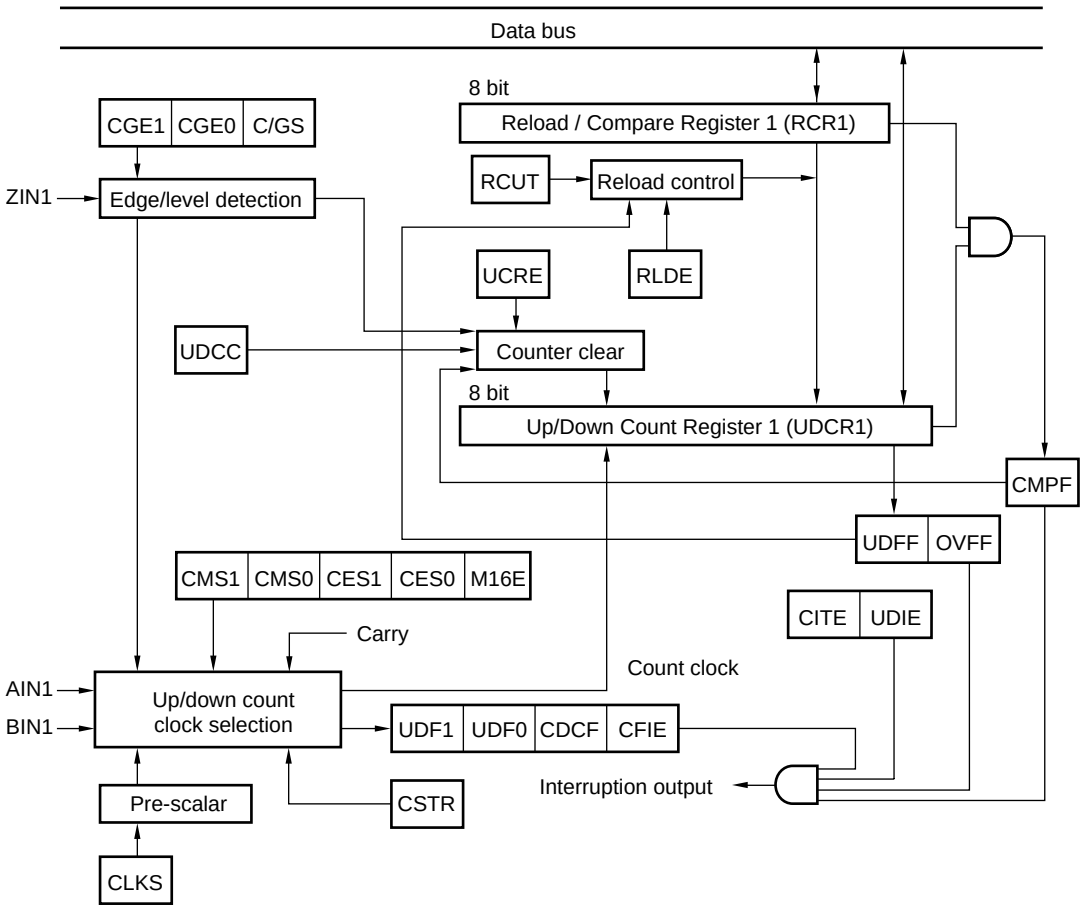
- **Characteristics of 8/16-bit Up/Down Counter / Timer**
- Counting from (0) d to (256) d is possible using an 8-bit counting register.
  (Counting from (0) d to (65535) d is possible in 16-bit × 1 operation mode.)
- 4 types of counting mode can be selected by the count clock
- Selection can be made from two types of internal clock as the count clock in timer mode.
- Detection edge of the external pin input signals can be selected in up/down count mode.
- Phase difference count mode is suited to count encoders such as motors. Turning angle and turning number, etc., can easily and accurately be counted by separately inputting phase A, B and Z outputs of the encoder.
- Selection can be made from two function types for the ZIN pin (valid for all modes) .
- Compare and reload functions are featured, and each function can be used alone or in combination. Up/down counting with random width can be carried out using both functions in combination.
- The count direction directly before can be identified by the count direction flag.
- Generation of interruptions in case of compared match, reload (underflow) or overflow and in cases where the count direction is changed can be controlled separately.

- **Block Diagram**

8/16-bit Up/Down Counter / Timer (ch0)



8/16-bit Up/Down Counter / Timer (ch1)



- **Register List**

31 24	23 16	15 8	7 0
RCR1	RCR0	UDCR1	UDCR0
CCRH0	CCRL0	—	CSR0
CCRH1	CCRL1	—	CSR1

Up/down count register ch0 (UDCR0)

bit	7	6	5	4	3	2	1	0
Address : 000087H	D07	D06	D05	D04	D03	D02	D01	D00

Up/down count register ch1 (UDCR1)

bit	15	14	13	12	11	10	9	8
Address : 000086H	D17	D16	D15	D14	D13	D12	D11	D10

Reload compare register ch0 (RCR0)

bit	7	6	5	4	3	2	1	0
Address : 000085H	D07	D06	D05	D04	D03	D02	D01	D00

Reload compare register ch1 (RCR1)

bit	15	14	13	12	11	10	9	8
Address : 000084H	D17	D16	D15	D14	D13	D12	D11	D10

Counter Status register ch0, 1 (CSR0, 1)

bit	7	6	5	4	3	2	1	0
Address : 00008BH 00008FH	CSTR	CITE	UDIE	CMPF	OVFF	UDFF	UDF1	UDF0

Counter control register ch0, 1 (CCRL0, 1)

bit	7	6	5	4	3	2	1	0
Address : 000089H 00008DH	—	CTUT	UCRE	RLDE	UDCC	CGSC	CGE1	CGE0

Counter control register ch0 (CCRH0)

bit	15	14	13	12	11	10	9	8
Address : 000088H	M16E	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0

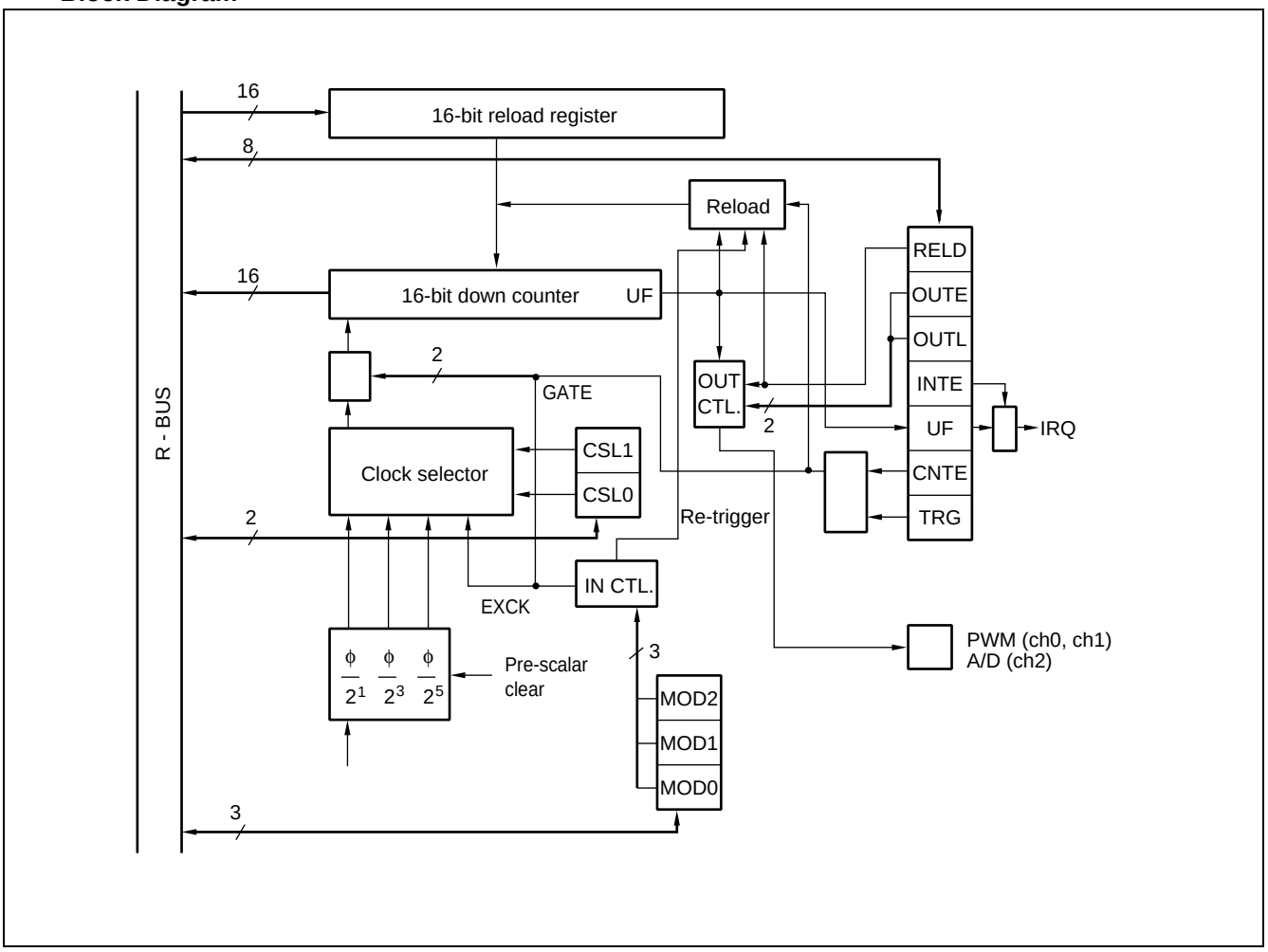
Counter control register ch1 (CCRH1)

bit	15	14	13	12	11	10	9	8
Address : 00008CH	—	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0

4. 16-bit Reload Timer

The 16-bit timer is configured with a 16-bit down counter, 16-bit reload register, pre-scalar to prepare the internal count clock and control register. Selection can be made from three types of internal clocks (machine clock 2 / 8 / 32 cycles) as the input clock. DMA transfer can be initiated by interruption. The MB91133/MB91F133 features a 5-channel timer.

- **Block Diagram**



Channel 2TO output of the reload timer is connected to the A/D converter inside the LSI. Thus, A/D conversion can be started up at the cycle set in the reload register.

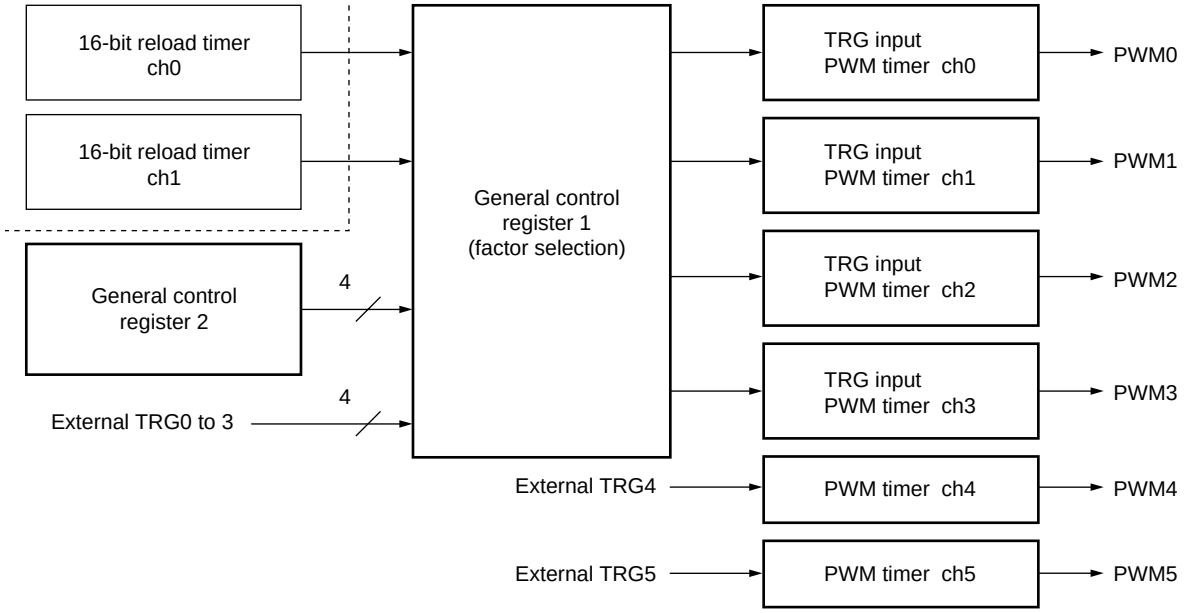
5. PPG Timer

The PPG timer can efficiently output accurate PWM waveforms. The MB91130 series features a 6-channel PPG timer.

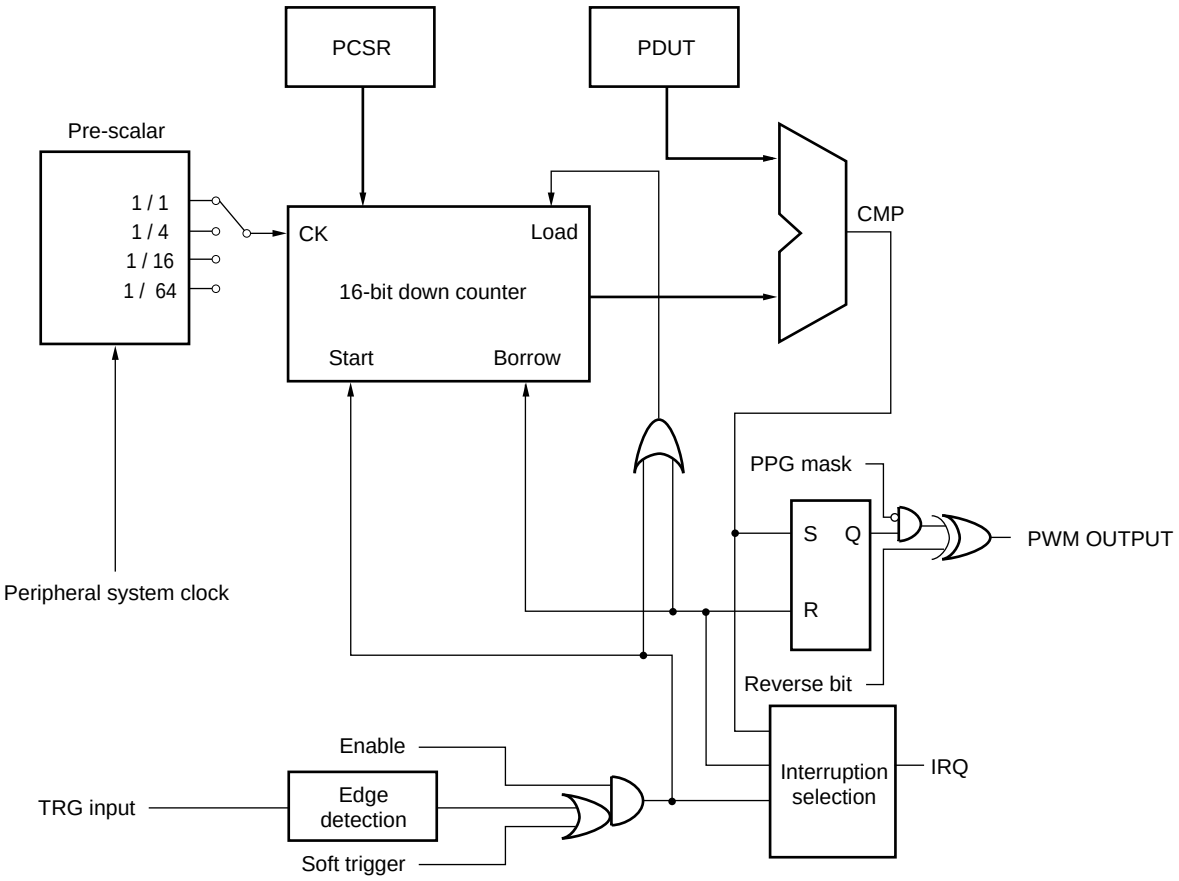
- **PPG Timer Characteristics**
- Each channel is configured with a 16-bit down counter, 16-bit data register with cycle setting buffer, 16-bit compare register with duty setting buffer and pin control area.
- Selection can be made from four types of count clocks for 16-bit down counters.
  Internal clock ϕ, ϕ4, ϕ16, ϕ64
- Counter values can be initialized to "FFFF$_H$" by resetting and counter borrowing.
- PWM output is available per channel.
- Register outline
  Cycle setting register : Reloading register with buffer
  Duty setting register : Compare register with buffer
  Transfer from buffer is carried out by counter borrowing.
- Pin control outline
  Set to "1" by duty match. (Priority)
  Resets to "0" by counter borrowing.
  All "L" (or "H") can simply be output by using the output values fixing mode.
  Polarization can also be specified.
- Interruption request can be generated by selecting from the following combinations.
  Initiation of this timer
  Counter borrow generation (cycle match)
  Duty match generation
  Counter borrow generation (cycle match) or duty match generation
  DMA transfer can be initiated by the above interruption requests.
- Simultaneous initiation of a number of channels can be set by software or other interval timers. Re-start during operation can also be set.

- **Block Diagram**

Overall Block Diagram of PPG Time



Block Diagram of PPG Timer for 1 Channel

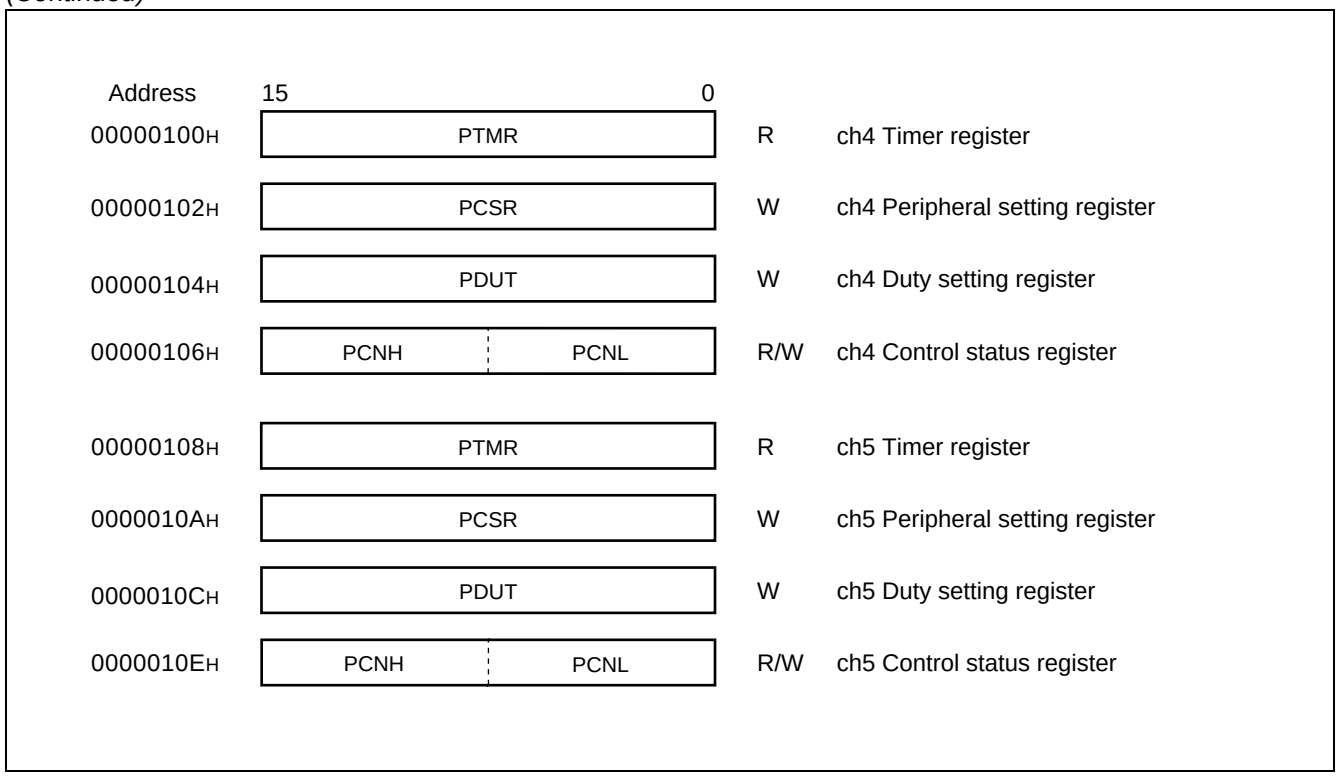


- **Register list**

Address	15	0		
000000DCH	GCN1		R/W	General control register 1
000000DFH	GCN2		R/W	General control register 2
000000E0H	PTMR		R	ch0 Timer register
000000E2H	PCSR		W	ch0 Peripheral setting register
000000E4H	PDUT		W	ch0 Duty setting register
000000E6H	PCNH	PCNL	R/W	ch0 Control status register
000000E8H	PTMR		R	ch1 Timer register
000000EAH	PCSR		W	ch1 Peripheral setting register
000000ECH	PDUT		W	ch1 Duty setting register
000000EEH	PCNH	PCNL	R/W	ch1 Control status register
000000F0H	PTMR		R	ch2 Timer register
000000F2H	PCSR		W	ch2 Peripheral setting register
000000F4H	PDUT		W	ch2 Duty setting register
000000F6H	PCNH	PCNL	R/W	ch2 Control status register
000000F8H	PTMR		R	ch3 Timer register
000000FAH	PCSR		W	ch3 Peripheral setting register
000000FCH	PDUT		W	ch3 Duty setting register
000000FEH	PCNH	PCNL	R/W	ch3 Control status register

(Continued)

(Continued)


Address
15
0
00000100H
PTMR
R
ch4 Timer register
00000102H
PCSR
W
ch4 Peripheral setting register
00000104H
PDUT
W
ch4 Duty setting register
00000106H
PCNH
PCNL
R/W
ch4 Control status register
00000108H
PTMR
R
ch5 Timer register
0000010AH
PCSR
W
ch5 Peripheral setting register
0000010CH
PDUT
W
ch5 Duty setting register
0000010EH
PCNH
PCNL
R/W
ch5 Control status register

6. Multifunction Timer

The multifunction timer unit is configured of a 16-bit freerun timer × 1, 16-bit output compare × 8, 16-bit input capture × 4, 16-bit PPG timer × 6 ch and waveform generation area modules. 12 independent waveform outputs based on a 16-bit free-run timer are possible using this function and measurement of input pulse width and external clock cycle is also possible.

- **Multifunction Timer Configuration**
- 16-bit free-run timer (× 1)
  The 16-bit free-run timer consists of a 16-bit up counter, control register, 16-bit compare clear register and pre-scalar. Output values of this counter are used as the base timer for output compare and input capture.
  - Counter operation clocks can be selected from six types.
    Six types of internal clocks (ϕ2, ϕ4, ϕ8, ϕ16, ϕ32, ϕ64)
    ϕ : Machine clock
  - Interruption can be generated by overflow of the counter value and a compared match with compare clear register. (Mode setting is required for a compared match.)
  - Counter value can be initialized to "0000_H" by a compared match with the reset, software clear or the compare clear register.

- Output compare (× 8)
  Output compare is configured of 16-bit compare register × 8, latch for compare output and control register. Interruption can be generated as well as reversing output level when the 16-bit free-run timer value and compare register value match.
  - 8 compare registers can be operated independently. Output pins and interruption flags support each compare register.
  - Output pins can be controlled by pairing two compare registers. Output pins are reversed using two compare registers.
  - Initial value of each output pin can be set.
  - Interruption can be generated by matching compare.

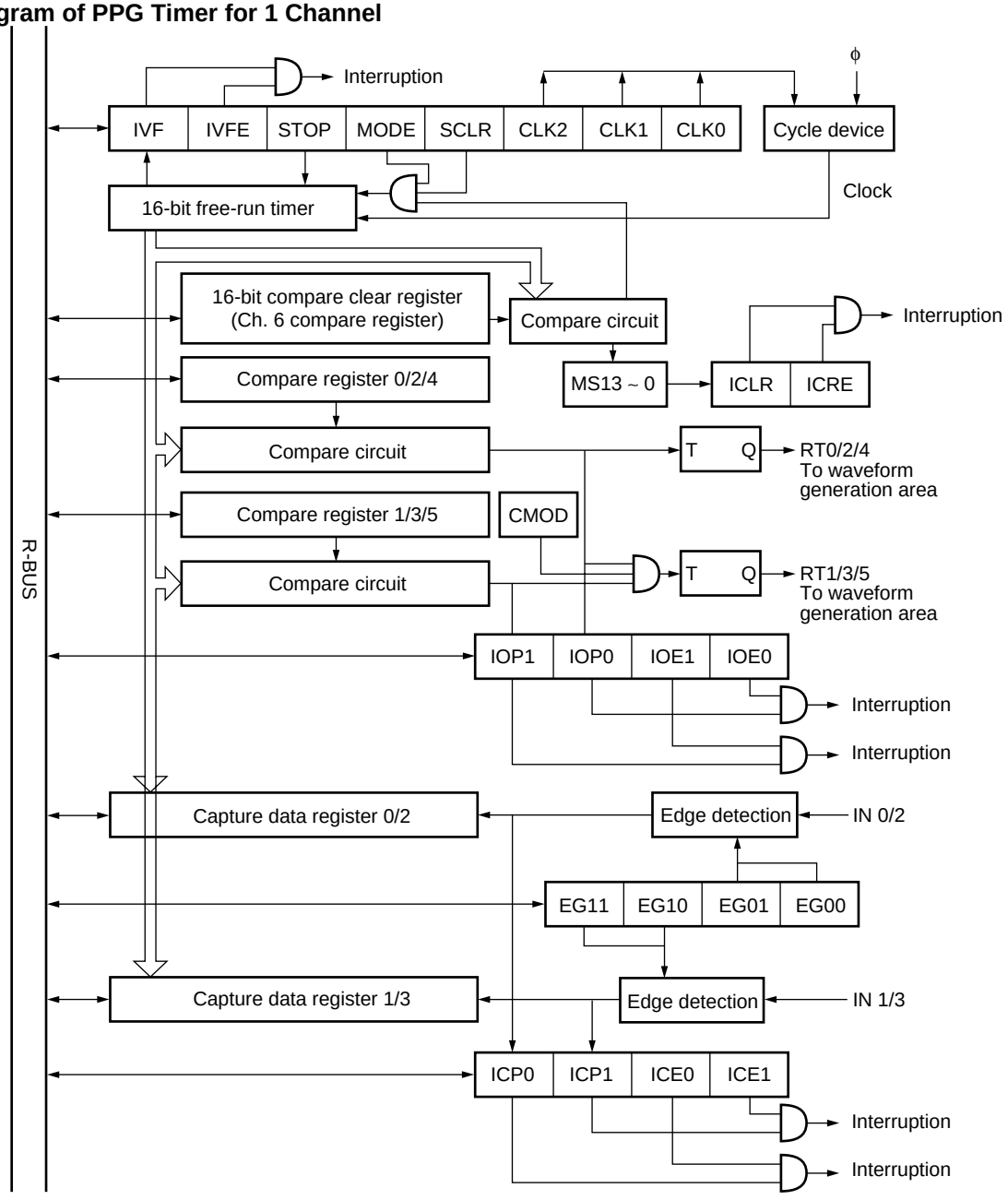
- Input capture (× 4)
  Input capture is configured with four independent external input pins , supported capture and control register. 16-bit free-run timer value is held in the capture register by detecting the random edge of signals that are input by the external input pin, and interruption can simultaneously be generated.
  - Valid edges (rising edge, falling edge, both edges) of external input signals can be selected.
  - Four input captures can be operated independently.
  - Interruption can be generated by the valid edges of external input signals.

- 16-bit PPG timer (× 6)
  Refer to PPG timer

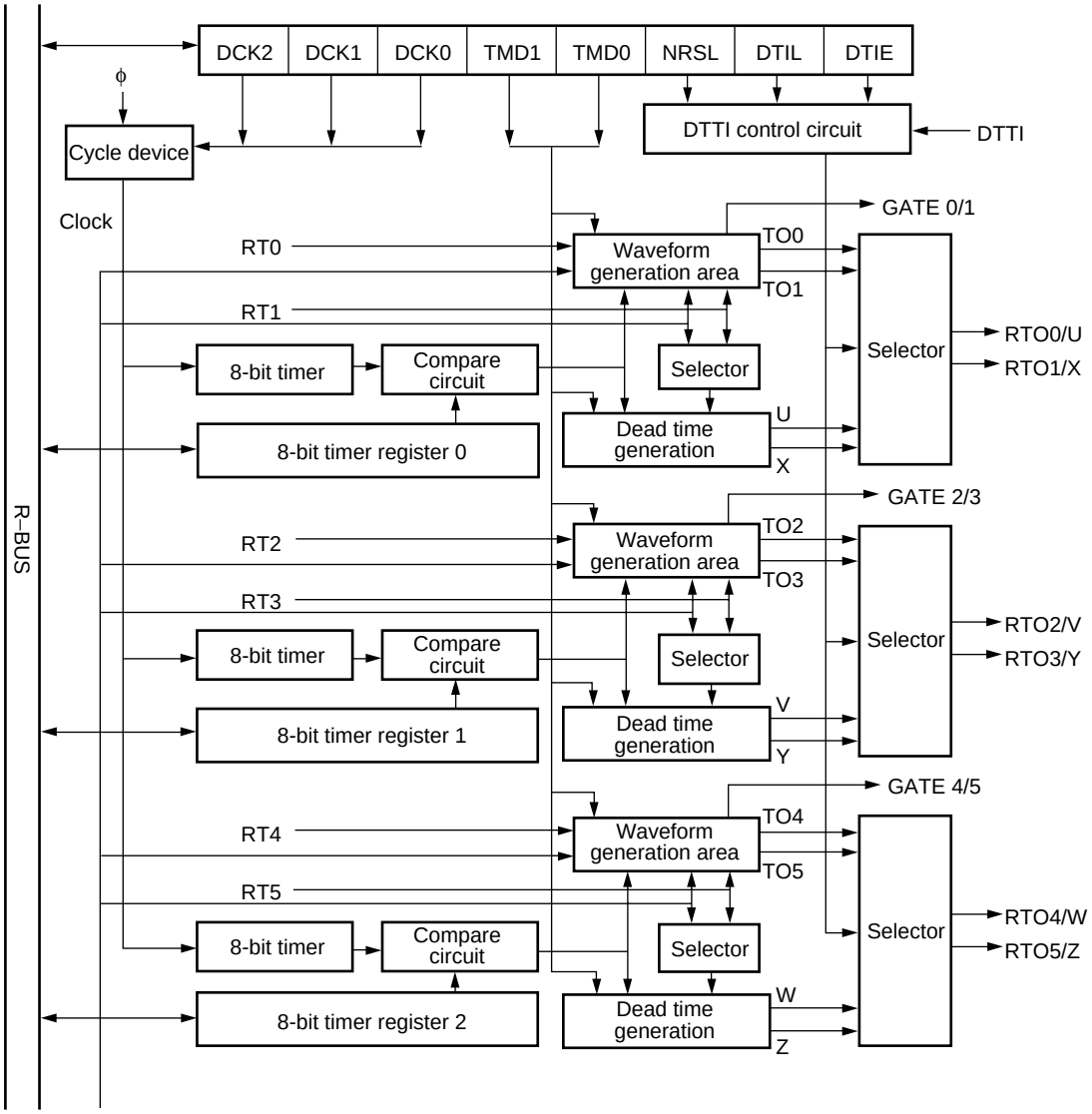
- Waveform Generation Area
  The waveform generation area is configured with 8-bit timer × 3, 8-bit reload register × 3, timer control register × 3 and 8-bit waveform control register. This control circuit controls the waveform of the 16-bit PPG timer and real-time output, and DC chopper output and non-overlapping 3-phase waveform output to be used for inverter control are possible.
  - Non-overlapping pulse output of the PPG timer is possible by setting dead time of the 8-bit timer (dead time timer function) .
  - Real timer output is operated by the 2-channel mode and non-overlapping output of the waveform is possible by setting the dead time of the 8-bit timer (dead time timer function) .
  - Operation of PPG timer can easily be started/stopped by generating a GATE signal for the PPG timer operation through match detection of real-time output compare (GATE function).
  - The 8-bit timer is operated by match detection of real-time output compare, and operation of the PPG timer can easily be started/stopped by generating a GATE signal for the PPG timer until the 8-bit timer is stopped (GATE function) .
  - Pin output can be forcibly controlled by input to the DTTI pin. Pins can be controlled externally even if oscillations stop due to lack of clocks for inputs to this pin. (Each pin level can be set by the program .) If this function is used, the port should be set to output (DDR = 1) and the output value should be described in the PDR beforehand.

- **Block Diagram**

Block Diagram of PPG Timer for 1 Channel



Block Diagram of Waveform Generation Area



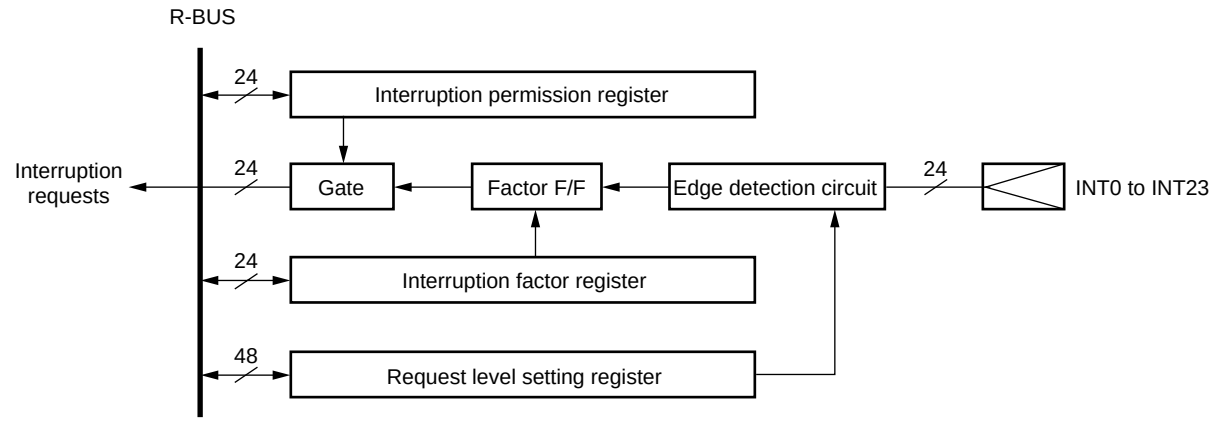
- **Registers List**

Address	15 8	7 0	
000044H to 4BH	IPCP		(R)
00004DH, 4FH		ICS	(R/W)
000054H to 63H	OCCP		(R/W)
000064H to 6BH	OCS		(R/W)
00006CH, 6DH	TCDT		(R/W)
00006EH, 6FH	TCCS		(R/W)
0000ACH, AEH B2H	DTCR		(R/W)
0000ADH, AFH B3H		TMRR	(R/W)
0000B1H		STGCR	(R/W)

7. External Interruption

The external interruption control area is the block that controls the external interruption requests input in INT0 to INT23. The level of request to be detected can be selected from “H”, “L”, “Rising edge” or “ Falling edge”.

- **Block diagram**



- **Register List**

External interruption permission register (ENIR)

bit	15	14	13	12	11	10	9	8
	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0

External interruption factor register (EIRR)

bit	15	14	13	12	11	10	9	8
	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0

Request level setting register (ELVR)

bit	7	6	5	4	3	2	1	0
	LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0

bit	15	14	13	12	11	10	9	8
	LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4

There are three sets of the above registers (for 8 channels) for a total of 24 channels.

8. Delay Interruption Module

The delay interruption module generates interruptions for task switching. Interruption requests to the CPU can be generated / cancelled using software with this module.

- **Block Diagram**

Refer to “9.(2) Block Diagram of Interruption Controller” for the block diagram of the delay interruption generation area.

- **Register List**

Address : 00000430H

bit 7	6	5	4	3	2	1	0	
—	—	—	—	—	—	—	DLYI	DICR
							R/W	

9. Interruption Controller

The interruption controller carries out interruption reception and arbitration.

- **Hardware configuration of the interruption controller**

This module consists of the following items.
- ICR register
- Interruption priority judgement circuit
- Interruption level, interruption number (vector) generation area
- Cancellation request generation area for HOLD request

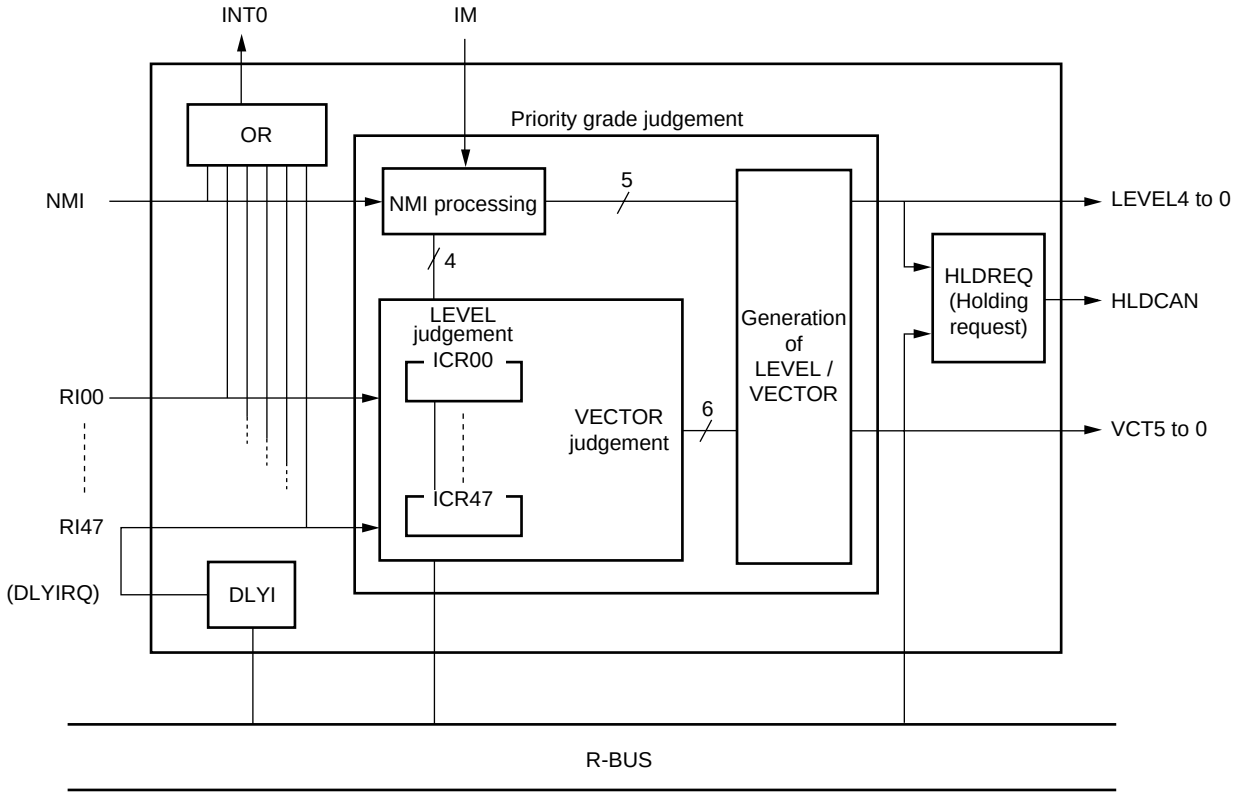
- **Major interruption controller functions**

This module has the following functions.
- Detection of interruption requests
- Priority grade judgement (depending on the level and number)
- Transferring interruption level of factors for the judgement results (to CPU)
- Transferring interruption number of factors for the judgement results (to CPU)
- Recovery instruction from stop mode by generating interruption
- Cancellation of HOLD request to the bus master

- **Resetting Interruption Factors**

There are restrictions between RETI instructions and those for resetting interruption factors in the interruption routine.

- **Block Diagram**



Note : DLYI shown in the figure indicates delay interruption area. (Refer to the chapter on the delay interruption module for details.)
INTO is the wake-up signal to the clock control area in case of sleep or stop.
HLDCAN is the bus vacation request signal to bus masters other than the CPU.
There is no NMI function in this model.

- **Register List**

	bit 7	6	5	4	3	2	1	0	
Address: 00000400H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR00
Address: 00000401H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR01
Address: 00000402H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR02
Address: 00000403H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR03
Address: 00000404H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR04
Address: 00000405H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR05
Address: 00000406H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR06
Address: 00000407H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR07
Address: 00000408H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR08
Address: 00000409H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR09
Address: 0000040AH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR10
Address: 0000040BH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR11
Address: 0000040CH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR12
Address: 0000040DH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR13
Address: 0000040EH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR14
Address: 0000040FH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR15
Address: 00000410H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR16
Address: 00000411H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR17
Address: 00000412H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR18
Address: 00000413H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR19
Address: 00000414H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR20
Address: 00000415H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR21
Address: 00000416H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR22
Address: 00000417H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR23
Address: 00000418H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR24
Address: 00000419H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR25
Address: 0000041AH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR26
Address: 0000041BH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR27
Address: 0000041CH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR28
Address: 0000041DH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR29
Address: 0000041EH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR30
Address: 0000041FH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR31
					R/W	R/W	R/W	R/W	

(Continued)

(Continued)

	bit 7	6	5	4	3	2	1	0	
Address : 00000420H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR32
Address : 00000421H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR33
Address : 00000422H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR34
Address : 00000423H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR35
Address : 00000424H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR36
Address : 00000425H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR37
Address : 00000426H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR38
Address : 00000427H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR39
Address : 00000428H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR40
Address : 00000429H	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR41
Address : 0000042AH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR42
Address : 0000042BH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR43
Address : 0000042CH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR44
Address : 0000042DH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR45
Address : 0000042EH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR46
Address : 0000042FH	—	—	—	—	ICR3	ICR2	ICR1	ICR0	ICR47
					R/W	R/W	R/W	R/W	

Address : 00000431H	—	—	—	—	LVL3	LVL2	LVL1	LVL0	HRCL
					R/W	R/W	R/W	R/W	

10. Clock Generation Area (low power consumption mechanism)

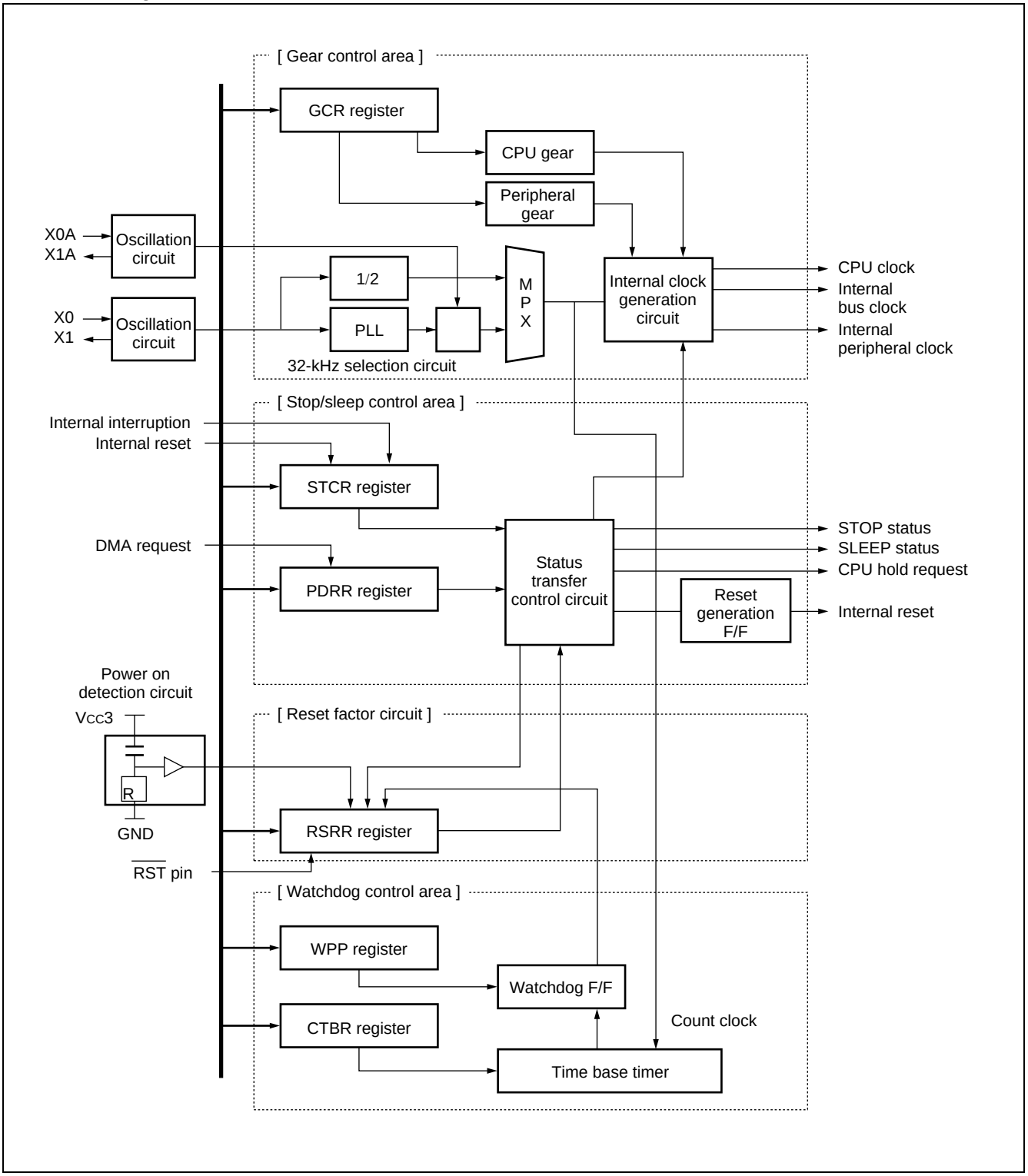
Clock generation area is a module with the following functions.

- CPU clock generation (including gear function)
- Peripheral clock generation (including gear function)
- Reset generation and holding factors
- Standby function (including hardware standby)
- PLL (Phase Locked Loop) is built in

- **Register list**

Address	7 ... 0	
000480H	RSRR/WTCR	Reset factor / watchdog cycle control register
000481H	STCR	Standby control register
000482H	PDRR	DMA request blocking register
000483H	CTBR	Time base timer clear register
000484H	GCR	Gear control register
000485H	WPR	Watchdog reset generation postponement register
000488H	PCTR	PLL / 32-K clock control register

- **Block diagram**



11. 8-/10-bit A/D Converter

The 8-/10-bit A/D converter features functions that convert analog input voltages to 10- or 8-bit digital values using the RC sequential comparison conversion method. The input signal is selected from 8-channel analog input pins and three types of conversion initiation can be selected from software, internal clock, or external pin trigger.

- **characteristics of 8-/10-bit A/D converter**

The A/D conversion function for converting analog voltages (input voltages) input into the analog input pins to digital values has the following characteristics.

- Conversion time is minimum 5.0 µs (including sampling time when machine clock is 33 MHz) .
- Conversion method is RC sequential comparison conversion method with sample holding circuit.
- 10- or 8-bit resolution can be selected.
- Analog input pin can be selected from 8 channels using the program.
- interruption request can be generated when A/D conversion ends.
- Data is not lost even during continuous conversion as conversion data protection function works while interruptions are permitted.
- Initiation factors for conversion can be selected from software, 16-bit reload timer 2 (rising edge) , or external pin trigger (L level detection) .

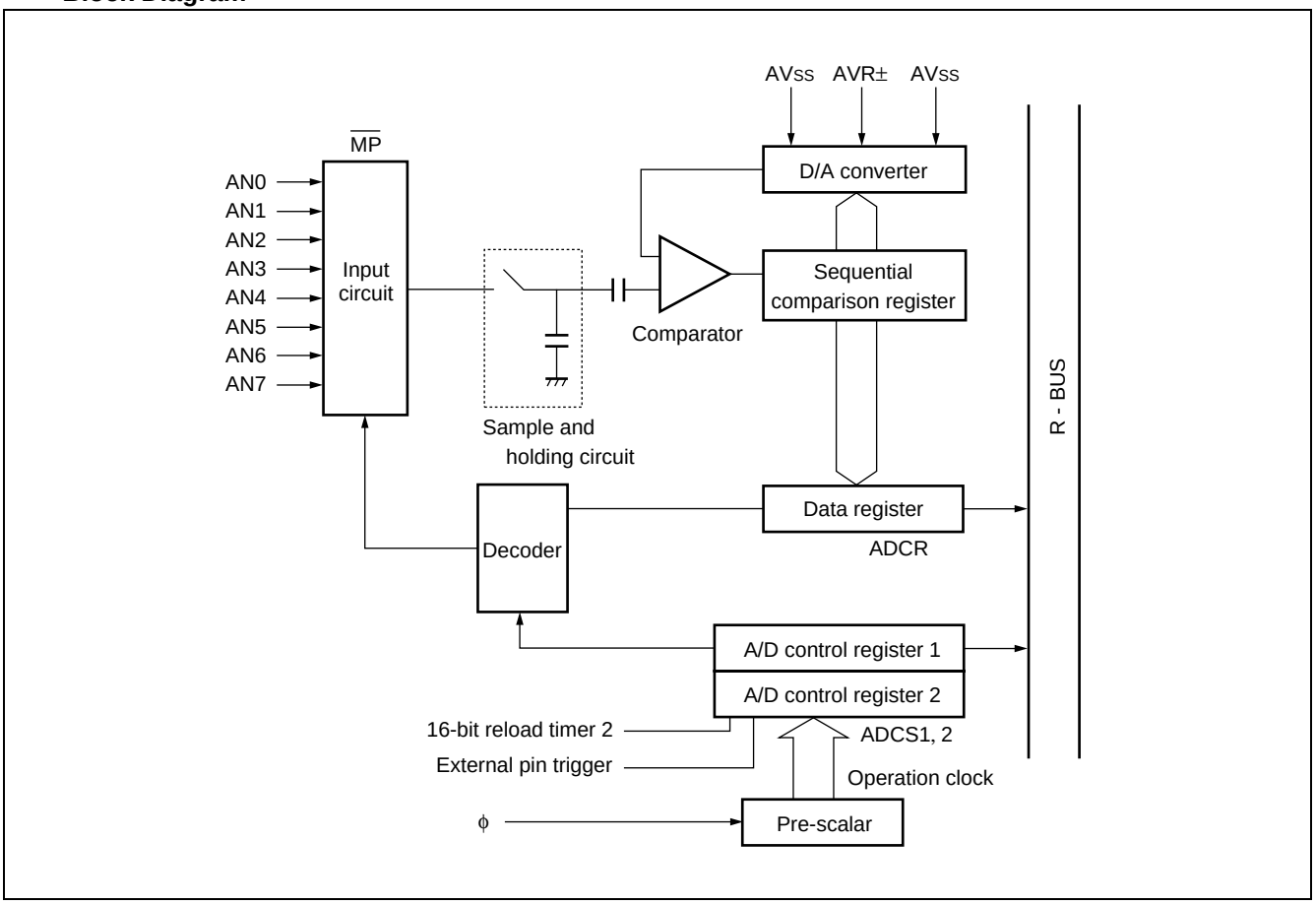
There are three types of conversion modes.

Table 13.1-1 Conversion Modes of 8-/10-bit A/D Converter

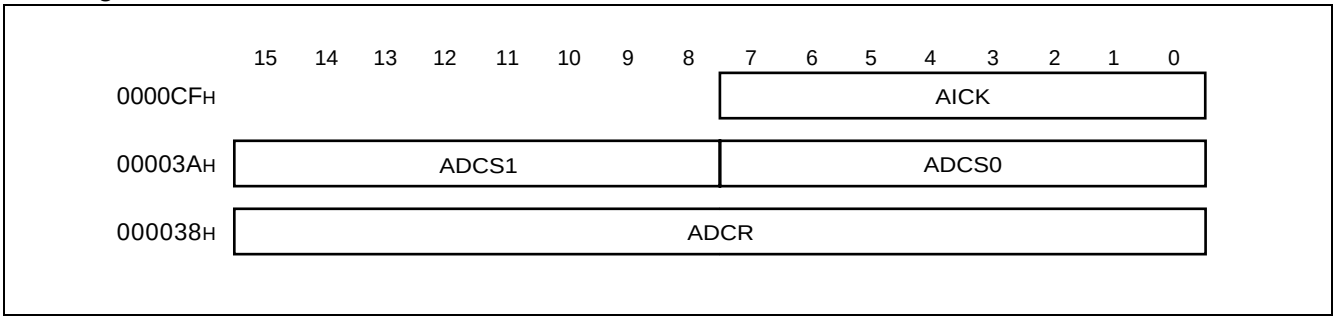
Conversion Modes	Single Conversion Operation	Scan Conversion Operation
Single conversion mode	Converts the specified channel (1 channel only) once and ends.	Converts a series of channels (up to 8 channels can be specified) once and ends.
Consecutive conversion mode	Repeatedly converts the specified channel (1 channel only) .	Repeatedly converts a series of channels (up to 8 channels can be specified) .
Stop conversion mode	Suspends after converting the specified channel (1 channel only) once and waits until the next one is initiated.	Converts a series of channels (up to 8 channels can be specified) but is suspended between each channel conversion and waits until the next one is initiated.

- Block Diagram of 8-/10-bit A/D Converter
  The 8-/10-bit A/D converter is configured with the following 9 blocks.
- A/D control status register (ADCS1, 2)
- A/D data register (ADCR)
- Clock selector (input clock selector to initiate A/D conversion)
- Decoder
- Analog channel selector
- Sample holding circuit
- D/A converter
- Comparator
- Control circuit

- **Block Diagram**



- **Register List**



12. 8-bit D/A Converter

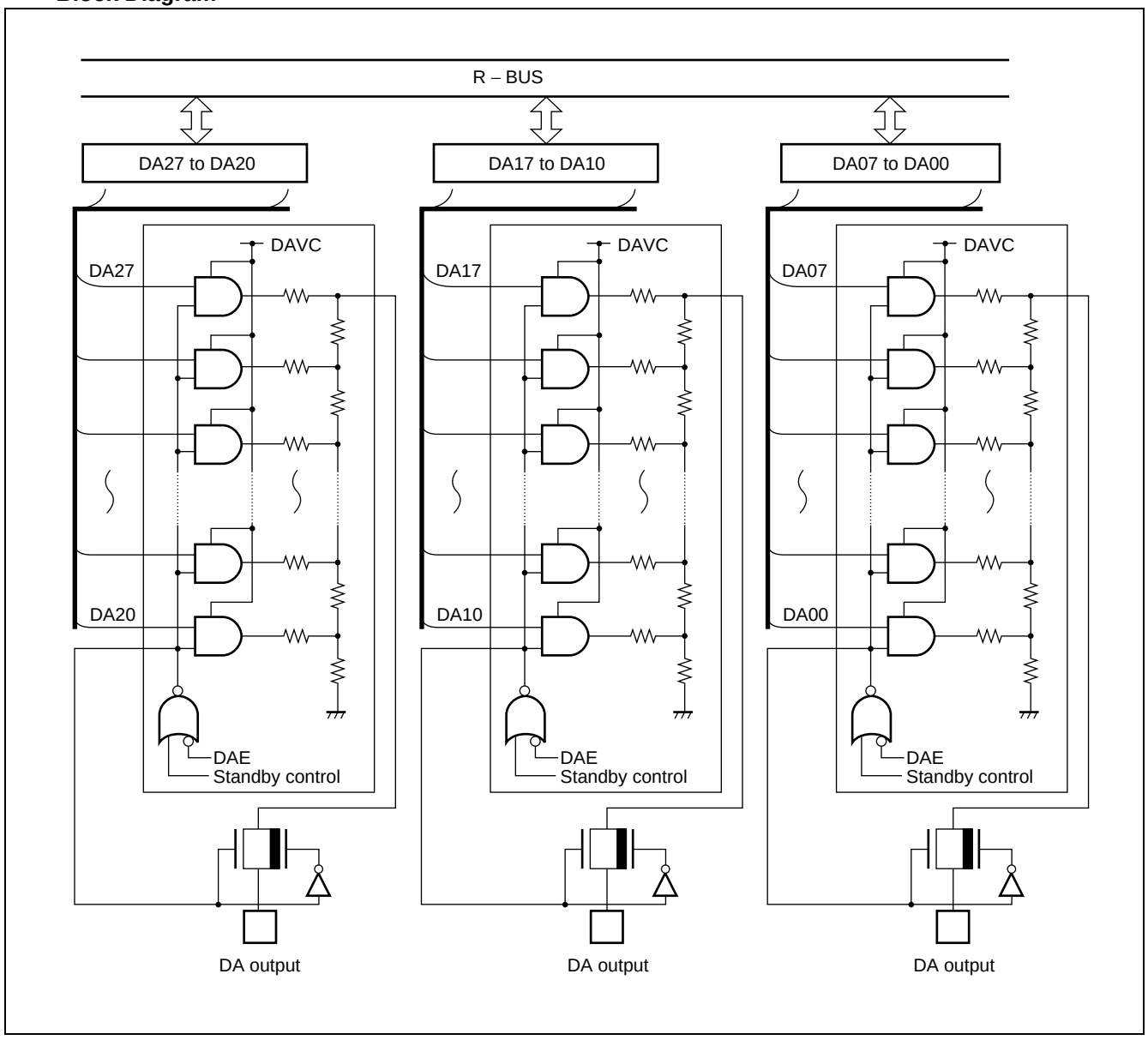
The 8-bit D/A converter is an R-2R type D/A converter with 8-bit resolution.

- **Characteristics of the 8-bit D/A converter**
  The MB81130 series features a 3-channel D/A converter and output control can be carried out individually by the D/A control register.
- Block Diagram of 8-bit D/A Converter

The 8-bit D/A converter is configured with the following three blocks.

- 8-bit resistance ladder
- Data register
- Control register

- **Block Diagram**



- **8-bit D/A Converter Pins**
  D/A converter pins are dedicated pins.

- **Registers of 8-bit D/A Converter**

The 8-bit D/A converter has the following two registers.

D/A control register (DACR0, 1, 2)
D/A data register (DADR2, 1, 0)

- **Register list**

D/A converter data register 0

DADR0
$00000AB_H$

bit	7	6	5	4	3	2	1	0
	DA07	DA06	DA05	DA04	DA03	DA02	DA01	DA00

D/A converter data register 1

DADR1
$00000AA_H$

bit	15	14	13	12	11	10	9	8
	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10

D/A converter data register 2

DADR2
$00000A9_H$

bit	23	22	21	20	19	18	17	16
	DA27	DA26	DA25	DA24	DA23	DA22	DA21	DA20

D/A control register 0

DACR0
$00000A7_H$

bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DAE0

D/A control register 1

DACR1
$00000A6_H$

bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	—	DAE1

D/A control register 2

DACR2
$00000A5_H$

bit	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	DAE2

13. 4-bit Level Comparator

The 4-bit level comparator is the module that compares input levels (large/small) and compares the size of the analog input voltage with 4-bit digital values.

- **Functions of the 4-bit level comparator**

Compares analog voltage that has been input to the analog input pins (input voltage) with 4-bit digital value and has the following characteristics.

- Conversion time is minimum 1 μs (including sampling time) .
- Sampling time is minimum 0.5 μs.
- Interruption requests can be generated when analog comparison ends.

- **Interruption of 4-bit level comparator**

Table 15.1-1 Interruption and DMAC of 4-bit level comparator

Interruption number	Interruption control register		Offset	TBR default address	DMAC
	Register name	Address			
#61 (3D$_H$)	ICR45	00042D$_H$	308$_H$	000FFF08$_H$	×

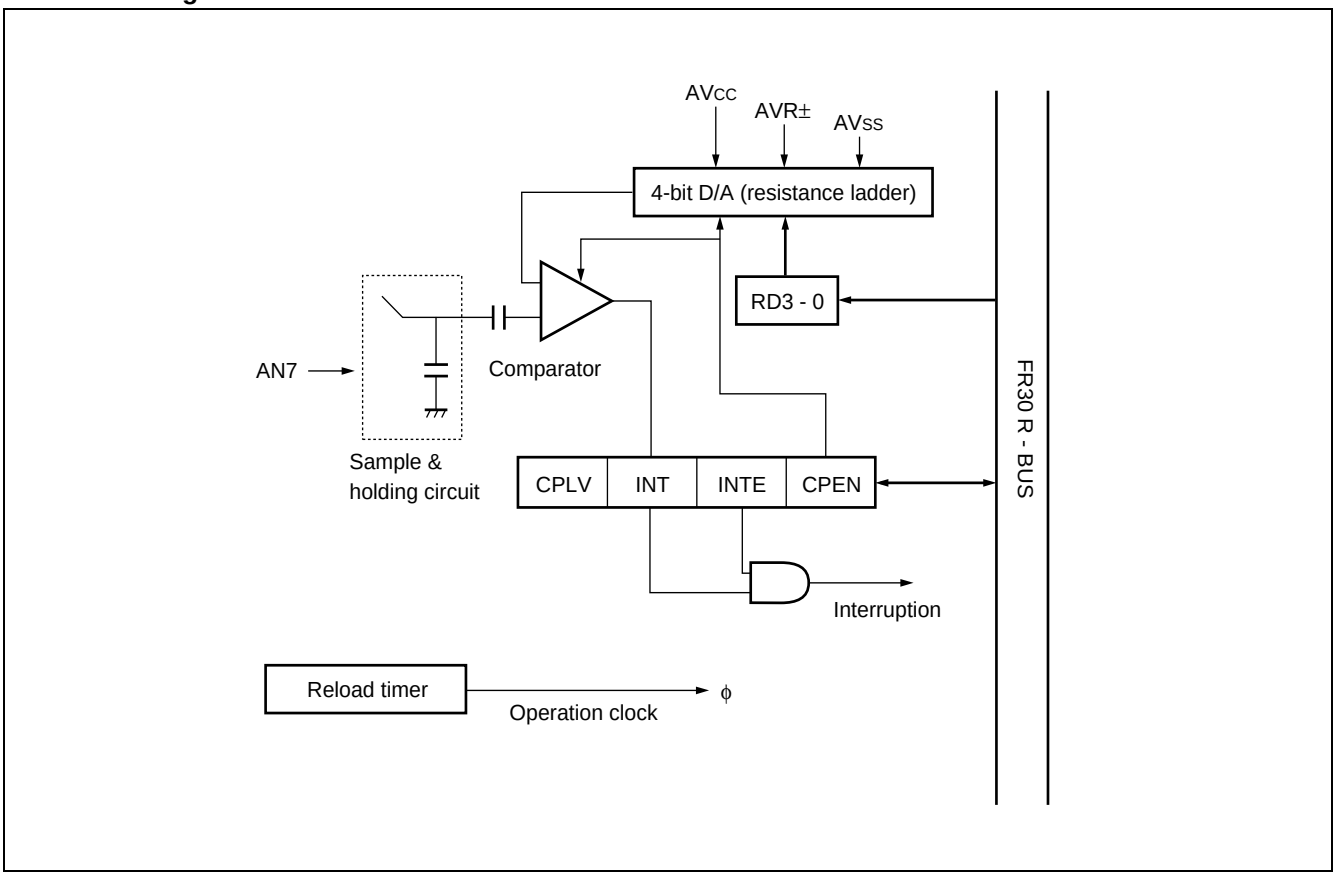
× : Initiation is impossible

- **Block Diagram of 4-bit Level Comparator**

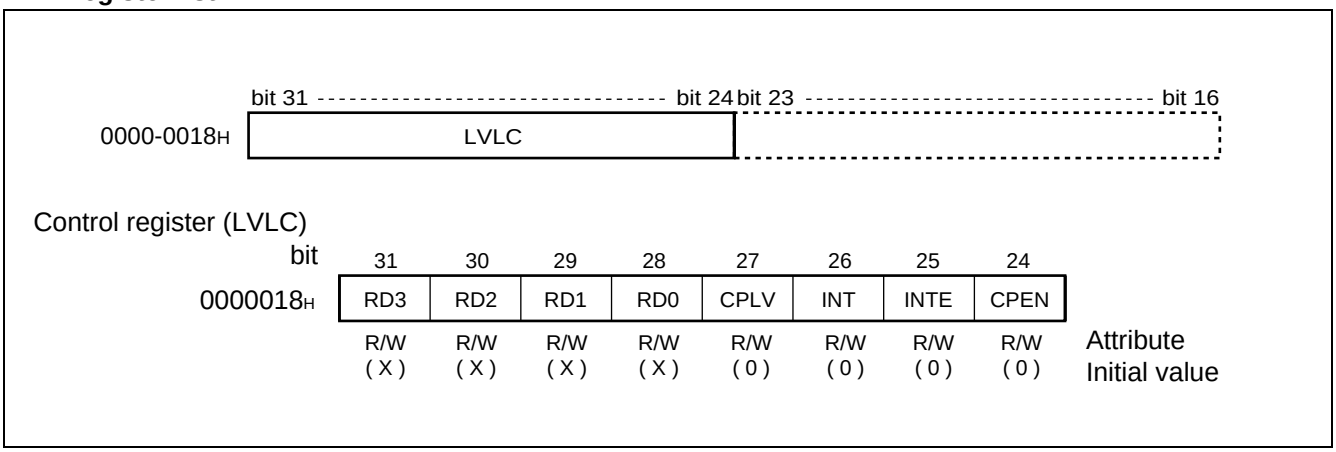
The 4-bit level comparator is configured with the following three blocks.

- Comparator
- 4-bit resistance ladder
- Control register

- **Block diagram**



- **Registers of 4-bit Lev el Comparator**
- **Register list**



14. UART

UART is the general-purpose serial data communications interface to carry out synchronous or asynchronous communication (start-stop synchronization) with external systems. It has a master/slave-type communications function (multiprocessor mode: supporting only master side) as well as normal bi-directional communications function (normal mode).

- **UART Functions**
  UART is the general-purpose serial data communications interface that sends and receives serial data to/from other CPUs and peripheral equipment, and has functions shown in Table 16.1-1.

Table 16.1-1 UART Functions

	Functions
Data buffer	Full-duplex double buffer
Transfer mode	• Clock synchronous (without start-stop bit) • Clock asynchronous (start-stop cycle)
Baud rate	• Dedicated baud rate generator is available. Can be selected from 8 types. • External clock input is possible. • Internal clock (Internal clocks that are provided from 16-bit reload timer supporting each channel can be used.)
Data length	• 7-bit (in case of asynchronous normal mode only) • 8-bit
Signal method	Non Return to Zero (NRZ) method
Reception error detection	• Framing error • Overrun error • Parity error (impossible in case of multiprocessor mode)
Interruption request	• Reception interruption (reception completion, reception error detection) • Transmission interruption (transmission completion)
Master/slave-type communications function (Multiprocessor mode)	Communication between 1 (master) and n (slaves) is possible (Only supports master side)

Note : Start / stop bits are not added by UART and only data is transferred.

Table 16.1-2 UART Operations Mode

Operations mode		**Data length**		**Synchronization method**	**Stop bit length**
		Without parity	**With parity**		
0	Normal mode	7-bit or 8-bit		Asynchronous	1-bit or 2-bit *2
1	Multiprocessor mode	8 + 1*1	—	Asynchronous	
2	Normal mode	8	—	Synchronous	N/A

— : Setting is impossible

*1 : " + 1" is address / data selection bit (A/D) to be used to control communications.

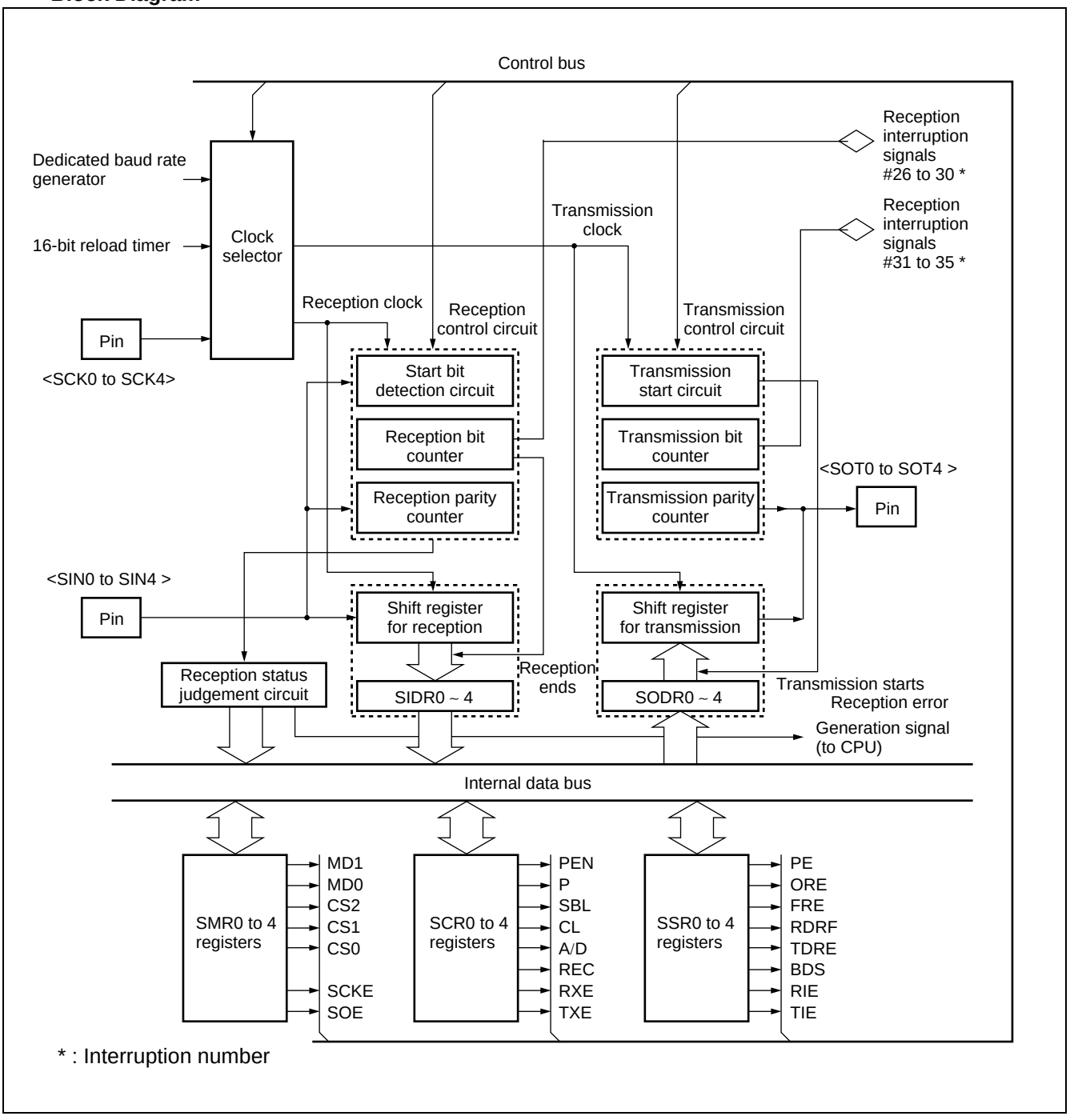
*2 : 1-bit only can be detected for stop bit in case of reception.

- **UART Block Diagram**

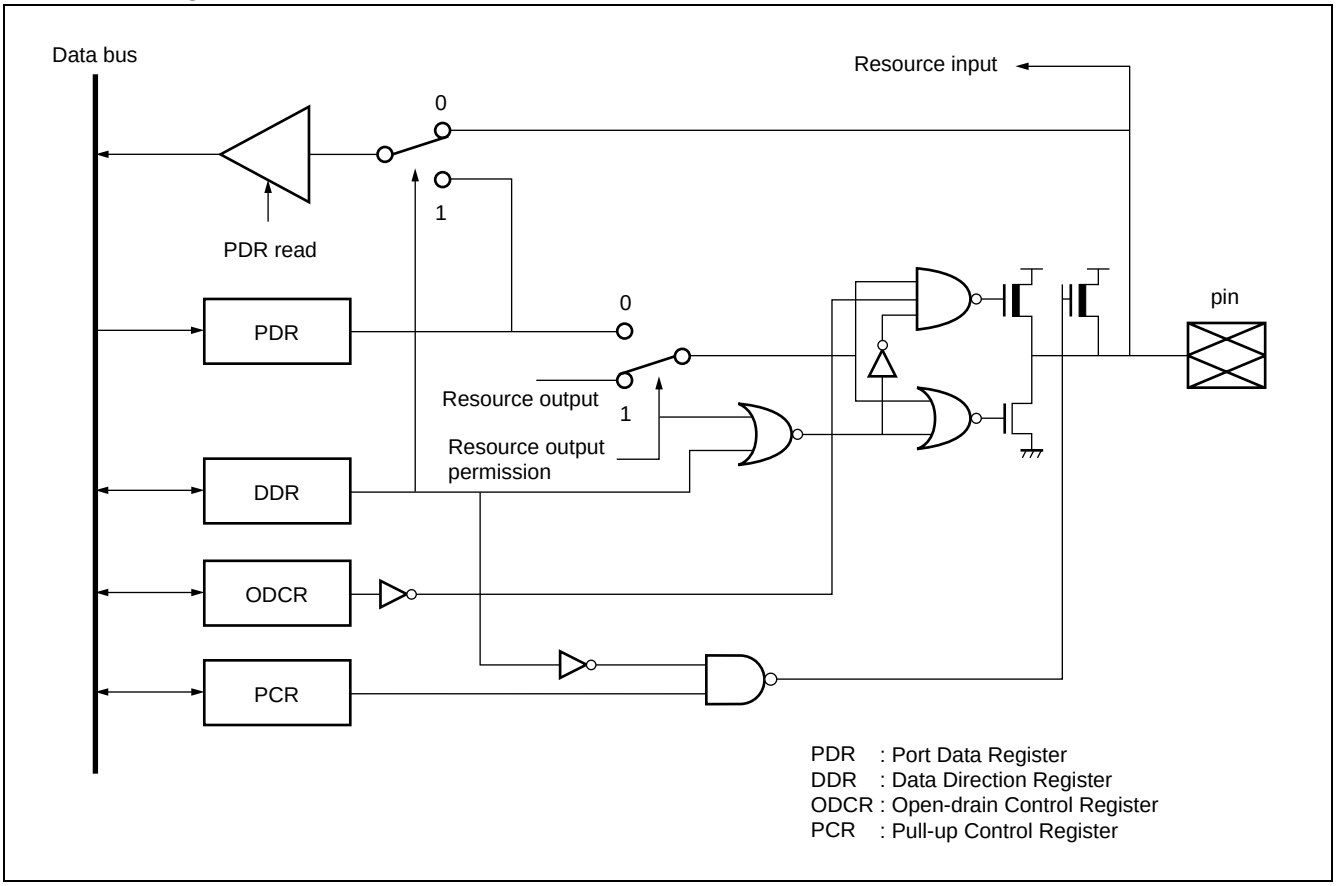
UART is configured with the following 11 blocks.

- Clock selector
- Reception control circuit
- Transmission control circuit
- Reception status judgement circuit
- Shift register for reception
- Sift register for transmission
- Mode register (SMR0 to 4)
- Control register (SCR0 to 4)
- Status register (SSR0 to 4)
- Input data register (SIDR0 to 4)
- Output data register (SODR0 to 4)

- **Block Diagram**



- **Block Diagram of UART Pins**



- **Register List**

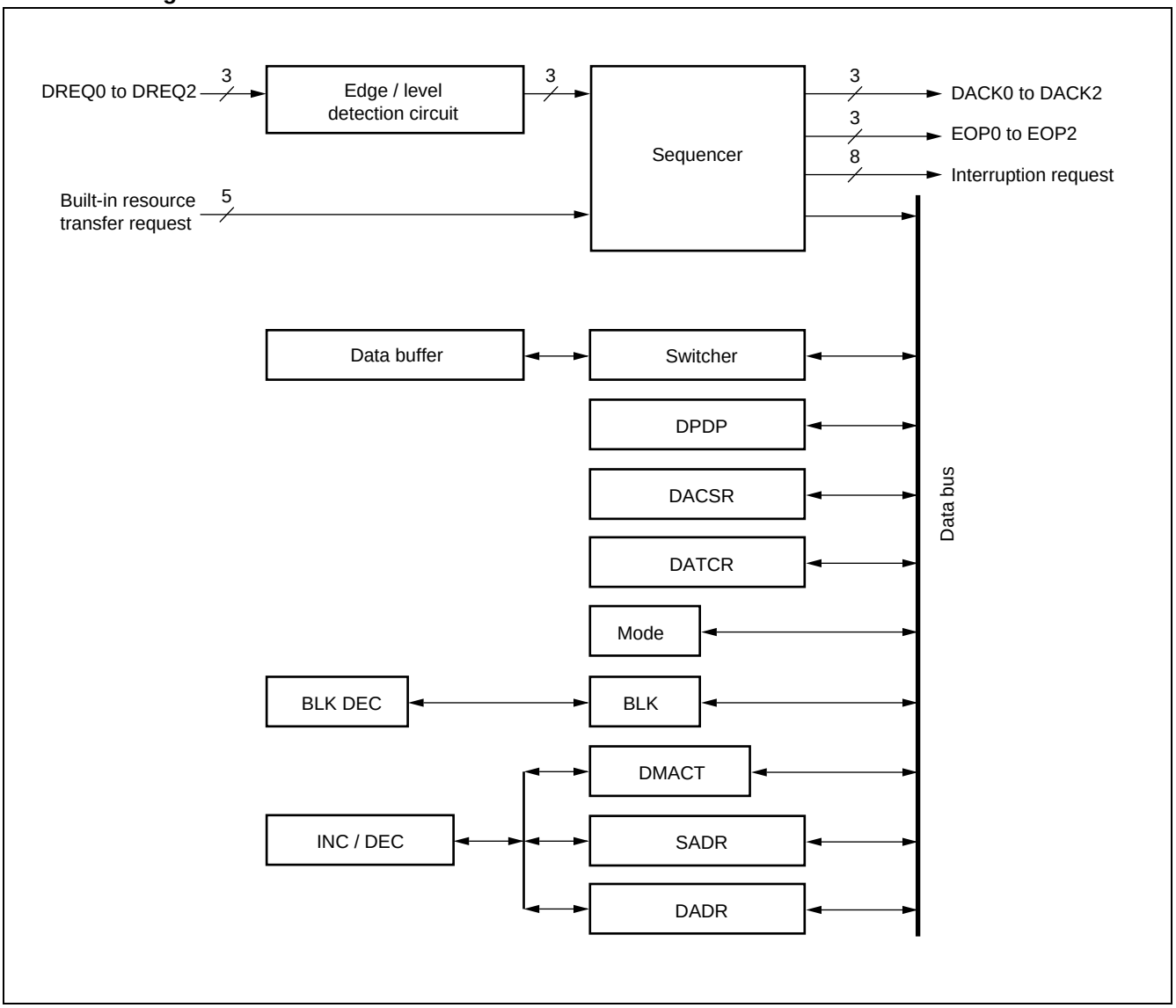
Address	bit 15 ---------- bit 8	bit 7 ---------- bit 0
ch0 : 0000_001EH, 1FH ch1 : 0000_0022H, 23H ch2 : 0000_0026H, 27H ch3 : 0000_0072H, 73H ch4 : 0000_0076H, 77H	Control register (SCR)	Mode register (SMR)
ch0 : 0000_001CH, 1DH ch1 : 0000_0020H, 21H ch2 : 0000_0024H, 25H ch3 : 0000_0070H, 71H ch4 : 0000_0074H, 75H	Status register (SSR)	Input/output data register (SIDR/SODR)
ch0 : 0000_007AH ch1 : 0000_0078H ch2 : 0000_007EH ch3 : 0000_007CH ch4 : 0000_0082H	Communications pre-scalar control register (CDCR)	Vacant

15. DMA Controller

The DMA controller is the built-in module of the MB91130 series that carrie out direct memory access (DMA) transfers.

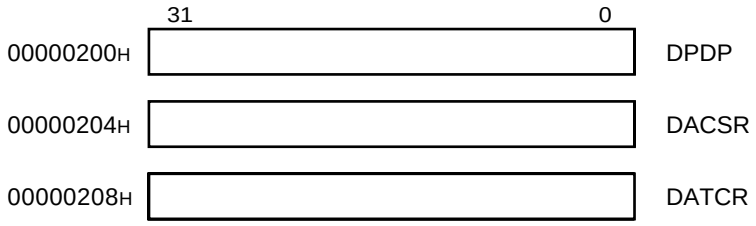
- **Characteristics of the DMA Controller**
- 8 channels
- 3 transfer mode types : single/block transfer, burst transfer, continuous transfer
- Transfer between overall address areas
- Maximum 65,536 transfers
- Interruption function when transfer ends
- Increase/decrease in transfer addresses can be selected using software
- 3 external transfer request input/output pins and 3 external transfer end output pins

- **Block Diagram**

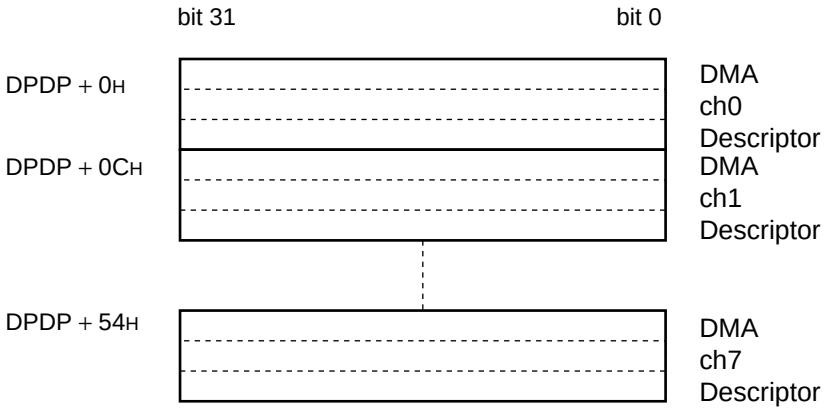


- **Register List**

(In DMAC : DMAC internal registers)



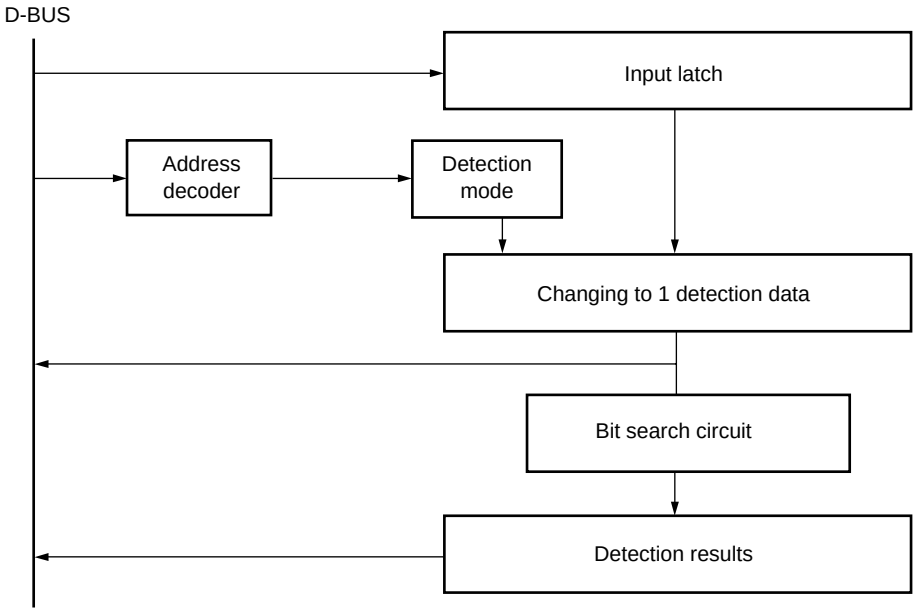
(On RAM : DMA descriptors)



16. Bit Search Module

The bit search module searches for 0, 1 or change points on data that has been written in the input register, and returns the detected bit position.

- **Block Diagram**



- **Register List**

		31 ... 0	
Address :	000003F0H	BSD0	Data register for 0 detection
Address :	000003F4H	BSD1	Data register for 1 detection
Address :	000003F8H	BSDC	Data register for change point detection
Address :	000003FCH	BSRR	Detection results register

17. FLASH Memory

The MB91FV130 / MB91F133 have a 254-KB (2 Mbit) capacity and feature a FLASH memory that can write each half-word (16 bits) using the FR-CPU, delete individual sectors sector and delete groups of sectors together using a single 3-V power source.

• Outline of FLASH Memory

This is a built-in 3-V 254-KB FLASH memory. This FLASH memory is the same as our 2-Mbit (256 K × 8 / 128 K × 16) FLASH memory MBM29LV400C and writing is possible from outside the device using a ROM writer. If used as a built-in ROM of the FR-CPU, as well as having an equivalent function to the MBM29LV400C, instructions / data can be read per word (32 bits) and high-speed operation of the device can be realized.

Refer to the MBM29LV400C data sheet as well as this manual.

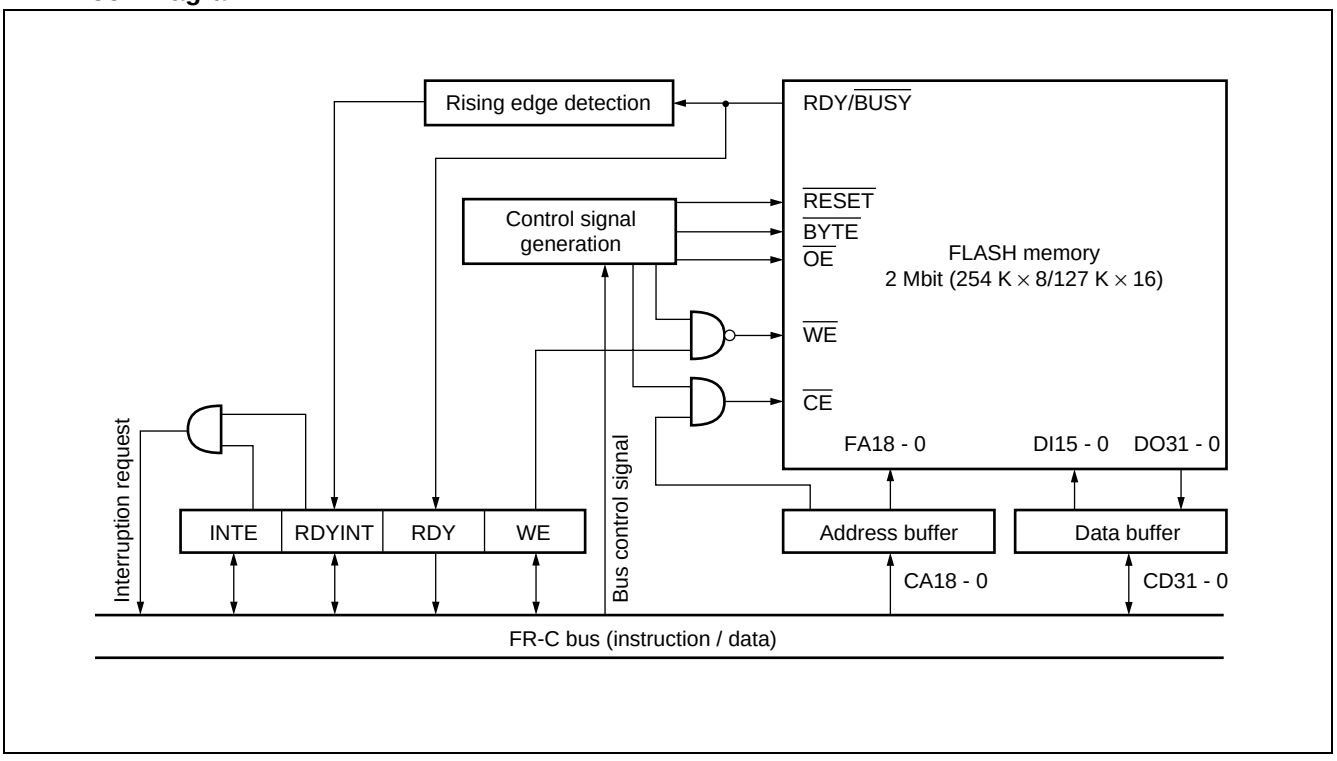
The following functions can be realised in MB91FV130 / MB91F133 by combining the FLASH memory macro and FR-CPU interface circuits.

- Functioning as memory for CPU program / data storage
  Access is possible with 32-bit bus width when used as ROM
  Reading / writing and erasing (automatic program algorithm *) are possible using CPU
- MBM29LV400C-equivalent function of single FLASH memory products
  Reading / writing and erasing (automatic program algorithm *) are possible using ROM writer

A case where this FLASH memory is used from FR-CPU is described in this section.
Refer to the ROM writer manual separately for details if this FLASH memory is used from ROM writer.

* : Automatic program algorithm = Embedded Algorithm ™
Embedded Algorithm ™ is the trademark of Advanced Micro Device.

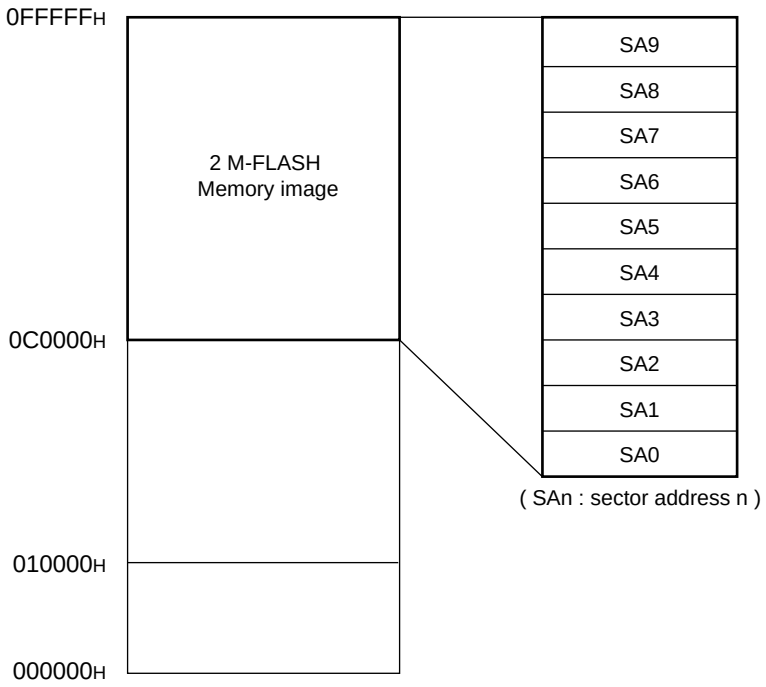
• Block Diagram



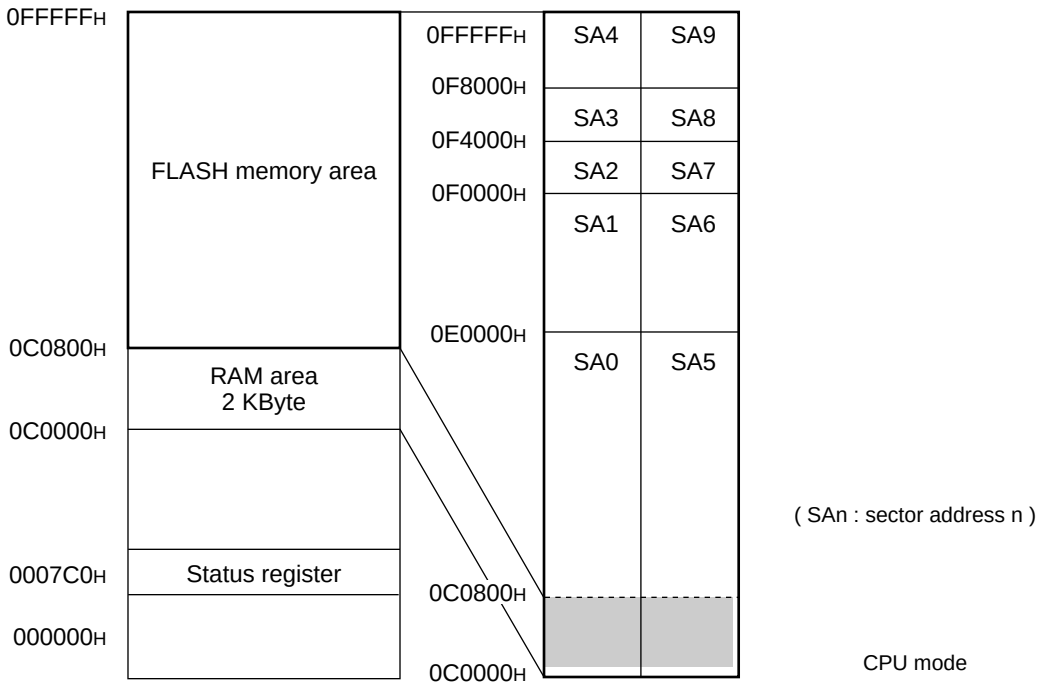
- **Memory Map**

FLASH memory mode and CPU mode for address mapping of FLASH memory are different. Mapping under each mode is shown as follows.

- **Memory map in FLASH memory mode**



- **Memory map in CPU memory mode**



- **Sector address table**

Sector Address	Address Area	Position of bit handled	Sector Capacity
SA5	000C0802, 3h to 000DFFFE, Fh (LSB side 16 bit)	bit 15 to 0	63 Kbyte
SA6	000E0002, 3h to 000EFFFE, Fh (LSB side 16 bit)	bit 15 to 0	32 Kbyte
SA7	000F0002, 3h to 000F3FFE, Fh (LSB side 16 bit)	bit 15 to 0	8 Kbyte
SA8	000F4002, 3h to 000F7FFE, Fh (LSB side 16 bit)	bit 15 to 0	8 Kbyte
SA9	000F8002, 3h to 000FFFFE, Fh (LSB side 16 bit)	bit 15 to 0	16 Kbyte
SA0	000C0800, 1h to 000DFFFC, Dh (MSB side 16 bit)	bit 31 to 16	63 Kbyte
SA1	000E0000, 1h to 000EFFFC, Dh (MSB side 16 bit)	bit 31 to 16	32 Kbyte
SA2	000F0000, 1h to 000F3FFC, Dh (MSB side 16 bit)	bit 31 to 16	8 Kbyte
SA3	000F4000, 1h to 000F7FFC, Dh (MSB side 16 bit)	bit 31 to 16	8 Kbyte
SA4	000F8000, 1h to 000FFFFC, Dh (MSB side 16 bit)	bit 31 to 16	16 Kbyte

- **Registers of FLASH Memory**

There are two types of FLASH memory registers, namely status register (FLCL) and wait register (FWTC).

- **Status Register (FLCR) (CPU mode)**

This register indicates the operation status of the FLASH memory. It controls interruption to the CPU and writing to the FLASH memory.

Access is possible only in CPU mode. This register must not be accessed under Read / Modify / Write instructions.

0007C0H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
INTE	RDYINT	WE	RDY	—	—	—	LPM
R/W	R/W	R/W	R	—	—	—	R/W
(0)	(0)	(0)	(X)	(X)	(X)	(X)	(0)

- **Wait Register (FWTC)**

Carries out wait control of the FLASH memory in CPU mode. Also, controls access to high-speed reading (33MHz) of FLASH memory. Configuration of Wait Register (FWTC) is as follows :

0007C4H

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
—	—	—	—	—	FACH	WTC1	WTC0
—	—	—	—	—	W	R/W	R/W
(—)	(—)	(—)	(—)	(—)	(0)	(0)	(0)

Note : FACH bit should be set to 1 or WTC1/0 should be set to 01b to operate machine clocks of CPUs exceeding 25 MHz.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power voltage	$V_{CC}5$	V_{SS} – 0.3	V_{SS} + 6.5	V	
Power voltage	$V_{CC}3$	V_{SS} – 0.3	V_{SS} + 3.8	V	
Analog power voltage	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.5	V	*1
Standard analog voltage	AVRH	V_{SS} – 0.3	V_{SS} + 6.5	V	*1
Input voltage	V_{I5}	V_{SS} – 0.3	$V_{CC}5$ + 0.3	V	
Input voltage	V_{I3}	V_{SS} – 0.3	$V_{CC}3$ + 0.3	V	X0, X1, X0A, X01A
Analog pin input voltage	V_{IA}	V_{SS} – 0.3	AV_{CC} + 0.3	V	
Output voltage	V_O	V_{SS} – 0.3	$V_{CC}5$ + 0.3	V	
Maximum “L” level output current	I_{OL}	—	10	mA	*2
Average “L” level output current	I_{OLAV}	—	4	mA	*3
Maximum total “L” level output current	ΣI_{OL}	—	100	mA	
Average “L” level total output current	ΣI_{OLAV}	—	50	mA	*4
Maximum “H” level output current	I_{OH}	—	–10	mA	*2
Average “H” level output current	I_{OHAV}	—	–4	mA	*3
Maximum total “H” level output current	ΣI_{OH}	—	–50	mA	
Average “H” level total output current	ΣI_{OHAV}	—	–20	mA	*4
Electricity consumption	P_D	—	500	mW	
Storage temperature	Tstg	–55	+150	°C	

*1 : Care must be taken that this does not exceed $V_{CC}5$ + 0.3 V when the power is turned on. Also, care must be taken that AV_{CC} does not exceed $V_{CC}5$ when the power is turned on. AV_{CC} should be set at the same electrical potential as $V_{CC}5$.

*2 : Peak value of the pin concerned is regulated as the maximum output current.

*3 : Average current within 100 ms flowing in the pin concerned is regulated as the average output current.

*4 : Average current within 100 ms flowing in all pins concerned is regulated as the average total output current.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter		Symbol	Value		Unit	Remarks
			Min.	Max.		
Power voltage	Common	$V_{CC}5$	4.5	5.5	V	Under normal operation
	EVA FLASH	$V_{CC}3$	3.0	3.6	V	Under normal operation
			3.0	3.6		RAM status kept in the case of stop
	MASK ROM	$V_{CC}3$	2.7	3.6	V	Under normal operation
			2.7	3.6	V	RAM status kept in the case of stop
Analog power voltage		AV_{CC}	V_{SS} + 4.5	V_{SS} + 5.5	V	
Standard analog voltage		AVRH	AV_{SS} – 0.3	AV_{CC}	V	
Operating temperature		T_A	0	+70	°C	In external ROM external bus / internal ROM external bus modes
		T_A	–40	+70	°C	In single-chip mode

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(MASK Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 2.7\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)
(FLASH Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 3.0\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	Input excluding following (*1)	—	0.7 $V_{CC}5$	—	$V_{CC}5 + 0.3$	V	
	V_{IHS}	*1 Hysteresis input pin	—	$V_{CC}5 - 0.4$	—	$V_{CC}5 + 0.3$	V	
"L" level input voltage	V_{IL}	Input excluding following (*1)	—	$V_{SS} - 0.3$	—	0.2 $V_{CC}5$	V	
	V_{ILS}	*1 Hysteresis input pin	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.4$	V	
"H" level output voltage	V_{OH}	—	$V_{CC}5 = 5.0\ V$, $I_{OH} = -4.0\ mA$	2.6	—	—	V	
"L" level output voltage	V_{OL}	—	$V_{CC}5 = 5.0\ V$, $I_{OL} = 4.0\ mA$	—	—	0.6	V	
Input leak current	I_{LI}	—	$V_{CC}5 = 5.0\ V$, $V_{SS} < V_I < V_{DD}$	− 5	—	5	µA	
Pull up resistance value	R_{PULL}	RST	—	—	50	—	kΩ	
Power current	$I_{CC}5$	$V_{CC}5$	$V_{CC}5 = 5.0\ V$	—	15	20	mA	*2
	$I_{CC}3$	$V_{CC}3$	$V_{CC}3 = 3.0\ V$	—	50	100	mA	
	$I_{CCS}5$	$V_{CC}5$	$V_{CC}5 = 5.0\ V$	—	15	20	mA	*2
	$I_{CCS}3$	$V_{CC}3$	$V_{CC}3 = 3.0\ V$	—	24	85	mA	
	$I_{CCH}5$	$V_{CC}5$	$V_{CC}5 = 5.0\ V$, $T_A = 25\ °C$	—	10	100	µA	*3
	$I_{CCH}3$	$V_{CC}3$	$V_{CC}3 = 3.0\ V$, $T_A = 25\ °C$	—	10	100	µA	
Power current (FLASH models)	$I_{CC}3$	$V_{CC}3$	$V_{CC}3 = 3.3\ V$	—	80	120	mA	
	$I_{CCS}3$	$V_{CC}3$	$V_{CC}3 = 3.3\ V$	—	50	90	mA	
Input capacity	C_{IN}	Other than V_{CC}, AV_{CC}, AV_{SS}, AV_{RH} and V_{SS}	—	—	10	—	pF	

*1 : Refer to "PIN FUNCTION DESCRIPTIONS"

*2 : In case of CLK pin output only ($C_L = 80\ pF$)

*3 : Output pin OPEN

4. AC Characteristics

(1) Clock Timing Standard

(MASK Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 2.7\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)
(FLASH Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 3.0\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)

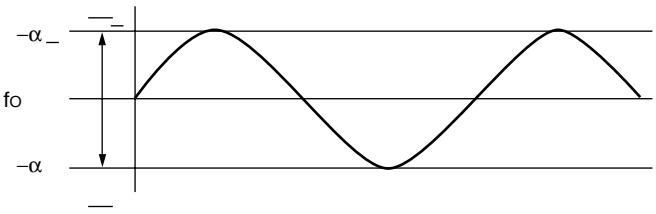
Parameter		Sym-bol	Pin name	Condi-tions	Value		Unit	Remarks
					Min.	Max.		
Clock frequency (high-speed, self-oscillation)		f_C	X0, X1	—	9	16.5	MHz	Self oscillation available area
Clock frequency (high-speed, PLL usage)								PLL usable area by self-oscillation input
Clock frequency (low-speed)		f_{CA}	X0A, X1A		32		kHz	Self oscillation
Clock cycle time		t_C	—		30.3	31250	ns	
Frequency fluctuation rate *1 (when PLL locked)		Δf	—		—	10	%	
Internal operation clock frequency	CPU system	f_{CP}	—	—	0.032	33	MHz	
	Bus system	f_{CPB}			0.032	25		
	Peripheral system	f_{CPP}			0.032	25		Excluding analog area *2
					1	25		Analog area *2
Internal operation clock cycle time	CPU system	t_{CP}	—		30.3	31250	ns	
	Bus system	t_{CPB}			40	31250		
	Peripheral system	t_{CPP}			40	31250		Excluding analog area *2
					40	1000		Analog area *2

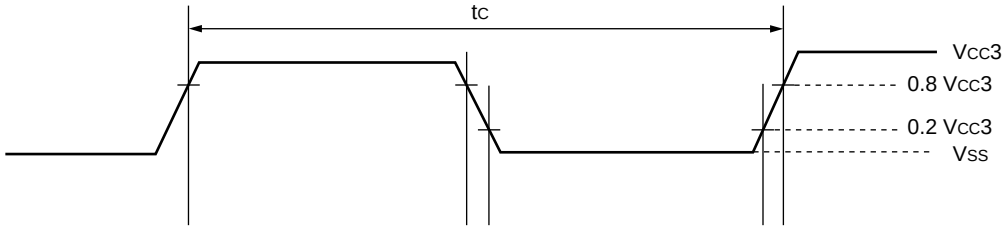
*1 : Frequency fluctuation rate indicates the maximum fluctuation ratio from the setting central frequency during locking in case of doubling.

*2 : The targeted analog areas are the A/D and level comparator.

$$\Delta f = \frac{|\alpha|}{f_O} \times 100\ (\%)$$

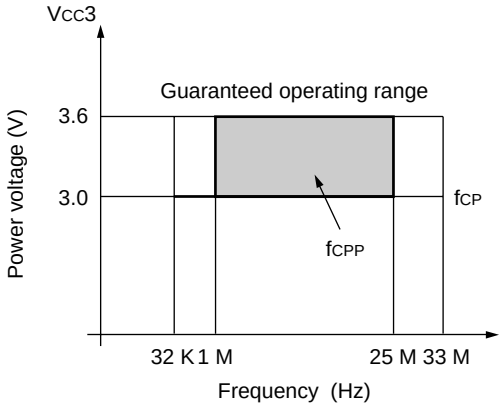
Central frequency f_O



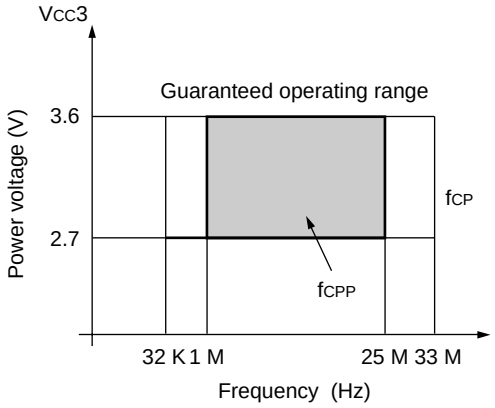


Peripheral system clock setting permitted area (A/D, D/A level comparator : 5 V ± 10%)

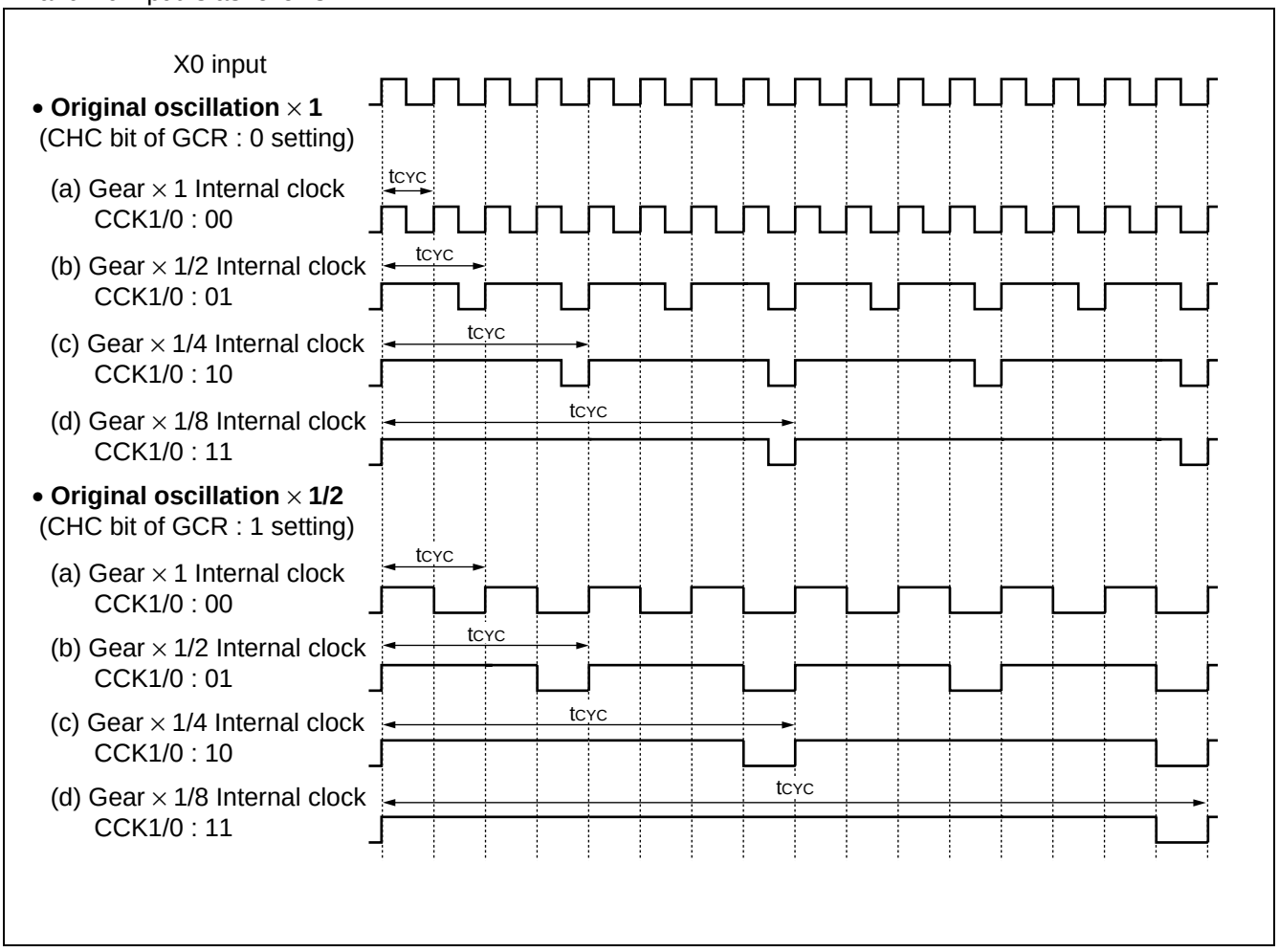
< FLASH model >



< MASK ROM model >



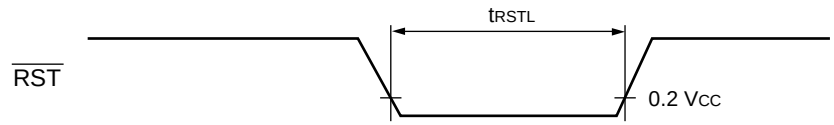
The relationship between the internal clock set by the CHC/CCK1/CCK0 bit of the Gear Control Register (GCR) and X0 input is as follows.



(2) Reset Input Standards

(MASK Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 2.7\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)
(FLASH Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 3.0\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)

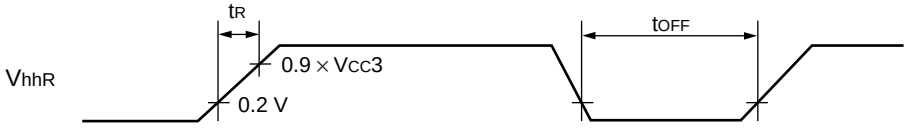
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	$\overline{RST}$	—	$t_{CP} \times 5$	—	ns	



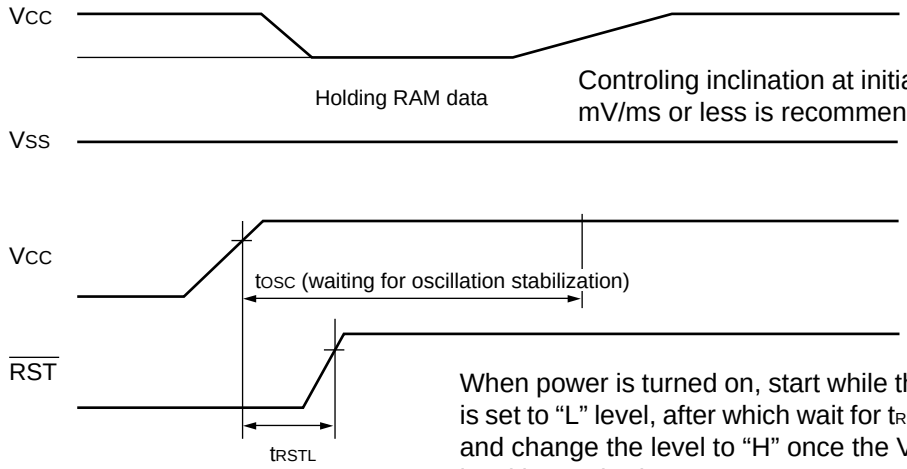
(3) Power On Reset

(MASK Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 2.7\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)
(FLASH Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 3.0\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Power startup time	f_R	V_{CC}	—	—	20	ms	
Power cut time	t_{OFF}			2	—	ms	
Waiting time for oscillation stabilization	t_{OSC}	—		$2^{13}\ t_C$	—	ns	



If the power voltage is changed rapidly, “Power On Reset” may be initiated. To start up smoothly, controlling any voltage fluctuations that may occur during operation is recommended.



When power is turned on, start while the $\overline{RST}$ pin is set to “L” level, after which wait for t_{RSTL} minutes and change the level to “H” once the V_{CC} power level is reached.

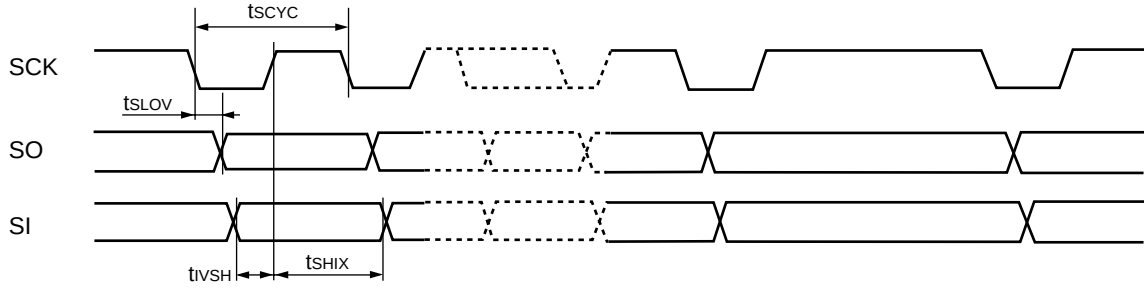
(4) Serial I/O (CH0 to 4)

(MASK Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 2.7\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)
(FLASH Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 3.0\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)

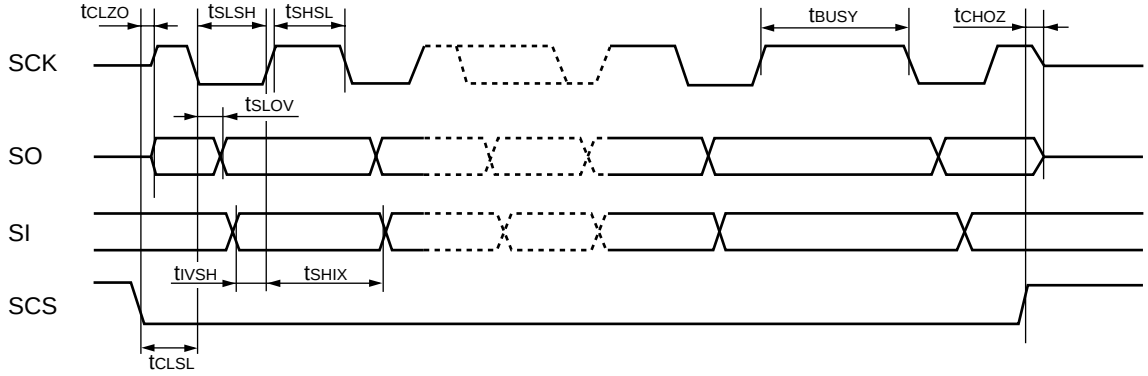
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	—	Internal clock	8 t_{CPP}	—	ns	
SCK ↓ → SO delay time	t_{SLOV}	—		−10	50	ns	
Valid SI → SCK ↑	t_{IVSH}	—		50	—	ns	
SCK ↑ → Valid SI holding time	t_{SHIX}	—		50	—	ns	
Serial clock H pulse width	t_{SHSL}	—	External clock	4 t_{CPP} – 10	—	ns	*
Serial clock L pulse width	t_{SLSH}	—		4 t_{CPP} – 10	—	ns	
SCK ↓ → SO delay time	t_{SLOV}	—		0	50	ns	
Valid SI → SCK ↑	t_{IVSH}	—		50	—	ns	
SCK ↑ → Valid SI holding time	t_{SHIX}	—		50	—	ns	
Serial busy period	t_{BUSY}	—		—	6 t_{CPP}	ns	
SCS ↓ → SCK, SO delay time	t_{CLZO}	—		—	50	ns	
SCS ↓ → SCK input MASK time	t_{CLSL}	—		—	3 t_{CPP}	ns	
SCS ↑ → SCK, SO Hi-Z time	t_{CHOZ}	—		50	—	ns	

*: Will be Min. 1 t_{CPP} – 10 if pre-scalar setting is CS2, 1, 0 = 000.

Internal shift clock mode



External shift clock mode

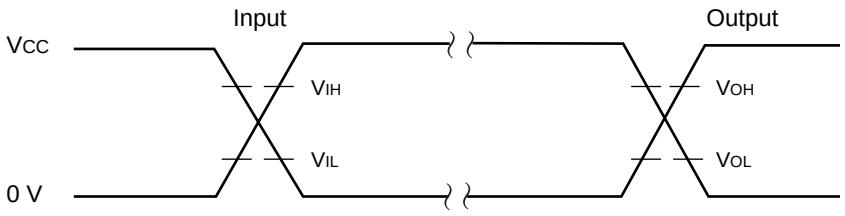


(5) External Bus Measurement Conditions

The following conditions apply to items without specific regulations.

- **Alternating current standard measurement condition**

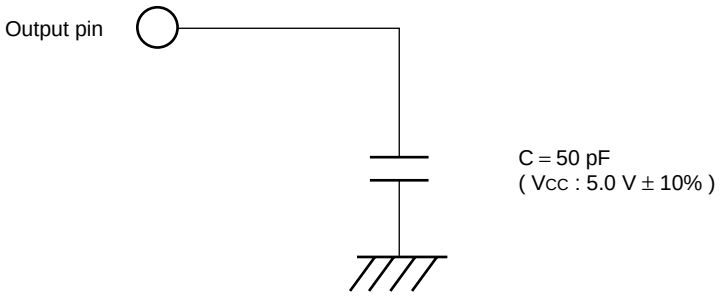
V_{CC} : 5.0 V ± 10%



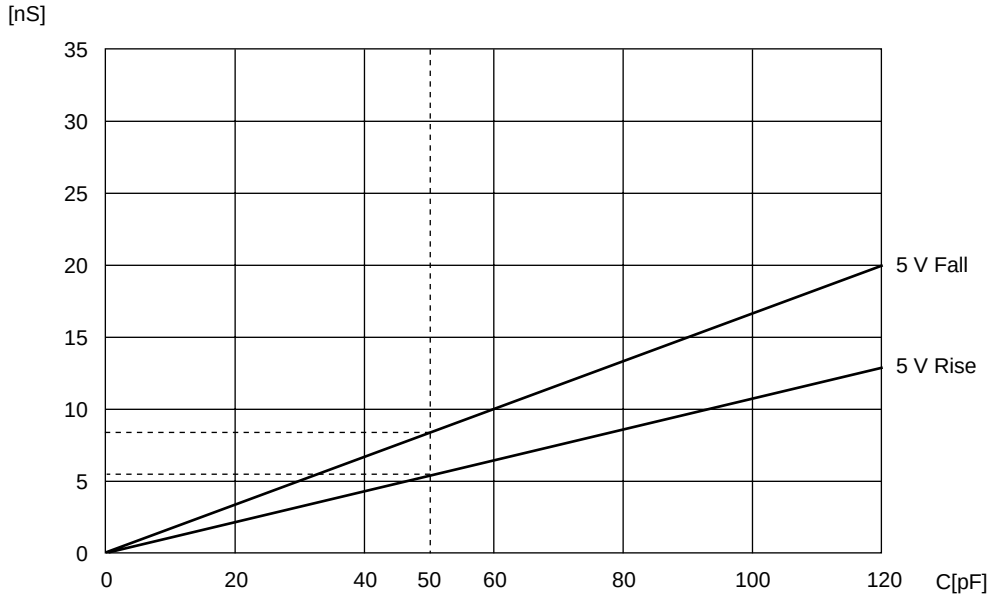
V_{IH}	2.4 V	V_{OH}	2.4V
V_{IL}	0.8 V	V_{OL}	0.8V

(Rise/fall time of input is 10 ns or less)

- **Load condition**



- **Load capacity – Delay time characteristic (Internally-based output delay)**



(6) Normal Bus Access Read/Write Operation

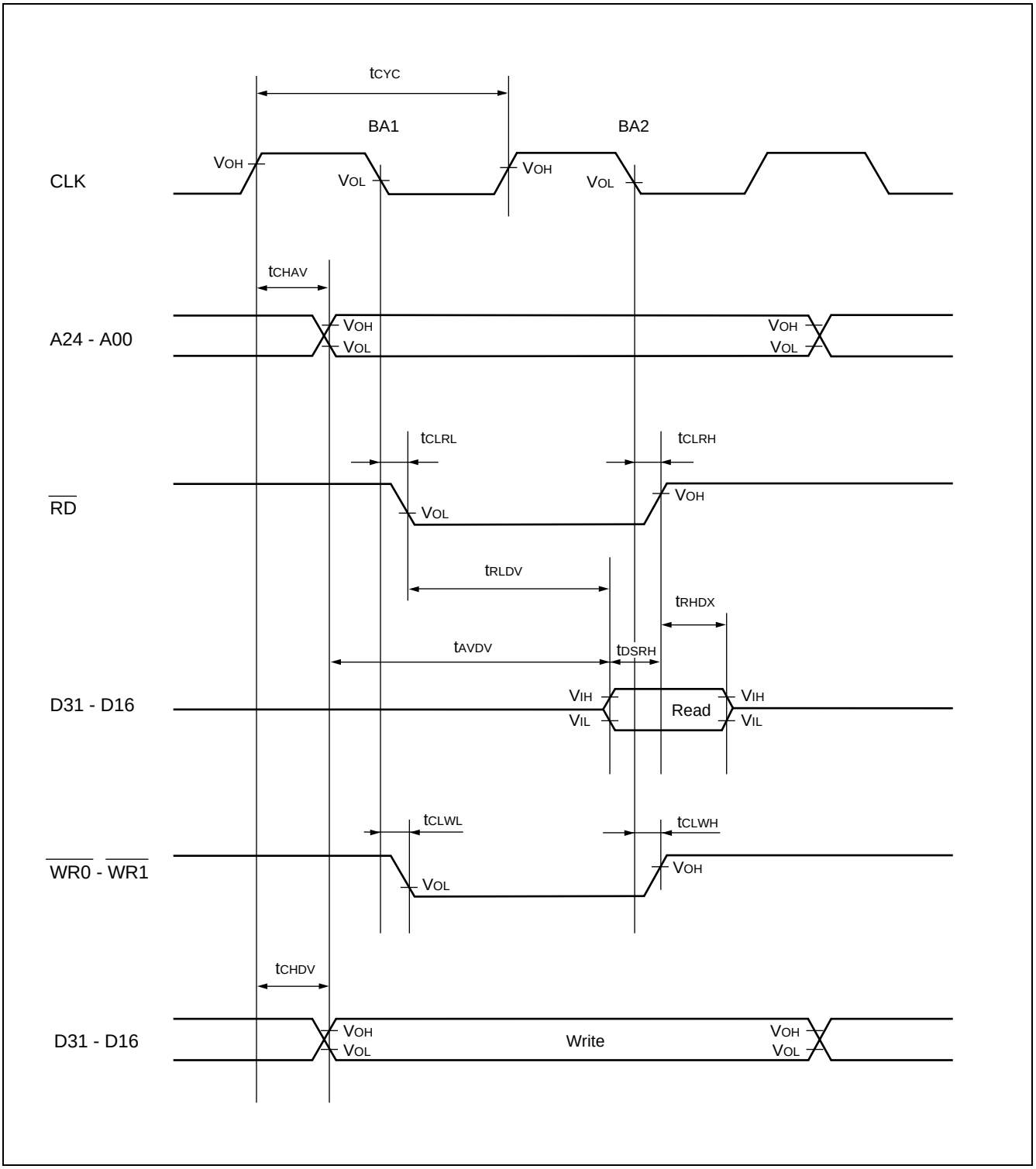
(MASK Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 2.7\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)
(FLASH Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 3.0\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
Address delay time	t_{CHAV}	CLK A23 to A00	—	—	15	ns	
Data delay time	t_{CHDV}	CLK D31 to D16		—	15	ns	
$\overline{RD}$ delay time	t_{CLRL}	CLK $\overline{RD}$		—	10	ns	
$\overline{RD}$ delay time	t_{CLRH}			—	10	ns	
$\overline{WR0}$ to $\overline{1}$ delay time	t_{CLWL}	CLK $\overline{WR0}$ to $\overline{1}$		—	10	ns	
$\overline{WR0}$ to $\overline{1}$ delay time	t_{CLWH}			—	10	ns	
Valid address / valid data input time	t_{AVDV}	A23 to A00 D31 to D16		—	$3 / 2 \times t_{CYC} - 25$	ns	*1, *2
$\overline{RD} \downarrow \rightarrow$ valid data input time	t_{RLDV}	$\overline{RD}$ D31 to D16		—	$t_{CYC} - 15$	ns	*1
Data setup $\rightarrow \overline{RD} \uparrow$ time	t_{DSRH}			15	—	ns	
$\overline{RD} \uparrow \rightarrow$ Data holding time	t_{RHDX}			0	—	ns	

*1 : Time ($t_{CYC} \times$ number of cycles extended) needs to be added to this standard if the bus is extended by automatic waiting insertion and RDY input.

*2 : Values of this standard are in case of gear cycle × 1.
If the gear cycle is set to 1/2, 1/4 or 1/8, calculation should be made using the following formula and replacing n with 1/2, 1/4 or 1/8.

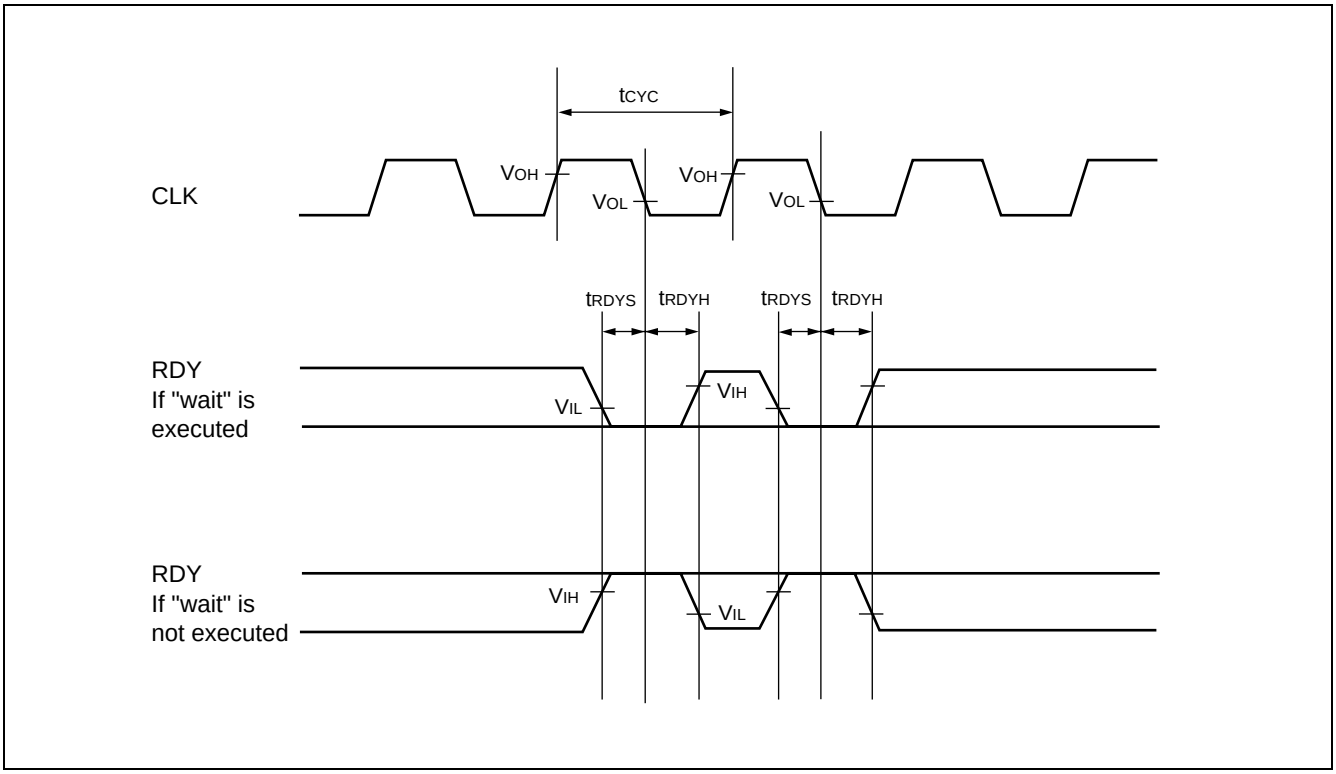
- Calculation formula : $(2 - n / 2) \times t_{CYC} - 25$


tCYC
BA1
BA2
CLK
VOH
VOL
tCHAV
A24 - A00
tCLRL
tCLRH
RD
tRLDV
tRHDX
tAVDV
tDSRH
D31 - D16
VIH
VIL
Read
tCLWL
tCLWH
WR0 - WR1
tCHDV
D31 - D16
Write

(7) Ready Input Timing

(MASK Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 2.7\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)
(FLASH Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 3.0\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
RDY setup time → CLK ↓	t_{RDYS}	RDY CLK	—	15	—	ns	
CLK ↓ → RDY holding time	t_{RDYH}	RDY CLK		0	—	ns	

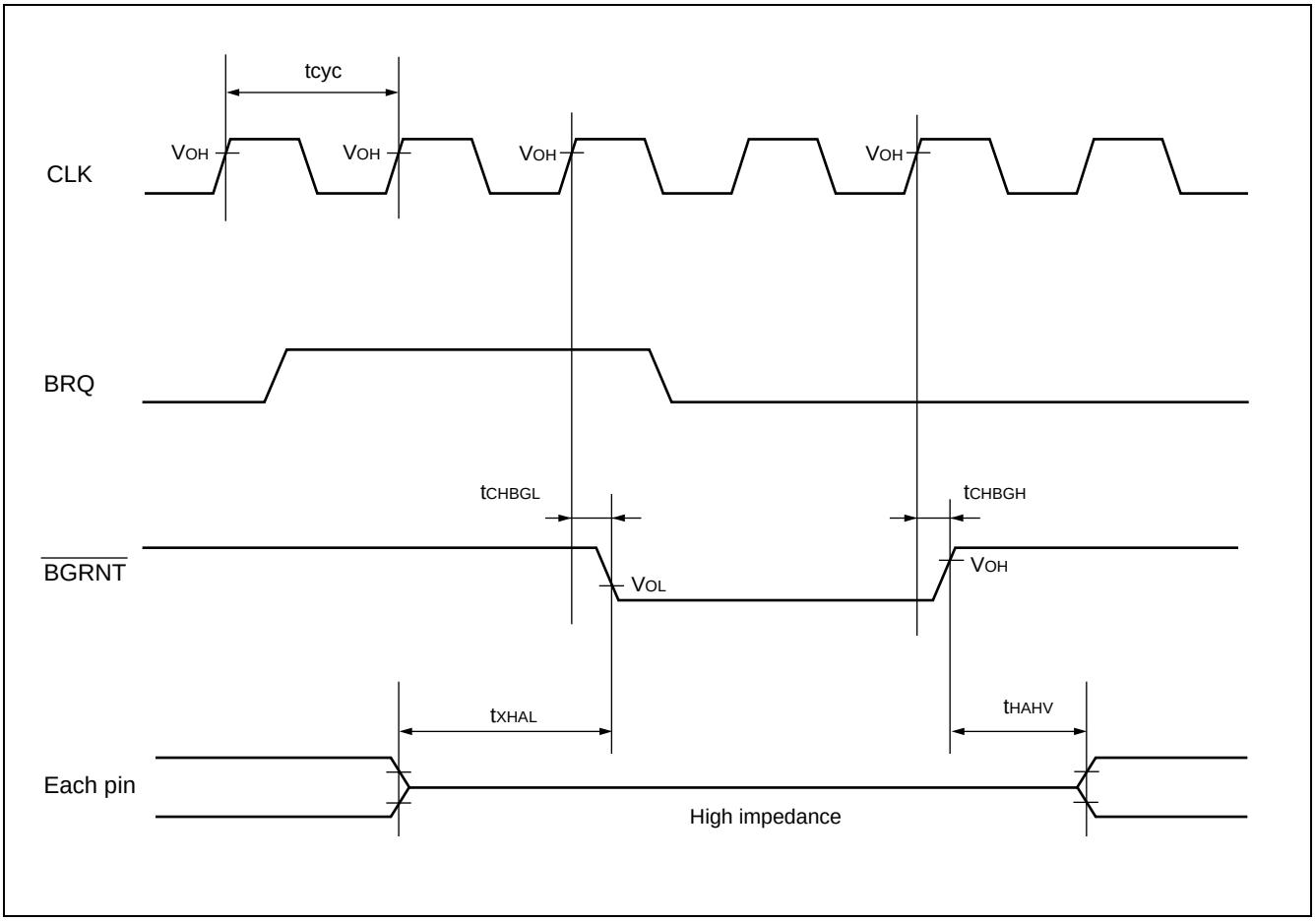


(8) Holding timing

(MASK Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 2.7\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)
(FLASH Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 3.0\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
$\overline{BGRNT}$ delay time	t_{CHBGL}	CLK $\overline{BGRNT}$	—	—	6	ns	
$\overline{BGRNT}$ delay time	t_{CHBGH}			—	6	ns	
Pin floating → $\overline{BGRNT}$ ↓ time	t_{XHAL}	$\overline{BGRNT}$		$t_{CYC} - 10$	$t_{CYC} + 10$	ns	
$\overline{BGRNT}$ ↑ → Pin valid time	t_{HAHV}			$t_{CYC} - 10$	$t_{CYC} + 10$	ns	

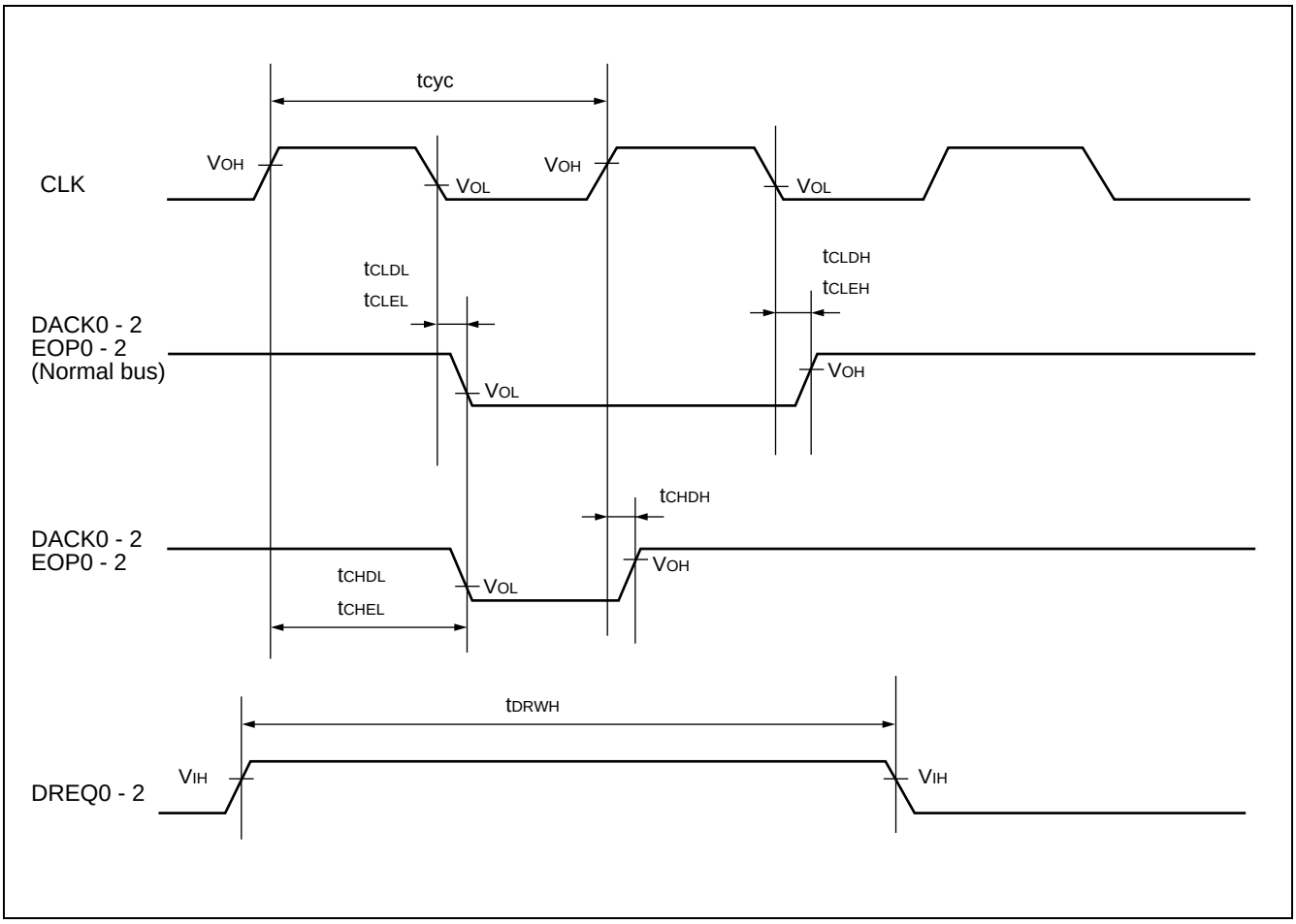
Note : It takes at least one cycle from loading the BRQ to when $\overline{BGRNT}$ is changed.



(9) DMA Controller Timing

(MASK Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 2.7\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)
(FLASH Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 3.0\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min.	Max.		
DREQ input pulse width	t_{DRWH}	DREQ0 to DREQ2	—	2 t_{CYC}	—	ns	
DACK delay time (Normal bus)	t_{CLDL}	CLK DACK0 to DACK2		—	6	ns	
	t_{CLDH}			—	6	ns	
EOP delay time (Normal bus)	t_{CLEL}	CLK EOP0 to EOP2		—	6	ns	
	t_{CLEH}			—	6	ns	
DACK delay time	t_{CHDL}	CLK DACK0 to DACK2		—	n / 2 × t_{CYC}	ns	
	t_{CHDH}			—	6	ns	
EOP delay time	t_{CHEL}	CLK EOP0 to EOP2		—	n / 2 × t_{CYC}	ns	
	t_{CHEH}			—	6	ns	



5. A/D Transition

(MASK Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 2.7\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)
(FLASH Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 3.0\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)

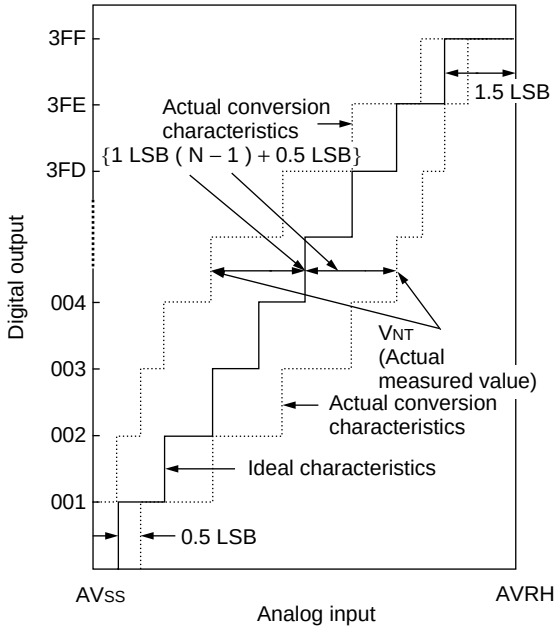
Parameter		Symbol	Pin name	Conditions	Value			Unit	Remarks
					Min.	Typ.	Max.		
Resolution		—	—	—	—	—	10	Bit	
Conversion time		—	—		5.0	—		µs	
Total tolerance		—	—	$AV_{CC} = 5.0\ V$, $AV_{RH} = 5.0\ V$	–4.0	—	4.0	LSB	
Straight-line tolerance		—	—		–3.5	—	3.5	LSB	
Differential straight-line tolerance		—	—		–2.0	—	2.0	LSB	
Zero transition tolerance		V_{OT}	AN0 to AN7	$AV_{CC} = 5.0\ V$, $AV_{RH} = 5.0\ V$	AV_{SS}–1.5	AV_{SS}+0.5	AV_{SS}+2.5	LSB	
Full-scale transition tolerance		V_{FST}	AN0 to AN7		$AV_{RH} - 5.5$	$AV_{RH} - 1.5$	$AV_{RH} + 0.5$	LSB	
Analog input current		I_{AIN}	AN0 to AN7	—	—	0.1	10	µA	
Analog input voltage		V_{AIN}	AN0 to AN7		AV_{SS}	—	AV_{RH}	V	
Standard voltage		AV_{RH}	AV_{RH}	—	—	—	AV_{CC}	V	
Power current	When conversion is activated	I_A	AV_{CC}	$AV_{CC} = 5.0\ V$	—	3.0	5.0	mA	
	When conversion is stopped	I_{AH}			—	—	5.0	µA	
Standard voltage current supplied	When conversion is activated	I_R	AV_{RH}	$AV_{CC} = 5.0\ V$, $AV_{RH} = 5.0V$	—	2.0	3.0	mA	
	When conversion is stopped	I_{RH}			—	—	10	µA	
Tolerance between channels		—	AN0 to AN7	—	—	—	4	LSB	

Notes : • As the $|AV_{RH}|$ becomes smaller, the tolerance becomes larger.

- Output impedance of external circuits other than analog input must be used if output impedance of external circuits < approx. 7 kΩ
  If the output impedance of the external circuits is too high, the sampling time for the analog voltage may be insufficient.
  (Sampling time = 1.6 µs at 33 MHz)

- **Definition of A/D Converter Terms**
- Resolution :
  Analog changes that can be identified by A/D converter
- Straight-line tolerance :
  Difference between the straight line linking the zero transition point (00 0000 0000 ←→ 00 0000 0001) to the full-scale transition point (11 1111 1110 ←→ 11 1111 1111) and actual conversion characteristics.
- Differential straight-line tolerance :
  Difference compared to the ideal input voltage value required to change the output code 1 LSB
- Total tolerance :
  Indicates the difference between the actual and theoretical values and includes zero transition tolerance, full-scale transition tolerance, and straight-line tolerance.

Total tolerance



$$\text{Total tolerance of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB'}\}}{1\ \text{LSB}}$$

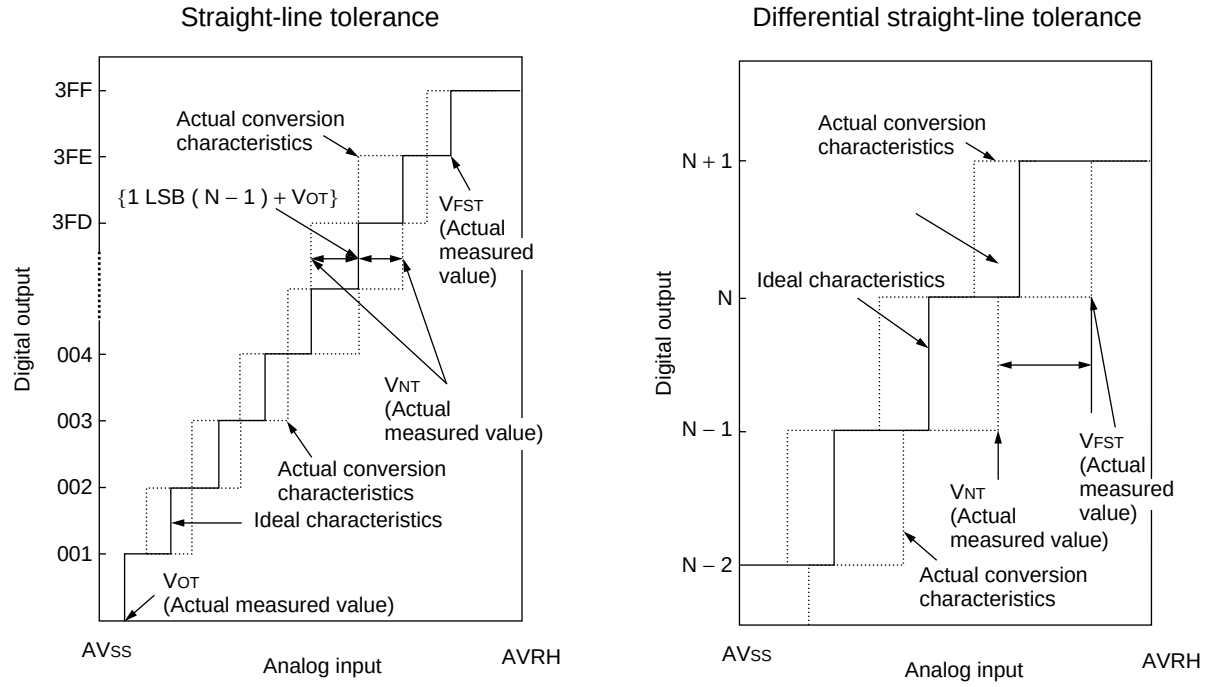
$$1\ \text{LSB (Ideal value)} = \frac{AVRH - AV_{SS}}{1024}\ [V]$$

V_{OT} (Ideal value) $= AV_{SS} + 0.5$ LSB' [V]

V_{FST} (Ideal value) $=$ AVRH $- 1.5$ LSB' [V] V_{NT} : Voltage of digital output transferred from (N + 1) to N

(Continued)

(Continued)



$$\text{Straight-line tolerance of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential straight-line tolerance of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ [\text{LSB}]$$

$$1\text{LSB (Ideal value)} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT} : Voltage with digital output transferred from $(000)_H$ to $(001)_H$

V_{FST} : Voltage with digital output transferred from $(3FE)_H$ to $(3FF)_H$

6. D/A Transition

(MASK Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 2.7\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)
(FLASH Model $V_{CC}5 = AV_{CC} = DAVC = 5.0\ V \pm 10\%$, $V_{CC}3 = 3.0\ V$ to $3.6\ V$, $V_{SS} = AV_{SS} = 0\ V$, $T_A = -40\ °C$ to $+70\ °C$)

Parameter	Symbol	Pin name	Condi-tions	Value			Unit	Re-marks
				Min.	Typ.	Max.		
Resolution	—	—	—	—	—	8	Bit	
Differential straight-line tolerance	—	—	—	—	—	±0.9	LSB	
Conversion time	—	—	—	—	10	20	µs	*
Analog output impedance	—	—	—	—	28	—	kΩ	

*: CL = 20 PF

■ INSTRUCTIONS (165 INSTRUCTIONS)

1. How to Read Instruction Set Summary

Mnemonic	Type	OP	CYC	NZVC	Operation	Remarks
ADD Rj, Ri	A	A6	1	CCCC	Ri + Rj → Ri	
* ADD #s5, Ri	C	A4	1	CCCC	Ri + s5 → Ri	
,	,	,	,	,	,	
,	,	,	,	,	,	
↓ (1) ↓ (2)	↓ (3)	↓ (4)	↓ (5)	↓ (6)	↓ (7)	

(1) Names of instructions
Instructions marked with * are not included in CPU specifications. These are extended instruction codes added/extended at assembly language levels.

(2) Addressing modes specified as operands are listed in symbols.
Refer to “2. Addressing mode symbols” for further information.

(3) Instruction types

(4) Hexa-decimal expressions of instructions

(5) The number of machine cycles needed for execution

a: Memory access cycle and it has possibility of delay by Ready function.

b: Memory access cycle and it has possibility of delay by Ready function.
If an object register in a LD operation is referenced by an immediately following instruction, the interlock function is activated and number of cycles needed for execution increases.

c: If an immediately following instruction operates to an object of R15, SSP or USP in read/write mode or if the instruction belongs to instruction format A group, the interlock function is activated and number of cycles needed for execution increases by 1 to make the total number of 2 cycles needed.

d: If an immediately following instruction refers to MDH/MDL, the interlock function is activated and number of cycles needed for execution increases by 1 to make the total number of 2 cycles needed.

For a, b, c and d, minimum execution cycle is 1.

(6) Change in flag sign

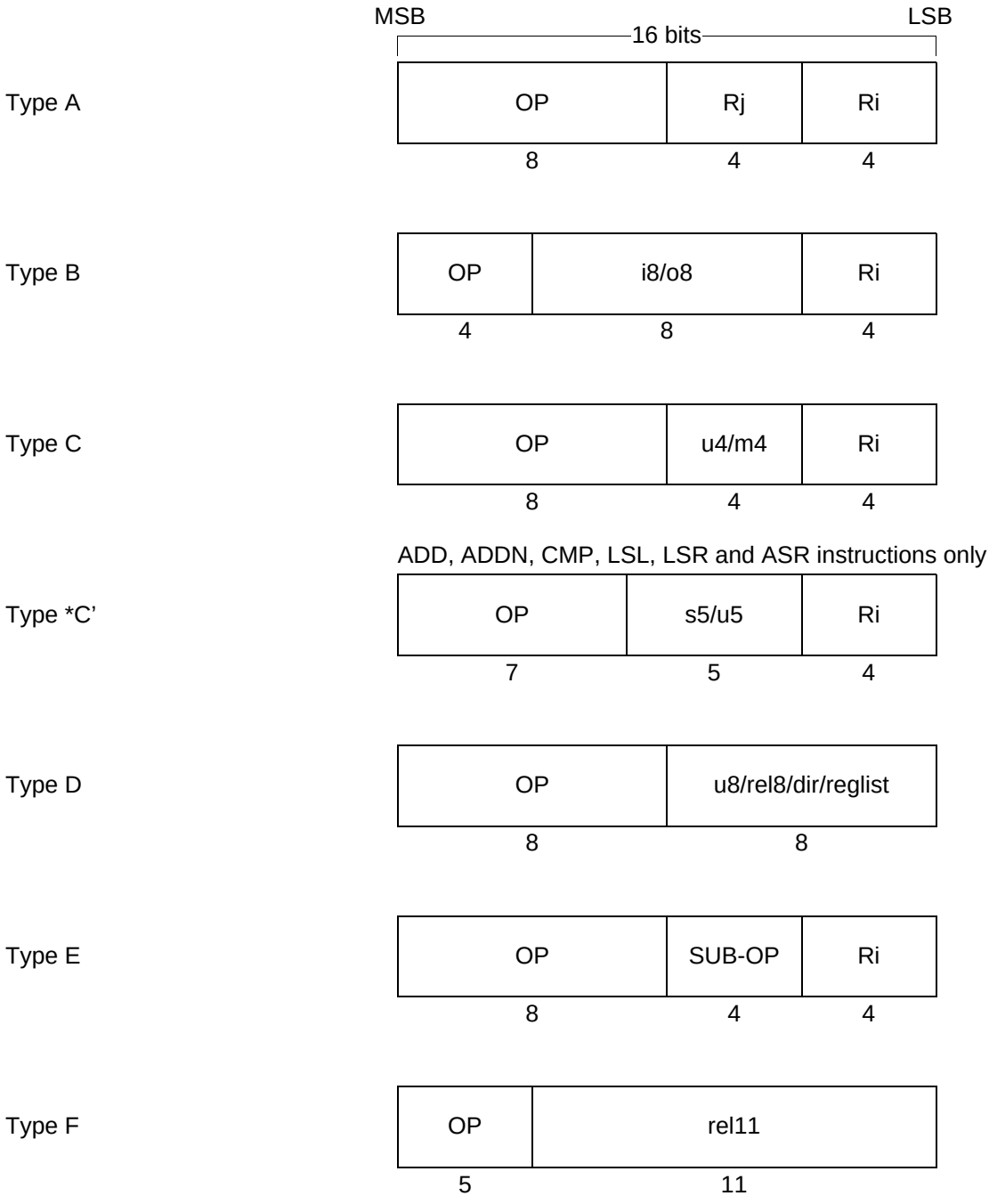
- Flag change
  C : Change
  – : No change
  0 : Clear
  1 : Set
- Flag meanings
  N : Negative flag
  Z : Zero flag
  V : Over flag
  C : Carry flag

(7) Operation carried out by instruction

2. Addressing Mode Symbols

Ri	: Register direct (R0 to R15, AC, FP, SP)
Rj	: Register direct (R0 to R15, AC, FP, SP)
R13	: Register direct (R13, AC)
Ps	: Register direct (Program status register)
Rs	: Register direct (TBR, RP, SSP, USP, MDH, MDL)
CRi	: Register direct (CR0 to CR15)
CRj	: Register direct (CR0 to CR15)
#i8	: Unsigned 8-bit immediate (–128 to 255) Note: –128 to –1 are interpreted as 128 to 255
#i20	: Unsigned 20-bit immediate (–0X80000 to 0XFFFFF) Note: –0X7FFFF to –1 are interpreted as 0X7FFFF to 0XFFFFF
#i32	: Unsigned 32-bit immediate (–0X80000000 to 0XFFFFFFFF) Note: –0X80000000 to –1 are interpreted as 0X80000000 to 0XFFFFFFFF
#s5	: Signed 5-bit immediate (–16 to 15)
#s10	: Signed 10-bit immediate (–512 to 508, multiple of 4 only)
#u4	: Unsigned 4-bit immediate (0 to 15)
#u5	: Unsigned 5-bit immediate (0 to 31)
#u8	: Unsigned 8-bit immediate (0 to 255)
#u10	: Unsigned 10-bit immediate (0 to 1020, multiple of 4 only)
@dir8	: Unsigned 8-bit direct address (0 to 0XFF)
@dir9	: Unsigned 9-bit direct address (0 to 0X1FE, multiple of 2 only)
@dir10	: Unsigned 10-bit direct address (0 to 0X3FC, multiple of 4 only)
label9	: Signed 9-bit branch address (–0X100 to 0XFC, multiple of 2 only)
label12	: Signed 12-bit branch address (–0X800 to 0X7FC, multiple of 2 only)
label20	: Signed 20-bit branch address (–0X80000 to 0X7FFFF)
label32	: Signed 32-bit branch address (–0X80000000 to 0X7FFFFFFF)
@Ri	: Register indirect (R0 to R15, AC, FP, SP)
@Rj	: Register indirect (R0 to R15, AC, FP, SP)
@(R13, Rj)	: Register relative indirect (Rj: R0 to R15, AC, FP, SP)
@(R14, disp10)	: Register relative indirect (disp10: –0X200 to 0X1FC, multiple of 4 only)
@(R14, disp9)	: Register relative indirect (disp9: –0X100 to 0XFE, multiple of 2 only)
@(R14, disp8)	: Register relative indirect (disp8: –0X80 to 0X7F)
@(R15, udisp6)	: Register relative (udisp6: 0 to 60, multiple of 4 only)
@Ri+	: Register indirect with post-increment (R0 to R15, AC, FP, SP)
@R13+	: Register indirect with post-increment (R13, AC)
@SP+	: Stack pop
@–SP	: Stack push
(reglist)	: Register list

3. Instruction Types



4. Detailed Description of Instructions

- **Add/subtract operation instructions (10 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
ADD	Rj, Ri	A	A6	1	C C C C	Ri + Rj → Ri	
* ADD	#s5, Ri	C'	A4	1	C C C C	Ri + s5 → Ri	MSB is interpreted as a sign in assembly language
ADD	#i4, Ri	C	A4	1	C C C C	Ri + extu (i4) → Ri	Zero-extension
ADD2	#i4, Ri	C	A5	1	C C C C	Ri + extu (i4) → Ri	Sign-extension
ADDC	Rj, Ri	A	A7	1	C C C C	Ri + Rj + c → Ri	Add operation with sign
ADDN	Rj, Ri	A	A2	1	– – – –	Ri + Rj → Ri	
* ADDN	#s5, Ri	C'	A0	1	– – – –	Ri + s5 → Ri	MSB is interpreted as a sign in assembly language
ADDN	#i4, Ri	C	A0	1	– – – –	Ri + extu (i4) → Ri	Zero-extension
ADDN2	#i4, Ri	C	A1	1	– – – –	Ri + extu (i4) → Ri	Sign-extension
SUB	Rj, Ri	A	AC	1	C C C C	Ri – Rj → Ri	
SUBC	Rj, Ri	A	AD	1	C C C C	Ri – Rj – c → Ri	Subtract operation with carry
SUBN	Rj, Ri	A	AE	1	– – – –	Ri – Rj → Ri	

- **Compare operation instructions (3 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
CMP	Rj, Ri	A	AA	1	C C C C	Ri – Rj	
* CMP	#s5, Ri	C'	A8	1	C C C C	Ri – s5	MSB is interpreted as a sign in assembly language
CMP	#i4, Ri	C	A8	1	C C C C	Ri + extu (i4)	Zero-extension
CMP2	#i4, Ri	C	A9	1	C C C C	Ri + extu (i4)	Sign-extension

- **Logical operation instructions (12 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
AND	Rj, Ri	A	82	1	C C – –	Ri & = Rj	Word
AND	Rj, @Ri	A	84	1 + 2a	C C – –	(Ri) & = Rj	Word
ANDH	Rj, @Ri	A	85	1 + 2a	C C – –	(Ri) & = Rj	Half word
ANDB	Rj, @Ri	A	86	1 + 2a	C C – –	(Ri) & = Rj	Byte
OR	Rj, Ri	A	92	1	C C – –	Ri | = Rj	Word
OR	Rj, @Ri	A	94	1 + 2a	C C – –	(Ri) | = Rj	Word
ORH	Rj, @Ri	A	95	1 + 2a	C C – –	(Ri) | = Rj	Half word
ORB	Rj, @Ri	A	96	1 + 2a	C C – –	(Ri) | = Rj	Byte
EOR	Rj, Ri	A	9A	1	C C – –	Ri ^ = Rj	Word
EOR	Rj, @Ri	A	9C	1 + 2a	C C – –	(Ri) ^ = Rj	Word
EORH	Rj, @Ri	A	9D	1 + 2a	C C – –	(Ri) ^ = Rj	Half word
EORB	Rj, @Ri	A	9E	1 + 2a	C C – –	(Ri) ^ = Rj	Byte

- **Bit manipulation arithmetic instructions (8 instructions)**

Mnemonic			Type	OP	Cycle	N Z V C	Operation	Remarks
BANDL	#u4, @Ri (u4: 0 to 0F$_H$)		C	80	1 + 2a	– – – –	(Ri) & = (F0$_H$ + u4)	Manipulate lower 4 bits
BANDH	#u4, @Ri (u4: 0 to 0F$_H$)		C	81	1 + 2a	– – – –	(Ri) & = ((u4<<4) + 0F$_H$)	Manipulate upper 4 bits
* BAND	#u8, @Ri	*1			–	– – – –	(Ri) & = u8	
BORL	#u4, @Ri (u4: 0 to 0F$_H$)		C	90	1 + 2a	– – – –	(Ri) | = u4	Manipulate lower 4 bits
BORH	#u4, @Ri (u4: 0 to 0F$_H$)		C	91	1 + 2a	– – – –	(Ri) | = (u4<<4)	Manipulate upper 4 bits
* BOR	#u8, @Ri	*2			–	– – – –	(Ri) | = u8	
BEORL	#u4, @Ri (u4: 0 to 0F$_H$)		C	98	1 + 2a	– – – –	(Ri) ^ = u4	Manipulate lower 4 bits
BEORH	#u4, @Ri (u4: 0 to 0F$_H$)		C	99	1 + 2a	– – – –	(Ri) ^ = (u4<<4)	Manipulate upper 4 bits
* BEOR	#u8, @Ri	*3			–	– – – –	(Ri) ^ = u8	
BTSTL	#u4, @Ri (u4: 0 to 0F$_H$)		C	88	2 + a	0 C – –	(Ri) & u4	Test lower 4 bits
BTSTH	#u4, @Ri (u4: 0 to 0F$_H$)		C	89	2 + a	C C – –	(Ri) & (u4<<4)	Test upper 4 bits

*1: Assembler generates BANDL if result of logical operation “u8&0x0F” leaves an active (set) bit and generates BANDH if “u8&0xF0” leaves an active bit. Depending on the value in the “u8” format, both BANDL and BANDH may be generated.
*2: Assembler generates BORL if result of logical operation “u8&0x0F” leaves an active (set) bit and generates BORH if “u8&0xF0” leaves an active bit.
*3: Assembler generates BEORL if result of logical operation “u8&0x0F” leaves an active (set) bit and generates BEORH if “u8&0xF0” leaves an active bit.

- **Add/subtract operation instructions (10 instructions)**

Mnemonic			Type	OP	Cycle	N Z V C	Operation	Remarks
MUL	Rj, Ri		A	AF	5	C C C –	Rj × Ri → MDH, MDL	32-bit × 32-bit = 64-bit
MULU	Rj, Ri		A	AB	5	C C C –	Rj × Ri → MDH, MDL	Unsigned
MULH	Rj, Ri		A	BF	3	C C – –	Rj × Ri → MDL	16-bit × 16-bit = 32-bit
MULUH	Rj, Ri		A	BB	3	C C – –	Rj × Ri → MDL	Unsigned
DIVOS	Ri		E	97 – 4	1	– – – –		Step calculation
DIVOU	Ri		E	97 – 5	1	– – – –		32-bit/32-bit = 32-bit
DIV1	Ri		E	97 – 6	d	– C – C		
DIV2	Ri		E	97 – 7	1	– C – C		
DIV3			E	9F – 6	1	– – – –		
DIV4S			E	9F – 7	1	– – – –		
* DIV	Ri	*1			–	– C – C	MDL/Ri → MDL, MDL%Ri → MDH	
* DIVU	Ri	*2			–	– C – C	MDL/Ri → MDL, MDL%Ri → MDH	Unsigned

*1: DIVOS, DIV1 × 32, DIV2, DIV3 and DIV4S are generated. A total instruction code length of 72 bytes.
*2: DIVOU and DIV1 × 32 are generated. A total instruction code length of 66 bytes.

- **Shift arithmetic instructions (9 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
LSL	Rj, Ri	A	B6	1	C C – C	Ri<<Rj → Ri	Logical shift
* LSL	#u5, Ri	C'	B4	1	C C – C	Ri<<u5 → Ri	
LSL	#u4, Ri	C	B4	1	C C – C	Ri<<u4 → Ri	
LSL2	#u4, Ri	C	B5	1	C C – C	Ri<<(u4 + 16) → Ri	
LSR	Rj, Ri	A	B2	1	C C – C	Ri>>Rj → Ri	Logical shift
* LSR	#u5, Ri	C'	B0	1	C C – C	Ri>>u5 → Ri	
LSR	#u4, Ri	C	B0	1	C C – C	Ri>>u4 → Ri	
LSR2	#u4, Ri	C	B1	1	C C – C	Ri>>(u4 + 16) → Ri	
ASR	Rj, Ri	A	BA	1	C C – C	Ri>>Rj → Ri	Logical shift
* ASR	#u5, Ri	C'	B8	1	C C – C	Ri>>u5 → Ri	
ASR	#u4, Ri	C	B8	1	C C – C	Ri>>u4 → Ri	
ASR2	#u4, Ri	C	B9	1	C C – C	Ri>>(u4 + 16) → Ri	

- **Immediate value data transfer instruction (immediate value set/16-bit/32-bit immediate value transfer instruction) (3 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
LDI: 32	#i32, Ri	E	9F – 8	3	– – – –	i32 → Ri	
LDI: 20	#i20, Ri	C	9B	2	– – – –	i20 → Ri	Upper 12 bits are zero-extended
LDI: 8	#i8, Ri	B	C0	1	– – – –	i8 → Ri	Upper 24 bits are zero-extended
* LDI	# {i8 | i20 | i32}, Ri *1					{i8 | i20 | i32} → Ri	

*1: If an immediate value is given in absolute, assembler automatically makes i8, i20 or i32 selection.
If an immediate value contains relative value or external reference, assembler selects i32.

- **Memory load instructions (13 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
LD	@Rj, Ri	A	04	b	– – – –	(Rj) → Ri	
LD	@(R13, Rj), Ri	A	00	b	– – – –	(R13 + Rj) → Ri	
LD	@(R14, disp10), Ri	B	20	b	– – – –	(R14 + disp10) → Ri	
LD	@(R15, udisp6), Ri	C	03	b	– – – –	(R15 + udisp6) → Ri	
LD	@R15 +, Ri	E	07 – 0	b	– – – –	(R15) → Ri, R15 + = 4	
LD	@R15 +, Rs	E	07 – 8	b	– – – –	(R15) → Rs, R15 + = 4	Rs: Special-purpose register
LD	@R15 +, PS	E	07 – 9	1 + a + b	C C C C	(R15) → PS, R15 + = 4	
LDUH	@Rj, Ri	A	05	b	– – – –	(Rj) → Ri	Zero-extension
LDUH	@(R13, Rj), Ri	A	01	b	– – – –	(R13 + Rj) → Ri	Zero-extension
LDUH	@(R14, disp9), Ri	B	40	b	– – – –	(R14 + disp9) → Ri	Zero-extension
LDUB	@Rj, Ri	A	06	b	– – – –	(Rj) → Ri	Zero-extension
LDUB	@(R13, Rj), Ri	A	02	b	– – – –	(R13 + Rj) → Ri	Zero-extension
LDUB	@(R14, disp8), Ri	B	60	b	– – – –	(R14 + disp8) → Ri	Zero-extension

Note: The relations between o8 field of TYPE-B and u4 field of TYPE-C in the instruction format and assembler description from disp8 to disp10 are as follows:
disp8 → o8 = disp8:Each disp is a code extension.
disp9 → o8 = disp9>>1:Each disp is a code extension.
disp10 → o8 = disp10>>2:Each disp is a code extension.
udisp6 → u4 = udisp6>>2:udisp4 is a 0 extension.

- **Memory store instructions (13 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
ST	Ri, @Rj	A	14	a	– – – –	Ri → (Rj)	Word
ST	Ri, @(R13, Rj)	A	10	a	– – – –	Ri → (R13 + Rj)	Word
ST	Ri, @(R14, disp10)	B	30	a	– – – –	Ri → (R14 + disp10)	Word
ST	Ri, @(R15, udisp6)	C	13	a	– – – –	Ri → (R15 + usidp6)	
ST	Ri, @–R15	E	17 – 0	a	– – – –	R15 – = 4, Ri → (R15)	
ST	Rs, @–R15	E	17 – 8	a	– – – –	R15 – = 4, Rs → (R15)	Rs: Special-purpose register
ST	PS, @–R15	E	17 – 9	a	– – – –	R15 – = 4, PS → (R15)	
STH	Ri, @Rj	A	15	a	– – – –	Ri → (Rj)	Half word
STH	Ri, @(R13, Rj)	A	11	a	– – – –	Ri → (R13 + Rj)	Half word
STH	Ri, @(R14, disp9)	B	50	a	– – – –	Ri → (R14 + disp9)	Half word
STB	Ri, @Rj	A	16	a	– – – –	Ri → (Rj)	Byte
STB	Ri, @(R13, Rj)	A	12	a	– – – –	Ri → (R13 + Rj)	Byte
STB	Ri, @(R14, disp8)	B	70	a	– – – –	Ri → (R14 + disp8)	Byte

Note: The relations between o8 field of TYPE-B and u4 field of TYPE-C in the instruction format and assembler description from disp8 to disp10 are as follows:
disp8 → o8 = disp8:Each disp is a code extension.
disp9 → o8 = disp9>>1:Each disp is a code extension.
disp10 → o8 = disp10>>2:Each disp is a code extension.
udisp6 → u4 = udisp6>>2:udisp4 is a 0 extension.

- **Transfer instructions between registers/special-purpose registers transfer instructions (5 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
MOV	Rj, Ri	A	8B	1	– – – –	Rj → Ri	Transfer between general-purpose registers
MOV	Rs, Ri	A	B7	1	– – – –	Rs → Ri	Rs: Special-purpose register
MOV	Ri, Rs	A	B3	1	– – – –	Ri → Rs	Rs: Special-purpose register
MOV	PS, Ri	E	17 – 1	1	– – – –	PS → Ri	
MOV	Ri, PS	E	07 – 1	c	C C C C	Ri → PS	

- **Non-delay normal branch instructions (23 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
JMP	@Ri	E	97 – 0	2	– – – –	Ri → PC	
CALL	label12	F	D0	2	– – – –	PC + 2 → RP, PC + 2 + rel11 × 2 → PC	
CALL	@Ri	E	97 – 1	2	– – – –	PC + 2 → RP, Ri → PC	
RET		E	97 – 2	2	– – – –	RP → PC	Return
INT	#u8	D	1F	3+3a	– – – –	SSP – = 4, PS → (SSP), SSP – = 4, PC + 2 → (SSP), 0 → I flag, 0 → S flag, (TBR + 3FC – u8 × 4) → PC	
INTE		E	9F – 3	3 + 3a	– – – –	SSP – = 4, PS → (SSP), SSP – = 4, PC + 2 → (SSP), 0 → S flag, (TBR + 3D8 – u8 × 4) → PC	For emulator
RETI		E	97 – 3	2 + 2a	C C C C	(R15) → PC, R15 – = 4, (R15) → PS, R15 – = 4	
BNO	label9	D	E1	1	– – – –	Non-branch	
BRA	label9	D	E0	2	– – – –	PC + 2 + rel8 × 2 → PC	
BEQ	label9	D	E2	2/1	– – – –	PCif Z = = 1	
BNE	label9	D	E3	2/1	– – – –	PCif Z = = 0	
BC	label9	D	E4	2/1	– – – –	PCif C = = 1	
BNC	label9	D	E5	2/1	– – – –	PCif C = = 0	
BN	label9	D	E6	2/1	– – – –	PCif N = = 1	
BP	label9	D	E7	2/1	– – – –	PCif N = = 0	
BV	label9	D	E8	2/1	– – – –	PCif V = = 1	
BNV	label9	D	E9	2/1	– – – –	PCif V = = 0	
BLT	label9	D	EA	2/1	– – – –	PCif V xor N = = 1	
BGE	label9	D	EB	2/1	– – – –	PCif V xor N = = 0	
BLE	label9	D	EC	2/1	– – – –	PCif (V xor N) or Z = = 1	
BGT	label9	D	ED	2/1	– – – –	PCif (V xor N) or Z = = 0	
BLS	label9	D	EE	2/1	– – – –	PCif C or Z = = 1	
BHI	label9	D	EF	2/1	– – – –	PCif C or Z = = 0	

Notes:
- "2/1" in cycle sections indicates that 2 cycles are needed for branch and 1 cycle needed for non-branch.
- The relations between rel8 field of TYPE-D and rel11 field of TYPE-F in the instruction format and assembler discription label9 and label12 are as follows.
  label9 → rel8 = (label9 – PC – 2)/2
  label12 → rel11 = (label12 – PC – 2)/2
- RETI must be operated while S flag = 0.

- **Branch instructions with delays (20 instructions)**

Mnemonic		Type	OP	Cycle	N Z V C	Operation	Remarks
JMP:D	@Ri	E	9F – 0	1	– – – –	Ri → PC	
CALL:D	label12	F	D8	1	– – – –	PC + 4 → RP, PC + 2 + rel11 × 2 → PC	
CALL:D	@Ri	E	9F – 1	1	– – – –	PC + 4 → RP, Ri → PC	
RET:D		E	9F – 2	1	– – – –	RP → PC	Return
BNO:D	label9	D	F1	1	– – – –	Non-branch	
BRA:D	label9	D	F0	1	– – – –	PC + 2 + rel8 × 2 → PC	
BEQ:D	label9	D	F2	1	– – – –	PCif Z = = 1	
BNE:D	label9	D	F3	1	– – – –	PCif Z = = 0	
BC:D	label9	D	F4	1	– – – –	PCif C = = 1	
BNC:D	label9	D	F5	1	– – – –	PCif C = = 0	
BN:D	label9	D	F6	1	– – – –	PCif N = = 1	
BP:D	label9	D	F7	1	– – – –	PCif N = = 0	
BV:D	label9	D	F8	1	– – – –	PCif V = = 1	
BNV:D	label9	D	F9	1	– – – –	PCif V = = 0	
BLT:D	label9	D	FA	1	– – – –	PCif V xor N = = 1	
BGE:D	label9	D	FB	1	– – – –	PCif V xor N = = 0	
BLE:D	label9	D	FC	1	– – – –	PCif (V xor N) or Z = = 1	
BGT:D	label9	D	FD	1	– – – –	PCif (V xor N) or Z = = 0	
BLS:D	label9	D	FE	1	– – – –	PCif C or Z = = 1	
BHI:D	label9	D	FF	1	– – – –	PCif C or Z = = 0	

Notes:
- The relations between rel8 field of TYPE-D and rel11 field of TYPE-F in the instruction format and assembler discription label9 and label12 are as follows.
  label9 → rel8 = (label9 – PC – 2)/2
  label12 → rel11 = (label12 – PC – 2)/2
- Delayed branch operation always executes next instruction (delay slot) before making a branch.
- Instructions allowed to be stored in the delay slot must meet one of the following conditions. If the other instruction is stored, this device may operate other operation than defined.
  The instruction described “1” in the other cycle column than branch instruction.
  The instruction described “a”, “b”, “c” or “d” in the cycle column.

- **Direct addressing instructions**

Mnemonic	Type	OP	Cycle	N Z V C	Operation	Remarks
DMOV @dir10, R13	D	08	b	– – – –	(dir10) → R13	Word
DMOV R13, @dir10	D	18	a	– – – –	R13 → (dir10)	Word
DMOV @dir10, @R13+	D	0C	2a	– – – –	(dir10) → (R13), R13 + = 4	Word
DMOV @R13+, @dir10	D	1C	2a	– – – –	(R13) → (dir10), R13 + = 4	Word
DMOV @dir10, @–R15	D	0B	2a	– – – –	R15 – = 4, (dir10) → (R15)	Word
DMOV @R15+, @dir10	D	1B	2a	– – – –	(R15) → (dir10), R15 + = 4	Word
DMOVH @dir9, R13	D	09	b	– – – –	(dir9) → R13	Half word
DMOVH R13, @dir9	D	19	a	– – – –	R13 → (dir9)	Half word
DMOVH @dir9, @R13+	D	0D	2a	– – – –	(dir9) → (R13), R13 + = 2	Half word
DMOVH @R13+, @dir9	D	1D	2a	– – – –	(R13) → (dir9), R13 + = 2	Half word
DMOVB @dir8, R13	D	0A	b	– – – –	(dir8) → R13	Byte
DMOVB R13, @dir8	D	1A	a	– – – –	R13 → (dir8)	Byte
DMOVB @dir8, @R13+	D	0E	2a	– – – –	(dir8) → (R13), R13 + +	Byte
DMOVB @R13+, @dir8	D	1E	2a	– – – –	(R13) → (dir8), R13 + +	Byte

Note: The relations between the dir field of TYPE-D in the instruction format and the assembler description from disp8 to disp10 are as follows:
disp8 → dir + disp8:Each disp is a code extension
disp9 → dir = disp9>>1:Each disp is a code extension
disp10 → dir = disp10>>2:Each disp is a code extension

- **Resource instructions (2 instructions)**

Mnemonic	Type	OP	Cycle	N Z V C	Operation	Remarks
LDRES @Ri+, #u4	C	BC	a	– – – –	(Ri) → u4 resource Ri + = 4	u4: Channel number
STRES #u4, @Ri+	C	BD	a	– – – –	u4 resource → (Ri) Ri + = 4	u4: Channel number

- **Co-processor instructions (4 instructions)**

Mnemonic	Type	OP	Cycle	N Z V C	Operation	Remarks
COPOP #u4, #CC, CRj, CRi	E	9F – C	2 + a	– – – –	Calculation	
COPLD #u4, #CC, Rj, CRi	E	9F – D	1 + 2a	– – – –	Rj → CRi	
COPST #u4, #CC, CRj, Ri	E	9F – E	1 + 2a	– – – –	CRj → Ri	
COPSV #u4, #CC, CRj, Ri	E	9F – F	1 + 2a	– – – –	CRj → Ri	No error traps

- **Other instructions (16 instructions)**

Mnemonic			Type	OP	Cycle	N Z V C	Operation	Remarks
NOP			E	9F – A	1	– – – –	No changes	
ANDCCR ORCCR	#u8 #u8		D D	83 93	c c	C C C C C C C C	CCR and u8 → CCR CCR or u8 → CCR	
STILM	#u8		D	87	1	– – – –	i8 → ILM	Set ILM immediate value
ADDSP	#s10	*1	D	A3	1	– – – –	R15 + = s10	ADD SP instruction
EXTSB EXTUB EXTSH EXTUH	Ri Ri Ri Ri		E E E E	97 – 8 97 – 9 97 – A 97 – B	1 1 1 1	– – – – – – – – – – – – – – – –	Sign extension 8 → 32 bits Zero extension 8 → 32 bits Sign extension 16 → 32 bits Zero extension 16 → 32 bits	
LDM0	(reglist)		D	8C	*4	– – – –	(R15) → reglist, R15 increment	Load-multi R0 to R7
LDM1	(reglist)		D	8D	*4	– – – –	(R15) → reglist, R15 increment	Load-multi R8 to R15
* LDM	(reglist)	*3			–	– – – –	(R15 + +) → reglist,	Load-multi R0 to R15
STM0	(reglist)		D	8E	*6	– – – –	R15 decrement, reglist → (R15)	Store-multi R0 to R7
STM1	(reglist)		D	8F	*6	– – – –	R15 decrement, reglist → (R15)	Store-multi R8 to R15
* STM2	(reglist)	*5			–	– – – –	reglist → (R15 + +)	Store-multi R0 to R15
ENTER	#u10	*2	D	0F	1+a	– – – –	R14 → (R15 – 4), R15 – 4 → R14, R15 – u10 → R15	Entrance processing of function
LEAVE			E	9F – 9	b	– – – –	R14 + 4 → R15, (R15 – 4) → R14	Exit processing of function
XCHB	@Rj, Ri		A	8A	2a	– – – –	Ri → TEMP, (Rj) → Ri, TEMP → (Rj)	For SEMAFO management Byte data

*1: In the ADDSP instruction, the reference between u8 of TYPE-D in the instruction format and assembler description s10 is as follows.
s10 → s8 = s10>>2

*2: In the ENTER instruction, the reference between i8 of TYPE-C in the instruction format and assembler description u10 is as follows.
u10 → u8 = u10>>2

*3: If either of R0 to R7 is specified in reglist, assembler generates LDM0. If either of R8 to R15 is specified, assembler generates LDM1. Both LDM0 and LDM1 may be generated.

*4: The number of cycles needed for execution of LDM0 (reglist) and LDM1 (reglist) is given by the following calculation; $a \times (n - 1) + b + 1$ when “n” is number of registers specified.

*5: If either of R0 to R7 is specified in reglist, assembler generates STM0. If either of R8 to R15 is specified, assembler generates STM1. Both STM0 and STM1 may be generated.

*6: The number of cycles needed for execution of STM0 (reglist) and STM1 (reglist) is given by the following calculation; $a \times n + 1$ when “n” is number of registers specified.

- **20-bit normal branch macro instructions**

Mnemonic		Operation	Remarks
* CALL20	label20, Ri	Next instruction address → RP, label20 → PC	Ri: Temporary register *1
* BRA20	label20, Ri	label20 → PC	Ri: Temporary register *2
* BEQ20	label20, Ri	if (Z = = 1) then label20 → PC	Ri: Temporary register *3
* BNE20	label20, Ri	ifs/Z = = 0	Ri: Temporary register *3
* BC20	label20, Ri	ifs/C = = 1	Ri: Temporary register *3
* BNC20	label20, Ri	ifs/C = = 0	Ri: Temporary register *3
* BN20	label20, Ri	ifs/N = = 1	Ri: Temporary register *3
* BP20	label20, Ri	ifs/N = = 0	Ri: Temporary register *3
* BV20	label20, Ri	ifs/V = = 1	Ri: Temporary register *3
* BNV20	label20, Ri	ifs/V = = 0	Ri: Temporary register *3
* BLT20	label20, Ri	ifs/V xor N = = 1	Ri: Temporary register *3
* BGE20	label20, Ri	ifs/V xor N = = 0	Ri: Temporary register *3
* BLE20	label20, Ri	ifs/(V xor N) or Z = = 1	Ri: Temporary register *3
* BGT20	label20, Ri	ifs/(V xor N) or Z = = 0	Ri: Temporary register *3
* BLS20	label20, Ri	ifs/C or Z = = 1	Ri: Temporary register *3
* BHI20	label20, Ri	ifs/C or Z = = 0	Ri: Temporary register *3

*1: CALL20

(1) If label20 – PC – 2 is between –0x800 and +0x7fe, instruction is generated as follows;

```
CALL    label12
```

(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:20  #label20, Ri
CALL    @Ri
```

*2: BRA20

(1) If label20 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
BRA     label9
```

(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:20  #label20, Ri
JMP     @Ri
```

*3: Bcc20 (BEQ20 to BHI20)

(1) If label20 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
Bcc     label9
```

(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
  Bxcc    false         xcc is a revolt condition of cc
  LDI:20  #label20, Ri
  JMP     @Ri
false:
```

- **20-bit delayed branch macro instructions**

Mnemonic	Operation	Remarks
* CALL20:D label20, Ri	Next instruction address + 2 → RP, label20 → PC	Ri: Temporary register *1
* BRA20:D label20, Ri	label20 → PC	Ri: Temporary register *2
* BEQ20:D label20, Ri	if (Z = = 1) then label20 → PC	Ri: Temporary register *3
* BNE20:D label20, Ri	ifs/Z = = 0	Ri: Temporary register *3
* BC20:D label20, Ri	ifs/C = = 1	Ri: Temporary register *3
* BNC20:D label20, Ri	ifs/C = = 0	Ri: Temporary register *3
* BN20:D label20, Ri	ifs/N = = 1	Ri: Temporary register *3
* BP20:D label20, Ri	ifs/N = = 0	Ri: Temporary register *3
* BV20:D label20, Ri	ifs/V = = 1	Ri: Temporary register *3
* BNV20:D label20, Ri	ifs/V = = 0	Ri: Temporary register *3
* BLT20:D label20, Ri	ifs/V xor N = = 1	Ri: Temporary register *3
* BGE20:D label20, Ri	ifs/V xor N = = 0	Ri: Temporary register *3
* BLE20:D label20, Ri	ifs/(V xor N) or Z = = 1	Ri: Temporary register *3
* BGT20:D label20, Ri	ifs/(V xor N) or Z = = 0	Ri: Temporary register *3
* BLS20:D label20, Ri	ifs/C or Z = = 1	Ri: Temporary register *3
* BHI20:D label20, Ri	ifs/C or Z = = 0	Ri: Temporary register *3

*1: CALL20:D

(1) If label20 – PC – 2 is between –0x800 and +0x7fe, instruction is generated as follows;

```
CALL:D  label12
```

(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:20  #label20, Ri
CALL:D  @Ri
```

*2: BRA20:D

(1) If label20 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
BRA:D   label9
```

(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:20  #label20, Ri
JMP:D   @Ri
```

*3: Bcc20:D (BEQ20:D to BHI20:D)

(1) If label20 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
Bcc:D   label9
```

(2) If label20 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
  Bxcc    false       xcc is a revolt condition of cc
  LDI:20  #label20, Ri
  JMP:D   @Ri
false:
```

- **32-bit normal macro branch instructions**

Mnemonic		Operation	Remarks
* CALL32	label32, Ri	Next instruction address → RP, label32 → PC	Ri: Temporary register *1
* BRA32	label32, Ri	label32 → PC	Ri: Temporary register *2
* BEQ32	label32, Ri	if (Z = = 1) then label32 → PC	Ri: Temporary register *3
* BNE32	label32, Ri	ifs/Z = = 0	Ri: Temporary register *3
* BC32	label32, Ri	ifs/C = = 1	Ri: Temporary register *3
* BNC32	label32, Ri	ifs/C = = 0	Ri: Temporary register *3
* BN32	label32, Ri	ifs/N = = 1	Ri: Temporary register *3
* BP32	label32, Ri	ifs/N = = 0	Ri: Temporary register *3
* BV32	label32, Ri	ifs/V = = 1	Ri: Temporary register *3
* BNV32	label32, Ri	ifs/V = = 0	Ri: Temporary register *3
* BLT32	label32, Ri	ifs/V xor N = = 1	Ri: Temporary register *3
* BGE32	label32, Ri	ifs/V xor N = = 0	Ri: Temporary register *3
* BLE32	label32, Ri	ifs/(V xor N) or Z = = 1	Ri: Temporary register *3
* BGT32	label32, Ri	ifs/(V xor N) or Z = = 0	Ri: Temporary register *3
* BLS32	label32, Ri	ifs/C or Z = = 1	Ri: Temporary register *3
* BHI32	label32, Ri	ifs/C or Z = = 0	Ri: Temporary register *3

*1: CALL32

(1) If label32 – PC – 2 is between –0x800 and +0x7fe, instruction is generated as follows;

```
CALL    label12
```

(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:32  #label32, Ri
CALL    @Ri
```

*2: BRA32

(1) If label32 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
BRA     label9
```

(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:32  #label32, Ri
JMP     @Ri
```

*3: Bcc32 (BEQ32 to BHI32)

(1) If label32 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
Bcc     label9
```

(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
  Bxcc    false         xcc is a revolt condition of cc
  LDI:32  #label32, Ri
  JMP     @Ri
false:
```

- **32-bit delayed macro branch instructions**

Mnemonic	Operation	Remarks
* CALL32:D label32, Ri	Next instruction address + 2 → RP, label32 → PC	Ri: Temporary register *1
* BRA32:D label32, Ri	label32 → PC	Ri: Temporary register *2
* BEQ32:D label32, Ri	if (Z = = 1) then label32 → PC	Ri: Temporary register *3
* BNE32:D label32, Ri	ifs/Z = = 0	Ri: Temporary register *3
* BC32:D label32, Ri	ifs/C = = 1	Ri: Temporary register *3
* BNC32:D label32, Ri	ifs/C = = 0	Ri: Temporary register *3
* BN32:D label32, Ri	ifs/N = = 1	Ri: Temporary register *3
* BP32:D label32, Ri	ifs/N = = 0	Ri: Temporary register *3
* BV32:D label32, Ri	ifs/V = = 1	Ri: Temporary register *3
* BNV32:D label32, Ri	ifs/V = = 0	Ri: Temporary register *3
* BLT32:D label32, Ri	ifs/V xor N = = 1	Ri: Temporary register *3
* BGE32:D label32, Ri	ifs/V xor N = = 0	Ri: Temporary register *3
* BLE32:D label32, Ri	ifs/(V xor N) or Z = = 1	Ri: Temporary register *3
* BGT32:D label32, Ri	ifs/(V xor N) or Z = = 0	Ri: Temporary register *3
* BLS32:D label32, Ri	ifs/C or Z = = 1	Ri: Temporary register *3
* BHI32:D label32, Ri	ifs/C or Z = = 0	Ri: Temporary register *3

*1: CALL32:D

(1) If label32 – PC – 2 is between –0x800 and +0x7fe, instruction is generated as follows;

```
CALL:D  label12
```

(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:32  #label32, Ri
CALL:D  @Ri
```

*2: BRA32:D

(1) If label32 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
BRA:D   label9
```

(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
LDI:32  #label32, Ri
JMP:D   @Ri
```

*3: Bcc32:D (BEQ32:D to BHI32:D)

(1) If label32 – PC – 2 is between –0x100 and +0xfe, instruction is generated as follows;

```
Bcc:D   label9
```

(2) If label32 – PC – 2 is outside of the range given in (1) or includes external reference symbol, instruction is generated as follows;

```
  Bxcc    false       xcc is a revolt condition of cc
  LDI:32  #label32, Ri
  JMP:D   @Ri
false:
```

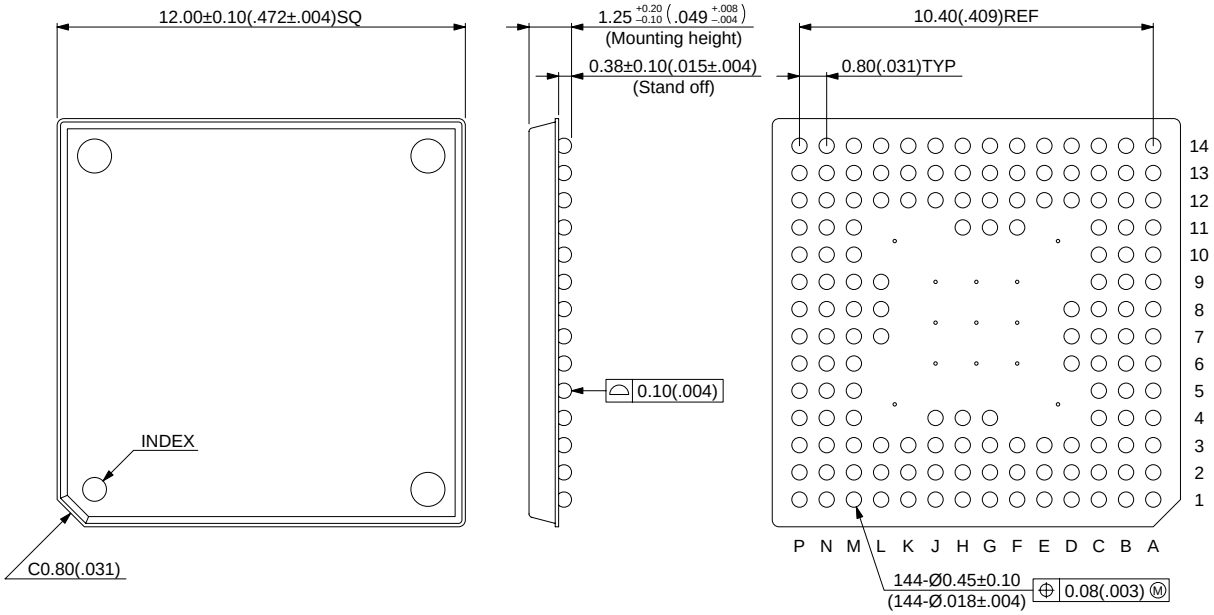
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91133PMT2-XXX	144-pin plastic LQFP (FPT-144P-M08)	
MB91133PBT-XXX	144-pin plastic FBGA (BGA-144P-M01)	
MB91F133PMT2	144-pin plastic LQFP (FPT-144P-M08)	
MB91F133PBT	144-pin plastic FBGA (BGA-144P-M01)	
MB91FV130CR-ES	299-pin ceramic PGA (PGA-299)	

■ PACKAGE DIMENSIONS

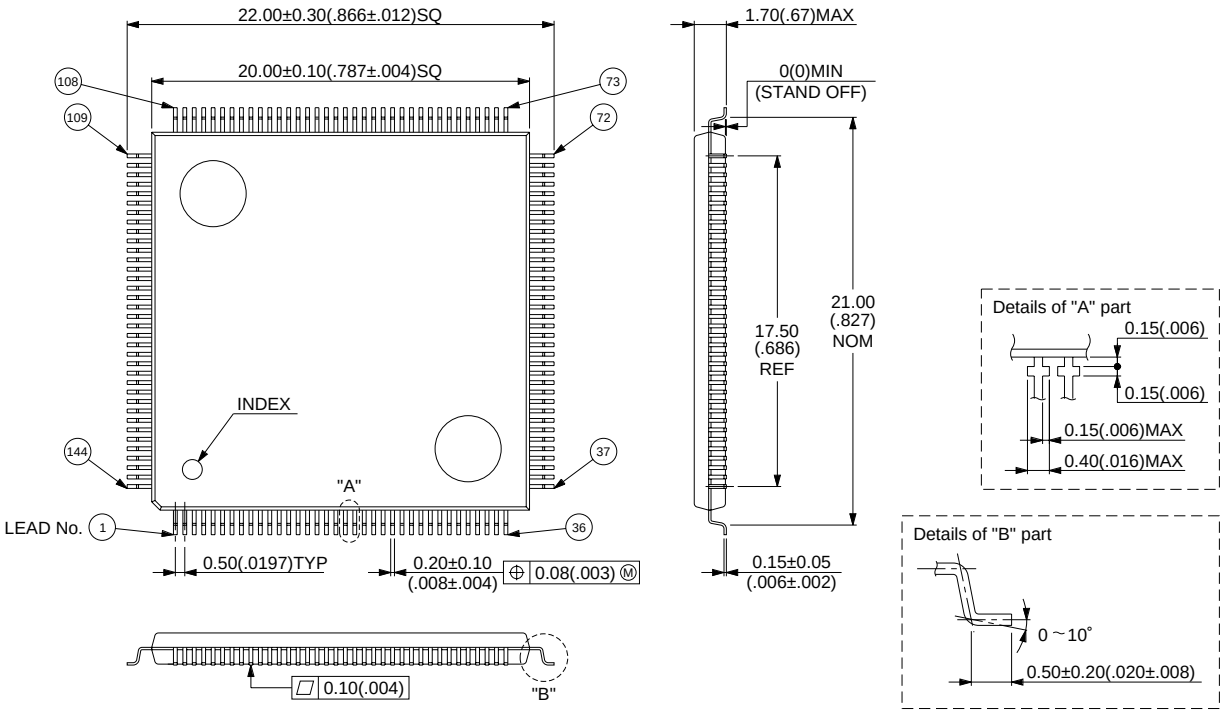
144-pin plastic FBGA
(BGA-144P-M01)

Note) Corner shape may differ from the diagram.



Dimensions in mm (inches)

144-pin plastic LQFP
(FPT-144P-M08)



Dimensions in mm (inches)

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