128K x 32 EEPROM

EEPROM Memory Array

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-94585
- MIL-STD-883

FEATURES

- Access times of 120, 140, 150, 200, 250, and 300 ns
- Built in decoupling caps for low noise operation
- Organized as 128K x32; User configurable as 256K x16 or 512K x8
- Operation with single 5 volt supply
- Low power CMOS
- TTL Compatible Inputs and Outputs
- Operating Temperature Ranges:
  Military: -55°C to +125°C
  Industrial: -40°C to +85°C

OPTIONS MARKINGS

- Timing

120 ns	-120
140 ns	-140
150 ns	-150
200 ns	-200
250 ns	-250
300 ns	-300

- Package

Ceramic Quad Flat Pack	Q
Ceramic Quad Flat Pack	Q3
Pin Grid Array- 8 Series	P
Pin Grid Array- 8 Series	PN

GENERAL DESCRIPTION

The AS8E128K32 is a 4 Megabit EEPROM Module organized as 128K x 32 bit. User configurable to 256K x16 or 512Kx 8. The module achieves high speed access, low power consumption and high reliability by employing advanced CMOS memory technology.

The military grade product is manufactured in compliance to the SMD and MIL-STD 883, making the AS8E128K32 ideally suited for military or space applications.

The module is offered in a 1.075 inch square ceramic pin grid array substrate. This package design provides the optimum space saving solution for boards that accept through hole packaging.

The module is also offered as a 68 lead 0.990 inch square ceramic quad flat pack. It has a max. height of 0.200 inch. This package design is targeted for those applications which require low profile SMT Packaging.

For more products and information please visit our web site at

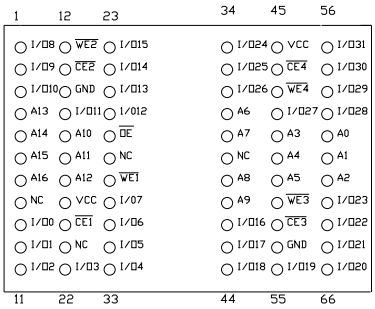
www.micross.com

PIN ASSIGNMENT

(Top View)

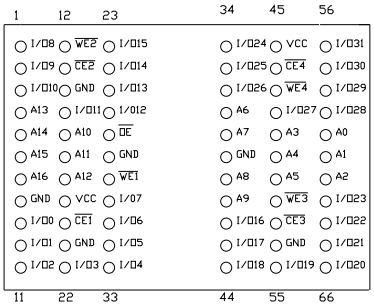
66 Lead PGA

(Pins 8, 21, 28, 39 are no connects on the PN package)

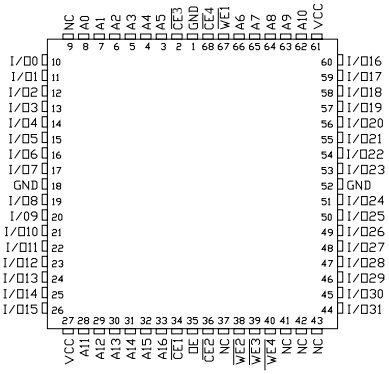


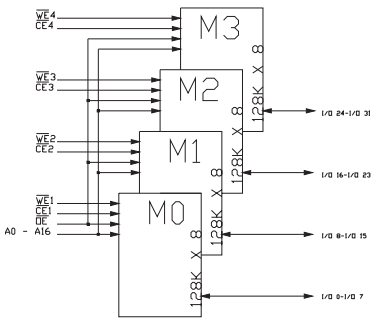
66 Lead PGA

(Pins 8, 21, 28, 39 are grounds on the P package)



68 Lead CQFP





DEVICE IDENTIFICATION

An extra 128 bytes of EEPROM memory is available on each die for user identification. By raising A9 to 12V ± 0.5V and using address locations 1FF80H to 1FFFFH the bytes may be written to or read from in the same manner as the regular memory array.

DEVICE OPERATION

The 128K x 32 EEPROM memory solution is an electrically erasable and programmable memory module that is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 128-byte-page register to allow writing of up to 128 bytes of data simultaneously. During a write cycle, the address and 1 to 128 bytes of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by DATA polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

READ

The memory module is accessed like a Static RAM. When CE\ and OE\ are low and WE\ is High, the data stored at the memory location determined by the address pins is asserted on the outputs. The module can be read as a 32 bit, 16 bit or 8 bit device. The outputs are put in the high impedance state when either CE\ or OE\ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

BYTE WRITE

A low pulse on the WE\ or CE\ input with CE\ or WE\ low (respectively) and OE\ high initiates a write cycle. The address is latched on the falling edge of CE\ or WE\, whichever occurs last. The data is latched by the first rising edge of CE\ or WE\. Once a BWDW (byte, word or double word) write has been started it will automatically time itself to completion.

PAGE WRITE

The page write operation of the 128K x 32 EEPROM allows 1 to 128 BWDWs of data to be written into the device during a single internal programming period. Each new BWDW must be written within 150-µ sec (t_{BLC}) of the previous BWDW. If the t_{BLC} limit is exceeded the memory module will cease accepting data and commence the internal programming operation. For each WE high to low transition during the page write operation, A7-A16 must be the same.

The A0-A6 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

DATA POLLING

This memory module features DATA Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. DATA Polling may begin at anytime during the write cycle.

TOGGLE BIT

In addition to DATA Polling the module provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 of the accessed die toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Reading the toggle bit may begin at any time during the write cycle.

DATA PROTECTION

If precautions are not taken, inadvertent writes may occur during transitions of the host power supply. The E^2 module has incorporated both hardware and software features that will protect the memory against inadvertent writes.

HARDWARE PROTECTION

Hardware features protect against inadvertent writes to the module in the following ways: (a) Vcc sense - if Vcc is below 3.8 V (typical) the write function is inhibited; (b) Vcc power-on delay - once Vcc has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a write; (c) write inhibit - holding any one of OE\ low, CE\ high or WE\ high inhibits write cycles; (d) noise filter - pulses of less than 15 ns (typical) on the WE\ or CE\ inputs will not initiate a write cycle.

SOFTWARE DATA PROTECTION

A software controlled data protection feature has been implemented on the memory module. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user and is shipped with SDP disabled, SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to Software Data Protection Algorithm). After writing the three byte command sequence and after t_{WC} the entire module will be protected from inadvertent write operations. It should be noted, that once protected the host may still perform a byte of page write to the module. This is done by preceding the data to be written by the same three byte command sequence used to enable SDP. Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the 128K x 32 EEPROM during power-up and Power-down conditions. All command sequences must conform to the page write timing specifications. The data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the three byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss
Vcc .....-.5V to +7.0V
Storage Temperature ....-65°C to +150°C
Voltage on any Pin Relative to Vss.....-.5V to Vcc+1 V
Max Junction Temperature**.....+150°C
Thermal Resistance junction to case (θ_{JC}):
Package Type Q.....11.3° C/W
Package Type P & PN.....2.8° C/W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
**Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow, and humidity (plastics).

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55^oC \leq T_A \leq 125^oC$ or -40^oC to $+85^oC$; V_{CC} = 5V ± 10%)

PARAMETER	CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC} +0.3	V
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V
INPUT LEAKAGE CURRENT	$0V \leq V_{IN} \leq V_{CC}$	I_{LI}	--	10	µA
OUTPUT LEAKAGE CURRENT	Outputs(s) Disabled, $0V \leq V_{OUT} \leq V_{CC}$	I_{LO}	--	10	µA
Output High Voltage	I_{OH} = -0.4mA	V_{OH}	2.4	–	V
Output Low Voltage	I_{OL} = 2.1mA	V_{OL}	--	0.45	V
Supply Voltage		V_{CC}	4.5	5.5	V

PARAMETER	CONDITIONS	SYM	MAX For All Speed Options	UNITS
Power Supply Current: Operating	CE\≤V_{IL}; V_{CC}=MAX, f = MAX = $1/t_{RC}$ (MIN) Outputs Open	I_{cc}	250	mA
Power Supply Current: Standby	CE\≥V_{IH}; All Other Inputs ≤V_{IL} or ≥V_{IH}; V_{CC}=MAX, f =0 Hz	I_{SBT1}	15	mA
	CE\≥V_{CC}-0.2V; V_{CC}=MAX, $V_{IL} \leq V_{SS}$ +0.2V or $V_{IH} \geq V_{CC}$ -0.2V; f = 0 Hz	I_{SBT2}	1	mA
	CE\=V_{CC}, OE\=V_{IH}; I/O 0 through 31 = open; Input=V_{CC}=5.5Vdc.; A0 through A16 change at 5 MHz; CMOS levels	I_{SBT3}	5	mA

CAPACITANCE TABLE[1] (V_{IN} = 0V, f = 1 MHz, T_A = 25°C)

SYMBOL	PARAMETER	MAX	UNITS
C_{ADD}	A0 - A16 Capacitance	40	pF
C_{OE}	OE\ Capacitance	40	pF
C_{WE}, C_{CE}	WE\ and CE\ Capacitance	10	pF
C_{IO}	I/O 0- I/O 31 Capacitance	12	pF

NOTE: 1. This parameter is guaranteed but not tested.

TRUTH TABLE				
MODE	**CE**	**OE**	**WE**	**I/O**
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write (2)	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write	V_{IH}	X (1)	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z

NOTES: 1. X can be V_{IL} or V_{IH}
2. Refer to AC Programming Waveforms

AC TEST CONDITIONS

TEST SPECIFICATIONS

Input pulse levels.....V_{SS} to 3V
Input rise and fall times.....5ns
Input timing reference levels.....1.5V
Output reference levels.....1.5V
Output load.....See Figure 1

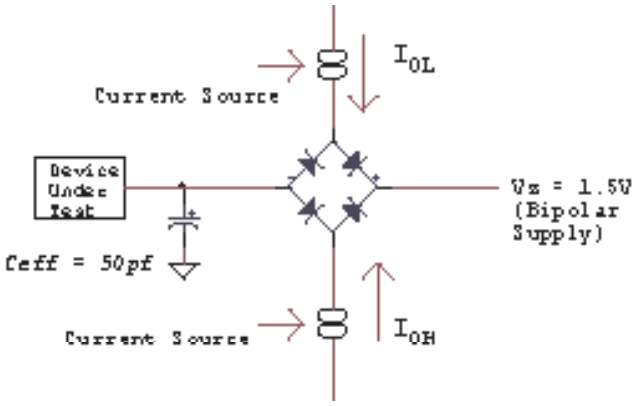


Figure 1

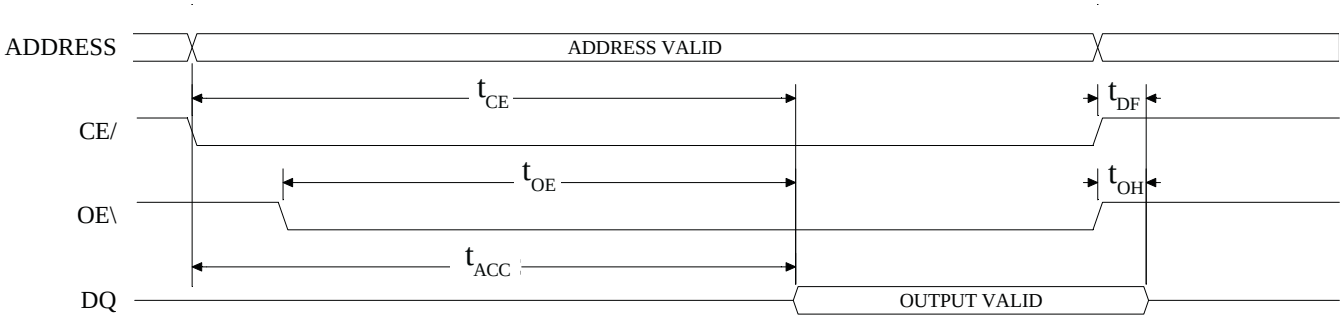
NOTES:
Vz is programmable from -2V to + 7V.
I_{OL} and I_{OH} programmable from 0 to 16 mA.
Vz is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(-55°C ≤ T_A ≤ +125°C or -40°C to +85°C; Vcc = 5V ±10%)

DESCRIPTION	SYMBOL	120		140		150		200		250		300		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Address to Output Delay	t_{ACC}		120		140		150		200		250		300	ns
CE\ to Output Delay	t_{CE}		120		140		150		200		250		300	ns
OE\ to Output Delay	t_{OE}	0	50	0	55	0	55	0	55	0	55	0	55	ns
CE\ or OE\ to Output Float	t_{DF}		55		55		55		55		55		55	ns
Output Hold from OE\, CE\ or Address, whichever comes first	t_{OH}	0		0		0		0		0		0		ns

AC READ WAVEFORMS(1,2,3)



NOTES:

1. CE\ may be delayed to t_{ACC}-t_{CE} after the address transition without impact on t_{ACC}.
2. OE\ may be delayed to t_{CE}-t_{OE} after the falling edge of CE\ without impact on t_{CE} or by t_{ACC}-t_{OE} after an address change without inpact on t_{ACC}.
3. t_{DF} is specified from OE\ or CE\ whichever occurs first (C_L = 5pF).

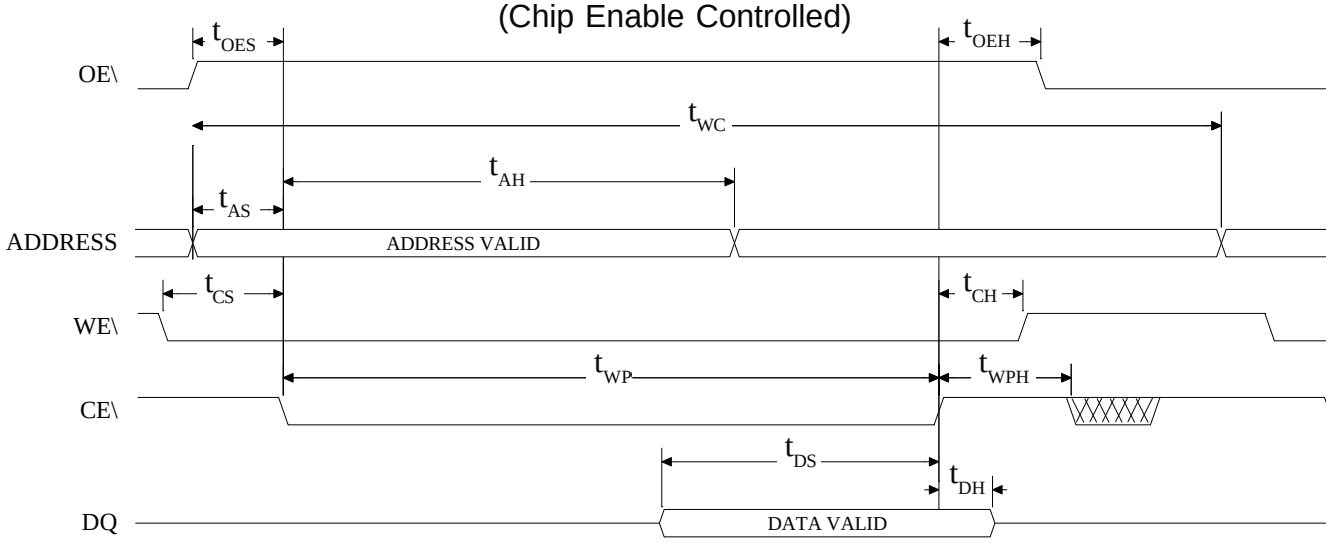
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC WRITE CHARACTERISTICS

(-55°C ≤ T_A ≤ +125°C; Vcc = 5V ±10%)

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cyce Time		10	ms
t_{AS}	Address Set-up Time	4		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	100		ns
t_{BLC}	Byte Load Cycle Time		150	µs
t_{WPH}	Write Pulse Width High	50		ns

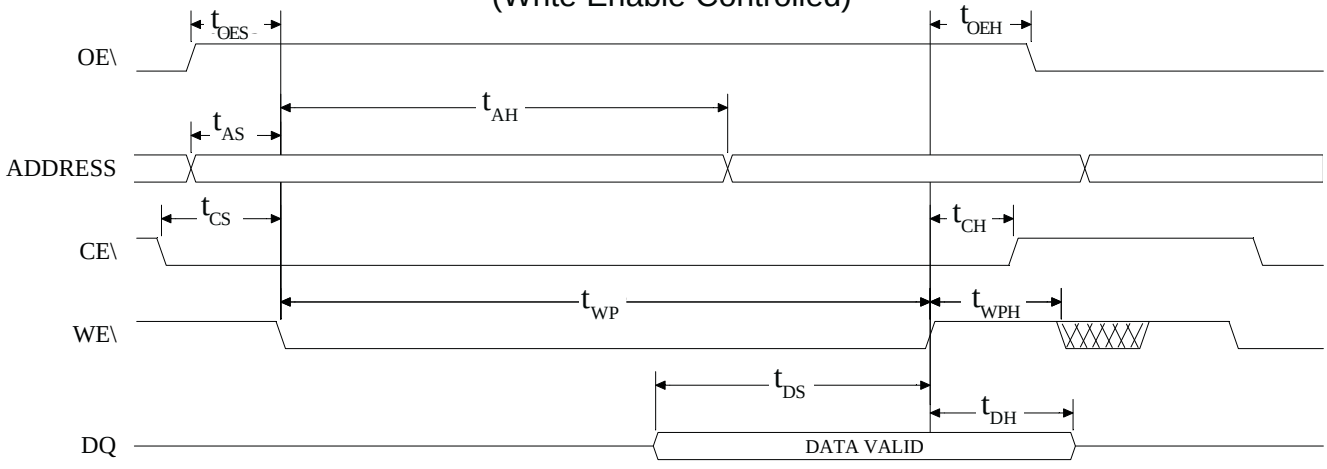
WRITE CYCLE NO 1.

(Chip Enable Controlled)



WRITE CYCLE NO 2.

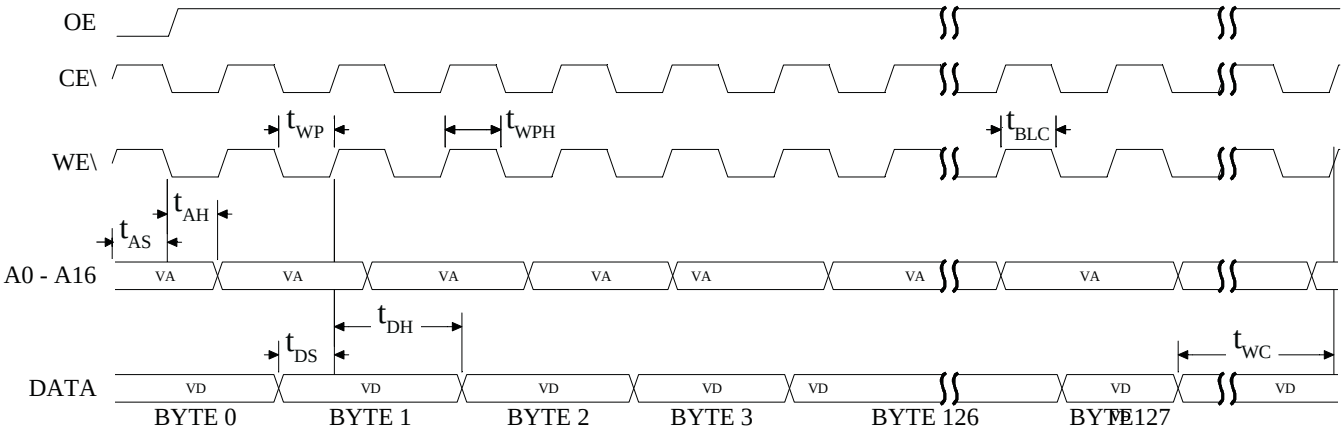
(Write Enable Controlled)



PAGE MODE CHARACTERISTICS

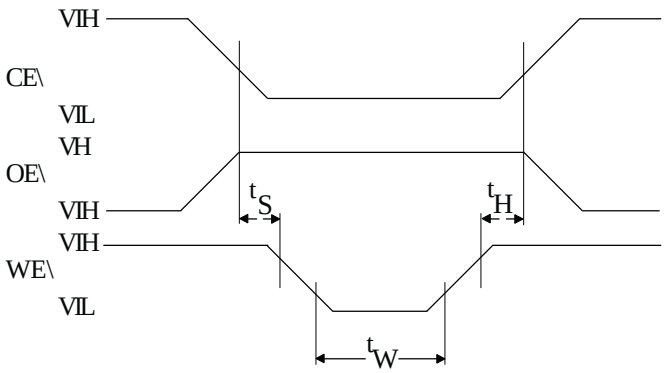
Symbol	Parameter	Min	Max	Unit
t_{AS}, t_{OES}	Address, OE\ Set-Up time	4		ns
t_{AH}	Address, Hold time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width (WE\ or CE\)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, OE\ Hold Time	10		ns

PAGE MODE WRITE WAVEFORMS(1,2)



NOTES: 1. A7 through A16 must specify the page address during each high to low transition of WE\ (or CE\).
2. OE\ must be high only when WE\ and CE\ are both low.
3. VD - Valid Data
4. VA - Valid Address

CHIP ERASE WAVEFORMS

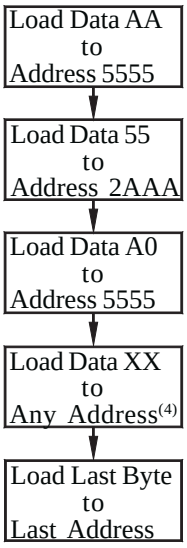


$t_S = 5$ msec (min.)

$t_W = tH = 10$ msec (min.)

$V_H = 12.0V \pm 0.5V$

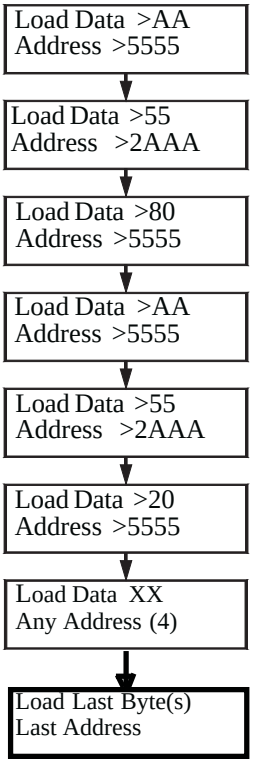
Software Data Protection Enable Algorithm(1)



Writes Enabled(2)

Enter Data Protect State

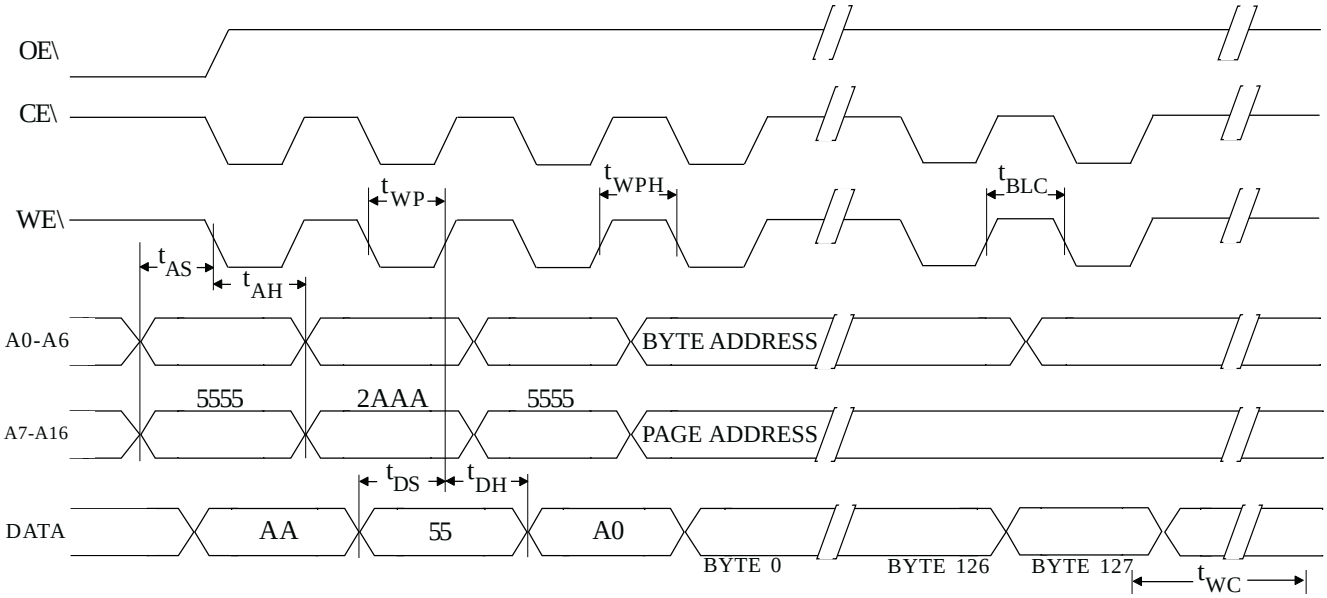
Software Data Protection Disable Algorithm(1)



;Exit Data Protect State(3)

NOTES:
1. Byte Data Format: I/O7 - I/O0, I/
   Address Format: A14 - A0 (Hex)
2. Write Protect state will be active at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of period even if no other data is loaded.
4. 1 to 128 bytes of data are loaded.

SOFTWARE PROTECTED PROGRAM CYCLE WAVEFORM(1)(2)(3)



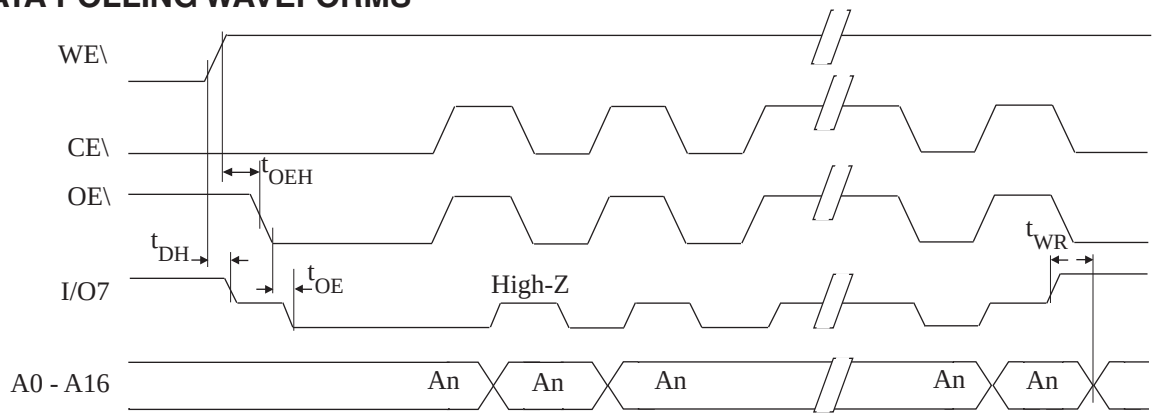
1. A0-A14 of the selected I/O bytes must conform to the addressing sequence for the first three bytes as shown above.
2. After the command sequence has been issued and a page write operation follows, the page address inputs (A7-A16) of the selected I/O bytes must be the same for each high to low transition of WE\ (or CE\).
3. OE Must be high only when WE\ and CE\ are both low.

DATA POLLING CHARACTERISTICS(1)

Symbol	Parameter	Min	Max	Units
t_{DH}	Data Hold Time	10		ns
t_{OEH}	OE\ Hold Time	10		ns
t_{OE}	OE\ to Output Delay (2)			ns
t_{WR}	Write Recovery Time	0		ns

NOTES: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

DATA POLLING WAVEFORMS

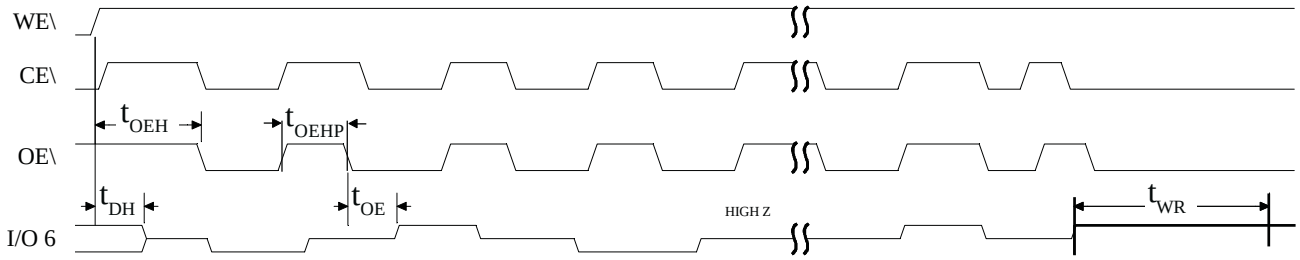


TOGGLE BIT CHARACTERISTICS(1)

Symbol	Parameter	Min	Max	Units
t_{DH}	Data Hold Time	10		ns
t_{OEH}	OE\ Hold Time	10		ns
t_{OE}	OE\ to Output Delay(2)			ns
t_{OEHP}	OE\ High Pulse	150		ns
t_{WR}	Write Recovery Time	0		ns

NOTES: 1. These parameters are characterized and not 100% tested.
2. See AC Read Characteristics.

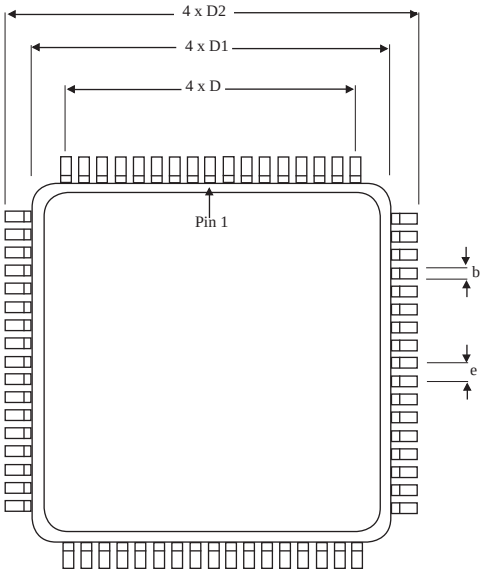
TOGGLE BIT WAVEFORMS(1,2,3)



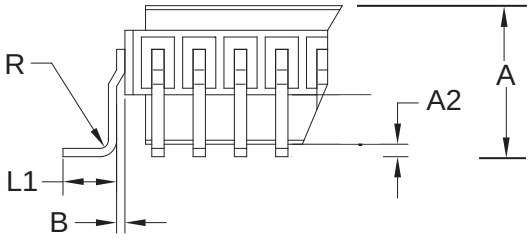
NOTES: 1. Toggling either OE or CE or Both OE and CE will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

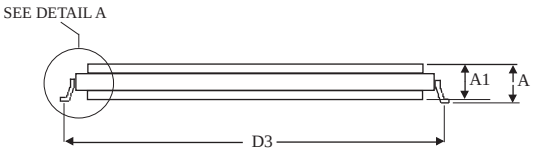
MECHANICAL DEFINITIONS*

Micross Case #703 (Package Designator Q)
SMD 5962-94585, Case Outline M



DETAIL A



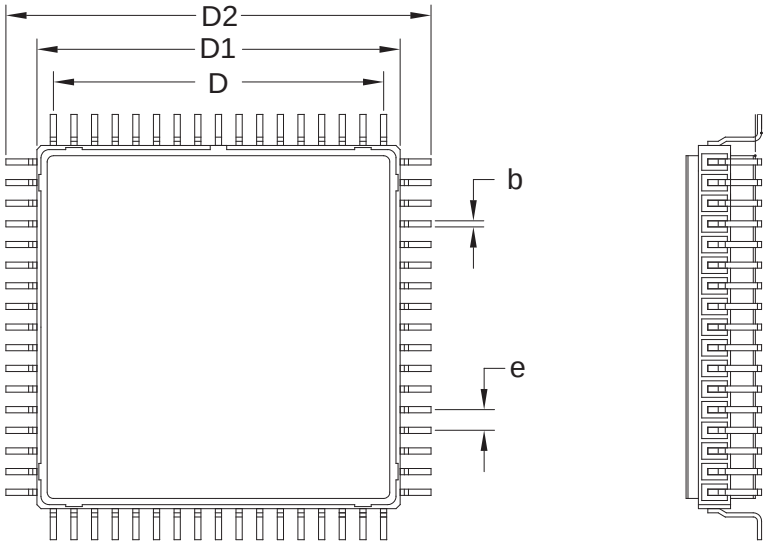


SYMBOL	MICROSS PACKAGE SPECIFICATIONS	
	MIN	MAX
A	0.123	0.200
A1	0.118	0.186
A2	0.005	0.020
b	0.013	0.017
B	0.010 REF	
D	0.800 BSC	
D1	0.870	0.890
D2	0.980	1.000
D3	0.936	0.956
e	0.050 BSC	
R	0.005	---
L1	0.035	0.045

All measurements are in inches.

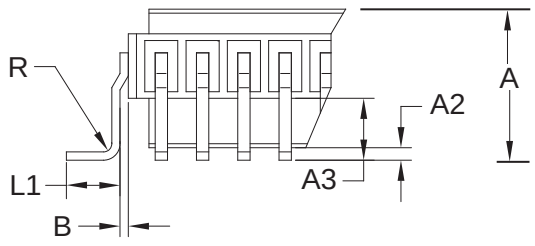
MECHANICAL DEFINITIONS*

Micross Package Designator Q3



PACKAGE SPECIFICATION		
Symbol	Min	Max
A		.200
A2	.010	.025
A3	.070	.080
b	.013	.017
B	.010 REF	
D	.800 BSC	
D1	.870	.890
D2	.980	1.00
e	.050 BSC	
R	.010 TYP	
L1	.035	.045

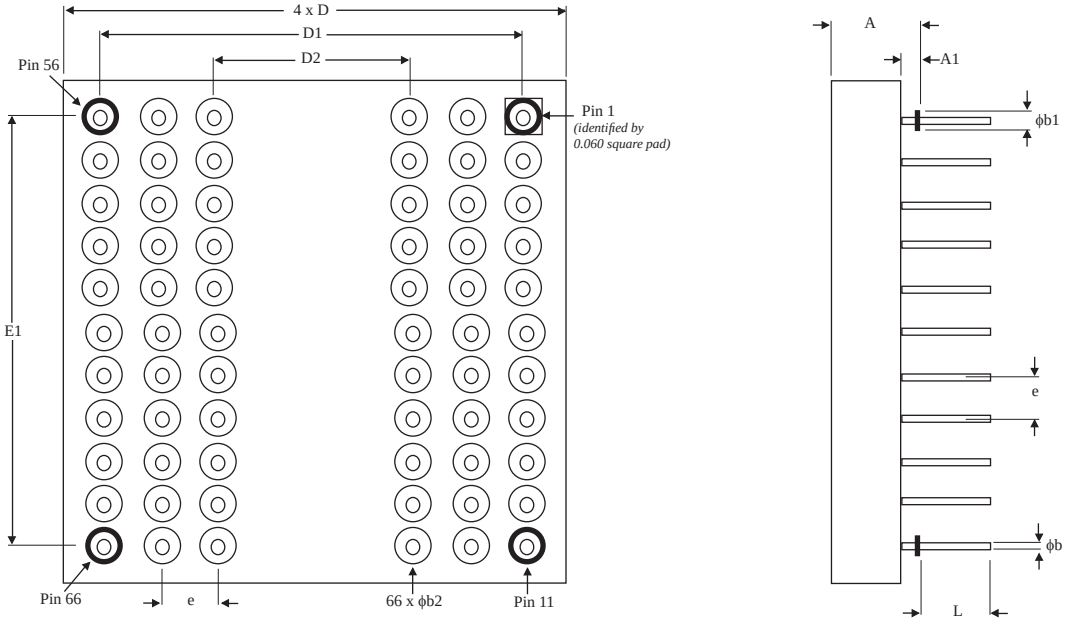
Dimensions are in inches.



All measurements are in inches.

MECHANICAL DEFINITIONS*

Micross Case #904 (Package Designator P & PN)
SMD 5962-94585, Case Outline 4 and 5



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.135	0.181
A1	0.025	0.035
ϕb	0.016	0.020
ϕb1	0.045	0.055
ϕb2	0.065	0.075
D	1.065	1.085
D1/E1	1.000 BSC	
D2	0.600 BSC	
e	0.100 BSC	
L	0.132	0.155

All measurements are in inches.

ORDERING INFORMATION

EXAMPLE: AS8E128K32Q-250/XT

Device Number	Package Type	Speed ns	Process
AS8E128K32	Q	-120	/*
AS8E128K32	Q3	-120	/*
AS8E128K32	Q	-140	/*
AS8E128K32	Q3	-140	/*
AS8E128K32	Q	-150	/*
AS8E128K32	Q3	-150	/*
AS8E128K32	Q	-200	/*
AS8E128K32	Q3	-200	/*
AS8E128K32	Q	-250	/*
AS8E128K32	Q3	-250	/*
AS8E128K32	Q	-300	/*
AS8E128K32	Q3	-300	/*

EXAMPLE: AS8E128K32P-200/883C

Device Number	Package Type	Speed ns	Process
AS8E128K32	P	-120	/*
AS8E128K32	PN	-120	/*
AS8E128K32	P	-140	/*
AS8E128K32	PN	-140	/*
AS8E128K32	P	-150	/*
AS8E128K32	PN	-150	/*
AS8E128K32	P	-200	/*
AS8E128K32	PN	-200	/*
AS8E128K32	P	-250	/*
AS8E128K32	PN	-250	/*
AS8E128K32	P	-300	/*
AS8E128K32	PN	-300	/*

*AVAILABLE PROCESSES

IT = Industrial Temperature Range -40°C to +85°C
XT = Extended Temperature Range -55°C to +125°C
883C = Full Military Processing -55°C to +125°C

PACKAGE NOTES

P = Pins 8, 21, 28, and 39 are grounds.
PN = Pins 8, 21, 28, and 39 are no connects.

MICROSS TO DSCC PART NUMBER CROSS REFERENCE*

Micross Package Designator Q

Micross Part #	SMD Part #
AS8E128K32Q-120/883C	5962-9458506HMA
AS8E128K32Q-120/883C	5962-9458506HMC
AS8E128K32Q-140/883C	5962-9458505HMA
AS8E128K32Q-140/883C	5962-9458505HMC
AS8E128K32Q-150/883C	5962-9458504HMA
AS8E128K32Q-150/883C	5962-9458504HMC
AS8E128K32Q-200/883C	5962-9458503HMA
AS8E128K32Q-200/883C	5962-9458503HMC
AS8E128K32Q-250/883C	5962-9458502HMA
AS8E128K32Q-250/883C	5962-9458502HMC
AS8E128K32Q-300/883C	5962-9458501HMA
AS8E128K32Q-300/883C	5962-9458501HMC

ASI Package Designator P & PN

Micross Part #	SMD Part #
AS8E128K32P-120/883C	5962-9458506H5A
AS8E128K32P-120/883C	5962-9458506H5C
AS8E128K32P-140/883C	5962-9458505H5A
AS8E128K32P-140/883C	5962-9458505H5C
AS8E128K32P-150/883C	5962-9458504H5A
AS8E128K32P-150/883C	5962-9458504H5C
AS8E128K32P-200/883C	5962-9458503H5A
AS8E128K32P-200/883C	5962-9458503H5C
AS8E128K32P-250/883C	5962-9458502H5A
AS8E128K32P-250/883C	5962-9458502H5C
AS8E128K32P-300/883C	5962-9458501H5A
AS8E128K32P-300/883C	5962-9458501H5C
AS8E128K32PN-120/883C	5962-9458506H4A
AS8E128K32PN-120/883C	5962-9458506H4C
AS8E128K32PN-140/883C	5962-9458505H4A
AS8E128K32PN-140/883C	5962-9458505H4C
AS8E128K32PN-150/883C	5962-9458504H4A
AS8E128K32PN-150/883C	5962-9458504H4C
AS8E128K32PN-200/883C	5962-9458503H4A
AS8E128K32PN-200/883C	5962-9458503H4C
AS8E128K32PN-250/883C	5962-9458502H4A
AS8E128K32PN-250/883C	5962-9458502H4C
AS8E128K32PN-300/883C	5962-9458501H4A
AS8E128K32PN-300/883C	5962-9458501H4C

**Micross part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.*

DOCUMENT TITLE
128K x 32 EEPROM EEPROM Memory Array

Rev #	History	Release Date	Status
8.2	Updated Q3 Package, pg 11	July 2010	Release