

# 74AC/ACT11193

## Asynchronous Presettable Synchronous 4-Bit Binary Up/ Down Counter w/Dual Clock

Objective Specification

### ACL Products

#### FEATURES

- Synchronous, reversible counting
- Positive edge-triggered clock
- 4-bit binary
- Asynchronous Parallel Load capability
- Output capability:  $\pm 24\text{mA}$
- CMOS (AC) and TTL (ACT) voltage level inputs
- $50\Omega$  incident wave switching
- Center-pin  $V_{CC}$  and ground configuration to minimize high-speed switching noise
- $I_{CC}$  category: MSI

#### DESCRIPTION

The 74AC/ACT11193 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11193 is an asynchronously presettable up/down 4-bit binary counter. Separate up/down clocks,  $CP_U$  and  $CP_D$  respectively, simplify operation, the outputs change state synchronously with the Low-to-High transition of either Clock input. If the  $CP_U$  clock is pulsed while  $CP_D$  is held High, the device will

#### GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS $T_A = 25^\circ\text{C}; \text{GND} = 0\text{V};$ $V_{CC} = 5.0\text{V}$	TYPICAL		UNIT
			AC	ACT	
$t_{PLH}/t_{PHL}$	Propagation delay $CP_x$ to $Q_n$ ( $PL = \text{High}$ )	$C_L = 50\text{pF}$	6.8	8.5	ns
$C_{PD}$	Power dissipation capacitance <sup>1</sup>	$f = 1\text{MHz}; C_L = 50\text{pF}$	68	70	pF
$C_{IN}$	Input capacitance	$V_I = 0\text{V}$ or $V_{CC}$	4.0	4.0	pF
$I_{LATCH}$	Latch-up current	Per JEDEC JC40.2 Standard 17	500	500	mA
$f_{MAX}$	Maximum clock frequency, $CP_x, Q_n$	$C_L = 50\text{pF}$	125	110	MHz

Note:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

$f_I$  = input frequency in MHz,  $C_L$  = output load capacitance in pF,

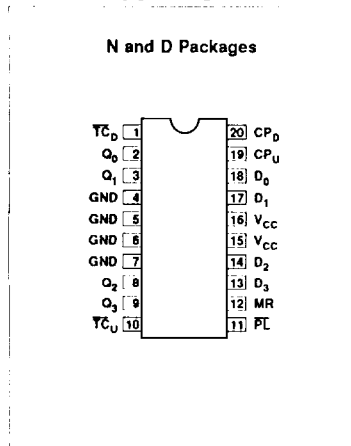
$f_O$  = output frequency in MHz,  $V_{CC}$  = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_O)$  = sum of outputs

#### ORDERING INFORMATION

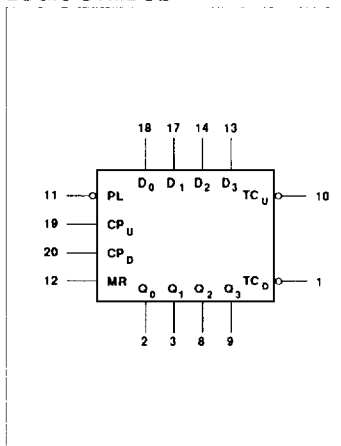
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11193N 74ACT11193N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11193D 74ACT11193D

#### PIN CONFIGURATION

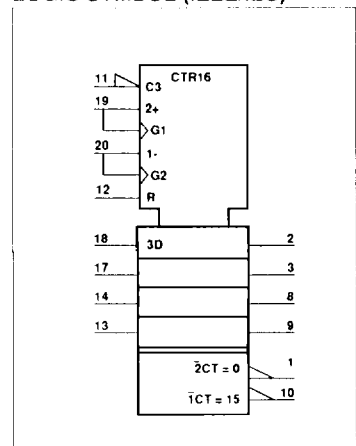


June 2, 1989

#### LOGIC SYMBOL



#### LOGIC SYMBOL (IEEE/IEC)



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count up, if  $CP_D$  is pulsed while  $CP_U$  is held High, the device will count down. Only one Clock input can be held High at any time, or erroneous operation will result.

Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, preset load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master such that a Low-to-High transition on the  $CP_D$  input will decrease the count by one, while a similar transition on the  $CP_U$  input will advance the count by one.

One clock must be held High while counting with the other because the circuit will

either count by two's or not at all depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is Low. Applications requiring reversible operation must make the reversing decision while the activating clock is High to avoid erroneous counts.

The Terminal Count Up ( $\overline{TC}_U$ ) and Terminal Count Down ( $\overline{TC}_D$ ) outputs are normally High. When the circuit has reached the maximum count state of 15, the next High-to-Low transition of  $CP_U$  will cause  $\overline{TC}_U$  to go Low.  $\overline{TC}_U$  will stay Low until  $CP_U$  goes High again, duplicating the count up clock, although delayed by two gate delays. Likewise, the  $\overline{TC}_D$  output will go Low when the circuit is in the zero state and the  $CP_D$  goes Low. The  $\overline{TC}$  outputs can be used as the Clock input signals to the next higher order circuit in a multi-

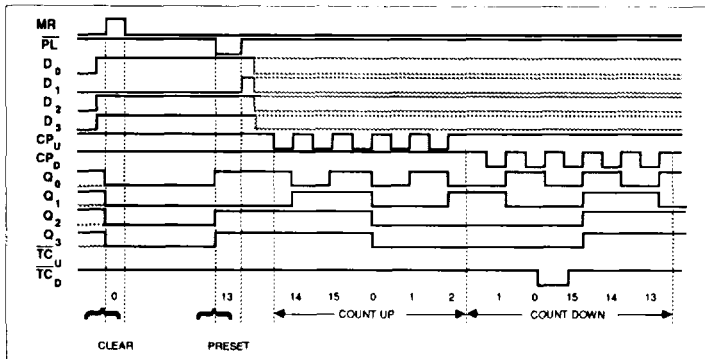
stage counter, since they duplicate the clock waveforms. Multi-stage counters will not be fully synchronous, since there is a two-gate delay time difference added for each stage that is added.

Asynchronous Parallel Load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs ( $D_0 - D_3$ ) is loaded into the counter and appears on the outputs when the Parallel Load ( $\overline{PL}$ ) input is Low. A High level on the Master Reset ( $\overline{MR}$ ) input will disable the parallel load gates, override both Clock inputs, and set all Q outputs Low. If one of the Clock inputs is Low during and after a reset or load operation, the next Low-to-High transition of that clock will be interpreted as a legitimate signal and will be counted.

### PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
12	MR	Master reset input
11	$\overline{PL}$	Parallel load input (active-Low)
19	$CP_U$	Count up clock input (active rising edge)
20	$CP_D$	Count down clock input (active rising edge)
18, 17, 14, 13	$D_0 - D_3$	Data inputs
2, 3, 8, 9	$Q_0 - Q_3$	Counter outputs
10	$\overline{TC}_U$	Terminal count up (carry) output (active-Low)
1	$\overline{TC}_D$	Terminal count down (carry) output (active-Low)
4, 5, 6, 7	GND	Ground (0V)
15, 16	$V_{CC}$	Positive supply voltage

### TIMING DIAGRAM



# Asynchronous Presettable Synchronous 4-Bit Binary Up/Down Counter w/Dual Clock

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### MODE SELECT—FUNCTION TABLE

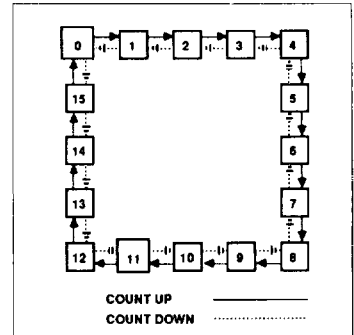
OPERATING MODE	INPUTS								OUTPUTS					
	MR	PL	CP <sub>U</sub>	CP <sub>D</sub>	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>	TC <sub>U</sub>	TC <sub>D</sub>
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	H	X	H	H	H	H	H	H	H	H	L	H
Count up	L	H	↑	H	X	X	X	X	Count up				H <sup>(1)</sup>	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	H <sup>(2)</sup>

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 ↑ = Low-to-High clock transition

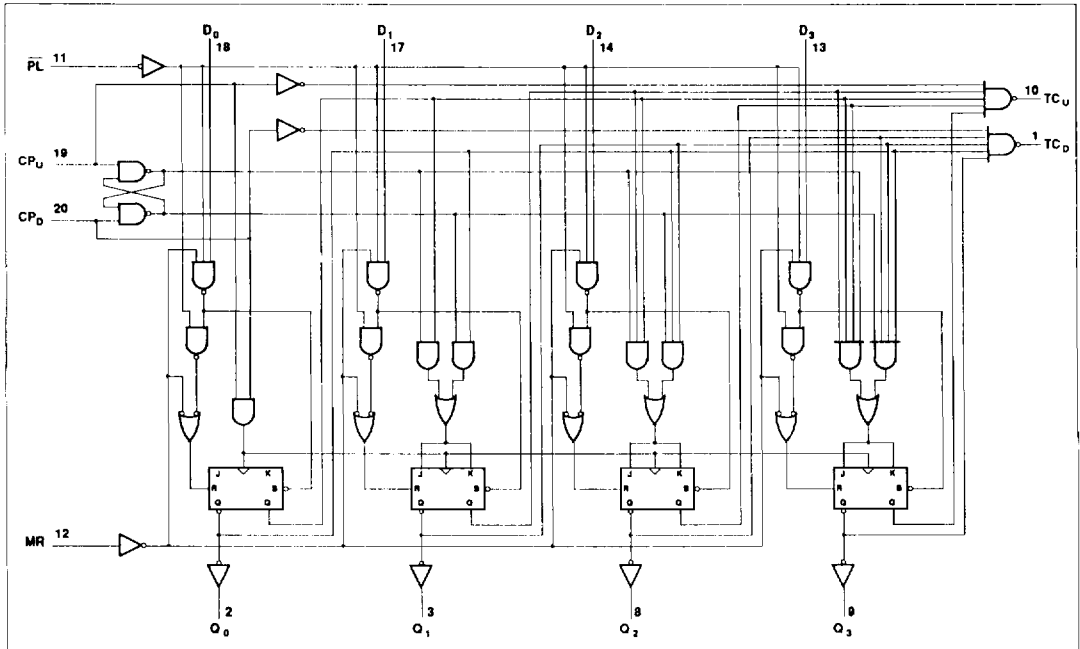
**NOTES:**

1. TC<sub>U</sub> = CPU at terminal count up (HHHH).
2. TC<sub>D</sub> = CPD at terminal count down (LLLL).

### STATE DIAGRAM



### LOGIC DIAGRAM



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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11193			74ACT11193			UNIT
		Min	Nom	Max	Min	Nom	Max	
$V_{CC}$	DC supply voltage	3.0 <sup>1</sup>	5.0	5.5	4.5	5.0	5.5	V
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
$T_A$	Operating free-air temperature	-40		+85	-40		+85	°C

### NOTE:

- No electrical or switching characteristics are specified at  $V_{CC} < 3V$ . Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$I_{IK}$ or $V_I$	DC input diode current <sup>2</sup>	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
$I_{OK}$ or $V_O$	DC output diode current <sup>2</sup>	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
$I_O$	DC output source or sink current per output pin	$V_O = 0$ to $V_{CC}$	±50	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ current		±150	mA
	DC ground current		±150	
$T_{STG}$	Storage temperature		-65 to 150	°C
$P_{TOT}$	Power dissipation per package Plastic DIP	Above 70°C: derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C: derate linearly by 6mW/K	400	mW

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# Asynchronous Presettable Synchronous 4-Bit Binary Up/Down Counter w/Dual Clock

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**DC ELECTRICAL CHARACTERISTICS**

SYMBOL	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> V	74AC11193				74ACT11193				UNIT
				T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		
				Min	Max	Min	Max	Min	Max	Min	Max	
V <sub>IH</sub>	High-level input voltage		3.0	2.10		2.10						V
			4.5	3.15		3.15		2.0		2.0		
			5.5	3.85		3.85		2.0		2.0		
V <sub>IL</sub>	Low-level input voltage		3.0		0.90		0.90					V
			4.5		1.35		1.35	0.8		0.8		
			5.5		1.65		1.65	0.8		0.8		
V <sub>OH</sub>	High-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = -50μA	3.0	2.9		2.9					V
				4.5	4.4		4.4		4.4		4.4	
				5.5	5.4		5.4		5.4		5.4	
			I <sub>OH</sub> = -4mA	3.0	2.58		2.48					
				4.5	3.94		3.8		3.94		3.8	
				5.5	4.94		4.8		4.94		4.8	
I <sub>OH</sub> = -75mA <sup>1</sup>	5.5			3.85				3.85				
V <sub>OL</sub>	Low-level output voltage	V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OL</sub> = 50μA	3.0		0.1		0.1				V
				4.5		0.1		0.1	0.1	0.1		
				5.5		0.1		0.1	0.1	0.1		
			I <sub>OL</sub> = 12mA	3.0		0.36		0.44				
				4.5		0.36		0.44	0.36	0.44		
			I <sub>OL</sub> = 24mA	3.0		0.36		0.44	0.36	0.44		
				5.5		0.36		0.44	0.36	0.44		
I <sub>OL</sub> = 75mA <sup>1</sup>	5.5				1.65		1.65					
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5		8.0		80		8.0		80	μA
ΔI <sub>CC</sub>	Supply current, TTL inputs High <sup>2</sup>	One input at 3.4V, other inputs at V <sub>CC</sub> or GND	5.5						0.9		1.0	mA

**NOTES:**

- Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
- This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V<sub>CC</sub>.