19-0894; Rev 1; 7/95

# MAXIM

# CMOS 8-Bit 8-Channel Data Acquisition System



## General Description

The MAX161 and MX7581 are CMOS single-chip 8-bit, 8-channel data acquisition systems (DAS). Each chip includes an 8-bit A/D converter, 8-channel multiplexer, 8 x 8 dual port RAM with contention logic, and microprocessor compatible I/O logic. When combined with a voltage reference, a complete data acquisition system is produced that interfaces with the majority of microprocessors.

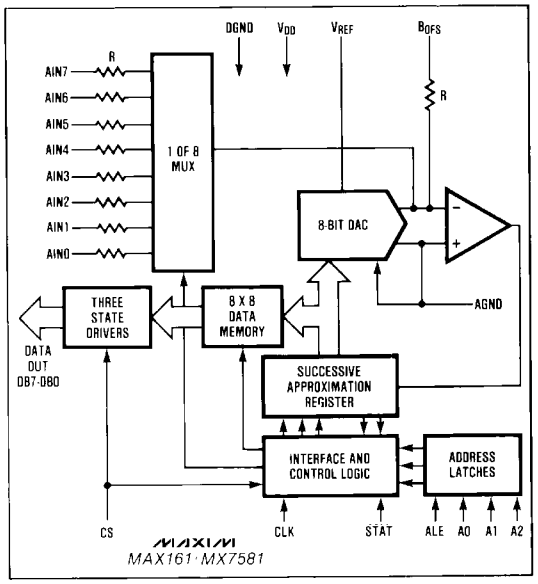
Conversions take place on a continuous, channel sequencing basis using a microprocessor clock or control signal. Data is stored automatically in dual port RAM so that any channel can be read at any time under microprocessor control.

The MAX161 is an enhanced, pin-compatible version of the MX7581. Improvements include faster conversion and interface timing, lower zero error and drift, reduced power dissipation, and availability in military temperature grades. All devices are available in 28 pin DIP and Small Outline (SO) packages.

## Applications

Digital Signal Processing
Data Loggers
Automatic Test Equipment
Robotics
Process Control

## Functional Diagram




MAXIM
MAX161/MX7581

## Features

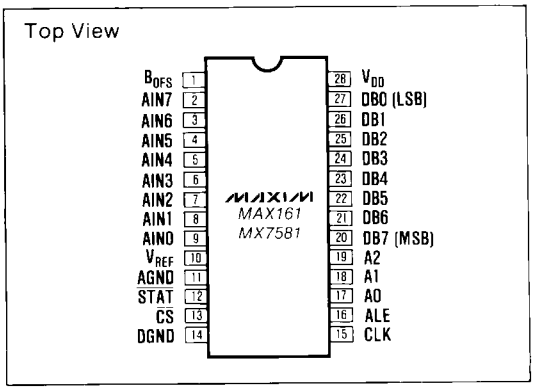
- ◆ **Fast Conversion Time: 20μsec (MAX161)**
- ◆ **No Missing Codes Over Temperature**
- ◆ **On Chip 8 x 8 Dual Port RAM**
- ◆ **Interfaces Directly To Z80/8085/6800**
- ◆ **Ratiometric Capability**
- ◆ **Interleaved DMA Operation**

## Ordering Information

| PART | TEMP. RANGE | PACKAGE* | ERROR |
|---|---|---|---|
| MAX161ACPI | 0° C to +70° C | Plastic DIP | 1 7/8 LSB |
| MAX161BCPI | 0° C to +70° C | Plastic DIP | 3/4 LSB |
| MAX161CCPI | 0° C to +70° C | Plastic DIP | 1/2 LSB |
| MAX161ACWI | 0° C to +70° C | Small Outline | 1 7/8 LSB |
| MAX161BCWI | 0° C to +70° C | Small Outline | 3/4 LSB |
| MAX161CCWI | 0° C to +70° C | Small Outline | 1/2 LSB |
| MAX161CC/D | 0° C to +70° C | Dice | 1 7/8 LSB |
| MAX161AEPI | -40° C to +85° C | Plastic DIP | 1 7/8 LSB |
| MAX161BEPI | -40° C to +85° C | Plastic DIP | 3/4 LSB |
| MAX161CEPI | -40° C to +85° C | Plastic DIP | 1/2 LSB |
| MAX161AEWI | -40° C to +85° C | Small Outline | 1 7/8 LSB |
| MAX161BEWI | -40° C to +85° C | Small Outline | 3/4 LSB |
| MAX161CEWI | -40° C to +85° C | Small Outline | 1/2 LSB |
| MAX161AMJI | -55° C to +125° C | CERDIP** | 1 7/8 LSB |
| MAX161BMJI | -55° C to +125° C | CERDIP** | 3/4 LSB |
| MAX161CMJI | -55° C to +125° C | CERDIP** | 1/2 LSB |

* *All devices — 28 lead packages*
** *Maxim reserves the right to ship Ceramic Packages in lieu of CERDIP Packages.*
*Ordering Information continued on last page.*

## Pin Configuration



# CMOS 8-Bit 8-Channel Data Acquisition System

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to AGND ..... +7V
$V_{DD}$ to DGND ..... +7V
AGND to DGND ..... -0.3V, $V_{DD}$
Digital Input Voltage to DGND
(pins 13,16-19) ..... -0.3V, $V_{DD}$
Digital Output Voltage to DGND
(pins 12,20-27) ..... -0.3V, $V_{DD}$
CLK (pin 15) input voltage to DGND ..... -0.3V, $V_{DD}$
$V_{REF}$ (pin 10) to AGND ..... ±25V
$V_{BOFS}$ (pin 1) to AGND ..... ±17V
AIN (0-7) (pins 9-2) ..... ±17V

Operating Temperature Range
MAX161XC, MX7581J/K/L ..... 0°C to +70°C
MX7581A/B/C ..... -25°C to +85°C
MAX161XE ..... -40°C to +85°C
MAX161XM, MX7581S/T/U ..... -55°C TO +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C
Power Dissipation (Package)
Plastic DIP (Derate 12mW/°C above +50°C) ..... 1200mW
Ceramic (Derate 10mW/°C above +50°C) ..... 1000mW
CERDIP (Derate 10mW/°C above +50°C) ..... 1000mW
Small Outline (Derate 12mW/°C above +50°C) ..... 1000mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = +5V, $V_{REF}$ = -10V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|---|
| **ACCURACY (at $f_{CLK}$ = 4.0MHz for MAX161, 1.2MHz for MX7581)** | | | | | | | |
| Resolution | | | | 8 | | | Bits |
| Relative Accuracy | | MAX161A, MX7581J/A/S<br>MAX161B, MX7581K/B/T<br>MAX161C, MX7581L/C/U | | | ±¾<br>±½<br>±¼ | ±1⅞<br>±¾<br>±½ | LSB |
| Differential Nonlinearity | | MAX161A, MX7581J/A/S<br>MAX161B, MX7581K/B/T<br>MAX161C, MX7581L/C/U | | | ±¾<br>±½<br>±¼ | ±1⅞<br>±⅞<br>±¾ | LSB |
| **Offset Error (See Figure 5, Note 1)** | | **Adjustable to zero** | **MAX161A**<br>**MAX161B**<br>**MAX161C** | | **±60**<br>**±40**<br>**±20** | **±120**<br>**±60**<br>**±40** | mV |
| | | | MX7581J/A/S<br>MX7581K/B/T<br>MX7581L/C/U | | ±60<br>±40<br>±20 | ±200<br>±80<br>±50 | |
| Gain Error, Worst Channel (See Figure 5, Note 2) | | Adjustable to zero | MAX161A, MX7581J/A/S<br>MAX161B, MX7581K/B/T<br>MAX161C, MX7581L/C/U | | ±3<br>±2<br>±1 | ±6<br>±4<br>±2 | LSB |
| Gain Match Between Channels (See Figure 5) | | Adjustable to zero | MAX161A, MX7581J/A/S<br>MAX161B, MX7581K/B/T<br>MAX161C, MX7581L/C/U | | 2<br>1<br>½ | 3<br>2<br>1 | LSB |
| $B_{OFS}$ Gain Error (Note 3) | | | | | ±1 | | LSB |
| **ANALOG INPUTS** | | | | | | | |
| Input Resistance at $V_{REF}$, $B_{OFS}$, and AIN7-AIN0 | $R_{IN}$ | Pins 1 to 10 (Note 4) | | 10 | 20 | 30 | kΩ |
| $V_{REF}$ (For Specified Performance) | $V_{REF}$ | | | -10.5 | | -9.5 | V |
| $V_{REF}$ Range | | | | -5V to -15V | | | V |
| Nominal Analog Input Range | | +Unipolar Mode (See Figure 5)<br>-Unipolar Mode (See Figure 7)<br>Bipolar Mode (See Figure 9) | | 0<br>$-V_{REF}$<br>$-V_{BOFS}$ | | $+V_{REF}$<br>0<br>$\lvert V_{REF}\rvert$<br>$-V_{BOFS}$ | V |
| **DIGITAL INPUTS (CS, ALE, CLK, A0-A2)** | | | | | | | |
| Logic HIGH Threshold | $V_{INH}$ | | | +2.4 | +2.0 | | V |
| Logic LOW Threshold | $V_{INL}$ | | | | +1.2 | +0.8 | V |
| Input Leakage Current | $I_{IN}$ | $V_{IN}$ = 0V or $V_{DD}$ | | | 0.01 | 1 | µA |
| Input Capacitance | $C_{IN}$ | (Note 5) | | | 4 | 5 | pF |

## ELECTRICAL CHARACTERISTICS (Continued)

($V_{DD}$ = +5V, $V_{REF}$ = -10V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise specified)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|---|
| **DIGITAL OUTPUTS (STAT, DB0-DB7)** | | | | | | |
| Output HIGH Voltage | $V_{OH}$ | $I_{SOURCE}$ = 40μA | 4.5 | 4.8 | | V |
| Output LOW Voltage | $V_{OL}$ | $I_{SINK}$ = 1.6mA | | 0.2 | 0.6 | V |
| Floating State Leakage | $I_{LKG}$ | DB0-DB7 | | 0.3 | 10 | μA |
| Floating State Capacitance | | DB0-DB7, $V_{OUT}$ = 0V to $V_{DD}$ | | 5 | 10 | pF |
| Output Code | | See Figure 5<br>See Figure 7<br>See Figure 9 | Unipolar Binary<br>Complementary Binary<br>Offset Binary | | | |
| **POWER REQUIREMENTS** | | | | | | |
| Supply Voltage | $V_{DD}$ | | +4.5 | +5.0 | +5.5 | V |
| **Supply Current** | $I_{DD}$ | MAX161, MX7581 Static<br>**MAX161 Dynamic ($f_{CLK}$ = 4.0MHz)**<br>MX7581 Dynamic ($f_{CLK}$ = 1.2MHz) | | 3<br>**3**<br>3 | 5<br>**5**<br>8 | mA |

**Note 1.** Typical offset temperature coefficient is **±25μV/°C for the MAX161** and ±150μV/°C for the MX7581.
**Note 2.** Gain error is measured after offset calibration. Maximum full scale change for any channel from +25°C to $T_{MIN}$ or $T_{MAX}$ is ±2LSBs.
**Note 3.** Typical change in $B_{OFS}$ gain from +25°C to $T_{MIN}$ or $T_{MAX}$ is ±2LSBs.
**Note 4.** $R_{BOFS}/R_{AIN}$ mismatch causes transfer function rotation about positive full scale. The effect is an offset and a gain term when using the circuits of Figure 7 and 9.
**Note 5.** Guaranteed but not 100% tested.

## TIMING CHARACTERISTICS — MAX161 ($C_L$ = 100pF, See Figure 1)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **ALE Pulse Width** | $t_H$ | **50** | **35** | | **ns** |
| **Address Valid to Latch Set-Up Time** | $t_{ALS}$ | **45** | **30** | | **ns** |
| **Address Valid to Latch Hold Time** | $t_{ALH}$ | **10** | **0** | | **ns** |
| **Address Latch to $\overline{CS}$ Set-Up Time** | $t_{LCS}$ | **10** | **0** | | **ns** |
| **$\overline{CS}$ to Output Propagation Delay** | $t_{ACC}$ | | **125** | **200** | **ns** |
| **$\overline{CS}$ Pulse Width** | $t_{CW}$ | **250** | **175** | | **ns** |
| **$\overline{CS}$ to Output Float Propagation Delay** | $t_{CF}$ | | **30** | **50** | **ns** |
| **$\overline{CS}$ to Low Impedance Bus** | $t_{CLZ}$ | | **70** | **100** | **ns** |
| **Clock Frequency (Note 6)** | $f_{CLK}$ | | **6** | **4.0** | **MHz** |

## TIMING CHARACTERISTICS — MX7581 ($C_L$ = 100pF, See Figure 1)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| ALE Pulse Width | $t_H$ | 80 | 50 | | ns |
| Address Valid to Latch Set-Up Time | $t_{ALS}$ | 70 | 45 | | ns |
| Address Valid to Latch Hold Time | $t_{ALH}$ | 20 | 10 | | ns |
| Address Latch to $\overline{CS}$ Set-Up Time | $t_{LCS}$ | 20 | 10 | | ns |
| $\overline{CS}$ to Output Propagation Delay | $t_{ACC}$ | | 200 | 250 | ns |
| $\overline{CS}$ Pulse Width | $t_{CW}$ | 280 | 250 | | ns |
| $\overline{CS}$ to Output Float Propagation Delay | $t_{CF}$ | | 50 | 80 | ns |
| $\overline{CS}$ to Low Impedance Bus | $t_{CLZ}$ | | 100 | 150 | ns |
| Clock Frequency (Note 6) | $f_{CLK}$ | | 1.6 | 1.2 | MHz |

**Note 6.** Guaranteed conversion time for stated accuracy of 20μs/channel with 4.0MHz clock for MAX161, and 66.7μs/channel with 1.2MHz clock for the MX7581.

# CMOS 8-Bit 8-Channel Data Acquisition System

## Detailed Description

### Basic Operation

The MAX161 and MX7581 sequentially convert analog signals on 8 input channels into separate 8-bit data words. The data is continually updated in on-chip RAM, with each channel's conversion result assigned to a separate RAM address. Consequently, the conversion process is user transparent in that output data is read directly from RAM. The device can run directly from a microprocessor clock (6800 type systems) or control signal (ALE in 8085 type systems). A functional diagram of the MAX161 and MX7581 is shown on the front page.

### A/D Conversion

Internally, the conversion process is divided into 10 phases, each 8 clock periods long. In the first phase, the input multiplexer is decremented and the control logic is reset. $\overline{STAT}$ (pin 12) goes low for 8 clock cycles at the beginning of this period. ($\overline{STAT}$ also goes low for 72 clock periods after channel 1 is converted). The successive approximation A/D conversion then takes place during phases 2 through 9. Finally, data is loaded into RAM during phase 10.

A single channel conversion takes 80 input clock periods while a complete scan through all channels requires 640 clock periods. Internal start-up logic initializes the converter within 800 clock periods after power is applied.

## Digital Interface

### Channel Selection

Table 1 shows the truth table for channel selection. RAM locations are addressed by AO-A2. In systems with a multiplexed address/data bus, the address is latched by ALE (pin 16). Alternatively, when address and data busses are separate, the address latches can be made transparent by tying ALE HIGH.

**Table 1:**
**Channel Selection Truth Table**

| A2 | A1 | A0 | ALE | CHANNEL DATA TO BE READ |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | Channel 0 |
| 0 | 0 | 1 | 1 | Channel 1 |
| 0 | 1 | 0 | 1 | Channel 2 |
| 0 | 1 | 1 | 1 | Channel 3 |
| 1 | 0 | 0 | 1 | Channel 4 |
| 1 | 0 | 1 | 1 | Channel 5 |
| 1 | 1 | 0 | 1 | Channel 6 |
| 1 | 1 | 1 | 1 | Channel 7 |

### Timing And Control

Control timing for the MAX161 and MX7581 is shown in Figure 1. When CS (pin 13) is HIGH, the three-state data drivers are in their high impedance state. The drivers switch to the active state when $\overline{CS}$ goes LOW. Output data is valid after time $t_{ACC}$.

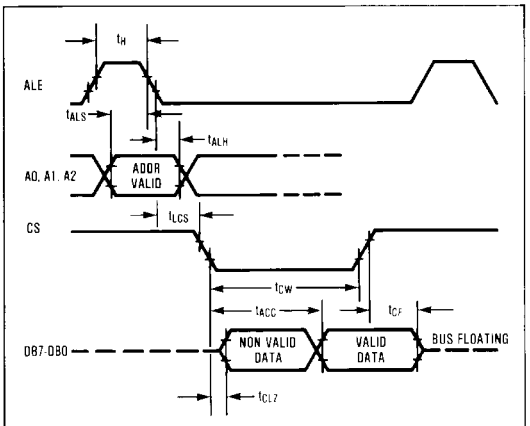



*Figure 1. Interface Timing Diagram*

### Data Read Operation

The MAX161 and MX7581 continuously scan and convert analog input signals without regard to the channel being selected for data output. The on-chip RAM and contention logic allow data to be read asynchronously with respect to the conversion process. The output data (RAM contents) is simply the most recent conversion result for the selected channel.

Automatic Interleaved DMA is provided by internal logic to ensure that memory updates do not take place when the memory is being addressed by a microprocessor. RAM is normally updated on a rising clock edge, 6 clock periods prior to $\overline{STAT}$ going LOW, provided $\overline{CS}$ is HIGH (i.e. data is not being read). If $\overline{CS}$ is LOW (read operation in progress), then the memory update is delayed by 3 clock periods. By delaying the update, data will not be written in RAM during a READ as long as $\overline{CS}$ is kept shorter than 3 clock periods. The possibility of a "contention" error with an asynchronous READ is therefore eliminated if $\overline{CS}$ is less than 3 clock periods long. Although asynchronous reading errors are eliminiated with this feature, it in no way restricts compatibility with other manufacturers' MX7581s.

### Channel Identification

In some real-time applications, it may be necessary to provide an interrupt signal when a particular channel receives updated data. To do this, the channel that is currently converting must be identified. $\overline{STAT}$ provides an identifying signal by staying low for an extended time (72 vs. 8 clock periods) when channel 0 is active (see Figure 2). Note that input channels are scanned in reverse order, i.e. AIN7,6...1,0.

A simple circuit for channel identification using $\overline{STAT}$ is shown in Figure 3. The time constant, RC, is chosen such that X2 ignores the short $\overline{STAT}$ pulses but responds to the wider (72 clock periods) pulse width occuring during channel 0 conversion. With a 1$\mu$s clock period, use 0.022$\mu$F for C and 1.8k$\Omega$ for R. An alternate means of channel identification uses the microprocessor to periodically interrogate the $\overline{STAT}$ output. A simple routine is shown in Figure 4.

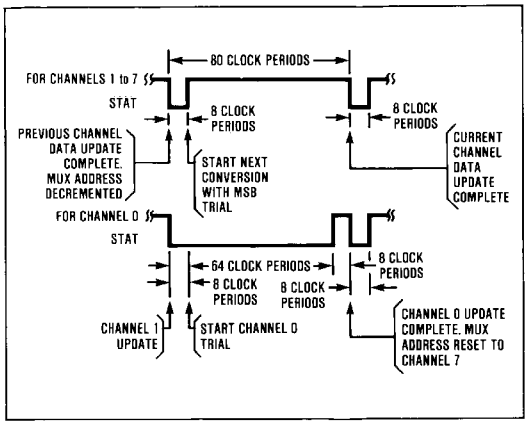



*Figure 2. $\overline{STAT}$ Timing Diagram*

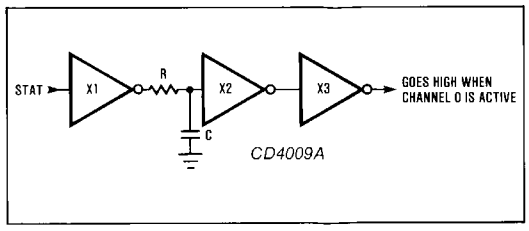



*Figure 3. Hardware Channel Identification*

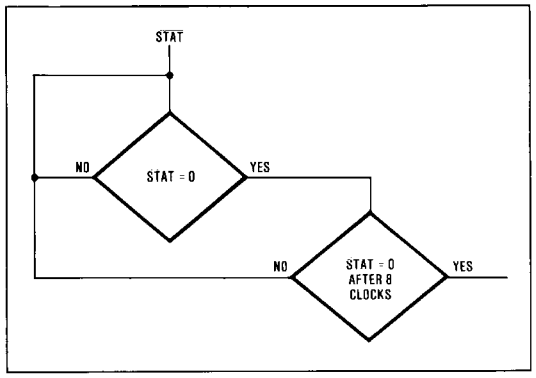



*Figure 4. Software Channel Identification*

## Operating Circuits

For the following circuits, the offset and gain adjustments shown in Figures 5, 7 and 9 are often not needed (The offset and gain error of the MAX161C are 1LSB and 2LSB respectively). In those cases, A1 and R1-R12 can be omitted. Note that in all cases where full scale is adjusted, offset must be trimmed first.

### Unipolar Binary Operation

Figures 5 and 6 show the analog circuit connections and the resulting transfer characteristic for basic unipolar operation (0 to +10V input). A -10V reference is connected to pin 10 through resistor R9 and a clock is connected to pin 15. Calibration is as follows:

#### Offset

Offset (zero error) is trimmed using the bipolar offset pin, $B_{OFS}$. Resistors R10-R12 form a voltage divider buffered by A1 which drives $B_{OFS}$. A0-A2 are taken LOW and latched using ALE so that channel 0 is continuously monitored. With AIN0 = +19.5mV (i.e. 1/2 LSB for 10V full scale) adjust R11 until DB7-DB1 are LOW and DB0(LSB) flickers. The offset of all channels is identical so one adjustment takes care of all eight inputs.

#### Full Scale

Apply +9.941V (F.S.-3/2LSB) to all inputs (AIN0-AIN7), then select one channel using A0-A2, and latch the address with ALE. Adjust trimmer RN of the selected input so that DB7-DB1 are HIGH and DB0 (LSB) flickers. Repeat for other channels.

# CMOS 8-Bit 8-Channel Data Acquisition System

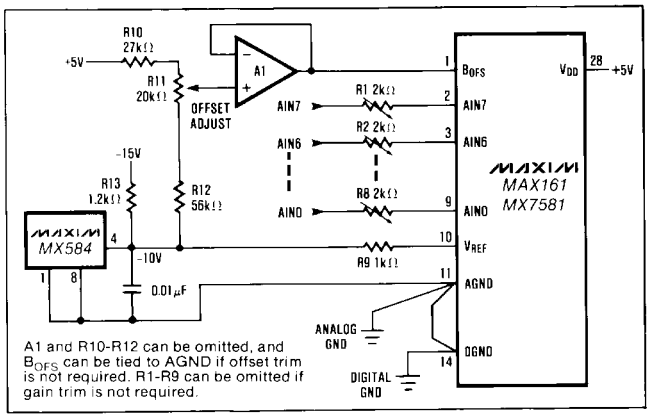



*Figure 5. Unipolar (0 to +10V) Operation*

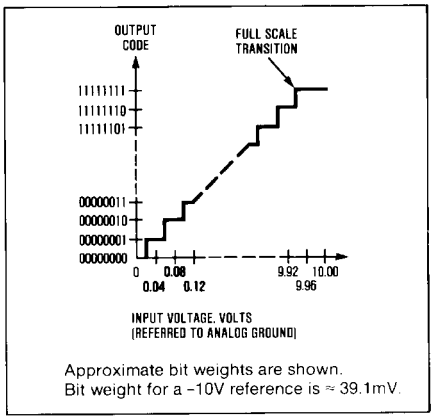



*Figure 6. Unipolar (0 to +10V) Transfer Characteristic*

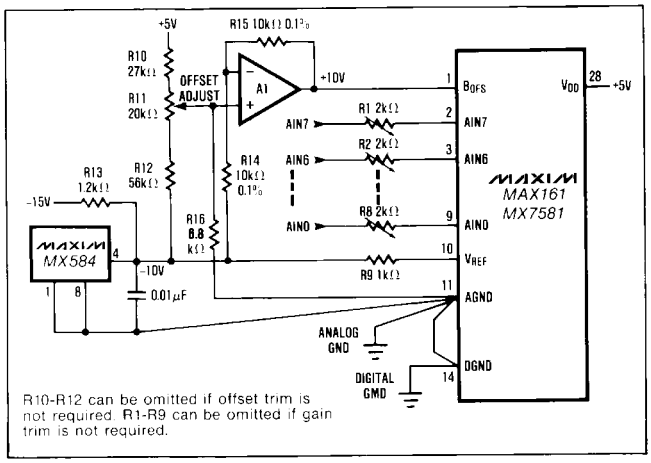



*Figure 7. Unipolar (0 to -10V) Operation*

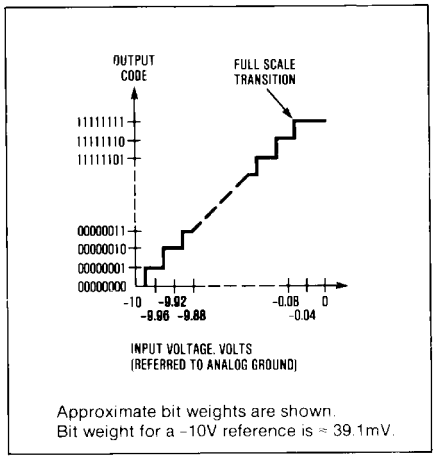



*Figure 8. Unipolar (0 to -10V) Transfer Characteristic*

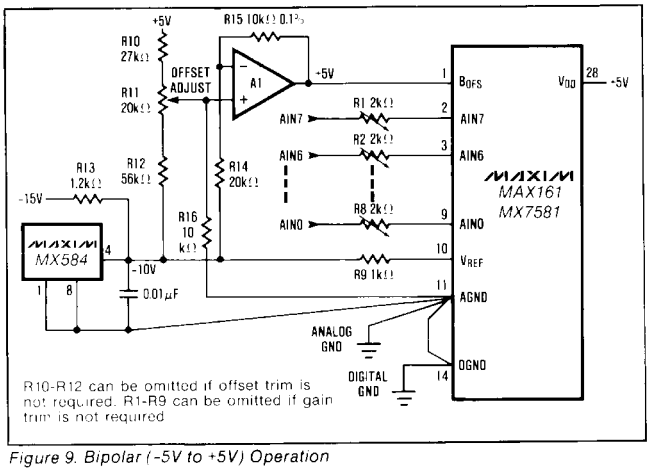



*Figure 9. Bipolar (-5V to +5V) Operation*

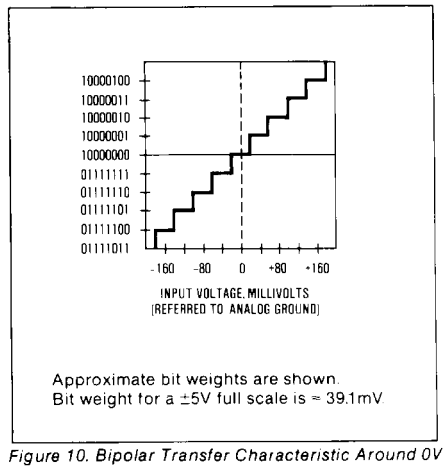



*Figure 10. Bipolar Transfer Characteristic Around 0V*

### Unipolar (Complimentary Binary) Operation

Figures 7 and 8 show the analog circuit connections and typical transfer characteristic for unipolar (0 to -10V input) complementary binary operation. Calibration is as follows:

#### Offset

A0-A2 are taken LOW and latched using ALE, activating channel 0. The offset voltage is identical for all channels so only one trim is needed. With AIN0 = -9.98V (i.e. -F.S.+1/2LSB), adjust R11 so that DB7-DB1 are LOW and DB0 (LSB) flickers.

#### Full Scale

Apply -58.6mV (3/2 LSB) to all channels (AIN0-AIN7) and select the required channel using A0-A2 and latch the address with ALE. Adjust trimmer RN of the selected channel until DB7-DB1 are HIGH and the DB0 (LSB) flickers. Repeat for other channels.

### Bipolar (Offset Binary) Operation

Figures 9 and 10 show the analog circuit connections and typical transfer characteristic for ±5V bipolar operation. Calibration is as follows:

#### Offset

A0-A2 are taken LOW and latched using ALE, selecting channel 0. The offset error is identical for all channels so only one trim is needed. With AIN0 = -4.980V (i.e. -F.S.+1/2LSB), adjust R11 so that DB1-DB7 are LOW and DB0 (LSB) flickers.

#### Full Scale

Apply +4.941V (+F.S.-3/2LSB) to all channels (AIN0-AIN7) and select the required channel using A0-A2 and latch the address with ALE. Adjust trimmer RN of the selected channel until DB1-DB7 are HIGH and DB0 (LSB) flickers. Apply -19.5mV to each gain trimmed channel. If the output code does not flicker between 01111111 and 1000000, repeat the calibration procedure.

## Application Hints

### Analog and Digital Ground

AGND and DGND should be connected together at the device to prevent the possibility of injecting noise into the A/D converter. In systems where the AGND-DGND connection is not local, connect clamp diodes (1N914 or equivalent) between the AGND and DGND pins.

VDD (pin 28) should be bypassed to AGND using a 10µF electrolytic and 0.1 µF ceramic capacitor. Lead lengths should be kept as short as possible.

### Logic Deglitching In µP Applications

Unspecified states on the address bus (due to different rise and fall times) can cause glitches at the $\overline{CS}$ pin, initiating unwanted reads. These glitches can be avoided by gating the address decoding logic with $\overline{RD}$ (8085A) or VMA (6800) as shown in Figures 11 and 12.

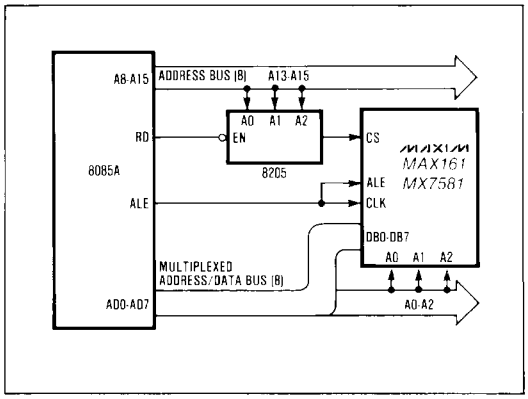



*Figure 11. 8085A Interface*

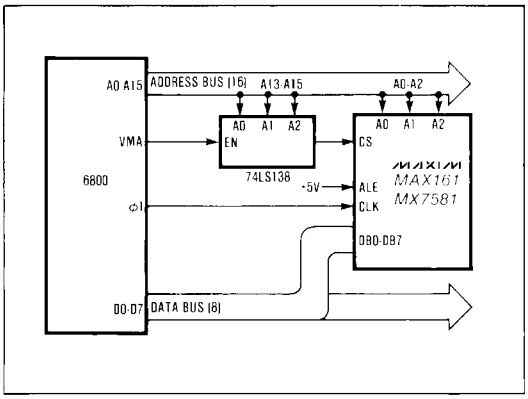



*Figure 12. 6800 Interface*

# CMOS 8-Bit 8-Channel Data Acquisition System

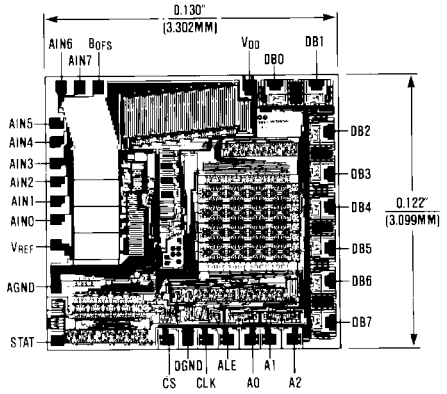
## Ordering Information (continued)

| PART | TEMP. RANGE | PACKAGE* | ERROR |
|---|---|---|---|
| MX7581JN | 0°C to +70°C | Plastic DIP | 1 7/8 LSB |
| MX7581KN | 0°C to +70°C | Plastic DIP | 3/4 LSB |
| MX7581LN | 0°C to +70°C | Plastic DIP | 1/2 LSB |
| MX7581JCWI | 0°C to +70°C | Small Outline | 1 7/8 LSB |
| MX7581KCWI | 0°C to +70°C | Small Outline | 3/4 LSB |
| MX7581LCWI | 0°C to +70°C | Small Outline | 1/2 LSB |
| MX7581J/D | 0°C to +70°C | Dice | 1 7/8 LSB |
| MX7581AD | -25°C to +85°C | Ceramic | 1 7/8 LSB |
| MX7581BD | -25°C to +85°C | Ceramic | 3/4 LSB |
| MX7581CD | -25°C to +85°C | Ceramic | 1/2 LSB |
| MX7581AQ | -25°C to +85°C | CERDIP** | 1 7/8 LSB |
| MX7581BQ | -25°C to +85°C | CERDIP** | 3/4 LSB |
| MX7581CQ | -25°C to +85°C | CERDIP** | 1/2 LSB |
| MX7581SQ | -55°C to +125°C | CERDIP** | 1 7/8 LSB |
| MX7581TQ | -55°C to +125°C | CERDIP** | 3/4 LSB |
| MX7581UQ | -55°C to +125°C | CERDIP** | 1/2 LSB |

* *All devices — 28 lead packages*

** *Maxim reserves the right to ship Ceramic Packages in lieu of CERDIP Packages.*

## Chip Topography



# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

MAX161BEWI+ MAX161BEWI+T MAX161CEWI+T MX7581JCWI+ MX7581JCWI+T MAX161CCWI+T MAX161AEPI+ MAX161BCPI+ MAX161BEPI+ MX7581JN+ MX7581KN+