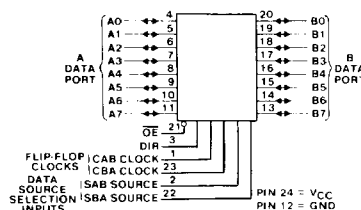


CD54HC648/3A
CD54HCT648/3A

**Octal Bus Transceiver/Register,
3-State, Non-Inverting**

The RCA CD54HC648 and CD54HCT648 are octal bus transceivers/registers with 3-state non-inverting outputs. These devices are bus transceivers with D-type flip-flops which act as internal storage registers. Data on the A bus or the B bus can be clocked into the registers on the LOW-to-HIGH transition of either CAB or CBA clock inputs. Output enable (OE) and direction (DIR) inputs control the transceiver functions. Data present at the high impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The direction control determines which data bus will receive data when the output enable (OE) is LOW. In the high impedance mode (output enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the direction (DIR) and output enable (OE) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.



FUNCTIONAL DIAGRAM

Package Specifications

See Section 11, Fig. 15

Static Electrical Characteristics (Limits with black dots (•) are tested 100%) — Bus Type

| CHARACTERISTICS | TEST CONDITIONS | | | | | | | | UNITS | |
|---|-----------------|----------------|----------------|------------------------|------------------------------------|------------------------------------|----------|-------|-------|----|
| | HC/HCT | | | | V _{IN} | | LIMITS | | | |
| | V _{DD} | V _O | I _O | V _{CC} or GND | V _{IL} or V _{IH} | V _{IL} or V _{IH} | MIN. | MAX. | | |
| Output High (Source) Current I _{OH} Min. - TTL Load | 25°C | 4.5 | 3.98 | — | — | 0, 4.5 | 0, 4.5 | -6• | — | mA |
| | -55°C | 4.5 | 3.70 | — | — | 0, 4.5 | 0, 4.5 | -6• | — | |
| | +125°C | 4.5 | 3.70 | — | — | 0, 4.5 | 0, 4.5 | -6• | — | |
| Output Low (Sink) Current I _{OL} Min. - TTL Load | 25°C | 4.5 | 0.26 | — | — | 0, 4.5 | 0, 4.5 | 6• | — | |
| | -55°C | 4.5 | 0.40 | — | — | 0, 4.5 | 0, 4.5 | 6• | — | |
| | +125°C | 4.5 | 0.40 | — | — | 0, 4.5 | 0, 4.5 | 6• | — | |
| High Level Output Voltage V _{OH} - TTL Load | 25°C | 4.5 | — | -6 | — | 1.35, 3.15 | 0.8, 2.0 | 3.98• | — | V |
| | -55°C | 4.5 | — | -6 | — | 1.35, 3.15 | 0.8, 2.0 | 3.70• | — | |
| | +125°C | 4.5 | — | -6 | — | 1.35, 3.15 | 0.8, 2.0 | 3.70• | — | |
| Low Level Output Voltage V _{OL} - TTL Load | 25°C | 4.5 | — | 6 | — | 1.35, 3.15 | 0.8, 2.0 | — | 0.26• | |
| | -55°C | 4.5 | — | 6 | — | 1.35, 3.15 | 0.8, 2.0 | — | 0.40• | |
| | +125°C | 4.5 | — | 6 | — | 1.35, 3.15 | 0.8, 2.0 | — | 0.40• | |
| Quiescent Device Current I _{CC} | 25°C | 6 | — | — | 6, 0 | — | — | — | 8• | μA |
| | -55°C | 6 | — | — | 6, 0 | — | — | — | 160• | |
| | +125°C | 6 | — | — | 6, 0 | — | — | — | 160• | |

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

HCT INPUT LOADING TABLE

| INPUT | UNIT LOAD* |
|---------------------|------------|
| OE | 1.3 |
| DIR | 0.75 |
| Clock A → B, B → A | 0.6 |
| Select A, Select B | 0.45 |
| Inputs A0-A7, B0-B7 | 0.3 |

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

CD54HC648/3A CD54HCT648/3A

Switching Speed (Limits with black dots (•) are tested 100%.)

SWITCHING CHARACTERISTICS ($C_L = 50$ pF, Input $t_r, t_f = 6$ ns)

| CHARACTERISTIC | SYMBOL | V_{CC} V | 25°C | | | | -55°C to +125°C | | | | UNITS |
|-------------------------------------|-----------|---------------|------|------|------|------|-----------------|------|-------|------|-------|
| | | | HC | | HCT | | 54HC | | 54HCT | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| Propagation Delay | | 2 | — | 240 | — | — | — | 360 | — | — | ns |
| Store A data to B bus | | 4.5 | — | 48• | — | 54• | — | 72• | — | 81• | |
| Store \bar{B} data to A bus | | 6 | — | 41 | — | — | — | 61 | — | — | |
| \bar{A} data to B bus | t_{PLH} | 2 | — | 150 | — | — | — | 225 | — | — | |
| \bar{B} data to A bus | | 4.5 | — | 30• | — | 37• | — | 45• | — | 56• | |
| Select to Data | t_{PHL} | 6 | — | 26 | — | — | — | 38 | — | — | |
| | | 2 | — | 190 | — | — | — | 285 | — | — | |
| 3-State Disabling Time | t_{PLZ} | 4.5 | — | 38• | — | 46• | — | 57• | — | 69• | |
| | | 6 | — | 32 | — | — | — | 48 | — | — | |
| Bus to Output or Register to Output | t_{PHZ} | 2 | — | 175 | — | — | — | 265 | — | — | |
| 3-State Enabling Time | t_{PZL} | 4.5 | — | 35• | — | 35• | — | 53• | — | 53• | |
| | | 6 | — | 30 | — | — | — | 45 | — | — | |
| Bus to Output or Register to Output | t_{PZH} | 2 | — | 175 | — | — | — | 265 | — | — | |
| Output Transition Time | t_{LH} | 4.5 | — | 60 | — | — | — | 90 | — | — | |
| | | 6 | — | 12 | — | 12 | — | 18 | — | 18 | |
| Time | t_{HL} | 2 | — | 10 | — | — | — | 15 | — | — | |
| Input Capacitance | C_I | — | — | 10 | — | 10 | — | 10 | — | 10 | pF |
| 3-State Output Capacitance | C_O | — | — | 20 | — | 20 | — | 20 | — | 20 | |

5

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

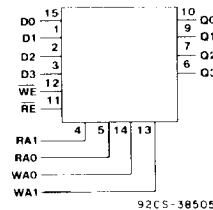
| Static | STATIC BURN-IN I | | | STATIC BURN-IN II | | |
|---------------|------------------|--------------|-------------------|-------------------|----------------------------------|---------------|
| | OPEN | GROUND | V_{CC} (6V) | OPEN | GROUND | V_{CC} (6V) |
| CD54HC/HCT648 | 4-11 | 1-3,12-23 | 24 | — | 12 | 1-11,13-24 |
| Dynamic | OPEN | GROUND | 1/2 V_{CC} (3V) | V_{CC} (6V) | OSCILLATOR 50 kHz 25 kHz | |
| CD54HC/HCT648 | — | 1-3,12,21,22 | 4-11 | 24 | 23 | 13-20 |

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

4 x 4 Register File, 3-State

CD54HC670/3A CD54HCT670/3A

The RCA CD54HC670 and CD54HCT670 are 16-bit register files organized as 4 words x 4 bits each. Read and write address and enable inputs allow simultaneous writing into one location while reading another. Four data inputs are provided to store the 4-bit word. The write address inputs (WA0 and WA1) determine the location of the stored word in the register. When write enable (WE) is low the word is entered into the address location and it remains transparent to the data. The outputs will reflect the true form of the input data. When (WE) is high data and address inputs are inhibited. Data acquisition from the four registers is made possible by the read address inputs (RA1 and RA0). The addressed word appears at the output when the read enable (RE) is low. The output is in the high impedance state when the (RE) is high. Outputs can be tied together to increase the word capacity to 512 x 4 bits.



FUNCTIONAL DIAGRAM

Package Specifications

See Section 11, Fig. 11