PRELIMINARY

The MACH® 5 Value Plus™ Family

Fifth Generation MACH Architecture

Advanced
Micro
Devices

DISTINCTIVE CHARACTERISTICS

- **Fifth generation MACH architecture**
  - — 100% routable
  - — Pin-out retention
  - — Four power/speed options per block for maximum performance and lowest power
  - — Advanced synchronous and asynchronous clocking
  - — Asynchronous product- or sum-term reset
  - — Functions of up to 32 product terms
  - — Fixed, predictable delays
- **Fast**
  - — 7.5 ns pin-to-pin delays
  - — 125 MHz counter frequencies
- **High densities**
  - — 128 to 512 macrocells
  - — 16 to 64 output enables
  - — Multiple density options for each package
- **System design considerations**
  - — PCI compliant (-7/-10/-12)
  - — IEEE 1149.1 (JTAG) compliant
  - — In-system programmable
  - — Both 5-V and JEDEC-compliant 3.3-V versions
  - — 3.3-V devices accept 5-V inputs (safe for mixed voltage)
  - — 5-V devices will not overdrive 3-V inputs (safe for mixed voltage)
  - — Safe for hot socketing
  - — Bus-Friendly™ I/Os
  - — Individual output slew rate control
  - — Programmable security fuse
- **Leading-edge process technology**
  - — 0.35 and 0.5 micron (L_{eff}) processes
- **Supported by AMD software**
  - — DSL design entry ports to universal tools
  - — Low-cost entry-level tool
  - — Windows GUI interface
  - — Auto device selection
  - — Multiple device partitioning
- **Extensive universal tool support**
  - — Cadence
  - — Synario
  - — Mentor Graphics
  - — MINC
  - — Aldec
  - — Viewlogic
  - — Microsim
  - — Synopsys/Logic Modeling
- **Third-party programming support**

PRODUCT SELECTOR GUIDE

Device	Macro Cells	I/O Options	Speeds (t_{PD})	Packages
M5-128 M5LV-128	128	68, 104, 120	7, 10, 12, 15 COM 10, 12, 15, 20 IND	PQFP, TQFP
M5-192 M5LV-192	192	68, 104, 120, 160	7, 10, 12, 15 COM 10, 12, 15, 20 IND	PQFP, TQFP
M5-256 M5LV-256	256	68, 104, 120, 160	7, 10, 12, 15 COM 10, 12, 15, 20 IND	PQFP, TQFP
M5-320 M5LV-320	320	120, 160, 184, 192	7, 10, 12, 15 COM 10, 12, 15, 20 IND	PQFP, BGA
M5-384 M5LV-384	384	120, 160, 184, 192	7, 10, 12, 15 COM 10, 12, 15, 20 IND	PQFP, BGA
M5-512 M5LV-512	512	120, 160, 184, 192, 256	7, 10, 12, 15 COM 10, 12, 15, 20 IND	PQFP, BGA

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GENERAL DESCRIPTION

The MACH 5 Value Plus family consists of a broad range of high-density, high-performance, and low-power complex programmable logic devices (CPLDs) with features such as in-system programmability, JTAG testability, and advanced clocking options. These fifth-generation MACH devices have advanced power management options which allow designers to incrementally reduce power. Both the 3.3-V and 5-V device versions are safe for mixed voltage design, are safe for hot-socketing, and the 7.5-, 10-, and 12-ns devices are compliant with the *PCI Local Bus Specification*. The MACH Value Plus family is manufactured in AMD's own state-of-the-art fabrication facilities on 0.5 and 0.35 micron L_{eff} EECMOS process technology.

All devices are available with pin-to-pin delays as fast as 7.5 ns and possess the density required for full system logic integration. The largest device, the M5-512, has 512 macrocells. MACH 5's unique hierarchical architecture is ideal for PAL device integration and a wide range of other applications including high-speed computing, low-power applications, communications, and embedded control.

Several features have been incorporated to accommodate changing designs and fixed pinout. The routing resources include a logic switch matrix which reassigns logic to macrocells. Often designers may need to incorporate additional logic in their designs without moving to a larger package. The MACH 5 Macrocell/Package options are designed for such an occurrence (Table 2). Any two MACH 5 logic densities in the same package have the same pinout to eliminate wasted logic and to provide a migration path when more logic is required.

MACH designs can be implemented using industry-standard, universal design tools. AMD and universal fitter company, MINC, Inc., have developed a strategic partnership that ensures timely universal software support for the MACH 5 Value Plus. MINC develops back-end PLD software for nearly every major industry-standard PLD and board-level design tool. This back-end software fits a design into a device and creates a JEDEC file. Schematic capture, boolean, state machine, VHDL, and Verilog design entry and simulation are features of the front-end tool. MINC produces the back-end for PC tools such as Microsim Design Center, Viewlogic Synario, and others. MINC also supplies the back-end for workstation tools from Cadence, Mentor Graphics, Synopsys, and Viewlogic. Thus, the AMD-MINC partnership provides timely, accurate, and quality support for MACH devices in almost every design environment. Please see AMD's Universal Tools brochure for more information.

Table 1. MACH Value Plus Device Features

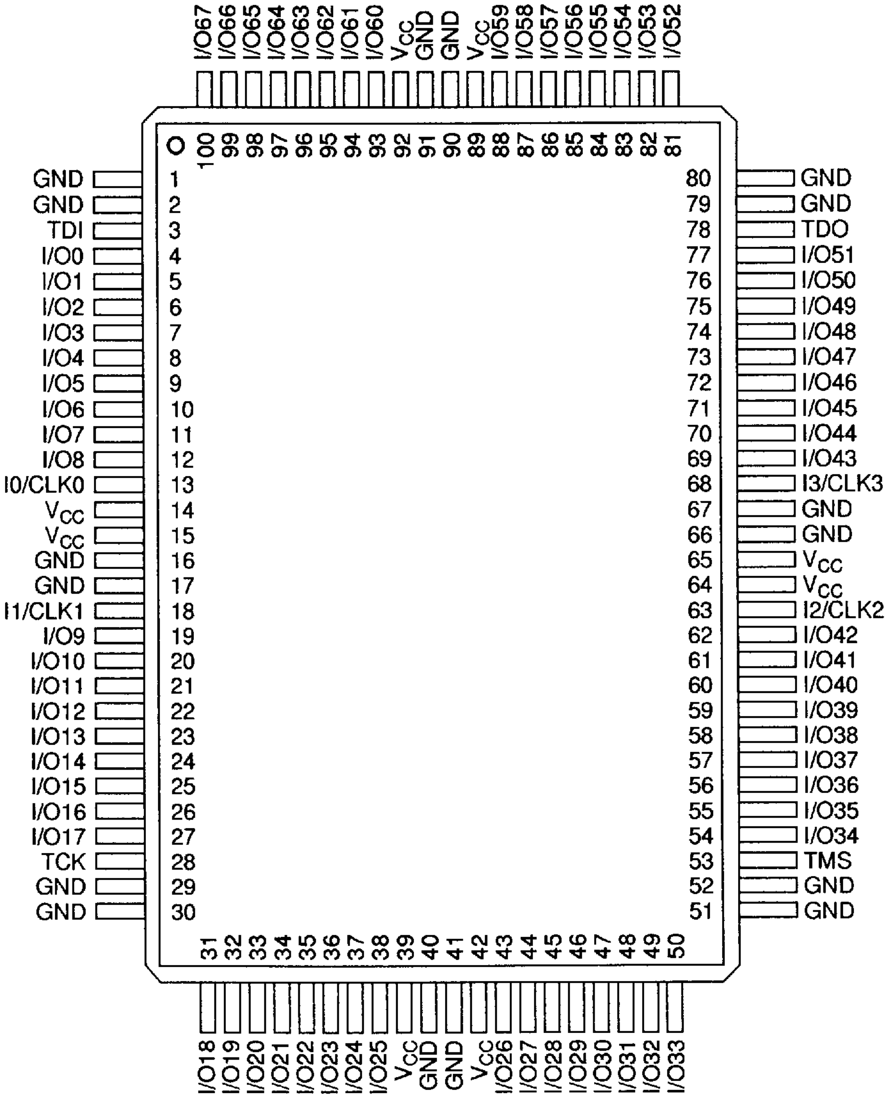
Feature	M5-128 M5LV-128	M5-192 M5LV-192	M5-256 M5LV-256	M5-320 M5LV-320	M5-384 M5LV-384	M5-512 M5LV-512
PLD Gates	5000	7500	10000	12000	15000	20000
Usable Gates	2500	3750	5000	6000	7500	10000
Macrocells	128	192	256	320	384	512
Maximum I/0	120	160	160	192	192	256
Power (mA)	25	40	50	60	75	100
t_{PD} (ns)	7.5	7.5	7.5	7.5	7.5	7.5
t_{SU} (ns)	4	4	4	4	4	4
t_{CO} (ns)	7.5	7.5	7.5	7.5	7.5	7.5
f_{CNT} (MHz)	125	125	125	125	125	125
JTAG Compliant	Yes	Yes	Yes	Yes	Yes	Yes
PCI Compliant	-7/-10/-12	-7/-10/-12	-7/-10/-12	-7/-10/-12	-7/-10/-12	-7/-10/-12

Table 2. Package and Device Options

Package	M5-128 M5LV-128	M5-192 M5LV-192	M5-256 M5LV-256	M5-320 M5LV-320	M5-384 M5LV-384	M5-512 M5LV-512
100 PQFP (68 I/O)	X	X	X			
100 TQFP (68 I/O)	X	X	X			
144 PQFP (104 I/O)	X	X	X			
160 PQFP (120 I/O)	X	X	X	X	X	X
208 PQFP (160 I/O)		X	X	X	X	X
240 PQFP (184 I/O)				X	X	X
256 BGA (192 I/O)				X	X	X
352 BGA (256 I/O)						X

CONNECTION DIAGRAMS

Top View



100 PQFP

M5-128/68, M5LV-128/68

M5-192/68, M5LV-192/68

M5-256/68, M5LV-256/68

PIN DESIGNATIONS

CLK = Clock

GND = Ground

I = Input

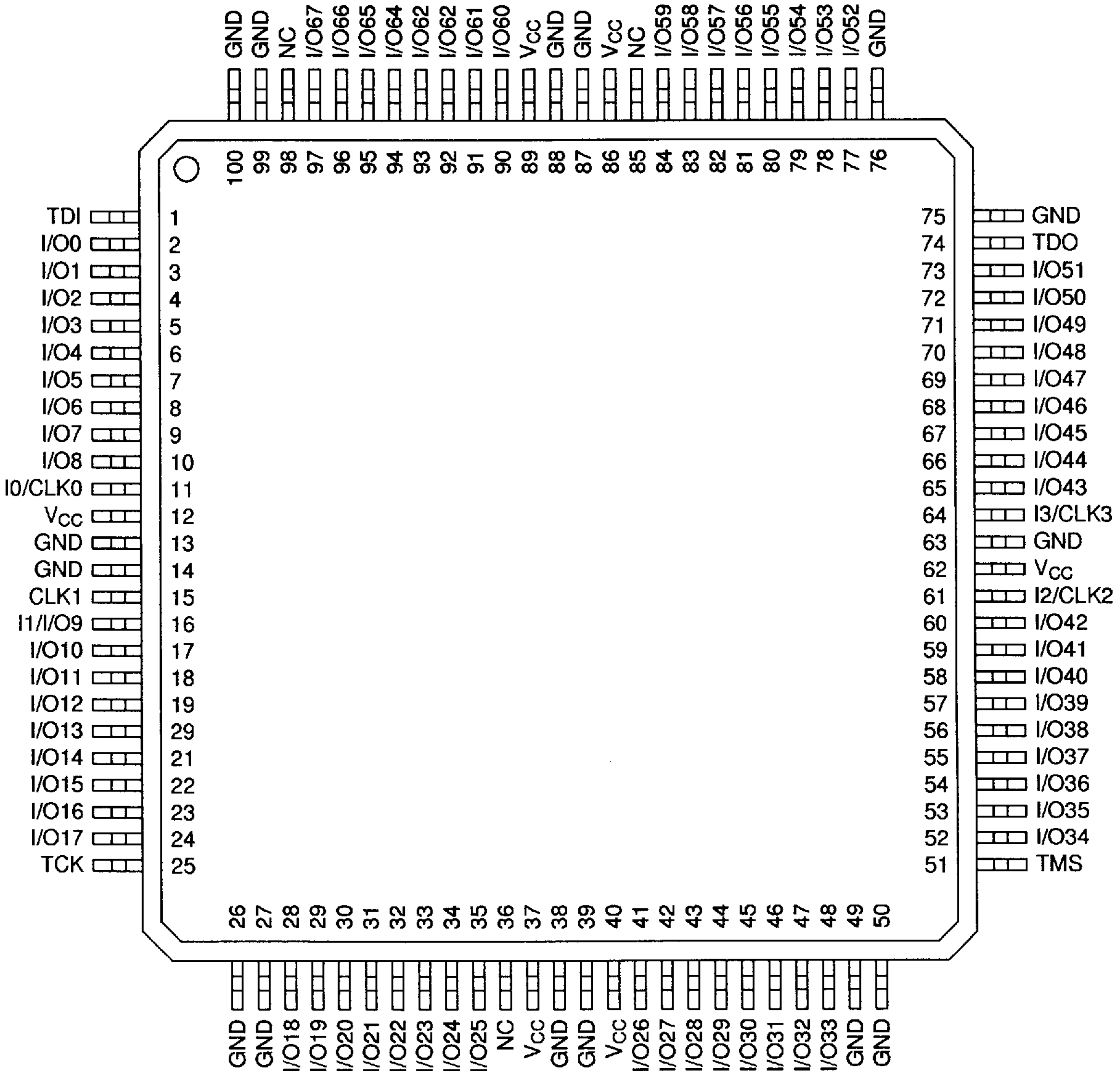
I/O = Input/Output

NC = No Connect

V_{CC} = Supply Voltage

CONNECTION DIAGRAMS (continued)

Top View



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100 TQFP

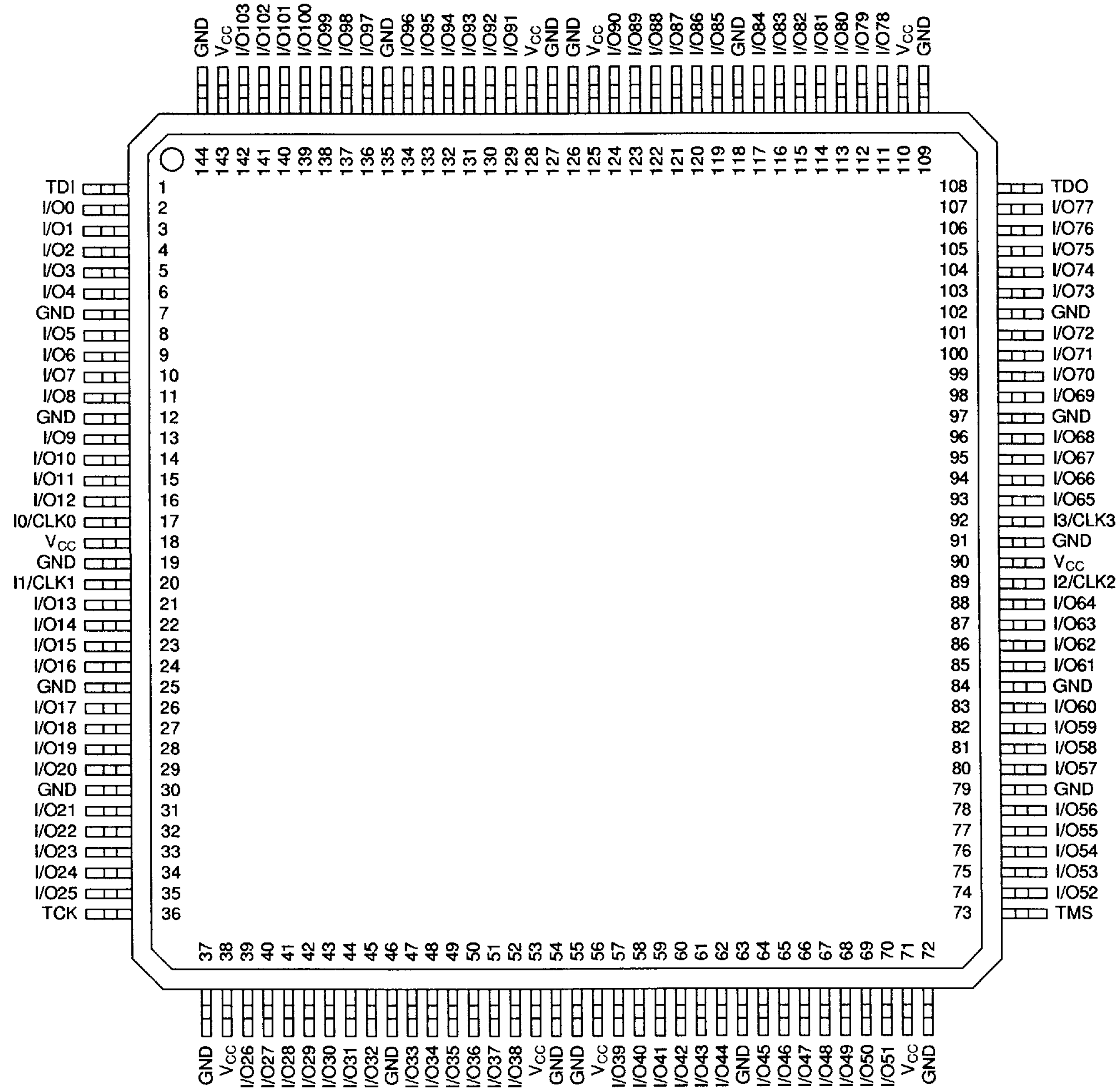
M5-128/68, M5LV-128/68

M5-192/68, M5LV-192/68

M5-256/68, M5LV-256/68

CONNECTION DIAGRAMS (continued)

Top View



144 PQFP

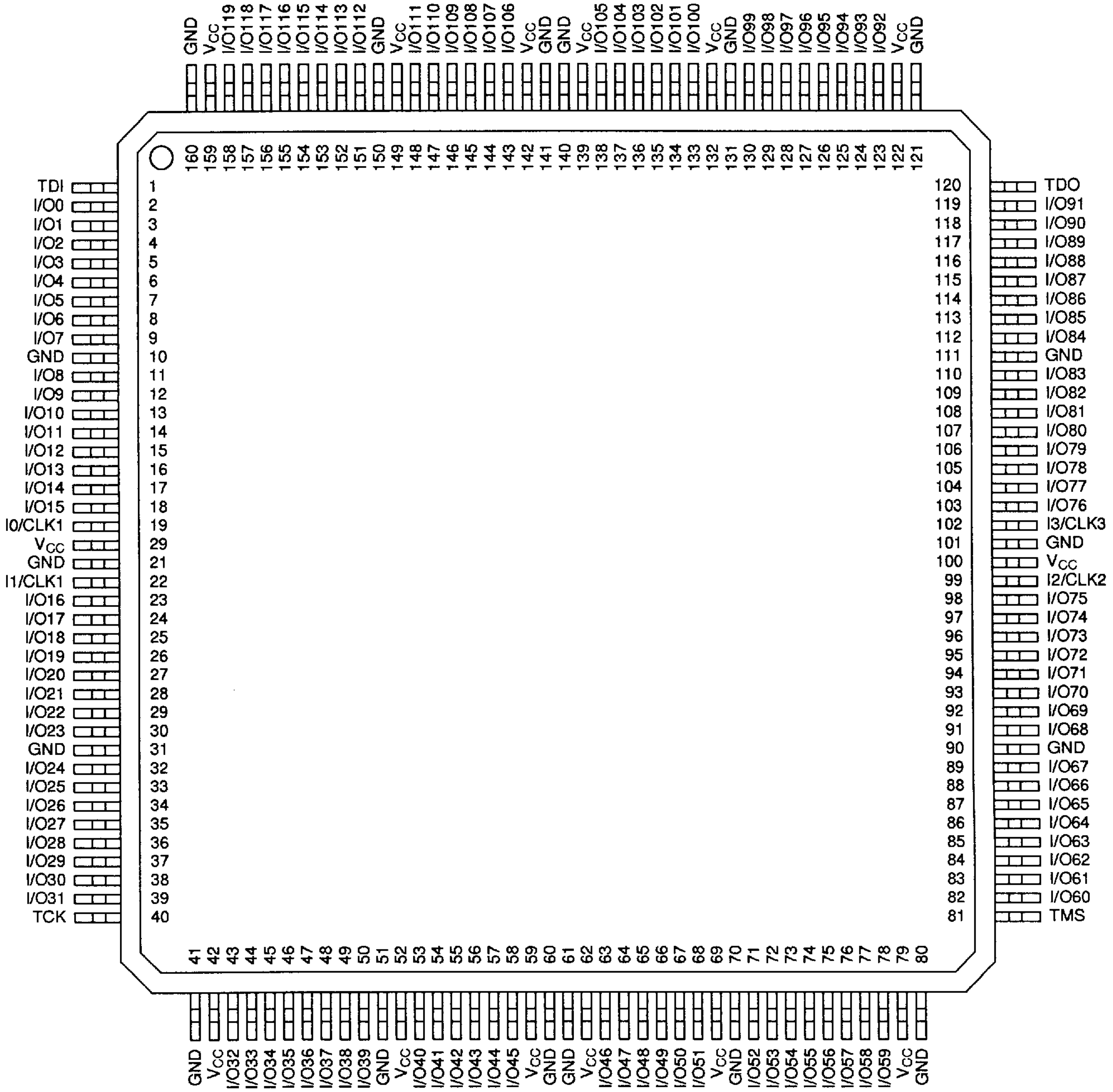
M5-128/104, M5LV-128/104

M5-192/104, M5LV-192/104

M5-256/104, M5LV-256/104

CONNECTION DIAGRAMS (continued)

Top View



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160 PQFP

M5-128/120, M5LV-128/120

M5-192/120, M5LV-192/120

M5-256/120, M5LV-256/120

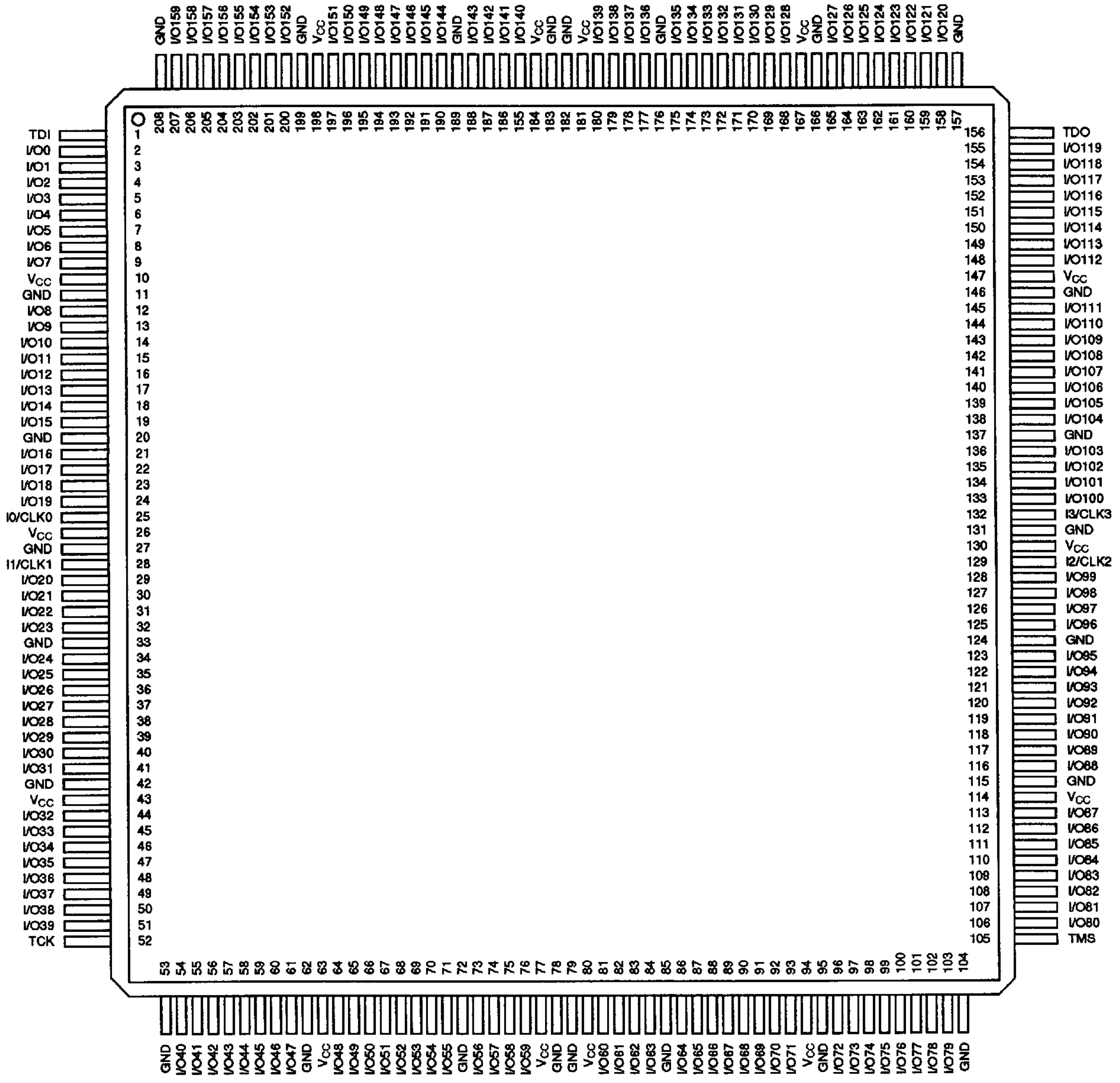
M5-320/120, M5LV-320/120

M5-384/120, M5LV-384/120

M5-512/120, M5LV-512/120

CONNECTION DIAGRAMS (continued)

Top View



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208 PQFP

M5-192/120, M5LV-192/120

M5-256/120, M5LV-256/120

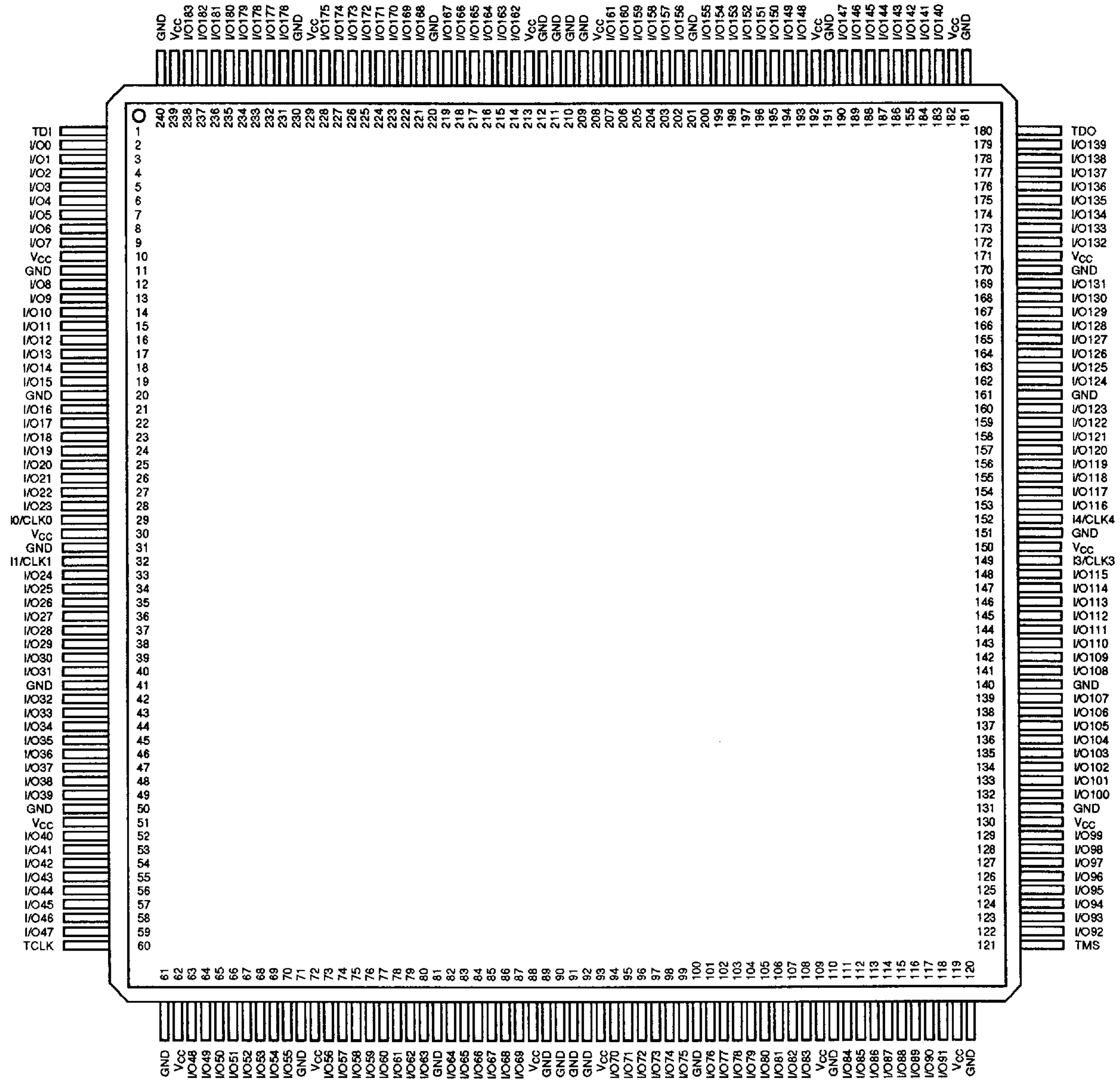
M5-320/120, M5LV-320/120

M5-384/120, M5LV-384/120

M5-512/120, M5LV-512/120

CONNECTION DIAGRAMS (continued)

Top View



240 PQFP

M5-320/184, M5LV-320/184

M5-384/184, M5LV-384/184

M5-512/184, M5LV-512/184

CONNECTION DIAGRAMS (continued)

Bottom View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y
1	GND	GND	I/O181	I/O182	I/O183	GND	I/O184	GND	I/O185	I/O186	GND	I/O187	GND	I/O188	GND	I/O189	I/O190	I/O191	GND	GND
2	GND	I/O164	I/O165	I/O166	I/O167	I/O168	I/O169	I/O170	I/O171	I3/CLK3	I2/CLK2	I/O172	I/O173	I/O174	I/O175	I/O176	I/O177	I/O178	I/O179	I/O180
3	GND	I/O148	V_{CC}	I/O149	I/O150	I/O151	I/O152	I/O153	I/O154	I/O155	I/O156	I/O157	I/O158	I/O159	I/O160	I/O161	I/O162	V_{CC}	I/O163	GND
4	I/O134	I/O135	I/O136	V_{CC}	TDO	I/O137	V_{CC}	I/O138	I/O139	I/O140	I/O141	I/O142	V_{CC}	I/O143	I/O144	TMS	V_{CC}	I/O145	I/O146	I/O147
5	I/O128	I/O129	I/O130	V_{CC}													V_{CC}	I/O131	I/O132	I/O133
6	GND	I/O122	I/O123	I/O124													I/O125	I/O126	I/O127	GND
7	I/O116	I/O117	I/O118	V_{CC}													V_{CC}	I/O119	I/O120	I/O121
8	I/O108	I/O109	I/O110	I/O111													I/O112	I/O113	I/O114	I/O115
9	GND	I/O102	I/O103	I/O104													I/O105	I/O106	I/O107	GND
10	GND	I/O96	I/O97	I/O98													I/O99	I/O100	I/O101	GND
11	GND	I/O90	I/O91	I/O92													I/O93	I/O94	I/O95	GND
12	GND	I/O84	I/O85	I/O86													I/O87	I/O88	I/O89	GND
13	I/O76	I/O77	I/O78	I/O79													I/O80	I/O81	I/O82	I/O83
14	I/O70	I/O71	I/O72	V_{CC}													V_{CC}	I/O73	I/O74	I/O75
15	GND	I/O64	I/O65	I/O66													I/O67	I/O68	I/O69	GND
16	I/O58	I/O59	I/O60	V_{CC}													V_{CC}	I/O61	I/O62	I/O63
17	I/O44	I/O45	I/O46	V_{CC}	TDI	I/O47	V_{CC}	I/O48	I/O49	I/O50	I/O51	I/O52	I/O53	V_{CC}	I/O54	TCK	V_{CC}	I/O55	I/O56	I/O57
18	GND	I/O28	V_{CC}	I/O29	I/O30	I/O31	I/O32	I/O33	I/O34	I/O35	I/O36	I/O37	I/O38	I/O39	I/O40	I/O41	I/O42	V_{CC}	I/O43	GND
19	I/O11	I/O12	I/O13	I/O14	I/O15	I/O16	I/O17	I/O18	I/O19	I0/CLK0	I1/CLK1	I/O20	I/O21	I/O22	I/O23	I/O24	I/O25	I/O26	I/O27	GND
20	GND	GND	I/O0	I/O1	I/O2	GND	I/O3	GND	I/O4	GND	I/O5	I/O6	GND	I/O7	GND	I/O8	I/O9	I/O10	GND	GND

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256 BGA

M5-320/192, M5LV-320/192

M5-384/192, M5LV-384/192

M5-512/192, M5LV-512/192

CONNECTION DIAGRAMS (continued)

Bottom View

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF
1	NC	NC	NC	GND	NC	I/O245	GND	I/O246	I/O247	GND	I/O248	I/O249	I3/CLK3	GND	I/O250	I/O251	I/O252	GND	I/O253	I/O254	GND	NC	I/O255	GND	NC	NC
2	NC	NC	NC	I/O224	I/O225	I/O226	I/O227	I/O228	I/O229	I/O230	I/O231	I/O232	I/O233	I/O234	I/O235	I/O236	I/O237	I/O238	I/O239	I/O240	I/O241	I/O242	I/O243	I/O244	GND	GND
3	GND	GND	NC	I/O205	I/O206	I/O207	I/O208	I/O209	I/O210	I2/CLK2	I/O211	I/O212	I/O213	I/O214	I/O215	I/O216	I/O217	I/O218	I/O219	I/O220	I/O221	I/O222	I/O223	TMS	NC	NC
4	NC	I/O188	NC	TDO	I/O189	I/O190	I/O191	V_{CC}	I/O192	V_{CC}	I/O193	I/O194	I/O195	V_{CC}	I/O196	I/O197	I/O198	V_{CC}	I/O199	V_{CC}	I/O200	I/O201	V_{CC}	I/O202	I/O203	I/O204
5	GND	I/O183	I/O184	V_{CC}																			I/O185	I/O186	I/O187	GND
6	NC	I/O176	I/O177	I/O178																			I/O179	I/O180	I/O181	I/O182
7	GND	I/O169	I/O170	I/O171																			I/O172	I/O173	I/O174	I/O175
8	I/O162	I/O163	I/O164	I/O165																			I/O166	I/O167	I/O168	NC
9	I/O156	I/O157	I/O158	I/O159																			V_{CC}	I/O160	I/O161	GND
10	GND	I/O150	I/O151	V_{CC}																			I/O152	I/O153	I/O154	I/O155
11	I/O142	I/O143	I/O144	I/O145																			I/O146	I/O147	I/O148	I/O149
12	I/O134	I/O135	I/O136	I/O137																			I/O138	I/O139	I/O140	I/O141
13	I/O128	I/O129	I/O130	I/O131																			V_{CC}	I/O132	I/O133	GND
14	GND	I/O122	I/O123	V_{CC}																			I/O124	I/O125	I/O126	I/O127
15	I/O114	I/O115	I/O116	I/O117																			I/O118	I/O119	I/O120	I/O121
16	NC	I/O107	I/O108	I/O109																			I/O110	I/O111	I/O112	I/O113
17	I/O101	I/O102	I/O103	I/O104																			V_{CC}	I/O105	I/O106	GND
18	GND	I/O95	I/O96	V_{CC}																			I/O97	I/O98	I/O99	I/O100
19	I/O87	I/O88	I/O89	I/O90																			I/O91	I/O92	I/O93	I/O94
20	I/O80	I/O81	I/O82	I/O83																			I/O84	I/O85	I/O86	GND
21	I/O73	I/O74	I/O75	I/O76																			I/O77	I/O78	I/O79	NC
22	GND	I/O68	I/O69	I/O70																			V_{CC}	I/O71	I/O72	GND
23	I/O51	I/O52	I/O53	V_{CC}	I/O54	I/O55	V_{CC}	I/O56	V_{CC}	I/O57	I/O58	I/O59	V_{CC}	I/O60	I/O61	I/O62	V_{CC}	I/O63	V_{CC}	I/O64	I/O65	I/O66	TCK	NC	I/O67	NC
24	NC	NC	TDI	I/O32	I/O33	I/O34	I/O35	I/O36	I/O37	I/O38	I/O39	I/O40	I0/CLK0	I/O41	I/O42	I/O43	I/O44	I/O45	I/O46	I/O47	I/O48	I/O49	I/O50	NC	GND	GND
25	GND	GND	I/O11	I/O12	I/O13	I/O14	I/O15	I/O16	I/O17	I/O18	I/O19	I/O20	I/O21	I/O22	I/O23	I/O24	I/O25	I/O26	I/O27	I/O28	I/O29	I/O30	I/O31	NC	NC	NC
26	NC	NC	GND	I/O0	NC	GND	I/O1	I/O2	GND	I/O3	I/O4	I/O5	GND	I1/CLK1	I/O6	I/O7	GND	I/O8	I/O9	GND	I/O10	NC	GND	NC	NC	NC

352 BGA

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M5-512/256, M5LV-512/256

ORDERING INFORMATION

MACH 5 COM -7.5, -10, -12, -15

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

M5- 512 /256 -7 A C

FAMILY TYPE
M5- = MACH 5 Value Plus (5-V V_{CC})

MACROCELL DENSITY
128 = 128 Macrocells
192 = 192 Macrocells
256 = 256 Macrocells
320 = 320 Macrocells
384 = 384 Macrocells
512 = 512 Macrocells

I/Os
/68 = 68 I/Os
/104 = 104 I/Os
/120 = 120 I/Os
/160 = 160 I/Os
/184 = 184 I/Os
/192 = 192 I/Os
/256 = 256 I/Os

OPTIONAL PROCESSING
Blank = Standard Processing

OPERATING CONDITIONS
C = Commercial (0°C to +70°C)

PACKAGE TYPE
Y = Plastic Quad Flat Pack (PQFP)
V = Thin Quad Flat Pack (TQFP)
A = Ball Grid Array (BGA)
H = Plastic Quad Flat Pack
with heat sink (PQFP)

SPEED
-7 = 7.5 ns t_{PD}
-10 = 10 ns t_{PD}
-12 = 12 ns t_{PD}
-15 = 15 ns t_{PD}

Valid Combinations		
M5-128/68	-7, -10, -12, -15	YC, VC
M5-128/104		YC
M5-128/120		YC, HC
M5-192/68		YC, VC
M5-192/104		YC
M5-192/120		YC, HC
M5-192/160		HC
M5-256/68		YC, VC
M5-256/104		YC
M5-256/120		YC, HC
M5-256/160		HC

Valid Combinations		
M5-320/120	-7, -10, -12, -15	HC
M5-320/160		HC
M5-320/184		HC
M5-320/192		AC
M5-384/120		HC
M5-384/160		HC
M5-384/184		HC
M5-384/192		AC
M5-512/120		HC
M5-512/160		HC
M5-512/184		HC
M5-512/192		AC
M5-512/256		AC

Device Marking

Actual device marking differs from the ordering part number (OPN). "MACH 5" is marked on a device wherever "M5-" is used in the OPN.

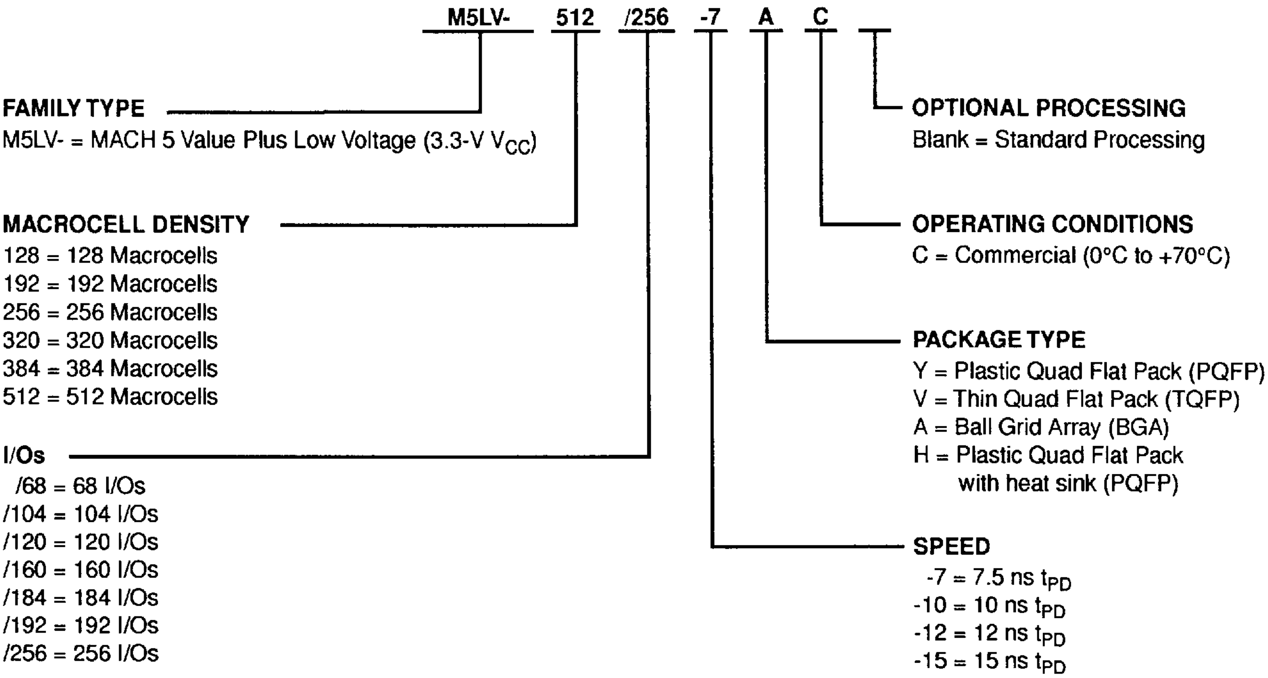
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

MACH 5 LV COM -7.5, -10, -12, -15

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



FAMILY TYPE
M5LV- = MACH 5 Value Plus Low Voltage (3.3-V V_{CC})

MACROCELL DENSITY
128 = 128 Macrocells
192 = 192 Macrocells
256 = 256 Macrocells
320 = 320 Macrocells
384 = 384 Macrocells
512 = 512 Macrocells

I/Os
/68 = 68 I/Os
/104 = 104 I/Os
/120 = 120 I/Os
/160 = 160 I/Os
/184 = 184 I/Os
/192 = 192 I/Os
/256 = 256 I/Os

OPTIONAL PROCESSING
Blank = Standard Processing

OPERATING CONDITIONS
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PACKAGE TYPE
Y = Plastic Quad Flat Pack (PQFP)
V = Thin Quad Flat Pack (TQFP)
A = Ball Grid Array (BGA)
H = Plastic Quad Flat Pack with heat sink (PQFP)

SPEED
-7 = 7.5 ns t_{PD}
-10 = 10 ns t_{PD}
-12 = 12 ns t_{PD}
-15 = 15 ns t_{PD}

Valid Combinations		
M5LV-128/68	-7, -10, -12, -15	YC, VC
M5LV-128/104		YC
M5LV-128/120		YC, HC
M5LV-192/68		YC, VC
M5LV-192/104		YC
M5LV-192/120		YC, HC
M5LV-192/160		HC
M5LV-256/68		YC, VC
M5LV-256/104		YC
M5LV-256/120		YC, HC
M5LV-256/160		HC

Device Marking

Actual device marking differs from the ordering part number (OPN). "MACH 5" is marked on a device wherever "M5-" is used in the OPN.

Valid Combinations		
M5LV-320/120	-7, -10, -12, -15	HC
M5LV-320/160		HC
M5LV-320/184		HC
M5LV-320/192		AC
M5LV-384/120		HC
M5LV-384/160		HC
M5LV-384/184		HC
M5LV-384/192		AC
M5LV-512/120		HC
M5LV-512/160		HC
M5LV-512/184		HC
M5LV-512/192		AC
M5LV-512/256		AC3

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

MACH 5 IND -10, -12, -15, -20

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

M5- 512 /256 -10 A I

FAMILY TYPE
M5- = MACH 5 Value Plus (5-V V_{CC})

MACROCELL DENSITY
128 = 128 Macrocells
192 = 192 Macrocells
256 = 256 Macrocells
320 = 320 Macrocells
384 = 384 Macrocells
512 = 512 Macrocells

I/Os
/68 = 68 I/Os
/104 = 104 I/Os
/120 = 120 I/Os
/160 = 160 I/Os
/184 = 184 I/Os
/192 = 192 I/Os
/256 = 256 I/Os

OPTIONAL PROCESSING
Blank = Standard Processing

OPERATING CONDITIONS
I = Industrial (-40°C to +85°C)

PACKAGE TYPE
Y = Plastic Quad Flat Pack (PQFP)
V = Thin Quad Flat Pack (TQFP)
A = Ball Grid Array (BGA)
H = Plastic Quad Flat Pack with heat sink (PQFP)

SPEED
-10 = 10 ns t_{PD}
-12 = 12 ns t_{PD}
-15 = 15 ns t_{PD}
-20 = 20 ns t_{PD}

Valid Combinations		
M5-128/68	-10, -12, -15, -20	YI, VI
M5-128/104		YI
M5-128/120		YI, HI
M5-192/68		YI, VI
M5-192/104		YI
M5-192/120		YI, HI
M5-192/160		HI
M5-256/68		YI, VI
M5-256/104		YI
M5-256/120		YI, HI
M5-256/160		HI

Device Marking

Actual device marking differs from the ordering part number (OPN). "MACH 5" is marked on a device wherever "M5-" is used in the OPN.

Valid Combinations		
M5-320/120	-10, -12, -15, -20	HI
M5-320/160		HI
M5-320/184		HI
M5-320/192		AI
M5-384/120		HI
M5-384/160		HI
M5-384/184		HI
M5-384/192		AI
M5-512/120		HI
M5-512/160		HI
M5-512/184		HI
M5-512/192		AI
M5-512/256		AI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

MACH 5 LV IND -10, -12, -15, -20

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

M5LV- 512 /256 -10 A I

FAMILY TYPE
M5LV- = MACH 5 Value Plus Low Voltage (3.3-V V_{CC})

MACROCELL DENSITY
128 = 128 Macrocells
192 = 192 Macrocells
256 = 256 Macrocells
320 = 320 Macrocells
384 = 384 Macrocells
512 = 512 Macrocells

I/Os
/68 = 68 I/Os
/104 = 104 I/Os
/120 = 120 I/Os
/160 = 160 I/Os
/184 = 184 I/Os
/192 = 192 I/Os
/256 = 256 I/Os

OPTIONAL PROCESSING
Blank = Standard Processing

OPERATING CONDITIONS
I = Industrial (–40°C to +85°C)

PACKAGE TYPE
Y = Plastic Quad Flat Pack (PQFP)
V = Thin Quad Flat Pack (TQFP)
A = Ball Grid Array (BGA)
H = Plastic Quad Flat Pack with heat sink (PQFP)

SPEED
-10 = 10 ns t_{PD}
-12 = 12 ns t_{PD}
-15 = 15 ns t_{PD}
-20 = 20 ns t_{PD}

Valid Combinations		
M5LV-128/68	-10, -12, -15, -20	YI, VI
M5LV-128/104		YI
M5LV-128/120		YI, HI
M5LV-192/68		YI, VI
M5LV-192/104		YI
M5LV-192/120		YI, HI
M5LV-192/160		HI
M5LV-256/68		YI, VI
M5LV-256/104		YI
M5LV-256/120		YI, HI
M5LV-256/160		HI

Device Marking

Actual device marking differs from the ordering part number (OPN). "MACH 5" is marked on a device wherever "M5-" is used in the OPN.

Valid Combinations		
M5LV-320/120	-10, -12, -15, -20	HI
M5LV-320/160		HI
M5LV-320/184		HI
M5LV-320/192		AI
M5LV-384/120		HI
M5LV-384/160		HI
M5LV-384/184		HI
M5LV-384/192		AI
M5LV-512/120		HI
M5LV-512/160		HI
M5LV-512/184		HI
M5LV-512/192		AI
M5LV-512/256		AI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The Fifth Generation MACH Architecture yields the highest speeds at the highest CPLD densities. Excellent routing resources ensure pinout retention as well as high utilization. The MACH 5 Value Plus architecture consists of PAL® blocks connected by two levels of interconnect. Each group of four PAL blocks is given its own routing resources, called **block interconnect**. Together, the four PAL blocks and their block interconnect are called a **segment**. The second level of interconnect, the **segment interconnect**, ties all of the segments together (see Figure 1). The only logic difference between any two MACH 5 devices is the number of segments, so once a designer is familiar with one device, consistent performance can be expected across the entire family. All devices have four pin clocks available which can also be used as logic inputs.

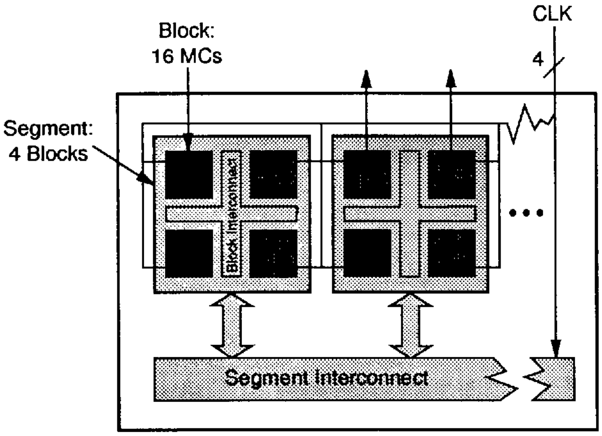

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Figure 1. MACH 5 Value Plus Block Diagram with Segment Numbers

Enhanced PAL Block

The MACH 5 PAL blocks consist of the elements listed below. While each PAL block resembles an independent PAL device, it has superior control and logic generation capabilities.

- Macrocell
- Logic array
- Logic allocator
- I/O cell
- Register control generator
- Output enable generator

The I/Os associated with each PAL block (Figure 2) have a path directly back to that PAL block called **local feedback**. If the I/O is used in another PAL block, the **interconnect feeder** assigns a **block interconnect** line to that signal. The interconnect feeder acts as an input switch matrix. The block and segment interconnect provide connections between any two signals in a device. The **block feeder** assigns block interconnect lines and local feedback lines to the PAL block inputs. Two inputs per PAL block can also be fed directly to a macrocell for registered input applications.

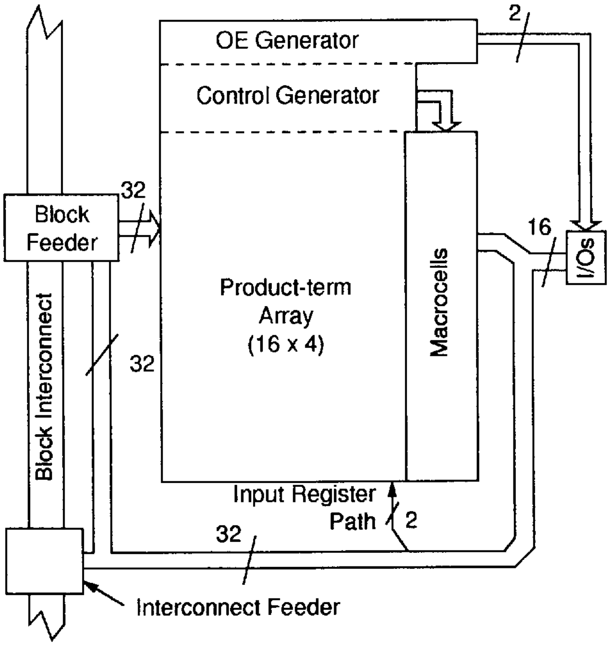

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Figure 2. PAL Block Structure

Logic Array and Allocator

The product-term array has the familiar sum-of-products architecture used in PAL devices. The logic allocator assigns product terms to macrocells. Up to eight clusters of four product terms can be steered to one macrocell, and product terms can be steered in a basic cluster of three or four product terms. If three product terms are steered away, one can be left for separate logic generation. The logic allocator acts as an output logic switch matrix: as a design changes, the **logic allocator** will reassign logic to macrocells to retain pinout. If not used in a cluster, the extra product term can be XORed with the basic cluster for functions such as data comparison. If the basic cluster of three product terms is steered away, the product term remaining can still be used for logic generation. The XOR gate available to each macrocell can be used for logic and/or for polarity control. The product term clusters available to each macrocell within a PAL block are shown in Table 3.

Rather than an output switch matrix which reassigns macrocells to pins to retain pinout, the wide logic allocator produces the same result by reassigning logic to macrocells. In addition, large equations (up to 32 product terms) can be implemented in a MACH 5 device with only one pass through the logic array.

Table 3. Product Term Steering Options for PT Clusters and Macrocells

Macrocell	Available Clusters
MC0	C0, C1, C2, C3, C4
MC1	C0, C1, C2, C3, C4, C5
MC2	C0, C1, C2, C3, C4, C5, C6
MC3	C0, C1, C2, C3, C4, C5, C6, C7
MC4	C0, C1, C2, C3, C4, C5, C6, C7
MC5	C1, C2, C3, C4, C5, C6, C7, C8
MC6	C2, C3, C4, C5, C6, C7, C8, C9
MC7	C3, C4, C5, C6, C7, C8, C9, C10
MC8	C5, C6, C7, C8, C9, C10, C11, C12
MC9	C6, C7, C8, C9, C10, C11, C12, C13
MC10	C7, C8, C9, C10, C11, C12, C13, C14
MC11	C8, C9, C10, C11, C12, C13, C14, C15
MC12	C8, C9, C10, C11, C12, C13, C14, C15
MC13	C9, C10, C11, C12, C13, C14, C15
MC14	C10,C11, C12, C13, C14, C15
MC15	C11, C12, C13, C14, C15

Macrocells

The macrocells for MACH 5 consist of a storage element, a control (clock and set or reset or latch enable) bus, and routing resources. The macrocell (Figure 3) and can be configured for combinatorial, registered or latched operation. The D-type flip-flops can be configured as T-type, J-K, or S-R operation through the use of the XOR gate associated with each macrocell.

Control Generator

The control generator provides four configurable clock lines and three configurable set/reset lines to each macrocell in a PAL block. Any of the four clock lines and any of the three set/reset lines can be independently selected by any flip-flop within a block. The clock lines (Figure 4) provide global (pin) clocks, product term clocks, sum term clocks, and latch enables. Positive or negative edge clocking is available as well as advanced clocking features such as **complementary** and **biphase** clocking. Complementary clocking provides two clock lines exactly 180 degrees out of phase, and is useful in applications such as fast data paths. A biphase clock line clocks flip-flops on both the positive and negative edges of the clock. The configuration options for the four clock lines per PAL block are as follows:

Clock Line 1 Options

- Global clock (1, 2, 3, or 4) with clock enable, clocked on the positive or negative edge of the clock
- Product-term clock (A*B*C)
- Sum-term clock (A+B+C)

Clock Line 2 Options

- Global clock (1, 2, 3, or 4) with positive edge clock enable
- Global clock (1, 2, 3, or 4) with negative edge clock enable
- Global clock (1, 2, 3, or 4) with positive and negative edge clock enable (biphase)

Clock Line 3 Options

- Global clock (1, 2, 3, or 4) with clock enable

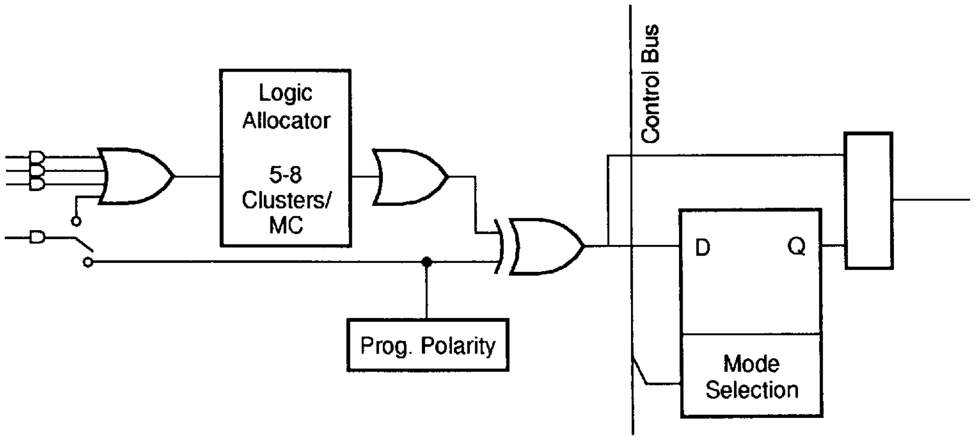

Figure 3. Macrocell Diagram

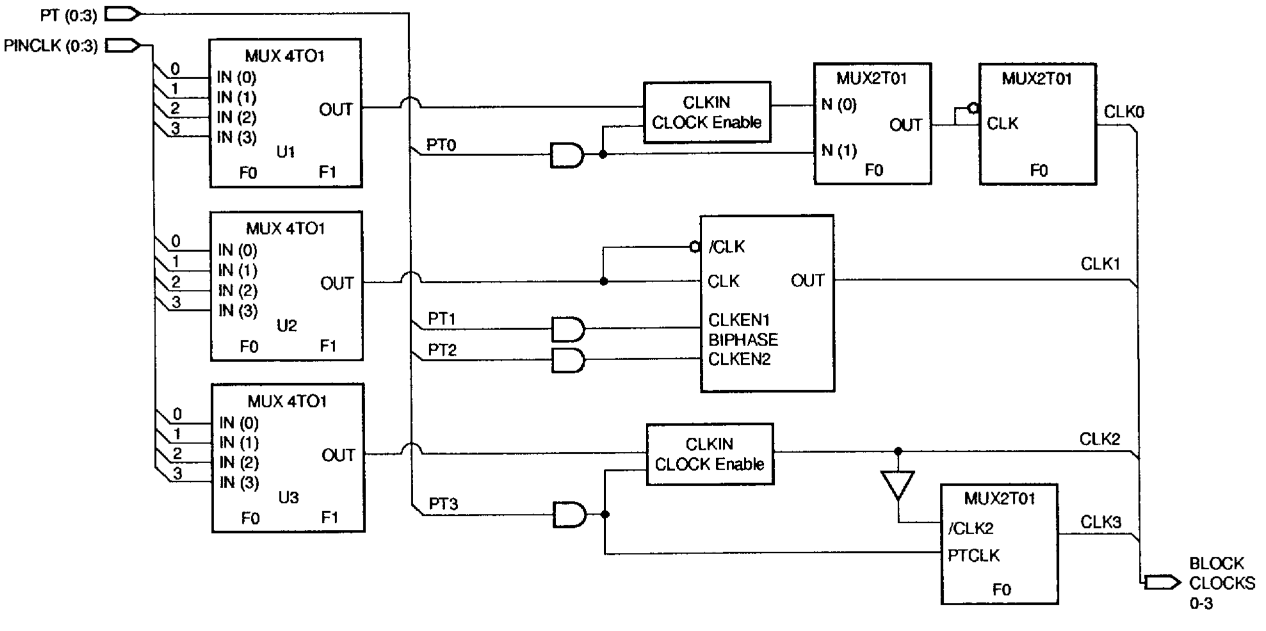

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Figure 4. Clock Generator

Clock Line 4 Options

- Complement of clock line 3 (same clock enable)
- Product-term clock (if clock line 3 does not use clock enable

Three of the four global clocks are available within any given PAL block. There are two product-term clocks and one sum-term clock available per PAL block.

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.

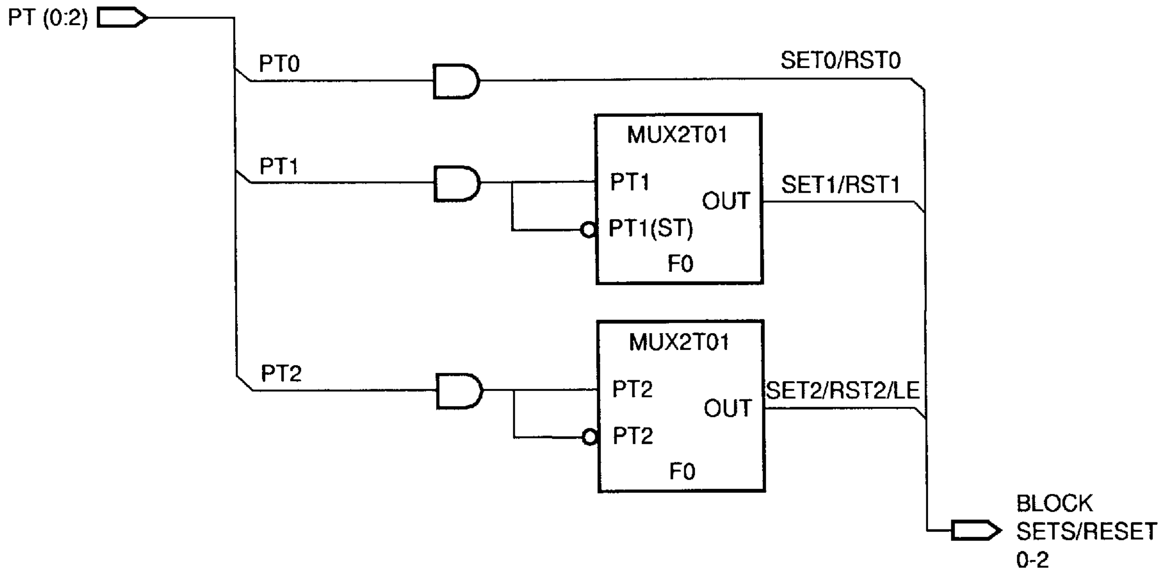

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Figure 5. Set/Reset Generator

OE Generator

There is one output enable (OE) generator per PAL block that generates two product-term driven output enables. Each I/O cell is simply an output buffer. Each macrocell within the PAL block can choose to be permanently enabled, permanently disabled, or choose one of the two product term output enables per PAL block (Figure 6).

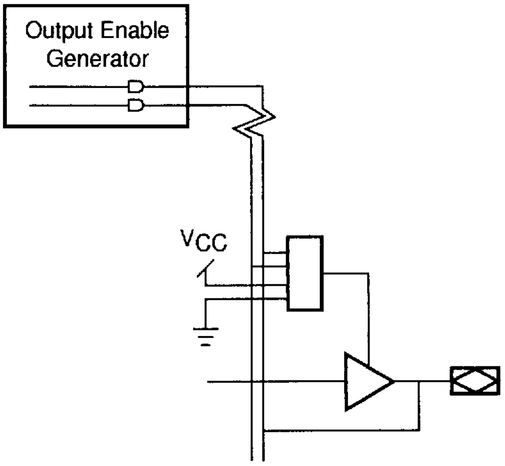


Figure 6. Output Enable Generator and I/O Cell

MACH 5 TIMING

MACH 5 timing can be modeled on any AMD approved software tool or it can be estimated using the model shown in Figure 7. Device timing will depend on the level of interconnect used and the power level chosen for a particular path. These are the path and power factors. The pin-to-pin delays can be calculated by following one path from input/feedback to output. For example, t_{PD} is the pin-to-pin delay for a signal within a PAL block. $t_{PD}+t_{BLK}$ is the pin-to-pin delay for a signal that uses the block interconnect and stays within a segment. $t_{PD}+t_{SEG}$ is the pin-to-pin delay for a signal that uses both the block and segment interconnect. Power level timing is calculated in the same manner. If a signal uses block interconnect and is placed in a low-power block, then the pin-to-pin delay will be $t_{PD}+t_{BLK}+t_{PL3}$.

3.3-V AND 5-V VERSIONS: SAFE FOR MIXED VOLTAGE DESIGNS

All MACH 5 device densities have both 3.3-V (V_{CC}) and 5-V (V_{CC}) versions available. Both versions are safe for mixed voltage designs. This means that the 3.3-V device will accept inputs up to 5.5 volts, and the 5-V device outputs will not drive above 3.3 volts. A MACH 5 device requires only one supply voltage: 5-V for M5 devices and 3.3-V for M5LV devices. Both the 3.3-V and

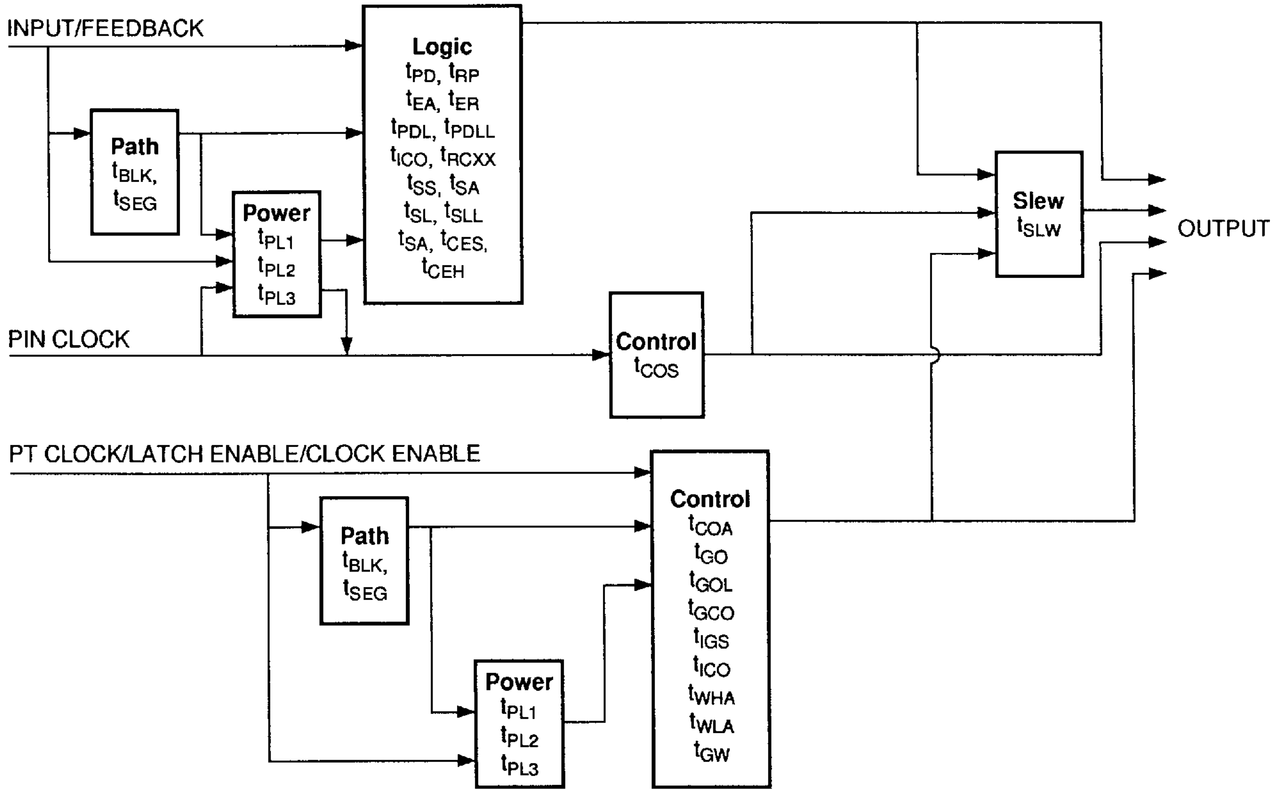


Figure 7. MACH 5 Timing Factors

5-V versions have the same performance and have only trivial power differences.

HOT SOCKETING

MACH 5 is ideal for PC add-on cards and other applications in which voltage may be applied to device inputs before V_{CC}. MACH 5 inputs are designed to accept up to 5.5 V on inputs when the supply voltage is at zero without latch-up and without any reliability concerns. During power-up and power-down, all of the I/O are tri-stated so that they will not interfere with other devices, and there is no I/O leakage during power down, so a MACH 5 device can safely be connected to an active bus. These devices are designed to be safe for **hot insertion**.

PCI COMPLIANCE

MACH 5 Value Plus family members in the -7/-10/-12 speeds are fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group (SIG). MACH 5 devices provide the speed, drive, density and I/Os for the most complex PCI designs. For more information on using MACH for PCI designs please see the application note "PCI Interface Using AMD PLDs."

DEVICE MIGRATION

Any two MACH 5 devices in the same package have the same pinout. If a design outgrows the macrocell count of one device, the higher macrocell count device in the same package will be a drop in replacement and no board relayout will be necessary. Designers that find that they need less logic can choose a lower density device in the same package and reduce waste.

JTAG, IN-SYSTEM PROGRAMMING

All MACH 5 devices are in-system programmable and are compliant to the JTAG standard, IEEE 1149.1, developed for checking circuit board connectivity. MACH in-system programming is implemented as an extension of this standard which uses manufacturer defined instructions and registers for program and verify. In-system programming eases prototyping and reduces manufacturing steps. MACH 5 devices can be programmed across the commercial temperature range. Minimum programming time is typically less than 5 seconds. For more information on the benefits of in-system programming, please see the application note "Introduction to JTAG and 5-V Programming" included in the 1995 MACH data book. AMD's MACHpro® software serializes JEDEC files and downloads them to the target board through the PC parallel port. MACH 5 devices can be programmed in any JTAG chain.

POWER MANAGEMENT

There are 4 power/speed options in each MACH 5 PAL block. The speed and power tradeoff can be tailored for each design. In large designs, there may be several different speed requirements for different portions of a design. In a computing design, a state machine controller may require the fastest speed available, while the data path portion may run at the slower speed of the bus.

Power level and resulting speed for the 7.5 ns devices

High Speed/High Power	100% power	7.5 ns
Medium High Speed/Medium High Power	67% power	10 ns
Medium Low Speed/Medium Low Power	40% power	15 ns
Low Speed/low Power	20% power	20 ns

PROGRAMMABLE SLEW-RATE

Each MACH 5 I/O has an individual programmable slew-rate control bit. Each output can be configured for the highest speed (3 V/ns) or for the lowest noise (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections and less noise. For designs with short traces or well terminated lines, the fast-slew rate can be used to achieve the highest speed. The slew-rate is adjusted independent of power.

POWER UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic and clock must be inactive until the reset delay time has elapsed.

SECURITY

A programmable security bit is provided to prevent unauthorized copying of array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern, securing proprietary designs from competitors. The security bit can only be erased in conjunction with the array during an erase cycle.

QUALITY AND TESTABILITY

MACH 5 devices are electrically erasable which allows for full AC and DC verification of every device. In addition this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

TECHNOLOGY

The MACH 5 devices are fabricated on AMD's own state-of-the-art 0.5 and 0.35 micron (L_{eff}) EECMOS technologies. This advanced technology allows MACH 5 to offer both the highest performance CPLDs and the lowest power CPLDs in the industry. The floating gate cells rely on Fowler-Nordheim tunneling to charge the gates, and have long proven their endurance and reliability.

The substrate of these devices is grounded to provide substrate clamp diodes on every input which makes inputs more immune to noisy input signals.

BUS-FRIENDLY I/O STRUCTURE

All of the MACH 5 devices have a Bus-Friendly input structure which weakly holds an input at its last driven state. While it is good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from threshold where noise can cause high-frequency switching. For more information on Bus-Friendly inputs, please see the AMD application note “Evolution of Bus-Friendly Inputs and I/Os.”

ABSOLUTE MAXIMUM RATINGS

MACH 5 COM -7.5, -10, -12, -15

Storage Temperature . . . . −65°C to +150°C

Supply Voltage
with Respect to Ground . . . . −0.5 V to +7.0 V

DC Input Voltage . . . . 0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . 2000 V

Latchup Current (0°C to +70°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Ambient Temperature (T_A)
Operating in Free Air. . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

5-V DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Description	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4	3.3	V
V_{OL}	Output LOW Voltage	I_{OL} = +16 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0, V_{CC} = Max (Note 2)		-10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		-10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)	-30	-160	mA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{ZH}.*
3. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = 2.0$ V	5 V, 25°C, 1 MHz	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0$ V	5 V, 25°C, 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

BASIC (all signals from within PAL block except global control signals)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O or Feedback to Combinatorial Output or Input, I/O or Feedback to Output through Transparent Output Latch	2	7.5	2	10	2	12	2	15	ns
t_{SS}	Setup Time from Input, I/O or Feedback to Global Clock	4		5		6		8		ns
t_{HS}	Register Data Hold Time Using a Global Clock	0		0		0		0		ns
t_{COS}	Global Clock to Output (Pin Clock)		5.5		6.5		8		10	ns
t_{WLS}	Global Clock High Width (Note 3)	3		5		6		6		ns
t_{WHS}	Global Clock Low Width (Note 3)	3		5		6		6		ns
f_{MAX}	External Feedback, PAL Block Level $1/(t_{SS} + t_{COS})$	105		87		71		55		MHz
	Internal Feedback PAL Block Level (MHz)	125		100		83.3		83.3		MHz
	No Feedback PAL Block Level	166.7		100		83.3		83.3		MHz
t_{SA}	Setup Time from Input, I/O or Feedback to Product Term Clock, PAL Block Level	0		0		0		0		ns
t_{HA}	Output Register Data Hold Time Using a Product Term Clock	4		5		6		7		ns
t_{COA}	Product Term Clock to Output		10		12		15		17	ns
t_{WLA}	Product Term Clock Width LOW	4		5		6		7		ns
t_{WHA}	Product Term Clock Width HIGH	4		5		6		7		ns
f_{MAXA}	External Feedback, PAL Block Level (MHz) $1/(t_{SUA} + t_{COA})$	100		83		67		59		MHz
	Internal Feedback, PAL Block level	111		95		83.3		71.4		MHz
	No Feedback, PAL Block level	125		100		83.3		71.4		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Product Term Gate	0		0		0		0		ns
t_{HL}	Latch Data Hold Time (Using Product Term Gate)	4		5		6		7		ns
t_{GO}	Latch Gate to Output		10		11		12		13	ns
t_{GOL}	Latch Gate to Output through Transparent Latch		17		18		19		20	ns

BASIC (all signals from within PAL block except global control signals) (continued)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{GCO}	Latch Gate to Combinatorial Output		17		18		19		20	ns
t_{IGS}	Latch Gate to Output Latch Setup	10		11		12		13		ns
t_{GW}	Gate Width LOW (for LOW Transparent) or High (for HIGH Transparent)	4		5		6		7		ns
t_{BUF}	Delay Savings for Using Internal Feedback Instead of Pin Feedback (I/Os Only, No Savings for Buried)	0.5	2	0.5	2	0.5	2	0.5	2	ns

ASYNCHRONOUS SET and RESET, OUTPUT ENABLE, CLOCK ENABLE

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RP}	Asynchronous Reset or Preset to Registered or Latched Output		10		12		14		16	ns
t_{PRW}	Asynchronous Reset or Preset Width	4		5		6		7		ns
t_{PRR}	Asynchronous Reset or Preset Recovery Time	7.5		8		9		10		ns
t_{EA}	Input I/O or Feedback to Output Enable	2	9.5	2	10	2	12	2	15	ns
t_{ER}	Input I/O or Feedback to Output Disable		9.5		10		12		15	ns
t_{CES}	Setup Time from Clock Enable to Next Clock Pulse	4		5		6		7		ns
t_{CEH}	Hold Time for Clock Enable After Last Enabled Clock Pulse	4		5		6		7		ns

REGISTERS and LATCHES (input and output, BLOCK level)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PDL}	Input, I/O or Feedback to Output Through Transparent Input Latch		8.5		10		12		15	ns
t_{ICO}	Input Register Clock to Combinatorial Output		12		14		16		18	ns
t_{SIRS}	Input Register Setup Time Using Global Clock	2		2		2		2		ns
t_{SIRA}	Input Register Setup Time Using Product Term Clock	0		0		0		0		ns
t_{HIRS}	Input Register Hold Time Using Global Clock	2		3		4		5		ns
t_{HIRA}	Input Register Hold Time Using Product Term Clock	6		7		8		9		ns
t_{WICW}	Input Register Clock Width Low or High	4		5		6		7		ns
f_{MAXI}	Maximum Input Register Frequency	125		100		83.3		71.4		MHz
t_{RCSS}	Register Using Global Clock to Output Register Using Global Clock Setup Time	7.5		10		12		15		ns
t_{RCSA}	Register Using Global Clock to Output Register Using Product Term Clock Setup Time	12.5		15		17		18		ns
t_{RCAS}	Register Using Product Term Clock to Output Register Using Global Clock Setup Time	12.5		15		17		18		ns
t_{RCAA}	Register Using Product Term Clock to Output Register Using Product Term Clock Setup Time	7.5		10		12		15		ns
t_{SIL}	Input Latch Setup Time	2		2		2		2		ns
t_{HIL}	Input Latch Hold Time	6		7		8		9		ns
t_{SLL}	Setup Time from Input, I/O or Feedback Through Transparent Input Latch to Output Gate	9		10		11		12		ns
t_{PDLL}	Input, I/O or Feedback to Output Through Transparent Input and Output Latches		12		14		16		18	ns

INTERCONNECT

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLK}	Interconnect delay between blocks. If a signal depends on inputs not in the same block, but in the same segment, this delay must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{SL}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}.		1.5		2.0		2.0		2.0	ns
t_{SEG}	Interconnect delay between segments. This parameter includes all block interconnect delay. If a signal depends on inputs not in the same segment, this delay must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{SL}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}.		5		6.0		6.0		6.0	ns

POWER and SLEW

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PL1}	Low-power level 1 delay. If a signal is selected as low power level 1, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		2.5		2.5		3.0		3.0	ns
t_{PL2}	Low-power level 2 delay. If a signal is selected as low power level 2, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		7.5		7.5		8		8	ns
t_{PL3}	Low-power level 3 delay. If a signal is selected as low power level 3, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		12.5		12.5		13		13	ns
t_{SLW}	Slow Slew Rate delay. If slow slew rate is selected, this parameter must be added to t_{PD}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{PDL}, t_{ICO}, t_{PDLL}.		2.5		2.5		2.5		2.5	ns

Notes:

2. See Switching Test Circuit for test conditions.

3. If a signal is used as both a clock and a logic array input, then the maximum input frequency applies (Fmax/2).

ABSOLUTE MAXIMUM RATINGS

MACH 5 IND -10, -12, -15, -20

Storage Temperature . . . . –65°C to +150°C

Supply Voltage
with Respect to Ground . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . 0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . 2000 V

Latchup Current (–40°C to +85°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Ambient Temperature (T_A)
Operating in Free Air. . . . . –40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

5-V DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Description	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4	3.3	V
V_{OL}	Output LOW Voltage	I_{OL} = –16 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0, V_{CC} = Max (Note 2)		-10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		-10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)	-30	-160	µA

Note:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.*
3. *Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = 2.0$ V	5 V, 25°C, 1 MHz	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0$ V	5 V, 25°C, 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)
BASIC (all signals from within PAL block except global control signals)

Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O or Feedback to Combinatorial Output or Input, I/O or Feedback to Output through Transparent Output Latch	2	10	2	12	2	15	2	20	ns
t_{SS}	Setup Time from Input, I/O or Feedback to Global Clock	5		6		8		10		ns
t_{HS}	Register Data Hold Time Using a Global Clock	0		0		0		0		ns
t_{COS}	Global Clock to Output (Pin Clock)		6.5		8		10		12	ns
t_{WLS}	Global Clock High Width (Note 3)	5		6		6		7		ns
t_{WHS}	Global Clock Low Width (Note 3)	5		6		6		7		ns
f_{MAX}	External Feedback, PAL Block Level 1/(t_{SU} + t_{COS})	87		71		55		45.5		MHz
	Internal Feedback PAL Block Level (MHz)	100		83.3		83.3		71.4		MHz
	No Feedback PAL Block Level	100		83.3		83.3		71.4		MHz
t_{SA}	Setup Time from Input, I/O or Feedback to Product Term Clock, PAL Block Level	0		0		0		0		ns
t_{HA}	Output Register Data Hold Time Using a Product Term Clock	5		6		7		8		ns
t_{COA}	Product Term Clock to Output		12		15		17		20	ns
t_{WLA}	Product Term Clock Width LOW	5		6		7		8		ns
t_{WHA}	Product Term Clock Width HIGH	5		6		7		8		ns
f_{MAXA}	External Feedback, PAL Block Level (MHz) 1/(t_{SUA} + t_{COA})	83		67		59		50		MHz
	Internal Feedback, PAL Block level	95		83.3		71.4		62.5		MHz
	No Feedback, PAL Block level	100		83.3		71.4		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Product Term Gate	0		0		0		0		ns
t_{HL}	Latch Data Hold Time (Using Product Term Gate)	5		6		7		8		ns
t_{GO}	Latch Gate to Output		11		12		13		14	ns
t_{GOL}	Latch (Input or Output) Gate to Output through Transparent Latch		18		19		20		21	ns

BASIC (all signals from within PAL block except global control signals) (continued)

Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{GCO}	Latch Gate to Combinatorial Output		18		19		20		21	ns
t_{IGS}	Latch Gate to Output Latch Setup	11		12		13		14		ns
t_{GW}	Gate Width LOW (for LOW Transparent) or High (for HIGH Transparent)	5		6		7		8		ns
t_{BUF}	Delay Savings for Using Internal Feedback Instead of Pin Feedback (I/Os Only, No Savings for Buried)	0.5	2	0.5	2	0.5	2	0.5	2	ns

ASYNCHRONOUS SET and RESET, OUTPUT ENABLE, CLOCK ENABLE

Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RP}	Asynchronous Reset or Preset to Registered or Latched Output		12		14		16		18	ns
t_{PRW}	Asynchronous Reset or Preset Width	5		6		7		8		ns
t_{PRR}	Asynchronous Reset or Preset Recovery Time	8		9		10		11		ns
t_{EA}	Input I/O or Feedback to Output Enable		10		12		15		20	ns
t_{ER}	Input I/O or Feedback to Output Disable		10		12		15		20	ns
t_{CES}	Setup Time from Clock Enable to Next Clock Pulse	5		6		7		8		ns
t_{CEH}	Hold Time for Clock Enable After Last Enabled Clock Pulse	5		6		7		8		ns

REGISTERS and LATCHES (input and output, BLOCK level)

Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PDL}	Input, I/O or Feedback to Output Through Transparent Input Latch		10		12		15		20	ns
t_{ICO}	Input Register Clock to Combinatorial Output		14		16		18		20	ns
t_{SIRS}	Input Register Setup Time Using Global Clock	2		2		2		2		ns
t_{SIRA}	Input Register Setup Time Using Product Term Clock	0		0		0		0		ns
t_{HIRS}	Input Register Hold Time Using Global Clock	3		4		5		6		ns
t_{HIRA}	Input Register Hold Time Using Product Term Clock	7		8		9		10		ns
t_{WICW}	Input Register Clock Width Low or High	5		6		7		8		ns
f_{MAXI}	Maximum Input Register Frequency	100		83.3		71.4		62.5		MHz
t_{RCSS}	Register Using Global Clock to Output Register Using Global Clock Setup Time	10		12		15		20		ns
t_{RCSA}	Register Using Global Clock to Output Register Using Product Term Clock Setup Time	15		17		18		20		ns
t_{RCAS}	Register Using Product Term Clock to Output Register Using Global Clock Setup Time	15		17		18		20		ns
t_{RCAA}	Register Using Product Term Clock to Output Register Using Product Term Clock Setup Time	10		12		15		20		ns
t_{SIL}	Input Latch Setup Time	2		2		2		2		ns
t_{HIL}	Input Latch Hold Time	7		8		9		10		ns
t_{SLL}	Setup Time from Input, I/O or Feedback Through Transparent Input Latch to Output Gate	10		11		12		13		ns
t_{PDLL}	Input, I/O or Feedback to Output Through Transparent Input and Output Latches		14		16		18		20	ns

INTERCONNECT

Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLK}	Interconnect delay between blocks. If a signal depends on inputs not in the same block, but in the same segment, this delay must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{SL}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RR}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}.		2.0		2.0		2.0		2.0	ns
t_{SEG}	Interconnect delay between segments. This parameter includes all block interconnect delay. If a signal depends on inputs not in the same segment, this delay must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{SL}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RR}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}.		6		6		6		6	ns

POWER and SLEW

Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PL1}	Low-power level 1 delay. If a signal is selected as low power level 1, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		2.5		3		3		3	ns
t_{PL2}	Low-power level 2 delay. If a signal is selected as low power level 2, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		7.5		8		8		8	ns
t_{PL3}	Low-power level 3 delay. If a signal is selected as low power level 3, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		12.5		13		13		13	ns
t_{SLW}	Slow Slew Rate delay. If slow slew rate is selected, this parameter must be added to t_{PD}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP} t_{EA}, t_{ER}, t_{PDL}, t_{ICO}, t_{PDLL}.		2.5		2.5		2.5		2.5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *If a signal is used as both a clock and a logic array input, then the maximum input frequency applies (Fmax/2).*

ABSOLUTE MAXIMUM RATINGS

MACH 5 LV COM -7.5, -10, -12, -15

Storage Temperature	−65°C to +150°C
Supply Voltage with Respect to Ground	−0.5 V to +7.0 V
DC Input Voltage	0.5 V to 5.5 V
Static Discharge Voltage	2000 V
Latchup Current (0°C to +70°C)	200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Ambient Temperature (T_A) Operating in Free Air	0°C to +70°C
Supply Voltage (V_{CC}) with Respect to Ground	+3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

3.3-V DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Description	Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = −100 µA	V_{CC} - 0.2		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OH} = 100 µA		0.2	V
V_{IH}	Input HIGH Voltage	$V_{OUT} \geq V_{OH}$ Min or $V_{OUT} \leq V_{OL}$ Max (Note 1)	2.0	5.5	V
V_{IL}	Input LOW Voltage	$V_{OUT} \geq V_{OH}$ Min or $V_{OUT} \leq V_{OL}$ Max (Note 1)	-0.3	0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6, V_{CC} = Max (Note 2)		5	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0, V_{CC} = Max (Note 2)		-5	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		5	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)		-5	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)	-15	-160	µA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.*
3. *Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	3.3 V, 25°C, 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	3.3 V, 25°C, 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

BASIC (all signals from within PAL block except global control signals)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O or Feedback to Combinatorial Output or Input, I/O or Feedback to Output through Transparent Output Latch	2	7.5	2	10	2	12	2	15	ns
t_{SS}	Setup Time from Input, I/O or Feedback to Global Clock	4		5		6		8		ns
t_{HS}	Register Data Hold Time Using a Global Clock	0		0		0		0		ns
t_{COS}	Global Clock to Output (Pin Clock)		5.5		6.5		8		10	ns
t_{WLS}	Global Clock High Width (Note 3)	3		5		6		6		ns
t_{WHS}	Global Clock Low Width (Note 3)	3		5		6		6		ns
f_{MAX}	External Feedback, PAL Block Level $1/(t_{SU} + t_{COS})$	105		87		71		55		MHz
	Internal Feedback PAL Block Level (MHz)	125		100		83.3		83.3		MHz
	No Feedback PAL Block Level	166.7		100		83.3		83.3		MHz
t_{SA}	Setup Time from Input, I/O or Feedback to Product Term Clock, PAL Block Level	0		0		0		0		ns
t_{HA}	Output Register Data Hold Time Using a Product Term Clock	4		5		6		7		ns
t_{COA}	Product Term Clock to Output		10		12		15		17	ns
t_{WLA}	Product Term Clock Width LOW	4		5						ns
t_{WHA}	Product Term Clock Width HIGH	4		5						ns
f_{MAXA}	External Feedback, PAL Block Level (MHz) $1/(t_{SUA} + t_{COA})$	100		83		67		59		MHz
	Internal Feedback, PAL Block level	111		95		83.3		83.3		MHz
	No Feedback, PAL Block level	125		100		83.3		83.3		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Product Term Gate	0		0		0		0		ns
t_{HL}	Latch Data Hold Time (Using Product Term Gate)	4		5		6		7		ns
t_{GO}	Latch Gate to Output		10		11		12		13	ns

BASIC (all signals from within PAL block except global control signals) (continued)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{GOL}	Latch Gate to Output through Transparent Latch		17		18		19		20	ns
t_{GCO}	Latch Gate to Combinatorial Output		17		18		19		20	ns
t_{IGS}	Latch Gate to Output Latch Setup	10		11		12		13		ns
t_{GW}	Gate Width LOW (for LOW Transparent) or High (for HIGH Transparent)	4		5		6		7		ns
t_{BUF}	Delay Savings for Using Internal Feedback Instead of Pin Feedback (I/Os Only, No Savings for Buried)	0.5	2	0.5	2	0.5	2	0.5	2	ns

ASYNCHRONOUS SET and RESET, OUTPUT ENABLE, CLOCK ENABLE

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RP}	Asynchronous Reset or Preset to Registered or Latched Output		10		12		14		16	ns
t_{PRW}	Asynchronous Reset or Preset Width	4		5		6		7		ns
t_{PRR}	Asynchronous Reset or Preset Recovery Time	7.5		8		9		10		ns
t_{EA}	Input I/O or Feedback to Output Enable	2	9.5	2	10	2	12	2	15	ns
t_{ER}	Input I/O or Feedback to Output Disable		9.5		10		12		15	ns
t_{CES}	Setup Time from Clock Enable to Next Clock Pulse	4		5		6		7		ns
t_{CEH}	Hold Time for Clock Enable Following Last Enabled Clock Pulse	4		5		6		7		ns

REGISTERS and LATCHES (input and output, BLOCK level)

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PDL}	Input, I/O or Feedback to Output Through Transparent Input Latch		8.5		10		12		15	ns
t_{ICO}	Input Register Clock to Combinatorial Output		12		14		16		18	ns
t_{SIRS}	Input Register Setup Time Using Global Clock	2		2		2		2		ns
t_{SIRA}	Input Register Setup Time Using Product Term Clock	0		0		0		0		ns
t_{HIRS}	Input Register Hold Time Using Global Clock	2		3		4		5		ns
t_{HIRA}	Input Register Hold Time Using Product Term Clock	6		7		8		9		ns
t_{WICW}	Input Register Clock Width Low or High	4		5		6		7		ns
f_{MAXI}	Maximum Input Register Frequency	125		100		83.3		71.4		MHz
t_{RCSS}	Register Using Global Clock to Output Register Using Global Clock Setup Time	7.5		10		12		15		ns
t_{RCSA}	Register Using Global Clock to Output Register Using Product Term Clock Setup Time	12.5		15		17		18		ns
t_{RCAS}	Register Using Product Term Clock to Output Register Using Global Clock Setup Time	12.5		15		17		18		ns
t_{RCAA}	Register Using Product Term Clock to Output Register Using Product Term Clock Setup Time	7.5		10		12		15		ns
t_{SIL}	Input Latch Setup Time	2		2		2		2		ns
t_{HIL}	Input Latch Hold Time	6		7		8		9		ns
t_{SLL}	Setup Time from Input, I/O or Feedback Through Transparent Input Latch to Output Gate	9		10		11		12		ns
t_{PDLL}	Input, I/O or Feedback to Output Through Transparent Input and Output Latches		12		14		16		18	ns

INTERCONNECT

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLK}	Interconnect delay between blocks. If a signal depends on inputs not in the same block, but in the same segment, this delay must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA},t_{SL}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RR} t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}.		1.5		2		2		2	ns
t_{SEG}	Interconnect delay between segments. This parameter includes all block interconnect delays. If a signal depends on inputs not in the same segment, this delay must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{SL}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RR} t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}.		5		6		6		6	ns

POWER and SLEW

Parameter Symbol	Parameter Description	-7		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PL1}	Low-power level 1 delay. If a signal is selected as low power level 1, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		2.5		2.5		3		3	ns
t_{PL2}	Low-power level 2 delay. If a signal is selected as low power level 2, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		7.5		7.5		8		8	ns
t_{PL3}	Low-power level 3 delay. If a signal is selected as low power level 3, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		12.5		12.5		13		13	ns
t_{SLW}	Slow Slew Rate delay. If slow slew rate is selected, this parameter must be added to t_{PD}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP} t_{EA}, t_{ER}, t_{PDL}, t_{ICO}, t_{PDLL}.		2.5		2.5		2.5		2.5	ns

Notes:

2. See Switching Test Circuit for test conditions.

3. If a signal is used as both a clock and a logic array input, then the maximum input frequency applies (Fmax/2).

ABSOLUTE MAXIMUM RATINGS

MACH 5 LV IND -10, -12, -15, -20

Storage Temperature . . . . –65°C to +150°C

Supply Voltage
with Respect to Ground . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . 0.5 V to 5.5 V

Static Discharge Voltage . . . . 2000 V

Latchup Current (0°C to +70°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Ambient Temperature (T_A)
Operating in Free Air. . . . . –40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

3.3-V DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Description	Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –100 µA	V_{CC} - 0.2		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OH} = 100 µA		0.2	V
V_{IH}	Input HIGH Voltage	$V_{OUT} \geq V_{OH}$ Min or $V_{OUT} \leq V_{OL}$ Max (Note 1)	2.0	5.5	V
V_{IL}	Input LOW Voltage	$V_{OUT} \geq V_{OH}$ Min or $V_{OUT} \leq V_{OL}$ Max (Note 1)	-0.3	0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6, V_{CC} = Max (Note 2)		5	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0, V_{CC} = Max (Note 2)		-5	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6, V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		5	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0, V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		-5	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL} (Note 3)	–15	–160	µA

Notes:

1. *These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.*
3. *Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	3.3 V, 25°C, 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	3.3 V, 25°C, 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

BASIC (all signals from within PAL block except global control signals)

Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Input, I/O or Feedback to Combinatorial Output or Input, I/O or Feedback to Output through Transparent Output Latch	2	10	2	12	2	15	2	20	ns
t_{SS}	Setup Time from Input, I/O or Feedback to Global Clock	5		6		8		10		ns
t_{HS}	Register Data Hold Time Using a Global Clock	0		0		0		0		ns
t_{COS}	Global Clock to Output (Pin Clock)		6.5		8		10		12	ns
t_{WLS}	Global Clock High Width (Note 3)	5		6		6		7		ns
t_{WHS}	Global Clock Low Width (Note 3)	5		6		6		7		ns
f_{MAX}	External Feedback, PAL Block Level 1/(t_{SU} + t_{COS})	87		71		55		45		MHz
	Internal Feedback PAL Block Level (MHz)	100		83.3		83.3		71.4		MHz
	No Feedback PAL Block Level	100		83.3		83.3		71.4		MHz
t_{SA}	Setup Time from Input, I/O or Feedback to Product Term Clock, PAL Block Level	0		0		0		0		ns
t_{HA}	Output Register Data Hold Time Using a Product Term Clock	5		6		7		8		ns
t_{COA}	Product Term Clock to Output		12		15		17		20	ns
t_{WLA}	Product Term Clock Width LOW	5		6		7		8		ns
t_{WHA}	Product Term Clock Width HIGH	5		6		7		8		ns
f_{MAXA}	External Feedback, PAL Block Level (MHz) 1/(t_{SUA} + t_{COA})	83		67		59		50		MHz
	Internal Feedback, PAL Block level	95		83.3		71.4		62.5		MHz
	No Feedback, PAL Block level	100		83.3		71.4		62.5		MHz
t_{SL}	Setup Time from Input, I/O, or Feedback to Product Term Gate	0		0		0		0		ns
t_{HL}	Latch Data Hold Time (Using Product Term Gate)	5		6		7		8		ns
t_{GO}	Latch Gate to Output		11		12		13		14	ns
t_{GOL}	Latch Gate to Output through Transparent Latch		18		19		20		21	ns
t_{GCO}	Latch Gate to Combinatorial Output		18		19		20		21	ns

BASIC (all signals from within PAL block except global control signals) (continued)

Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{IGS}	Latch Gate to Output Latch Setup	11		12		13		14		ns
t_{GW}	Gate Width LOW (for LOW Transparent) or High (for HIGH Transparent)	5		6		7		8		ns
t_{BUF}	Delay Savings for Using Internal Feedback Instead of Pin Feedback (I/Os Only, No Savings for Buried)	0.5	2	0.5	2	0.5	2	0.5	2	ns

ASYNCHRONOUS SET and RESET, OUTPUT ENABLE, CLOCK ENABLE

Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RP}	Asynchronous Reset or Preset to Registered or Latched Output		12		14		16		18	ns
t_{PRW}	Asynchronous Reset or Preset Width	5		6		7		8		ns
t_{PRR}	Asynchronous Reset or Preset Recovery Time	8		9		10		11		ns
t_{EA}	Input I/O or Feedback to Output Enable		10		12		15		20	ns
t_{ER}	Input I/O or Feedback to Output Disable		10		12		15		20	ns
t_{CES}	Setup Time from Clock Enable to Next Clock Pulse	5		6		7		8		ns
t_{CEH}	Hold Time for Clock Enable Following Last Enabled Clock Pulse	5		6		7		8		ns

REGISTERS and LATCHES (input and output, BLOCK level)

Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PDL}	Input, I/O or Feedback to Output Through Transparent Input Latch		10		12		15		20	ns
t_{ICO}	Input Register Clock to Combinatorial Output		14		16		18		20	ns
t_{SIRS}	Input Register Setup Time Using Global Clock	2		2		2		2		ns
t_{SIRA}	Input Register Setup Time Using Product Term Clock	0		0		0		0		ns
t_{HIRS}	Input Register Hold Time Using Global Clock	3		4		5		6		ns
t_{HIRA}	Input Register Hold Time Using Product Term Clock	7		8		9		10		ns
t_{WICW}	Input Register Clock Width Low or High	5		6		7		8		ns
f_{MAXI}	Maximum Input Register Frequency	100		83.3		71.4		62.5		MHz
t_{RCSS}	Register Using Global Clock to Output Register Using Global Clock Setup Time	10		12		15		20		ns
t_{RCSA}	Register Using Global Clock to Output Register Using Product Term Clock Setup Time	15		17		18		20		ns
t_{RCAS}	Register Using Product Term Clock to Output Register Using Global Clock Setup Time	15		17		18		20		ns
t_{RCAA}	Register Using Product Term Clock to Output Register Using Product Term Clock Setup Time	10		12		15		20		ns
t_{SIL}	Input Latch Setup Time	2		2		2		2		ns
t_{HIL}	Input Latch Hold Time	7		8		9		10		ns
t_{SLL}	Setup Time from Input, I/O or Feedback Through Transparent Input Latch to Output Gate	10		11		12		13		ns
t_{PDLL}	Input, I/O or Feedback to Output Through Transparent Input and Output Latches		14		16		18		20	ns

INTERCONNECT

Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{BLK}	Interconnect delay between blocks. If a signal depends on inputs not in the same block, but in the same segment, this delay must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{SL}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}.		2.0		2.0		2.0		2.0	ns
t_{SEG}	Interconnect delay between segments. This parameter includes all block interconnect delay. If a signal depends on inputs not in the same segment, this delay must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{SL}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP} t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}.		6		6		6		6	ns

POWER and SLEW

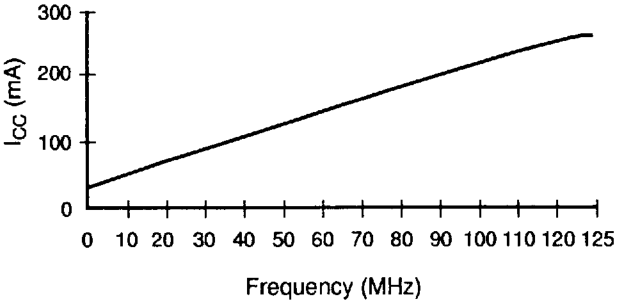
Parameter Symbol	Parameter Description	-10		-12		-15		-20		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PL1}	Low-power level 1 delay. If a signal is selected as low power level 1, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		2.5		3		3		3	ns
t_{PL2}	Low-power level 2 delay. If a signal is selected as low power level 2, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		7.5		8		8		8	ns
t_{PL3}	Low-power level 3 delay. If a signal is selected as low power level 3, this parameter must be added to t_{PD}, t_{SS}, t_{SA}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP}, t_{EA}, t_{ER}, t_{CES}, t_{PDL}, t_{ICO}, t_{RCSS}, t_{RCAS}, t_{RCAA}, t_{PDLL}, t_{SLL}, t_{SL}, t_{HIRS}, t_{HIRA}, t_{HIL}.		12.5		13		13		13	ns
t_{SLW}	Slow Slew Rate delay. If slow slew rate is selected, this parameter must be added to t_{PD}, t_{COA}, t_{GO}, t_{GOL}, t_{GCO}, t_{IGS}, t_{RP} t_{EA}, t_{ER}, t_{PDL}, t_{ICO}, t_{PDLL}.		2.5		2.5		2.5		2.5	ns

Notes:

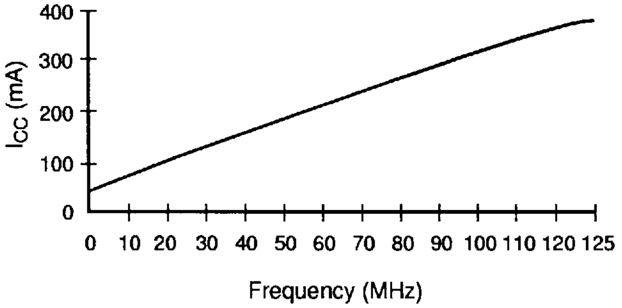
2. *See Switching Test Circuit for test conditions.*
3. *If a signal is used as both a clock and a logic array input, then the maximum input frequency applies (Fmax/2).*

I_{CC} VS. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected "typical" pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power.



M5-128/M5LV-128



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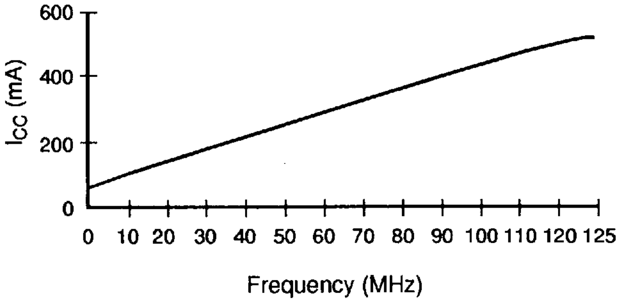
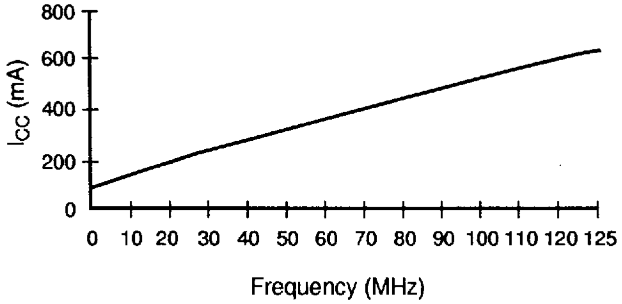
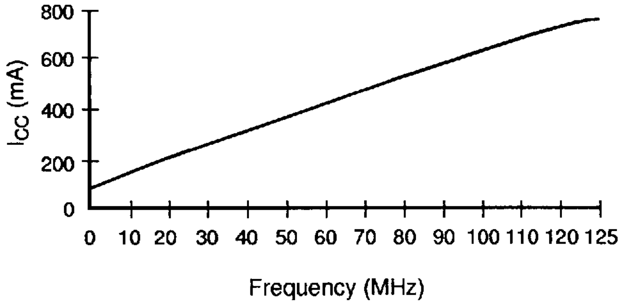


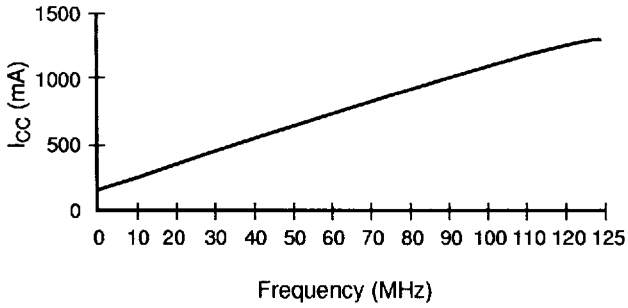
M5-256/M5LV-256



M5-320/M5LV-320



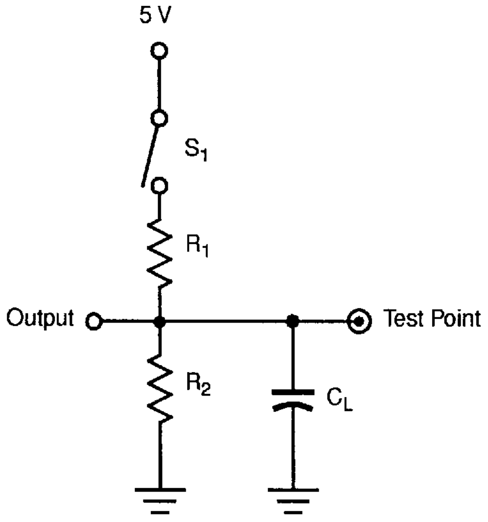
M5-384/M5LV-384



M5-512/M5LV-512

20446A-16

SWITCHING TEST CIRCUIT



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Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}, t_{CO}	Closed	35 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: $V_{OH} - 0.5$ V L → Z: $V_{OL} + 0.5$ V

** Switching several outputs simultaneously should be avoided for accurate measurement.*

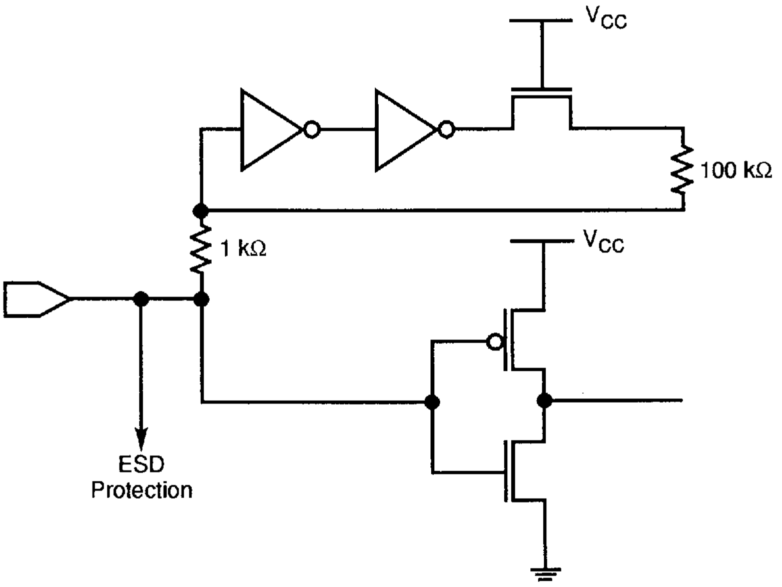
ENDURANCE CHARACTERISTICS

The MACH families are manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

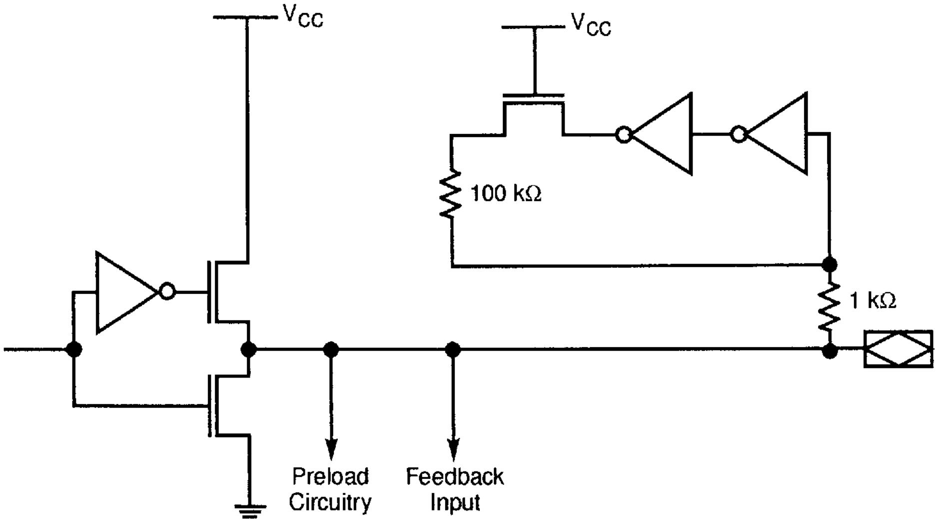
Endurance Characteristics

Parameter Symbol	Parameter Description	Min	Units	Test Conditions
t_{DR}	Min Pattern Data Retention Time	10	Years	Max Storage Temperature
		20	Years	Max Operating Temperature
N	Max Reprogramming Cycles	100	Cycles	Commercial Temperature Range

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Input



I/O

20446A-18

DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD Catalog.

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	MACHXL Software
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	Design Center/AMD Software
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	AMD-ABEL Software Data I/O MACH Fitters
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	Contact Manufacturer
Cadence Design Systems 555 River Oaks Pkwy San Jose, CA 95134 (408) 943-1234	PLD Designer Verilog, LeapFrog, RapidSim Simulators Ver. 9602
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	ABEL™ Synario™ Software
Logic Modeling 19500 NW Gibbs Dr. P.O. Box 310 Beaverton, OR 97075 (503) 690-6900	SmartModel® Library
Synopsys 700 E. Middlefield Rd. Mountain View, CA 94040	FPGA or Design Compiler (Requires MINC PLDesignerXL)
Mentor Graphics Corp. 8005 S.W. Boeckman Rd. Wilsonville, OR 97070-7777 (800) 547-3000 or (503) 685-7000	PLDSynthesis™ II QuickSim Simulator
MicroSim Corp. 20 Fairbanks Irvine, CA 92718 (714) 770-3022	Design Center Software
MINC Incorporated 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (800) 755-FPGA or (719) 590-1155	PLDesigner™-XL Software
SUSIE-CAD 10000 Nevada Highway, Suite 201 Boulder City, NV 89005 (702) 293-2271	SUSIE™ Simulator

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Teradyne EDA 321 Harrison Ave. Boston, MA 02118 (800) 777-2432 or (617) 422-2793	MultiSIM Interactive Simulator LASAR
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 442-4660 or (508) 480-0881	ViewPLD ViewSim Simulator
MANUFACTURER	**TEST GENERATION SYSTEM**
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 891-1995	ATGEN™ Test Generation Software
iNt GmbH Busenstrasse 6 D-8033 Martinsried, Munich, Germany (87) 857-6667	PLDCheck 90

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