
HM6289 Series

16384-word \times 4-bit High Speed CMOS Static RAM (with $\overline{\text{OE}}$)

HITACHI

Description

The Hitachi HM6289 is a high speed 64 k static RAM organized as 16-kword \times 4-bit. It realizes high speed access time (25/35 ns) and low power consumption, employing CMOS process technology. It is most advantageous for high speed and high density memory, such as in cache memory for mainframes or 32-bit MPUs. The HM6289, packaged in a 300-mil SOJ, is available for high density mounting. The low power version retains the data with battery backup.

Features

- High speed access time:
 - t_{AA} : 25/35 ns (max)
 - t_{OE} : 12/15 ns (max)
- High density 24-pin SOJ package
- Low power
 - Active mode: 300 mW (typ)
 - Standby mode: 100 μ W (typ)
- Single 5 V supply
- Completely static memory: No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible: All inputs and outputs

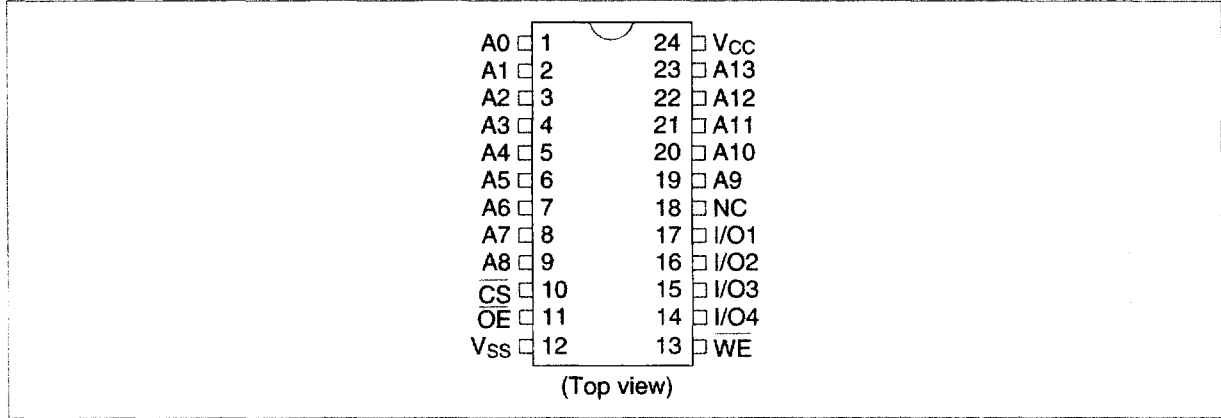
Ordering Information

| Type No. | Access Time | Package |
|--------------|-------------|------------------------------|
| HM6289JP-25 | 25 ns | 300-mil, 24-pin SOJ (CP-24D) |
| HM6289JP-35 | 35 ns | |
| HM6289LJP-25 | 25 ns | |
| HM6289LJP-35 | 35 ns | |



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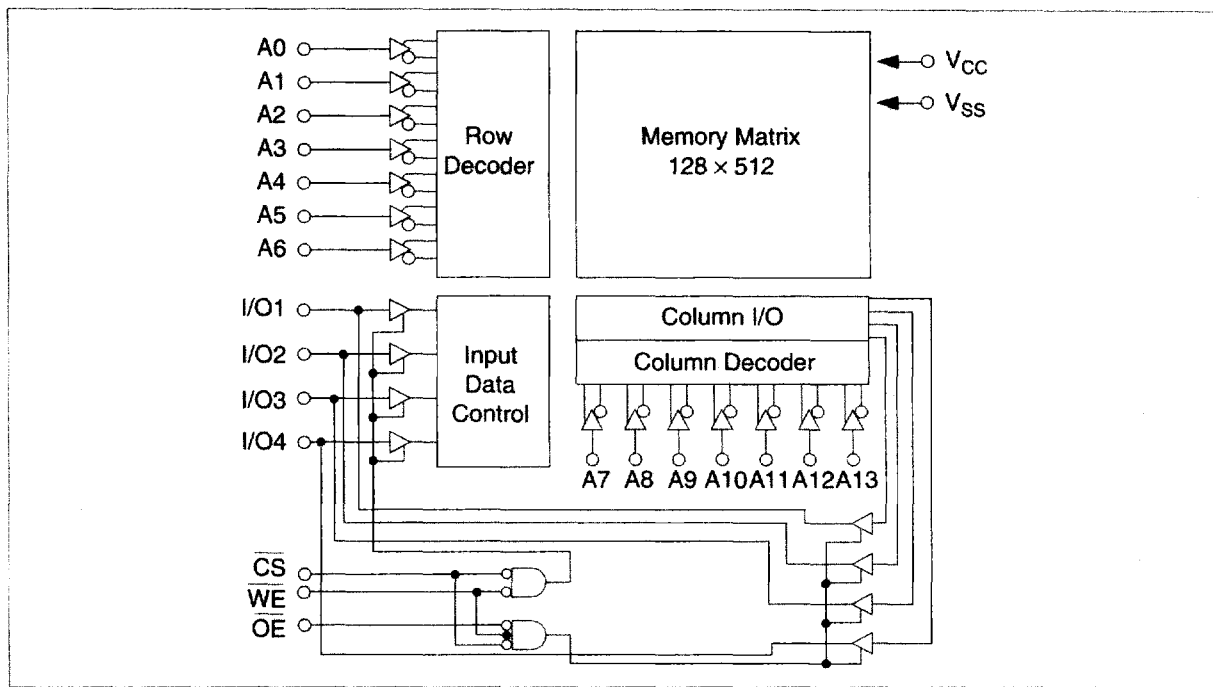
Pin Arrangement



Pin Description

| Pin Name | Function |
|-----------------|---------------|
| A0 – A13 | Address |
| I/O1 – I/O4 | Input/output |
| \overline{CS} | Chip select |
| \overline{OE} | Output enable |
| \overline{WE} | Write enable |
| V _{CC} | Power supply |
| V _{SS} | Ground |

Block Diagram



Truth Table

| \overline{CS} | \overline{OE} | \overline{WE} | Mode | V_{CC} current | I/O pin | Ref. cycle |
|-----------------|-----------------|-----------------|--------------|-------------------|---------|-----------------------|
| H | x | x | Not selected | I_{SB}, I_{SB1} | High-Z | — |
| L | L | H | Read | I_{CC} | Dout | Read cycle (1) – (3) |
| L | H | L | Write | I_{CC} | Din | Write cycle (1) – (2) |
| L | L | L | Write | I_{CC} | Din | Write cycle (3) – (6) |

Note: x: Don't care (H or L).

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Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|------------|----------------------------|------|
| Voltage on any pin relative to V_{SS} | V_{in} | -0.5 ¹⁾ to +7.0 | V |
| Power dissipation | P_T | 1.0 | W |
| Operating temperature range | T_{opr} | 0 to +70 | °C |
| Storage temperature range | T_{stg} | -55 to +125 | °C |
| Storage temperature range under bias | T_{bias} | -10 to +85 | °C |

Note: 1. V_{in} min = -2.0 V for pulse width \leq 10 ns.

Recommended DC Operating Conditions ($T_a = 0$ to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit |
|------------------------------|----------|--------------------|-----|-----|------|
| Supply voltage | V_{CC} | 4.5 | 5.0 | 5.5 | V |
| | V_{SS} | 0 | 0 | 0 | V |
| Input high (logic 1) voltage | V_{IH} | 2.2 | — | 6.0 | V |
| Input low (logic 0) voltage | V_{IL} | -0.5 ¹⁾ | — | 0.8 | V |

Note: 1. V_{IL} min = -2.0 V for pulse widths \leq 10 ns.

DC Characteristics ($T_a = 0$ to +70°C, $V_{CC} = 5$ V \pm 10%, $V_{SS} = 0$ V)

| Parameter | Symbol | Min | Typ ¹⁾ | Max | Unit | Test Conditions |
|------------------------------|----------------|-----|-------------------|-----|---------|--|
| Input leakage current | $ I_{IL} $ | — | — | 2.0 | μ A | $V_{CC} = \text{Max}$ $V_{in} = 0$ V to V_{CC} |
| Output leakage current | $ I_{LO} $ | — | — | 2.0 | μ A | $\overline{CS} = V_{IH}$, $V_{IO} = 0$ V to V_{CC} |
| Operating V_{CC} current | I_{CC} | — | 60 | 120 | mA | $\overline{CS} = V_{IL}$, $I_{out} = 0$ mA, min cycle |
| Standby V_{CC} current | I_{SB} | — | 15 | 30 | mA | $\overline{CS} = V_{IH}$, min cycle |
| Standby V_{CC} current (1) | I_{SB1} | — | 0.02 | 2.0 | mA | $\overline{CS} \geq V_{CC} - 0.2$ V, 0 V $\leq V_{in} \leq 0.2$ V or $V_{CC} - 0.2$ V $\leq V_{in}$ |
| | I_{SB1}^{*2} | — | — | 0.1 | μ A | |
| Output low voltage | V_{OL} | — | — | 0.4 | V | $I_{OL} = 8$ mA |
| Output high voltage | V_{OH} | 2.4 | — | — | V | $I_{OH} = -4.0$ mA |

Notes: 1. Typical values are at $V_{CC} = 5.0$ V, $T_a = +25^\circ\text{C}$ and not guaranteed.

2. L-version

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)*¹

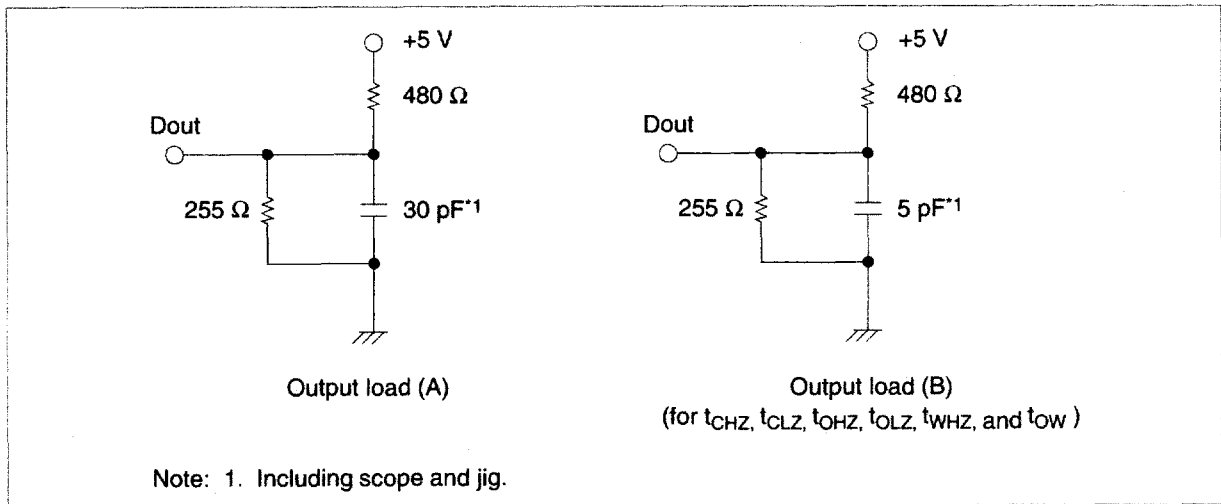
| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--------------------------|----------|-----|-----|-----|------|-----------------------|
| Input capacitance | C_{in} | — | — | 6 | pF | $V_{in} = 0\text{ V}$ |
| Input/output capacitance | C_{io} | — | — | 8 | pF | $V_{io} = 0\text{ V}$ |

Note: 1. These parameters are sampled and not 100% tested.

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, unless otherwise noted)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures



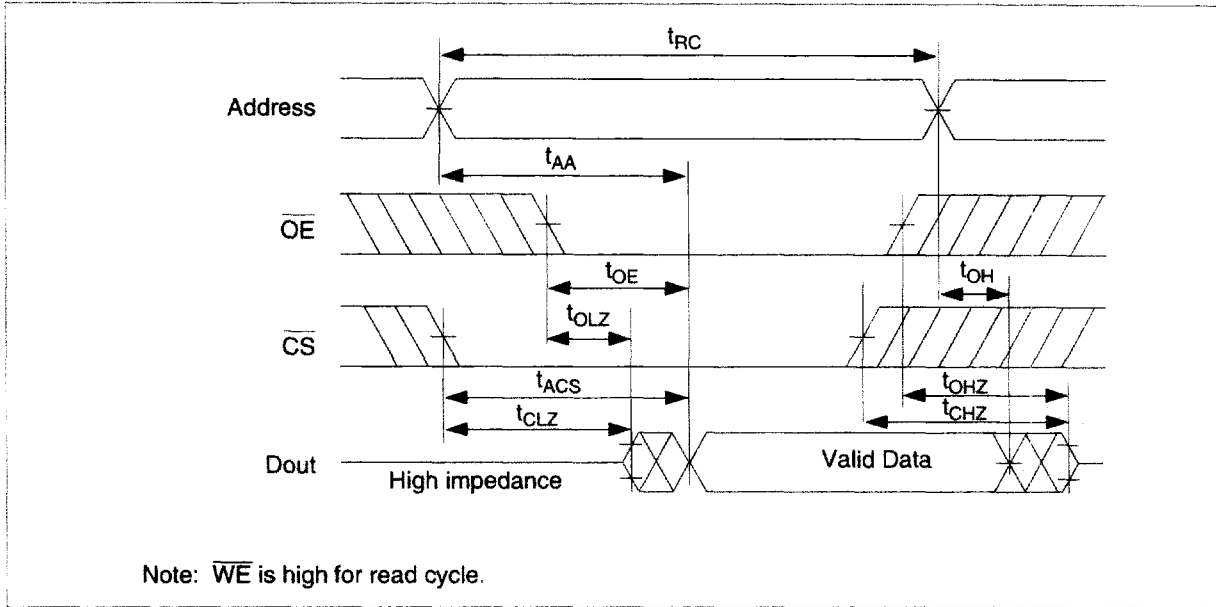
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Read Cycle

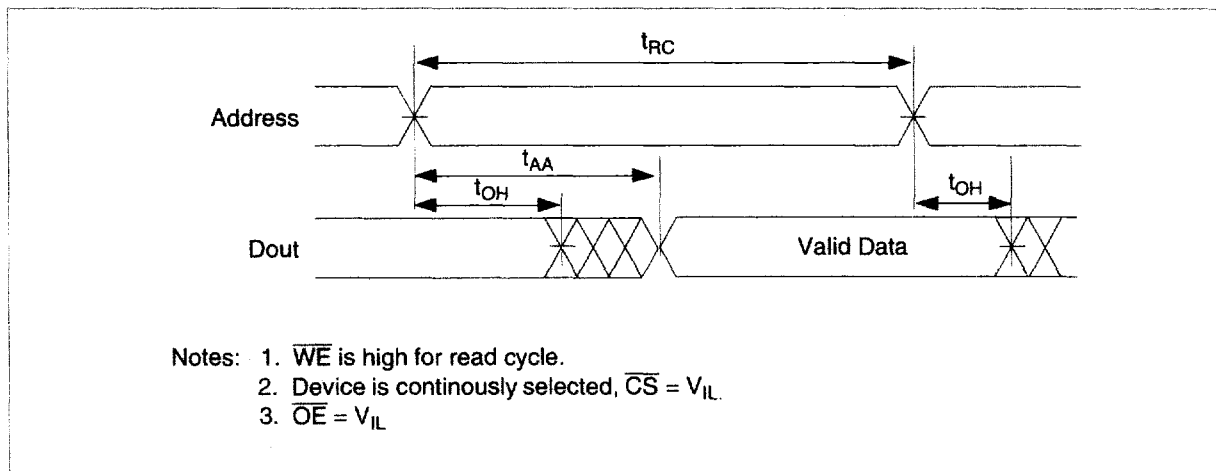
| Parameter | Symbol | HM6289-25 | | HM6289-35 | | Unit |
|--------------------------------------|----------------|-----------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | |
| Read cycle time | t_{RC} | 25 | — | 35 | — | ns |
| Address access time | t_{AA} | — | 25 | — | 35 | ns |
| Chip select access time | t_{ACS} | — | 25 | — | 35 | ns |
| Chip selection to output in low-Z | t_{CLZ}^{*1} | 5 | — | 5 | — | ns |
| Output enable to output valid | t_{OE} | — | 12 | — | 15 | ns |
| Output enable to output in low-Z | t_{OLZ}^{*1} | 0 | — | 0 | — | ns |
| Chip deselection to output in high-Z | t_{CHZ}^{*1} | 0 | 12 | 0 | 20 | ns |
| Chip disable to output high-Z | t_{OHZ}^{*1} | 0 | 10 | 0 | 10 | ns |
| Output hold from address change | t_{OH} | 3 | — | 5 | — | ns |

Note: 1. Output transition is measured ± 200 mV from steady state voltage with load (B). These parameters are sampled and not 100% tested.

Read Timing Waveform (1)

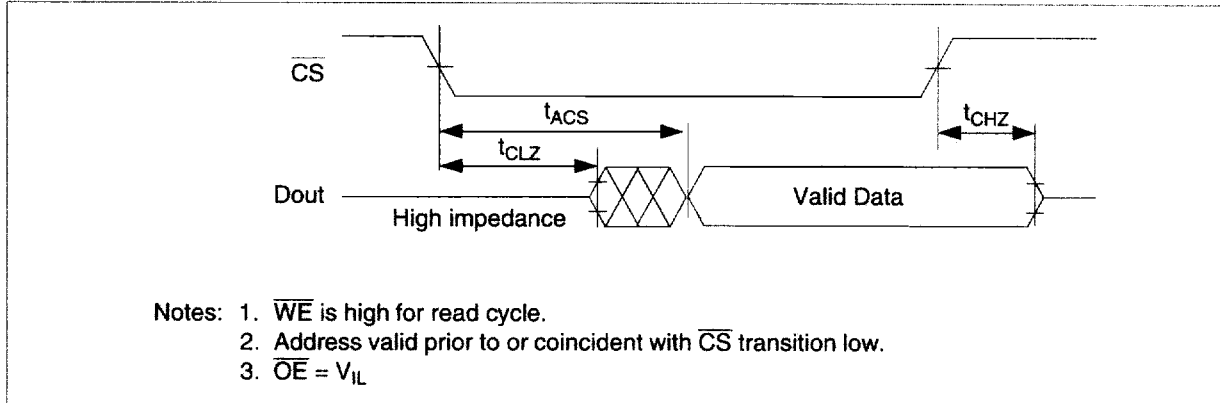


Read Timing Waveform (2)



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Read Timing Waveform (3)

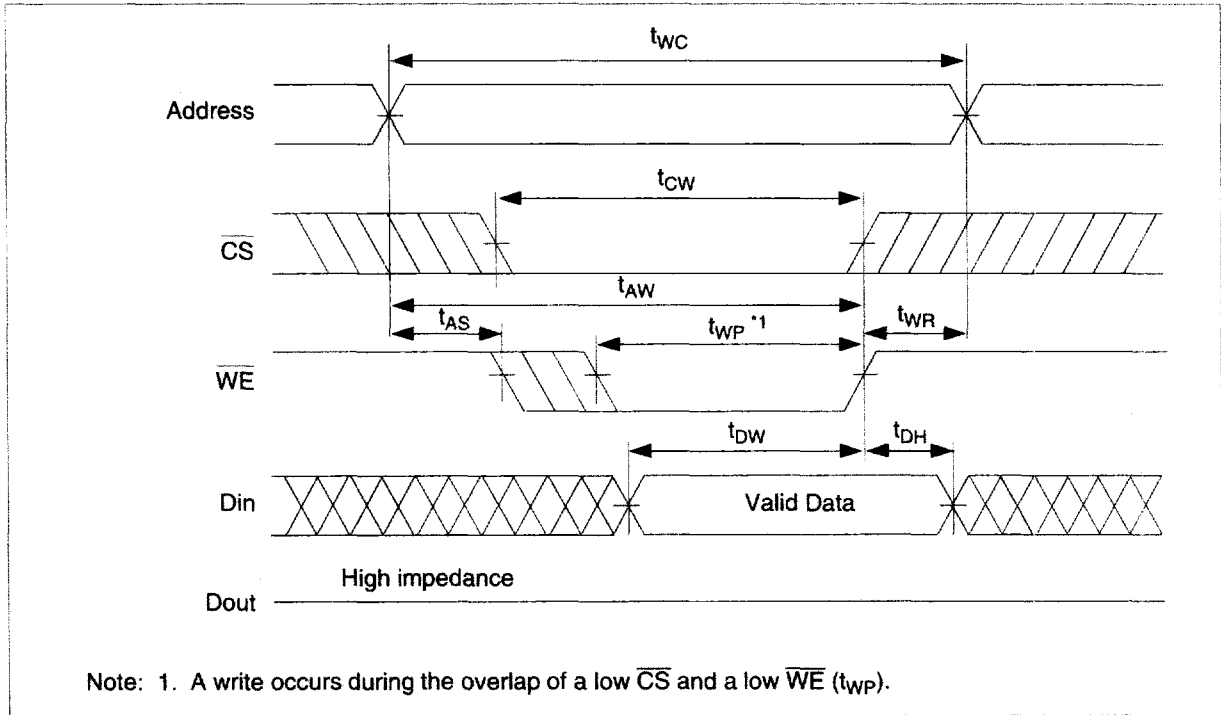


Write Cycle

| Parameter | Symbol | HM6289-25 | | HM6289-35 | | Unit |
|---|-----------|-----------|-----|-----------|-----|------|
| | | Min | Max | Min | Max | |
| Write cycle time | t_{WC} | 25 | — | 35 | — | ns |
| Chip selection to end of write | t_{CW} | 20 | — | 30 | — | ns |
| Address valid to end of write | t_{AW} | 20 | — | 30 | — | ns |
| Address setup time | t_{AS} | 0 | — | 0 | — | ns |
| Write pulse width | t_{WP} | 20 | — | 30 | — | ns |
| Write recovery time | t_{WR} | 0 | — | 0 | — | ns |
| Output disable to output in high-Z ¹ | t_{OHZ} | 0 | 10 | 0 | 10 | ns |
| Write to output in high-Z ¹ | t_{WHZ} | 0 | 8 | 0 | 10 | ns |
| Data to write time overlap | t_{DW} | 12 | — | 20 | — | ns |
| Data hold from write time | t_{DH} | 0 | — | 0 | — | ns |
| Output active from end of write ¹ | t_{OW} | 5 | — | 5 | — | ns |

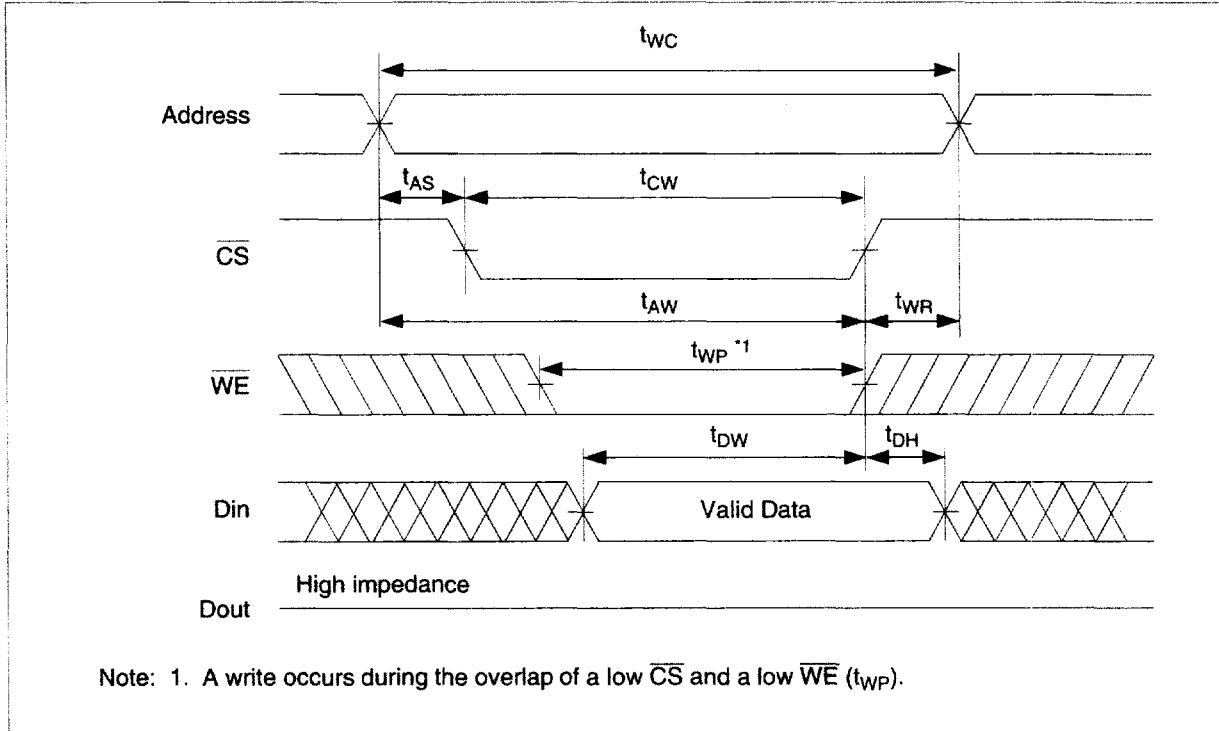
Note: 1. Output transition is measured ± 200 mV from steady state voltage with load (B). These parameters are sampled and not 100% tested.

Write Timing Waveform (1) (\overline{OE} = High, \overline{WE} = Controlled)

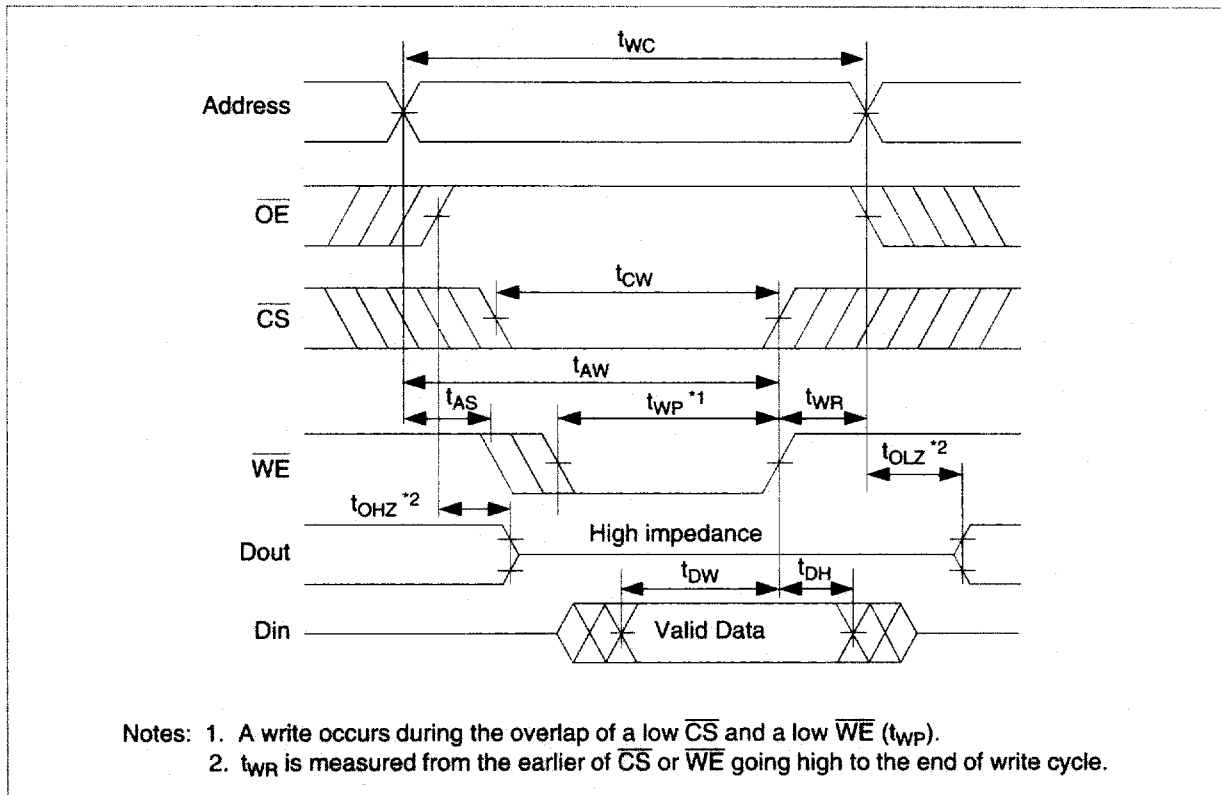


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Write Timing Waveform (2) ($\overline{OE} = \text{High}$, $\overline{CS} = \text{Controlled}$)

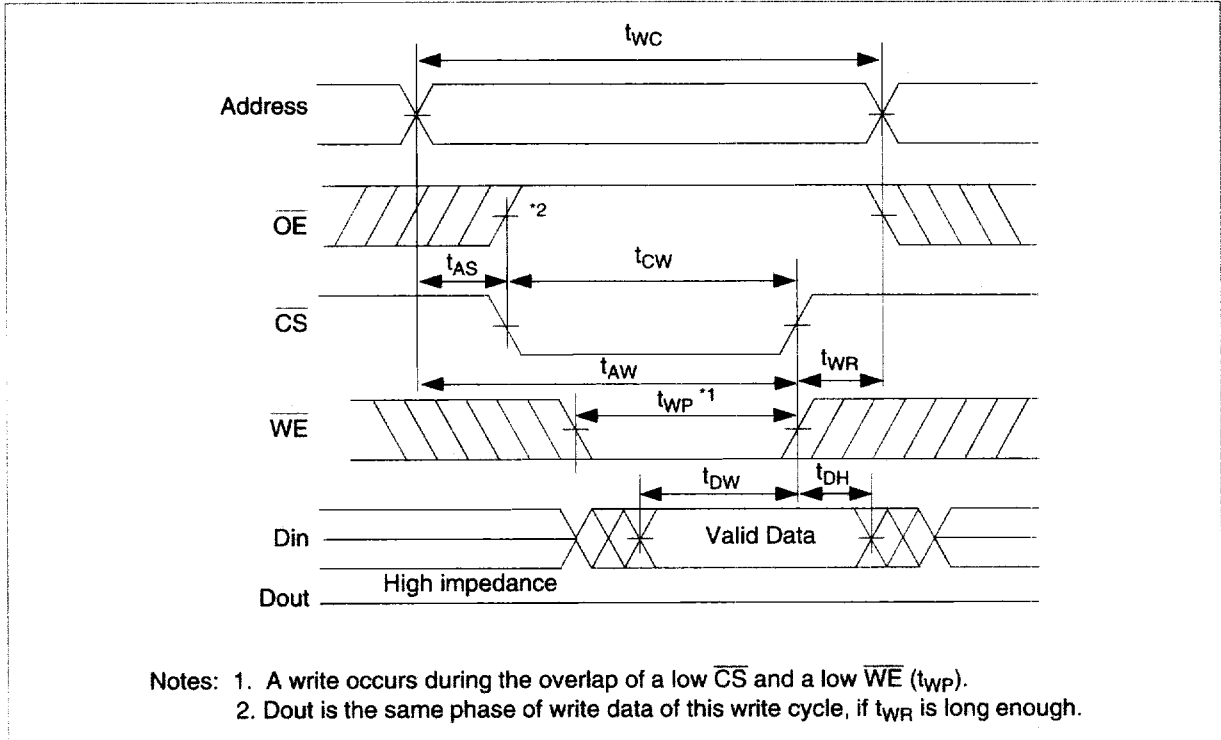


Write Timing Waveform (3) (\overline{OE} = Clocked, \overline{WE} = Controlled)

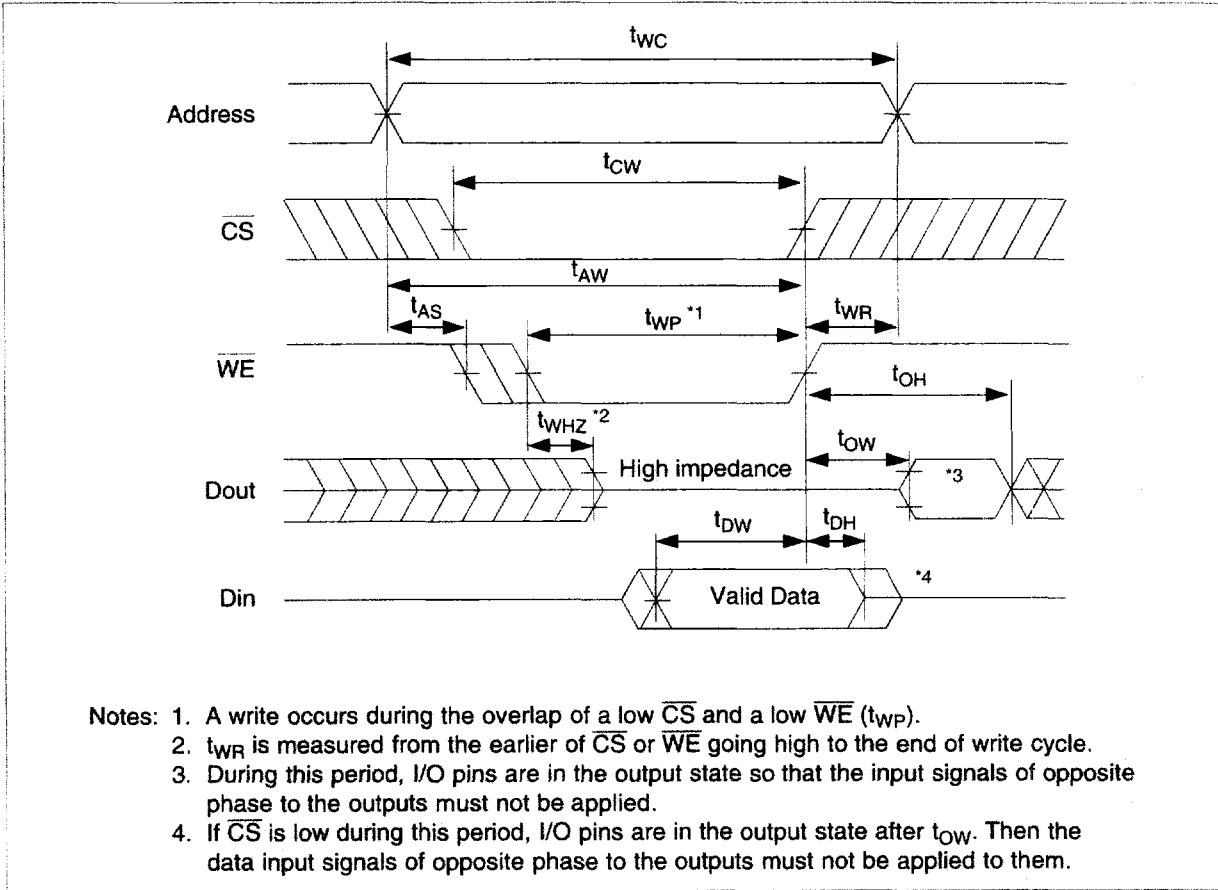


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Write Timing Waveform (4) (\overline{OE} = Clocked, \overline{CS} = Controlled)

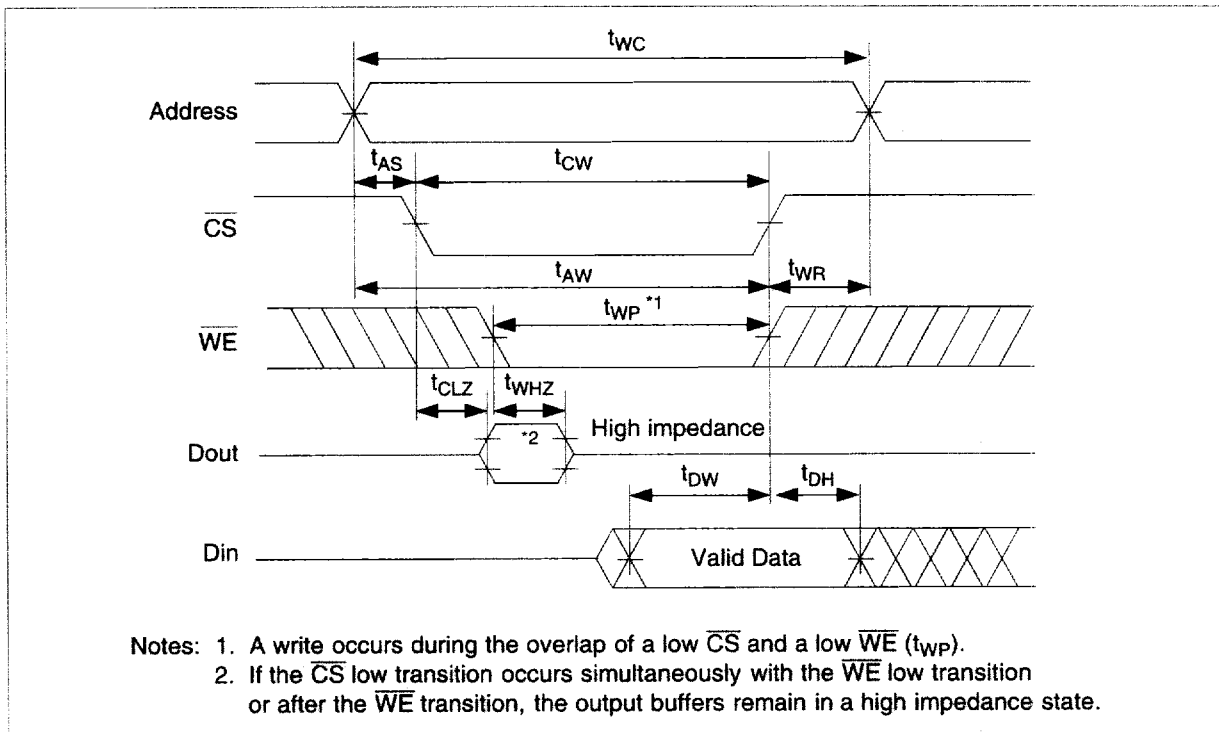


Write Timing Waveform (5) (\overline{OE} = Low, \overline{WE} = Controlled)



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Write Timing Waveform (6) (\overline{OE} = Low, \overline{CS} = Controlled)



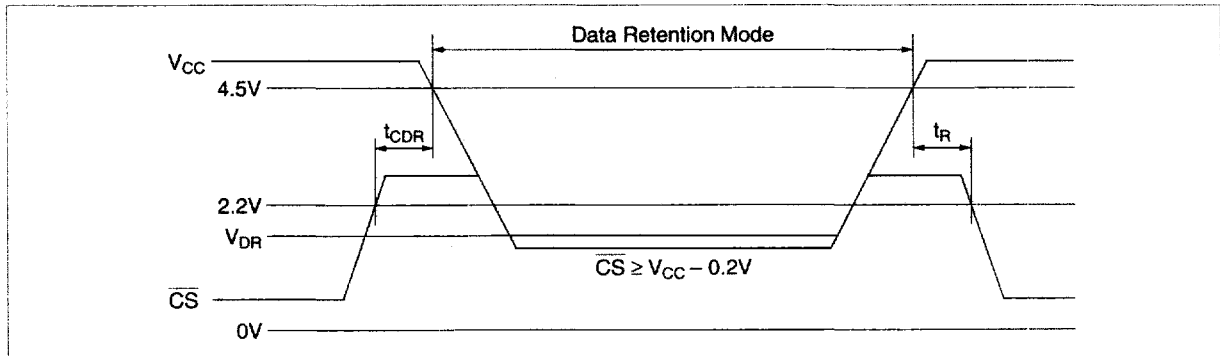
Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

These characteristics are guaranteed for the L-version only.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--------------------------------------|------------|---------------|-----|-----------|---------------|--|
| V_{CC} for data retention | V_{DR} | 2 | — | — | V | $\overline{CS} \geq V_{CC} - 0.2\text{ V}$, $V_{in} \geq V_{CC} - 0.2\text{ V}$ or $0\text{ V} \leq V_{in} \leq 0.2\text{ V}$ |
| Data retention current | I_{CCDR} | — | — | 50^{*2} | μA | |
| | | — | — | 35^{*3} | μA | |
| Chip deselect to data retention time | t_{CDR} | 0 | — | — | ns | See retention waveform |
| Operation recovery time | t_R | t_{RC}^{*1} | — | — | ns | |

- Notes: 1. t_{RC} = Read cycle time
 2. $V_{CC} = 3.0\text{ V}$
 3. $V_{CC} = 2.0\text{ V}$

Low V_{CC} Data Retention Waveform



HM6289 Series

Package Dimension

HM6289JP/LJP Series (CP-24D)

Unit: mm

