Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

• Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

HARRIS
SEMICONDUCTOR

HSP48410/883

January 1994

Histogrammer/Accumulating Buffer

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **10-Bit Pixel Data**
- **4k x 4k Frame Sizes**
- **Asynchronous Flash Clear Pin**
- **Fully Asynchronous 16-Bit or 24-Bit Host Interface**
- **DC to 33MHz Clock Rate**

Applications

- **Histogramming**
- **Histogram Equalization**
- **Image and Signal Analysis**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP48410GM-33/883	-55°C to +125°C	84 Lead PGA
HSP48410GM-25/883	-55°C to +125°C	84 Lead PGA

Description

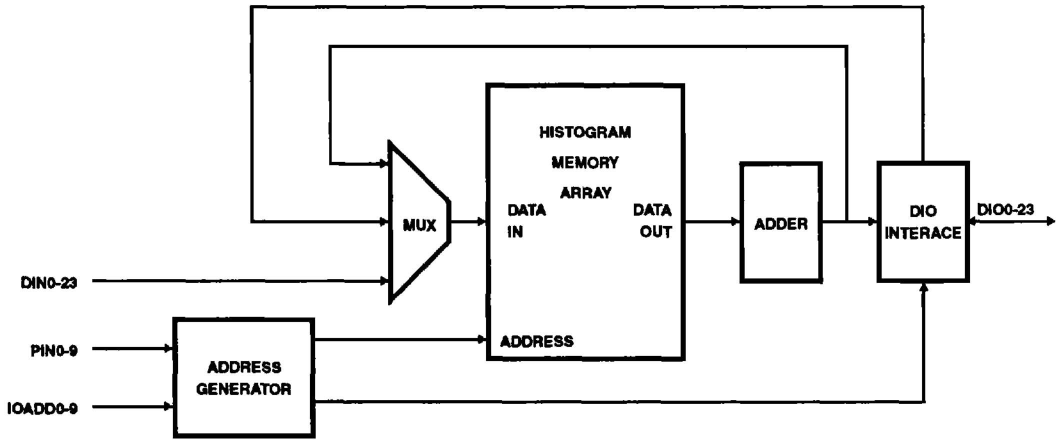
The Harris HSP48410 is an 84 lead Histogrammer IC intended for use in image and signal analysis. The on board memory is configured as 1024 x 24 array. This translates to a pixel resolution of 10-bits and an image size of 4k x 4k with no possibility of overflow.

In addition to Histogramming, the HSP48410 can generate and store the Cumulative Distribution Function for use in Histogram Equalization applications. Other capabilities of the HSP48410 include: Bin Accumulation, Look Up Table, 24-bit Delay memory, and Delay and Subtract mode.

A Flash Clear pin is available in all modes of operation and performs a single cycle reset on all locations of the internal memory array and all internal data paths.

The HSP48410 includes a fully asynchronous interface which provides a means for communications with a host, such as a microprocessor. The interface includes dedicated Read/Write pins and an address port which are asynchronous to the system clock. This allows random access of the Histogram Memory Array for analysis or conditioning of the stored data.

Block Diagram



Pinouts

84 LEAD PIN GRID ARRAY
TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L
11	DIN8	DIN10	DIN11	DIN13	DIN16	DIN17	DIN19	DIN22	DIO23	DIO22	DIO19
10	DIN5	DIN7	DIN9	DIN12	DIN15	DIN21	DIN20	DIN23	DIO21	DIO20	DIO17
9	DIN4	DIN6			DIN14	GND	DIN18			DIO18	DIO16
8	DIN2	DIN3								DIO15	DIO14
7	PIN9	DIN0	GND						DIO10	DIO12	DIO11
6	VCC	DIN1	CLK						DIO9	DIO8	DIO13
5	PIN8	PIN7	PIN6						DIO6	DIO7	GND
4	PIN5	PIN4								DIO4	DIO5
3	PIN3	PIN1			FCT0	IOADD 9	IOADD 8			DIO1	DIO3
2	PIN2	FC#	RD#	FCT2	WR#	UWS	IOADD 6	IOADD 3	IOADD 0	DIO0	DIO2
1	PIN0	START #	LD#	FCT1	GND	IOADD 5	IOADD 7	IOADD 4	IOADD 2	IOADD 1	VCC

PIN 'A1' ID

84 LEAD PIN GRID ARRAY
BOTTOM VIEW

L	K	J	H	G	F	E	D	C	B	A	
DIO19	DIO22	DIO23	DIN22	DIN19	DIN17	DIN16	DIN13	DIN11	DIN10	DIN8	11
DIO17	DIO20	DIO21	DIN23	DIN20	DIN21	DIN15	DIN12	DIN9	DIN7	DIN5	10
DIO16	DIO18			DIN18	GND	DIN14			DIN6	DIN4	9
DIO14	DIO15								DIN3	DIN2	8
DIO11	DIO12	DIO10						GND	DIN0	PIN9	7
DIO13	DIO8	DIO9						CLK	DIN1	VCC	6
GND	DIO7	DIO6						PIN6	PIN7	PIN8	5
DIO5	DIO4								PIN4	PIN5	4
DIO3	DIO1			IOADD 8	IOADD 9	FCT0			PIN1	PIN3	3
DIO2	DIO0	IOADD 0	IOADD 3	IOADD 6	UWS	WR#	FCT2	RD#	FC#	PIN2	2
VCC	IOADD 1	IOADD 2	IOADD 4	IOADD 7	IOADD 5	GND	FCT1	LD#	START #	PIN0	1

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
CLK	C6	I	Clock input. This input has no effect on the chips functionality when the chip is programmed to an asynchronous mode. All signals denoted as synchronous have their timing specified with reference to this signal.
PIN0-9	A1-5, A7, B3-5, C5	I	Pixel Input. This input bus is sampled by the rising edge of clock. It provides the on chip RAM with address values In Histogram, Bin Accumulate and LUT(write) mode. During Asynchronous modes it is unused.
LD#	C1	I	The Load pin is used to load the FCT0-2 bits into the FCT registers. (See below).
FCT0-2	D1-2, E3	I	These three pins are decoded to determine the mode of operation for the chip. The signals are sampled by the rising edge of LD# and take effect after the rising edge of LD#. Since the loading of this function is asynchronous to CLK, it is necessary to disable the START# pin during loading and enable START# at least 1 CLK cycle following the LD# pulse.
START#	B1	I	This pin informs the on chip circuitry which clock cycle will start and/or stop the current mode of operation. Thus, the modes are asynchronously selected (via LD#) but are synchronously started and stopped. This input is sampled by the rising edge of CLK. The actual function of this input depends on the mode that is selected. START# must always be held high (disabled) when changing modes. This will provide a smooth transition from one mode to the next by allowing the part to reconfigure itself before new mode begins. When START# is high, LUT(read) mode is enabled except for Delay and Delay and Subtract modes.
FC#	B2	I	Flash Clear. This input provides a fully asynchronous signal which effectively resets all bits in the RAM Array and the input and output data paths to zero.
DIN0-23	A8-11, B6-11, C10-11, D10-11, E9-11, F10-11, G9-11, H10-11	I	Data input bus. Provides data to the Histogrammer during Bin Accumulate, LUT, Delay and Delay and Subtract modes. Synchronous to CLK.
DIO0-23	J5-7, J10-11, K2-11, L2-4, L6-11	I/O	Asynchronous data bus. Provides RAM access for a microprocessor in preconditioning the memory array and reading the results of the previous operation. Configuarable as either a 24-bit or 16-bit bus
IOADD0-9	F1,F3,G1-3, H1-2, J1-2,K1	I	RAM address in asynchronous modes. Sampled on the falling edge of WR# or RD#.
UWS	F2	I	Upper Word Select. In 16-bit Asynchronous mode, a one on this pin denotes the contents of DIO0-7 as being the upper eight-bits of the data in or out of the Histogrammer. A zero means that DIO0-15 are the lower 16-bits. In all other modes, this pin has no effect.
WR#	E2	I	Write enable to the RAM for the data on DIO0-23 when the HSP48410 is configured in one of the asynchronous modes. Asynchronous to CLK.
RD#	C2	I	Read control for the data on DIO0-23 in asynchronous modes. Output enable for DIO0-23 in other modes. Asynchronous to CLK.
VCC	A6, L1		+5V
GND	C7, E1, F9, L5		Ground

Absolute Maximum Ratings

Supply Voltage .... +8.0V
Input, Output Voltage .... GND -0.5V to V_{CC} +0.5V
Storage Temperature .... -65°C to +150°C
Junction Temperature .... +175°C
Lead Temperature (Soldering 10s) .... +300°C
ESD .... Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic PGA Package	34.3°C/W	8.0°C/W

Maximum Package Power Dissipation at +125°C
Ceramic PGA Package .... 1.46 Watt
Gate Count .... 3500 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range .... +4.5V to +5.5V
Operating Temperature Range .... -55°C to +125°C

TABLE 1. DC ELECTRICAL SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	MIN	MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.2	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.8	V
High Level Clock Input	V_{IHC}	V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	3.0	-	V
Low Level Clock Input	V_{ILC}	V_{CC} = 4.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.8	V
Output High Voltage	V_{OH}	I_{OH} = -400µA, V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	2.6	-	V
Output Low Voltage	V_{OL}	I_{OL} = +2.0mA, V_{CC} = 4.5V (Note 1)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	0.4	V
Input Leakage Current	I_L	V_{IN} = VCC or GND, V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	10	µA
I/O Leakage Current	I_O	V_{OUT} = V_{CC} or GND, V_{CC} = 5.5V	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-10	10	µA
Standby Supply Current	I_{CCSB}	V_{IN} = V_{CC} or GND, V_{CC} = 5.5V, Outputs Open	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 25.6MHz, V_{IN} = V_{CC} or GND V_{CC} = 5.5V (Note 2)	1, 2, 3	-55°C ≤ T_A ≤ +125°C	-	308	mA
Functional Test	FT	(Notes 3,4)	7, 8	-55°C ≤ T_A ≤ +125°C	-	-	-

NOTES:

1. Interchanging of force and sense conditions is permitted.
2. Power Supply current is proportional to operating frequency. Typical rating for I_{CCOP} is12mA/MHz. Maximum junction temperature must be considered when operating part at high clock frequencies.
3. Tested as follows: f = 1MHz, V_{IH} = 2.6V, V_{IL} = 0.4V, $V_{OH} \geq 1.5V$, $V_{OL} \leq 1.5V$, V_{IHC} = 3.4V and V_{ILC} = 0.4V.
4. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_{CC} = 5.0V ± 10%, $T_A = -55^oC$ to $+125^oC$ (Note 1)

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	-33 (33MHz)		-25 (25.6MHz)		UNITS
					MIN	MAX	MIN	MAX	
Clock Period	T_{CP}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	30	-	39	-	ns
Clock Low	T_{CH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	12	-	15	-	ns
Clock High	T_{CL}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	12	-	15	-	ns
DIN Setup	T_{DS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	16	-	ns
DIN 0-23 Hold	T_{DH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	1	-	1	-	ns
Clock to DIO 0-23 Valid	T_{DO}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	19	-	24	ns
FC# Pulse Width	T_{FL}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	35	-	35	-	ns
FCT 0-2 Setup to LD#	T_{FS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	12	-	15	-	ns
FCT 0-2 Hold from LD#	T_{FH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	1	-	1	-	ns
START# Setup to CLK	T_{SS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	16	-	ns
START# Hold from CLK	T_{SH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	ns
PIN 0-9 Setup Time	T_{PS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	16	-	ns
PIN 0-9 Hold Time	T_{PH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	1	-	1	-	ns
LD# Pulse Width	T_{LL}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	12	-	15	-	ns
LD# Setup to START#	T_{LS}	Note 2	9, 10, 11	$-55^oC \le T_A \le +125^oC$	T_{CP}		T_{CP}	-	ns
WR# Low	T_{WL}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	20	-	ns
WR# High	T_{WH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	15	-	20	-	ns
Address Setup	T_{AS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	16	-	20	-	ns
Address Hold	T_{AH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	2	-	2	-	ns
DIO Setup to WR#	T_{WS}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	16	-	20	-	ns
DIO Hold from WR#	T_{WH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	2	-	2	-	ns
RD# Low	T_{RL}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	43	-	55	-	ns
RD# High	T_{RH}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	17	-	20	-	ns
RD# Low to DIO Valid	T_{RD}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	43	-	55	ns
Output Enable Time	T_{OE}	Note 3	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	19	-	24	ns
Read/Write Cycle Time	T_{CY}		9, 10, 11	$-55^oC \le T_A \le +125^oC$	65		80	-	ns

NOTES:

1. A.C. Testing is performed as follows: Input levels (CLK) 0.0V and 4.0V; Input levels (All other inputs) 0V and 3.0V. Timing reference levels (CLK) = 2.0V, (All others) = 1.5V. Output load circuit with C_L= 40pF. Output transition measured at $V_{OH} \ge 1.5V$ and $V_{OL} \ge 1.5V$.
2. There must be at least one rising edge of CLK between the rising edge of LD# and the falling edge of START#.
3. Transition is measured at ±200 mV from steady state voltage with loading as specified in test load circuit with C_L= 40pF.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	-33 (33MHz) MIN	-33 (33MHz) MAX	-25 (25.6MHz) MIN	-25 (25.6MHz) MAX	UNITS
Input Capacitance	C_{IN}	V_{CC} = Open, f = 1MHz, All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	12	-	12	pF
Output Capacitance	C_O	V_{CC} = Open, f = 1MHz, All measurements are referenced to device GND.	1	$T_A = +25^oC$	-	12	-	12	pF
DIO Valid After RD# High	T_{OH}		1, 2	$-55^oC \leq T_A \leq +125^oC$	0	-	0	-	ns
Output Disable Time	T_{OD}		1, 2	$-55^oC \leq T_A \leq +125^oC$	-	27	-	27	ns
Output Rise Time	T_R	From 0.8V to 2.0V	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	9	-	9	ns
Output Fall Time	T_F	From 2.0V to 0.8V	1, 2	$-55^oC \leq T_A \leq +125^oC$	-	9	-	9	ns

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
2. Loading is as specified in the test load circuit with C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2,3,8A,8B,10,11
Group A	-	1,2,3,7,8A,8B,9,10,11
Groups C and D	Samples/5005	1,7,9

Burn-In Circuits

84 LEAD GRID ARRAY
TOP VIEW

11	DIN8	DIN10	DIN11	DIN13	DIN16	DIN17	DIN19	DIN22	DIO23	DIO22	DIO19
10	DIN5	DIN7	DIN9	DIN12	DIN15	DIN21	DIN20	DIN23	DIO21	DIO20	DIO17
9	DIN4	DIN6			DIN14	GND	DIN18			DIO18	DIO16
8	DIN2	DIN3								DIO15	DIO14
7	PIN9	DIN0	GND						DIO10	DIO12	DIO11
6	VCC	DIN1	CLK						DIO9	DIO8	DIO13
5	PIN8	PIN7	PIN6						DIO6	DIO7	GND
4	PIN5	PIN4								DIO4	DIO5
3	PIN3	PIN1			FCT0	IOADD9	IOADD8			DIO1	DIO3
2	PIN2	FC#	RD#	FCT2	WR#	UWS	IOADD6	IOADD3	IOADD0	DIO0	DIO2
1	PIN0	START#	LD#	FCT1	GND	IOADD5	IOADD7	IOADD4	IOADD2	IOADD1	VCC

PIN 'A1'

A

PGA PIN	PIN NAME	BURN-IN SIGNAL
A1	PIN0	F1
A2	PIN2	F3
A3	PIN3	F4
A4	PIN5	F6
A5	PIN8	F9
A6	VCC	VCC
A7	PIN9	F10
A8	DIN2	F3
A9	DIN4	F5
A10	DIN5	F6
A11	DIN8	F9
B1	START#	F10
B2	FC#	F16
B3	PIN1	F2
B4	PIN4	F5
B5	PIN7	F8
B6	DIN1	F2
B7	DIN0	F1
B8	DIN3	F4
B9	DIN6	F7
B10	DIN7	F8
B11	DIN10	F11
C1	LD#	F11
C2	RD#	F1
C5	PIN6	F7
C6	CLK	F0
C7	GND	GND
C10	DIN9	F10
C11	DIN11	F12
D1	FCT1	F13
D2	FCT2	F14
D10	DIN12	F13
D11	DIN13	F14
E1	GND	GND
E2	WR#	F2
E3	FCT0	F12
E9	DIN14	F15
E10	DIN15	F1
E11	DIN16	F2
F1	IOADD5	F6
F2	UWS	F11
F3	IOADD9	F10
F9	GND	GND
F10	DIN21	F7
F11	DIN17	F3
G1	IOADD7	F8
G2	IOADD6	F7
G3	IOADD8	F9
G9	DIN18	F4
G10	DIN20	F6
G11	DIN19	F5
H1	IOADD4	F5
H2	IOADD3	F4
H10	DIN23	F9
H11	DIN22	F8
J1	IOADD2	F3
J2	IOADD0	F1
J5	DIO6	F7
J6	DIO9	F10
J7	DIO10	F11
J10	DIO21	F7
J11	DIO23	F9
K1	IOADD1	F2
K2	DIO0	F1
K3	DIO1	F2
K4	DIO4	F5
K5	DIO7	F8
K6	DIO8	F9
K7	DIO12	F13
K8	DIO15	F1
K9	DIO18	F4
K10	DIO20	F6
K11	DIO22	F8
L1	VCC	VCC
L2	DIO2	F3
L3	DIO3	F4
L4	DIO5	F6

NOTES:

1. $V_{CC}/2$ (2.7V ± 10%) used for outputs only.
2. 47KΩ (±20%) resistor connected to all pins except V_{CC} and GND.
3. $V_{CC} = 5.5 \pm 0.5V$.
4. 0.1µf (min) capacitor between V_{CC} and GND per position.
5. F_O = 100KHz ± 10%, F1 = F0/2, F2 = F1/2 . . . F16 = F15/2, 40% - 60% Duty Cycle.
6. Input Voltage Limits: V_{IL} = 0.8V max. V_{IH} = 4.5V ± 10%.

Metallization Topology

DIE DIMENSIONS:

330 x 281 x 19 ± 1mils

METALLIZATION:

Type: Si - Al or Si-Al-Cu
Thickness: 8kÅ

GLASSIVATION:

Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY:

0.47×10^5 A/cm^2

Metallization Mask Layout

HSP48410/883